IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 25 July 2023, accepted 25 August 2023, date of publication 30 August 2023, date of current version 7 September 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3310274

APPLIED RESEARCH

High-Reliability Solar Array Regulator for Deep Space Exploration Micro-Satellites

CRISTIAN TORRES, JOSÉ M. BLANES, AUSIÀS GARRIGÓS, (Senior Member, IEEE), DAVID MARROQUÍ, AND JOSÉ A. CARRASCO

Industrial Electronics Research Group (IE-g), Miguel Hernández University of Elche, 03202 Elche, Spain

Corresponding author: Cristian Torres (c.torres@umh.es)

This work was supported in part by the European Union NextGenerationEU and Generalitat Valenciana under Grant ASFAE/2022/21, and in part by Generalitat Valenciana and Fondo Social Europeo through Subvención Para la Contratación de Personal Investigador de Carácter Predoctoral under Grant ACIF2020/154.

ABSTRACT This work presents a single point failure free solar array regulator design for scientific deep space exploration micro-satellites, where reliability and fault tolerance are critical design aspects. The proposed regulator is composed by six independent dc/dc Buck converters controlled by a double control loop, which can control both the battery end-of-charge voltage if the battery is fully charged, or the power generated by the solar arrays otherwise. Besides, to optimize the extracted power, each phase has an analog maximum power point tracker circuit. In addition, the regulator has a redundant over voltage protection circuit that switches off the converters in case of battery overvoltage. Furthermore, this regulator is tolerant to the failure of any component. This paper describes the electronic design of the regulator, including a detailed system stability study, as well as the implementation of a 60W prototype and the tests that have been carried out to validate the design. The main contributions of this paper are: A practical solution for a solar array regulator for space applications is proposed; a detailed stability study is developed; a overvoltage protection circuit is presented; a prototype has been implemented using commercial off-the-shelf (COTS) components with space qualified equivalent versions; and extensive functional tests have been carried out under different space representative conditions to validate fault tolerance and robustness.

INDEX TERMS Fault-tolerant regulator, maximum power point tracker (MPPT), microsatellite power system, solar array regulator.

I. INTRODUCTION

In recent years, the use of small satellites, commonly known as microsatellites, whose weight range is between 1 and 100 kg, has increased exponentially, causing a revolution in the aerospace industry. The high success obtained by these platforms is because they allow scientific, commercial, and educational missions at a much lower cost than traditional space missions [1]. In this context, and with the aim to explore deep space and reach Near-Earth Objects (NEOs), small satellites platforms with capability of performing orbital rendezvous are nowadays being developed [2].

One of the main systems that enables this kind of mission is the Electrical Power System (EPS), whose mass is about 30% of the total dry mass of the satellite [3]. The EPS is responsible for constantly supplying power to the rest of the onboard systems, so if it fails, the satellite systems will be seriously affected. This is the main reason why the EPS must be highly reliable and, in most cases, tolerant to a single failure [4], [5]. Two recent examples have been described in [6] and [7]. In addition, some studies show that over 25% of all CubeSats failures are the result of EPS failures [8] and this mainly occurs during the four weeks after the launch, thus, high reliable EPS designs are usually recommended. As a result, most of the satellite EPS avoids the use of programmable digital systems that are powered from the EPS itself, as well as the use of Field Programmable Gate Arrays

The associate editor coordinating the review of this manuscript and approving it for publication was Zhehan Yi.

(FPGAs), which can be involuntarily reconfigured due to Single Event Upsets (SEU) [9].

Within the EPS, this paper focuses on the Solar Array Regulator (SAR), the subsystem responsible for extracting power from the Solar Arrays (SAs) and supplying the battery bus. SARs can be categorized into two main groups, Direct Energy Transfer (DET) and Maximum Power Point Tracker (MPPT). The operating principle of the DET systems consists of dividing the solar array into individual sections. These sections are connected sequentially to the main bus, each one going from 0 to 100% duty cycle, prior to the connection of the next one. This sequence is controlled as a function of the load demand, with the result that, for a given load condition, only one section is switching, and the others are in a digital state (fully connected to the bus or short-circuited). The efficiency of this converter is very high since only a part of the power is processed by the switching semiconductors and the rest of is connected to the bus through diodes. DET-based SARs (S3R, S4R…) are very simple systems, and are mainly found on Geostationary Orbit (GEO) telecommunication satellites due to its very high efficiency, very low mass, simplicity, and high reliability [10]. The main drawback of these systems is that the SA working point is directly given by the bus voltage and as the SA current-voltage (I-V) and power-voltage (P-V) curves depend on the irradiance and temperature conditions, which usually vary throughout the course of a space mission, this method is not capable of optimizing the power extracted from the SA. This problem can be solved using MPPT-based SARs [11]. These SARs use dc/dc converters, so they can modify the SA operation point, allowing Maximum Power Point (MPP) operation even if irradiance and temperature conditions vary.

Regardless of whether a DET or MPPT SAR architecture is used, the main dc power bus used can be regulated or unregulated. In the case of unregulated dc power bus, a battery is directly connected to it, while in the case of regulated bus, a bank of capacitors forms the main bus and dc/dc converters are used to charge and discharge the battery.

A comparison of MPPT-based EPS architectures for a 1U CubeSat (10cm × 10cm × 10cm nanosatellite) has been carried out in [12]. Different approaches were analyzed: series MPPT, series MPPT with series Battery Charge Regulator (BCR), series MPPT with series voltage regulator, series MPPT with parallel voltage regulator, parallel MPPT with series voltage regulator and sun-regulated dc-bus, concluding that the simple approach, series MPPT-SAR and unregulated bus has the highest reliability, the highest efficiency and extends the battery life.

Regarding the dc/dc converters used as SARs, the simplest structures offer the lowest number of components and improved reliability. However, for very high step-up or step-down conversion ratios, some limitations arise, and other approaches are required [13]. Buck [14] and boost [15] derived topologies are the most common, but also SEPIC [16] and other advanced topologies can be found [17].

This paper presents the design of a 60W MPPT-based SAR devised to be used on a microsatellite intended for scientific deep space exploration missions, being deep space one of the harshest environments known. The proposed design adapts the topology for high reliability solar array regulator presented in [18] following the European Space Agency (ESA) guidelines.

The main contributions of this paper with respect to the previous work published [18] are as follows: A practical solution for space applications is proposed; a detailed stability study is presented for all conditions encountered in different mission phases; a proposal for the overvoltage protection circuit is presented; a prototype has been implemented using commercial off-the-shelf (COTS) components but considering that space qualified equivalent version is feasible; extensive functional tests have been carried out under different space representative conditions to validate fault tolerance and robustness.

The rest of the paper is distributed as follows: section two details the solar array regulator topology and the stability study; section three presents the implementation of the prototype and the test conditions, and section four shows the experimental results. Finally, section five discusses the results and summarizes the main conclusions.

II. FAULT TOLERANT MICRO-SATELLITE SOLAR ARRAY REGULATOR DESIGN

The proposed SAR is made up of six independent dc/dc phases whose outputs are connected in parallel to the battery bus where the rest of satellite loads are connected, see Fig. 1. The main reason for using six phases is to take advantage of the satellite's form factor, which has two deployable panels, each one divided into six SA strings.

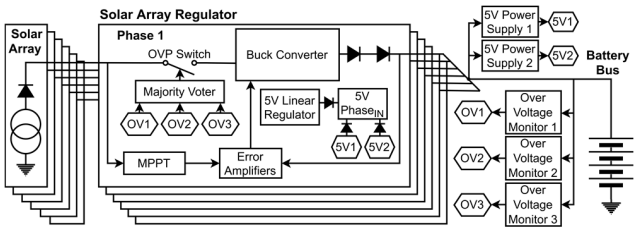

FIGURE 1. Block diagram of the proposed SAR.

Synchronous buck is used as dc/dc converter. This topology has been chosen due to the solar cell string and battery string configurations. Further, synchronous buck converter is widely known for its low part number required and simplicity. Each dc/dc converter is supplied by two SA strings and implements peak-current inner control loop. The outer loop is a voltage loop that controls the input voltage, i.e., SA MPP voltage, if the battery is not fully charged, or the output voltage, i.e., battery End of Charge (EOC) voltage, otherwise. Further, each phase has an independent analog MPPT circuit.

A redundant overvoltage battery circuit has been also implemented. This protection disconnects the SA strings

from the dc/dc converter if the battery voltage exceeds a preset threshold. Moreover, hot redundancy, n+1, is considered for SA and SAR, so that only five of the six phases are necessary to provide the total power required by the satellite. If one phase fails, this will be isolated, and the remaining five phases will supply the satellite.

A. SYNCHRONOUS BUCK CONVERTER AND PWM CONTROLLER

The synchronous buck converter is designed around the LT3845 pulse width modulation (PWM) controller. This PWM controller has a space-qualified equivalent, the RH3845MK, already proposed for space applications [19]. Single Point Failure Free (SPFF) reverse current protection is achieved by two series diodes connected at the output. LT3485 internally performs peak current control and includes anti-slope compensation circuit to eliminate the current limit reduction associated to slope compensation at high duty cycle. The output of the internal transconductance error amplifier is configured to be externally manipulated by the outer control loops. Reverse-current inhibit function is deactivated avoiding discontinuous current mode operation and pulse skipping at light loads.

B. MAXIMUM POWER POINT TRACKER

In conventional applications, MPPTs are implemented using digital devices such as microcontrollers but in space analog systems are preferable. This is due, among other things, to the fact that space-qualified programmable digital devices are expensive, the power consumption is high and besides can suffer of inadvertent reconfigurations due to radiation-induced single event upsets (SEUs). That is the reason because an analog oscillating MPPT circuit has been selected because its simplicity and large heritage in space applications [8], [20], [21], [22].

As represented in Fig. 2, the MPPT circuit has two sample-and-hold (S&H) circuits, two voltage dividers circuits, two comparators, a RS flip-flop and an integrator. As depicted in

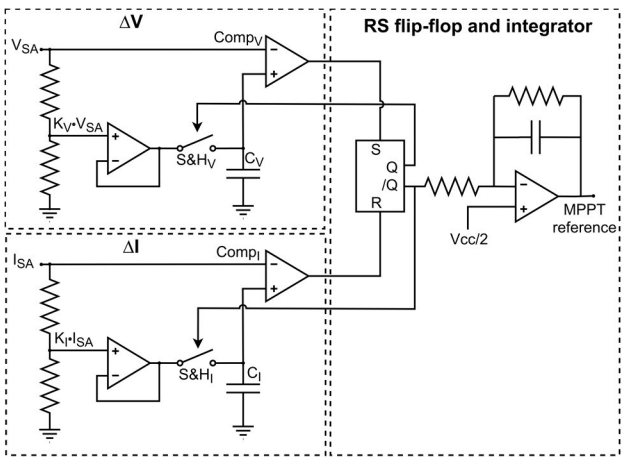

FIGURE 2. MPPT electrical diagram.

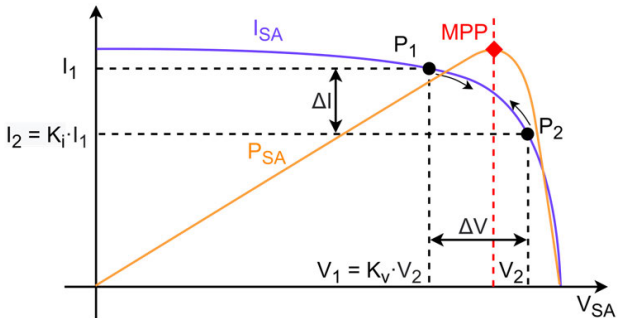

FIGURE 3. MPPT operating principle.

Fig. 3, the MPPT circuit operation is as follows. The solar array voltage (V_{SA}) and current (I_{SA}) are sensed. The two voltage dividers provide two outputs that are proportional (by a factor K_V for the voltage and K_I for the current) to the solar array voltage and current respectively. When the solar array voltage (V_{SA}) decreases certain ΔV and reaches $V_1 = K_V \cdot V_2$, the SET input of the RS flip-flop is activated, the current sample and hold circuit S&H$_I$ opens and retains a new limit $I_2 = K_I \cdot I_1$ and the MPPT reference signal becomes positive. Conversely, when I_{SA} decreases certain ΔI and reaches the limit $I_2 = K_I \cdot I_1$, the RESET input of the RS flip-flop is activated, the MPPT reference signal becomes positive, and a new limit $V_1 = K_V \cdot V_2$ is stored.

This process repeats continuously, producing a triangular MPPT reference output signal that results from the integration of the R-S flip-flop's output. MPPT voltage ripple, i.e., P_1 and P_2 locations, is adjusted by K_V and K_I and the MPPT frequency by the integrator time constant.

C. FEEDBACK CONTROL LOOP DESIGN

The LT3485 controller performs peak-current mode control. The voltage applied to the control pin, V_C, is proportional to the output inductor peak current. Output inductor current is measured with a shunt resistor (Ri) placed in series. To achieve input voltage regulation (MPPT operation) or output voltage regulation (EOC regulation), two outer error amplifiers are used, as represented in Fig. 4. An OR-diode

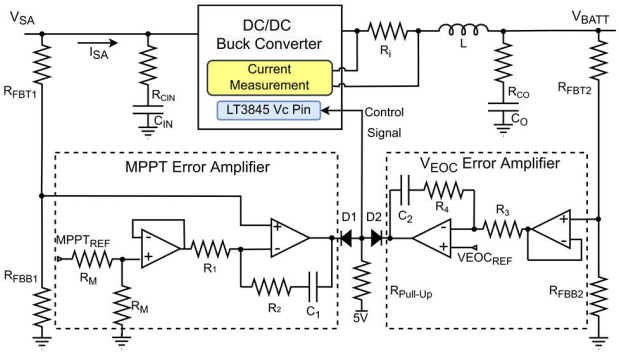

FIGURE 4. Control system electrical diagram.

circuit automatically selects the operation mode depending on the battery voltage [23]. Using independent external error amplifiers allows fine tuning of the Proportional and Integral (PI) controllers. The internal transconductance error amplifier is deactivated by pulling-up the feedback input, V_{FB}, with a 470kΩ resistor. Thus, the lowest control loop signal of the outer error amplifier finally determines the output current of the buck converter. If the battery is not fully charged, the V_{EOC} error amplifier saturates and the MPPT error amplifier sets the control signal.

As the voltage on the battery bus increases and approaches the V_{EOC}, the V_{EOC} error amplifier takes control to regulate end of charge voltage. The V_{EOC} error amplifier will continue controlling the converter until the battery voltage drops and the MPPT error amplifier takes control again. The detailed design of both control loops is shown below.

1) MPPT CONTROL LOOP

Fig. 5. shows the control loop diagram block that has been obtained from the small-signal analysis of the input voltage and peak-current controlled buck circuit shown in Fig. 6.

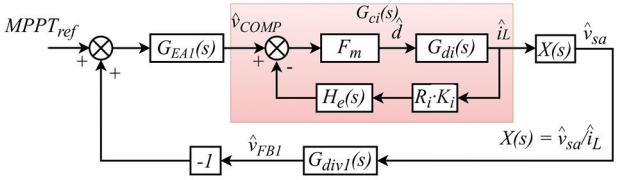

FIGURE 5. MPPT control loop diagram block.

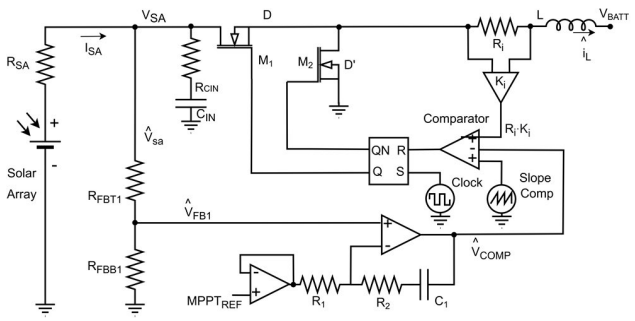

FIGURE 6. Buck and MPPT control loop simplified scheme.

The MPPT loop gain transfer function $T_{V1}(s)$ is given by (1), where $X(s)$, defined by (2), corresponds to the transfer function that relates the current through the inductor ($\hat{i}L$) with the SA voltage ($\hat{v}_{sa}$), G_{div1} (3) is the input voltage sense gain, $G_{EA1}(s)$ (4) is the error amplifier transfer function, and $G_{ci}(s)$ is the controller internal current loop transfer function, which calculation is explained in detail in [24] and it is given by (5). Further, $G_{ci}(s)$ depends on the control to duty cycle transfer function $Fm(s)$ (6), duty cycle to $\hat{i}L$ transfer function $G_{di}(s)$ (7), the current sensing gain $(Ri{\cdot}Ki)$, and the inductor current sampling and hold transfer function $H_e(s)$ (8). V_{se} corresponds to the internal slope compensation ramp amplitude, and f_{sw} is the switching frequency.

$$Tv_1(s) = X(s) \cdot G_{div1} \cdot G_{EA1}(s) \cdot G_{ci}(s) \tag{1}$$

where:

$$X(s) = \frac{\hat{i}_L}{\hat{v}_{SA}} = D \cdot R_{SA} \cdot \frac{1 + s \cdot C_{IN} \cdot R_{CIN}}{1 + s \cdot C_{IN} \cdot (R_{CIN} + R_{SA})} \tag{2}$$

$$G_{div1} = \frac{\hat{v}_{SA}}{\hat{v}_{FB1}} = \frac{R_{FBB1}}{R_{FBB1} + R_{FBT1}} \tag{3}$$

$$G_{EA1}(s) = \frac{\hat{v}_{FB1}}{\hat{v}_{COMP}} = \frac{1}{R_1 \cdot C_1} \cdot \frac{1 + S \cdot C_1 \cdot R_2}{S} \tag{4}$$

$$G_{ci}(s) = \frac{\hat{v}_{COMP}}{\hat{i}_L} = \frac{1}{R_i \cdot K_i} \cdot \frac{1}{1 + S\left(\frac{V_{SE} \cdot fsw \cdot L + (0.5 \cdot V_{SA} - V_{BATT}) Ki \cdot Ri}{\hat{v}_{SA} \cdot Ri \cdot fsw}\right)} \tag{5}$$

$$Fm(s) = \frac{f_{sw}}{\left(R_i \cdot \frac{V_{SA} - V_{BATT}}{L}\right) + (V_{SE} \cdot f_{sw})} \tag{6}$$

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{\hat{v}_{SA}}{s \cdot L} \tag{7}$$

$$H_e(s) = 1 - \frac{s}{2 \cdot f_{sw}} + \frac{s^2}{(\pi \cdot f_{sw})^2} \tag{8}$$

Substituting (2), (3), (4) and (5) in (1), results in the loop gain transfer function (9), $T_{V1}(s)$, used for design purposes. The gain, K_1, of $T_{V1}(s)$ is given by (10), the frequencies of the two zeros, f_{ZEA1} and f_{Zx}, are represented by (11) and (12), and the frequencies of the two poles, f_{Px} and f_{Pci}, are described by (13) and (14).

$$Tv_1(s) = K_1 \cdot \frac{(1 + \frac{S}{2 \cdot \pi \cdot fz_{EA1}}) \cdot (1 + \frac{S}{2 \cdot \pi \cdot fz_X})}{S \cdot (1 + \frac{S}{2 \cdot \pi \cdot fp_X}) \cdot (1 + \frac{S}{2 \cdot \pi \cdot fp_{ci}})} \tag{9}$$

where:

$$K_1 = D \cdot R_{SA} \cdot \frac{R_{FBB1}}{R_{FBB1} \cdot R_{FBT1}} \cdot \frac{1}{R_1 \cdot C_1} \cdot \frac{1}{Ri \cdot Ki} \tag{10}$$

$$fz_{EA1} = \frac{1}{2 \cdot \pi \cdot C_1 \cdot R_2} \tag{11}$$

$$fz_x = \frac{1}{2 \cdot \pi \cdot C_{IN} \cdot R_{CIN}} \tag{12}$$

$$fp_x = \frac{1}{2 \cdot \pi \cdot C_{IN} \cdot (R_{CIN} + R_{SA})} \tag{13}$$

$$fp_{ci} = \frac{V_{IN} \cdot Ri \cdot fsw}{2 \cdot \pi \cdot [V_{SE} \cdot fsw \cdot L + (0.5 \cdot V_{SA} - V_{BATT}) \cdot Ki \cdot Ri]} \tag{14}$$

A peak-current mode controlled buck converter powered by a photovoltaic source can become unstable if the input voltage is lower than the maximum power point voltage [25], [26]. Slope compensation of the peak current control can eliminate such instability, but (15) must be met for all working

conditions, where I_{SC} is the short-circuit current and Kp corresponds to the proportional gain of the PI type compensator.

$$\frac{-I_{SC}}{C_{IN} \cdot V_{SA_{min}}} \cdot \left(1 - \frac{V_{SA_{min}}}{I_{SC}} \cdot Kp\right) > 0 \tag{15}$$

2) VEOC CONTROL LOOP

The battery VEOC voltage control loop, shown in Fig. 7, has been obtained from the small-signal analysis of the output voltage and peak-current controlled buck circuit shown in Fig. 8.

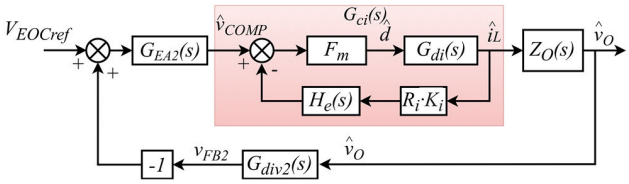

FIGURE 7. V_{EOC} mode control loop diagram block.

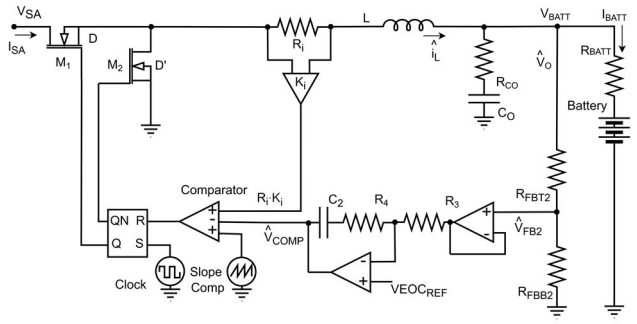

FIGURE 8. V_{EOC} mode control loop simplified scheme.

The V_{EOC} loop gain transfer function $T_{V2}(s)$ is defined by (16), where $Z_O(s)$ (17) corresponds to open loop output impedance, $G_{div2}(s)$ (18) is the output voltage sense gain and $G_{EA2}(s)$ (19) is the error amplifier transfer function.

$$Tv_2(s) = Z_O(s) \cdot G_{div2}(s) \cdot G_{EA2}(s) \cdot G_{ci}(s) \tag{16}$$

where:

$$Z_O(s) = \frac{\hat{v}_O}{\hat{i}_L} \approx R_{BATT} \cdot \frac{1 + S \cdot R_{CO} \cdot C_O}{1 + S \cdot (R_{CO} + R_{BATT}) \cdot C_O} \tag{17}$$

$$G_{div2} = \frac{\hat{v}_{SA}}{\hat{v}_{FB2}} = \frac{R_{FBB2}}{R_{FBB2} + R_{FBT2}} \tag{18}$$

$$G_{EA2}(s) = \frac{\hat{v}_{FB2}}{\hat{v}_{COMP}} = \frac{1}{R_3 \cdot C_2} \cdot \frac{1 + S \cdot C_2 \cdot R_4}{S} \tag{19}$$

Substituting (17), (18), (19) and (5) into (16), results in the loop gain transfer function (20) $T_{V2}(s)$. The gain, K_2, of $T_{V2}(s)$ is given by (21). The two zeros (f_{ZEA2} and f_{Zout}) are located at frequencies (22) and (23), and the two poles (f_{Pout} and f_{Pci}) are located at frequencies (24) and (25).

$$Tv_2 = K_2 \cdot \frac{(1 + \frac{S}{2 \cdot \pi \cdot fz_{EA2}}) \cdot (1 + \frac{S}{2 \cdot \pi \cdot fz_{out}})}{S \cdot (1 + \frac{S}{2 \cdot \pi \cdot fp_{out}}) \cdot (1 + \frac{S}{2 \cdot \pi \cdot fp_{ci}})} \tag{20}$$

where:

$$K_2 = R_{BATT} \cdot \frac{R_{FBB2}}{R_{FBB2} \cdot R_{FBT2}} \cdot \frac{1}{R_3 \cdot C_2} \cdot \frac{1}{Ri \cdot Ki} \tag{21}$$

$$fz_{EA2} = \frac{1}{2 \cdot \pi \cdot C_2 \cdot R_4} \tag{22}$$

$$fz_{out} = \frac{1}{2 \cdot \pi \cdot Co \cdot R_{CO}} \tag{23}$$

$$fp_{out} = \frac{1}{2 \cdot \pi \cdot (R_{CO} + R_{BATT}) \cdot Co} \tag{24}$$

$$fp_{ci} = \frac{V_{IN} \cdot Ri \cdot fsw}{2 \cdot \pi \cdot [V_{SE} \cdot fsw \cdot L + (0.5 \cdot V_{SA} - V_{BATT}) \cdot Ki \cdot Ri]} \tag{25}$$

D. OVER VOLTAGE PROTECTION

The main function of the Over Voltage Protection (OVP) system is to prevent the battery overcharge in case of any failure. First, three independent voltage monitors compare the battery voltage with a preset reference, generating a high-level signal at its output if the battery voltage is higher than the established threshold and generating a low-level signal otherwise. The output signals of these three voltage monitors are independently connected to six majority-voters circuits [26], each of them controlling one SAR phase. The majority-voter circuits generate a signal equal to the median of their inputs. Thus, if one of the voltage monitors provides a wrong value, this signal is discarded, and the system makes the decisions based on the two correct signals.

Finally, a P-type MOSFET, controlled by the output signal of the majority voters, disconnects the SA source from the buck converter. The diagram of this system is show in Fig. 9.

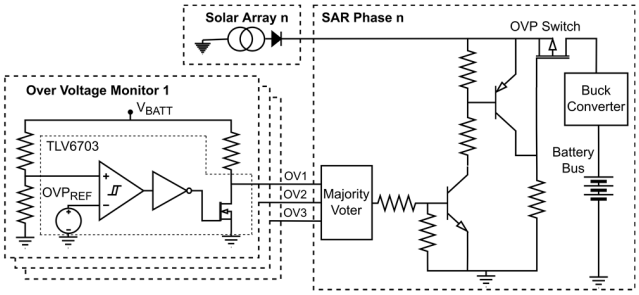

FIGURE 9. Over voltage protection (OVP) system diagram.

III. IMPLEMENTATION AND TEST SETUP

An experimental 60W prototype has been implemented to validate the proposed solar array regulator. This prototype has been designed following the European Cooperation for Space Standardization directives [28], [29], which are extensively used in ESA projects. Fig. 10 and Fig. 11 show the prototype's top and bottom sides respectively. Each subsystem is highlighted in the pictures in a different color.

TABLE 1 includes the most critical components and manufacturers for the system implementation, as well as the

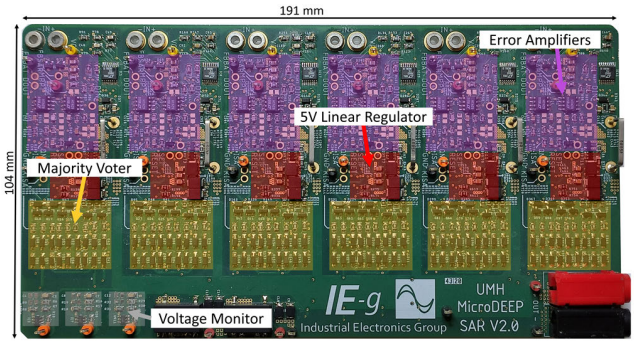

FIGURE 10. Top side of the implemented prototype. Error amplifiers, 5 v linear regulators, majority voters and voltage monitors are shown.

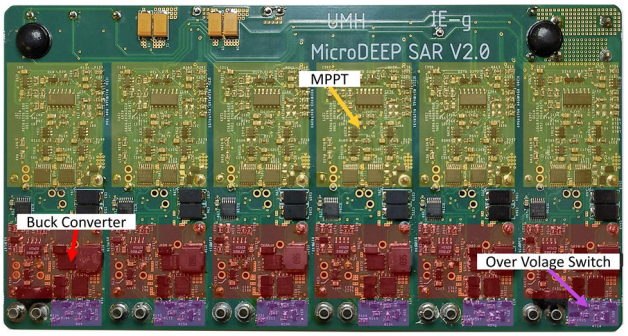

FIGURE 11. Bottom side of the implemented prototype. MPPTs, buck converters and overvoltage switches are shown.

TABLE 1. Prototype components.

Description	Part Used	Space Qualified
OVP Off MOSFET	SI2319DDS - VS	STRH40P10 - STM
OVP Voltage Monitor	TLV6703 - TI	TL431 + LM311 - TI
Buck Controller	LT3845 - AD	RH3845 - AD
Buck MOSFETs	BSC032N04 - IT	RH411 - AD
Buck Output Diodes	DFLS130 - DI	1N5819U - STM
NPN BJT Transistor	2N222 - STM	2N2222AHR - STM
Error Amp. Op. Amp.	LTC6241 - AD	RH1498 - AD
Error Amp. Diodes	BAT54 - OS	1N5819 - ST
MPPT Op. Amp.	LMV341 - TI	LM124AQML-SP-TI
MPPT Comparators	LMV761 - TI	LM111QLM-SP-TI
MPPT S&H Switch	MC14066 - OS	ADG201S - AD
MPPT flip-flop	CD4013 - TI	SN54HC74-SP-TI
MPPT Current Sens.	INA193 - TI	INA901-SP-TI

proposed space-grade qualified components for the flight model.

IV. EXPERIMENTAL RESULTS

A test bench made up of a set of four programmable solar array simulators (SAS), a power analyzer, a battery simulator, an electronic load, an oscilloscope, a vector network analyzer,

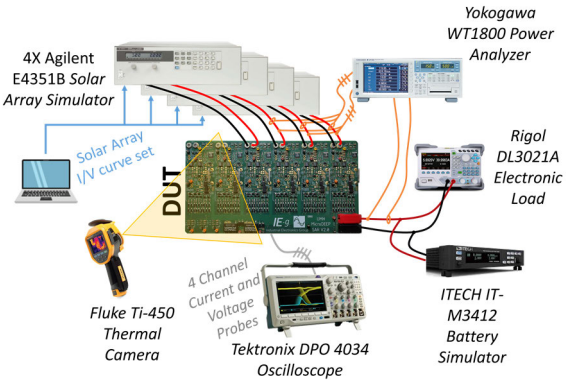

FIGURE 12. Test setup configuration.

TABLE 2. Prototype configuration.

Main Power System	Value
Battery bus configuration	4S3P Saft MP174865 xlr [31]
Battery bus voltage range	12.8-16.8 V
R_{BATT} (EOL (End of Life), BOL (Beginning of Life))	0.12 Ω, 0.15 Ω
Minimum power-on voltage	5.85 V
Solar array configuration	6 String 10S2P Azur Space 3G30C Advanced [32]
R_{SA} eq. (883 W/m^2, 220 W/m^2)	4.7 Ω, 16.8 Ω
Over Voltage System	***Value***
Maximum battery voltage	17.2 V
Buck Converter	***Value***
Controller data	V_{se} = 60 mV, K_i = 8.7
Switching frequency (fsw)	150 kHz
L	470 µH
C_{IN}	30 µF
C_O	44 µF
R_i	50 mΩ
Error Amplifiers	***Value***
C_1	100 nF
R_1, R_2	3.9 kΩ, 15 kΩ
R_{FBT1}	120 Ω
R_{FBB1}	3 kΩ
C_2	2.2 nF
R_3, R_4	4.7 kΩ, 10 kΩ
R_{FBT2}	43 kΩ
R_{FBB2}	11 kΩ

and a thermographic camera has been used for the experimental validation of the prototype, see Fig. 12.

TABLE 2 collects the most relevant parameters of the implemented prototype. While the parameters corresponding to the "Main Power System" section are determined by the satellite sizing for the proposed mission, the parameters related to the buck converters and the error amplifiers have been selected prioritizing the overall stability.

Tests carried out on the prototype have been divided into two groups. The first group includes four tests on a single phase to verify: converter stability, MPPT operation, control loop transition (MPPT to V_{EOC} and vice versa), and overvoltage protection. The second group focuses on multi-phase operation. Further, different tests have been performed simulating different irradiance and temperature conditions.

A. STABILITY MEASUREMENTS

Converter stability has been measured for two extreme conditions. The first scenario considers the beginning-of-life conditions being the microsatellite at 1.25 Astronomical Units (AU) with an approximate irradiance around 883 W/m^2 (V_{MPPT} = 26.7 V, I_{MPPT} = 0.56 A). The other scenario considers the end-of-life conditions, 2.5 AU and irradiance around 220 W/m^2 (V_{MPPT} = 31.41 V, I_{MPPT} = 0.146 A). Besides, extreme battery voltages, 12.8 V and 16.8 V, are considered.

Fig. 13 shows measured and theoretical, given by equation (9), Bode diagram of the MPPT loop gain transfer function. Crossover frequencies between 810 Hz and 1480 Hz are obtained with phase margins larger than 88° in all cases, as represented in TABLE 3.

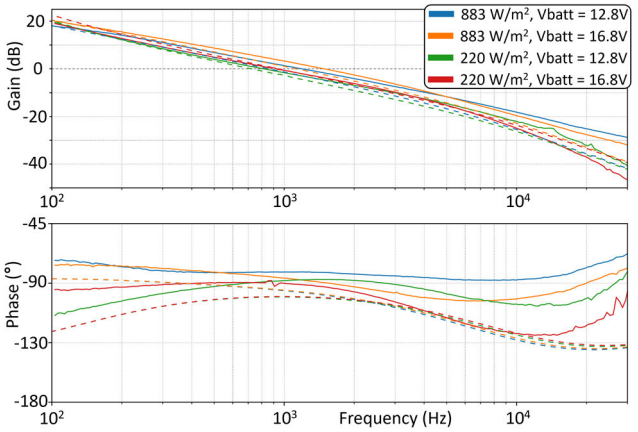

FIGURE 13. Bode diagram of the MPPT loop gain transfer function (TV1(s)). Continuous line corresponds to experimental results and dashed line corresponds to theoretical results.

Fig. 14 depicts measured and theoretical, given by equation (20), Bode diagram of the V_{EOC} loop gain. For this control loop, as shown in TABLE 3, the crossover frequencies vary between 899 Hz and 1176 Hz, and the phase margin is greater than 84° in all cases. Similar and very robust stability response is achieved in all cases.

B. MPPT MODE: START-UP

This test simulates the start-up of a single phase, from the exit of an eclipse (darkness) to illumination conditions. At the initial instant, the batteries are not fully charged, so the MPPT error amplifier controls the converter. The Solar Array Simulators (SAS) has been configured to provide VMPP = 27V and IMPP = 0.45A, which are the expected values at 1.25 AU.

TABLE 3. Loop gain results.

Control loop - MPPT mode				
	Theoretical		Measured	
	fc (Hz)	Φm (°)	fc (Hz)	Φm (°)
883 W/m^2, V_{BATT} = 12.8 V	859	85	1190	89
883 W/m^2, V_{BATT} = 16.8 V	1120	84	1480	90
220 W/m^2, V_{BATT} = 12.8 V	722	79	810	91
220 W/m^2, V_{BATT} = 16.8 V	942	80	930	88
Control loop - VEOC mode				
	Theoretical		Measured	
	fc (Hz)	Φm (°)	fc (Hz)	Φm (°)
883 W/m^2, Batt at BOL	839	86	899	84
883 W/m^2, Batt at EOL	1040	86	1105	84
220 W/m^2, Batt at BOL	845	88	942	90
220 W/m^2, Batt at EOL	1050	87	1176	87

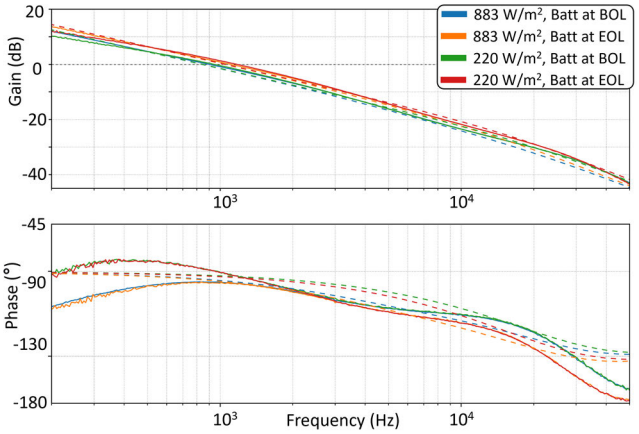

FIGURE 14. Bode diagram of the loop gain at VEOC mode (TV2(s)). Continuous line corresponds to experimental results and dashed line corresponds to theoretical results.

As it can be observed in Fig. 15, both the voltage and the current are zero initially since there is not power available from the SAS. Once the SAS turns on, the MPPT circuit forces the SAS to open-circuit operation point for approximately 80 ms and then start oscillating around the MPP properly. The oscillation frequency of the MPPT is around 20 Hz.

C. MPPT MODE: TRACKING

This test is carried out to verify that the buck converter follows the MPP when it varies over time. To perform the test, the SAS has been programmed so that MPP varies periodically from MPP1 = (27 V, 0.32 A) to MPP2 = (23 V, 0.42 A) in ten steps and 40 seconds. It should be noted that the steps programmed are limited by the resolution of the SA simulator. As shown in Fig. 16, the SAR input voltage (V_{SA} in green) and the current (I_{SA} in red) follows the programmed MPPs all the time. At t = 12 s cycle starts at MPP1, and then the MPPT circuit follows the MPP in each programmed step

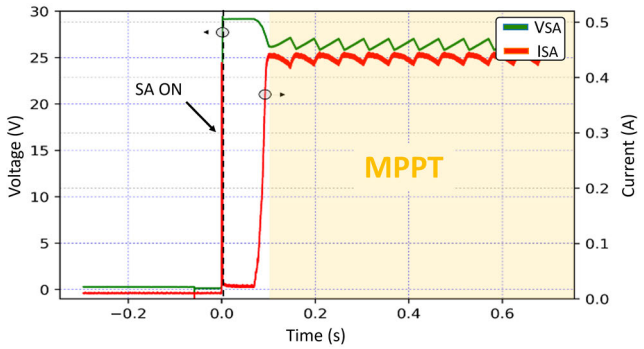

FIGURE 15. MPPT mode: start-up. Green line shows the SA voltage and the red line the SA current.

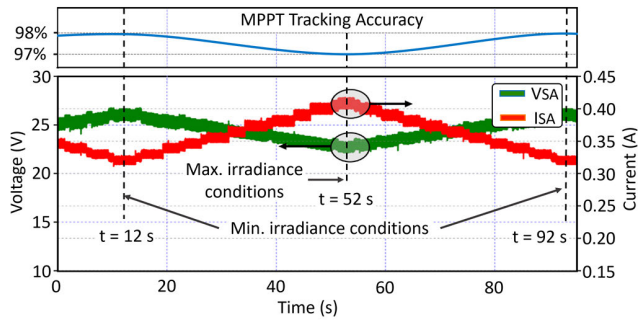

FIGURE 16. MPPT mode: tracking test. VSA (green) and ISA (red).

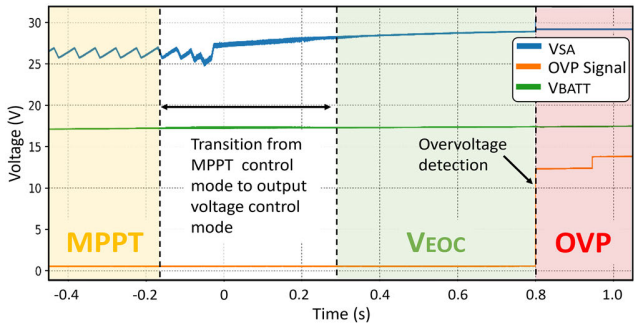

FIGURE 17. Change from MPPT mode to EOC mode. Overvoltage protection.

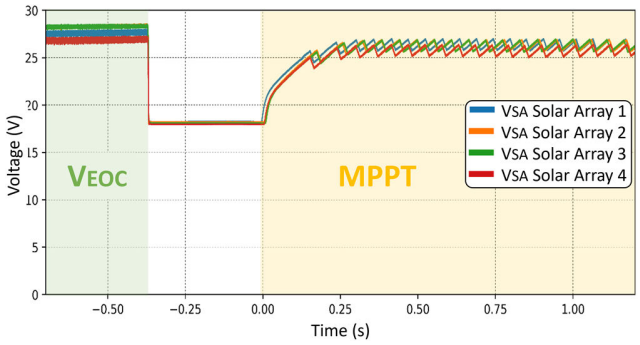

FIGURE 18. SAR change from output voltage control to MPPT mode.

to reach MPP2 at t = 52 s. Then, the I-V curve moves from MPP2 to MPP1 in ten steps during the following 40 seconds and again the MPPT circuit follow the MPP during all the time. The MPPT tracking accuracy was measured according to the EN50530 [30] been higher than 97% in all cases.

D. MODE TRANSITION: FROM MPPT TO EOC AND OVER VOLTAGE PROTECTION

This test shows the transition from the MPPT mode, performed by input voltage regulation, to battery end of charge control, achieved by output voltage regulation. The battery simulator has been configured as a low-capacity battery with an initial charge level of 95% to speed up the test. Fig. 17 shows that the converter starts in MPPT mode and battery reaches V_{EOC} at t = 0 s. At this point, the EOC loop takes over and SA voltage moves towards the open-circuit point providing less and less power. Finally, a battery overcharge fault is emulated (t = 0.8 s) and the OVP circuit isolates the SA. The SA will remain disconnected until the battery voltage drops below the preset limit.

E. MODE TRANSITION: FROM EOC TO MPPT. MULTIPLE PHASES

This test emulates a high-power step load, e.g., propulsion system turn-on, from a fully charged battery. The battery simulator has been programmed with a very low capacity to accelerate the test. As shown in fig. 18, four phases are initially in output voltage regulation and a step load takes

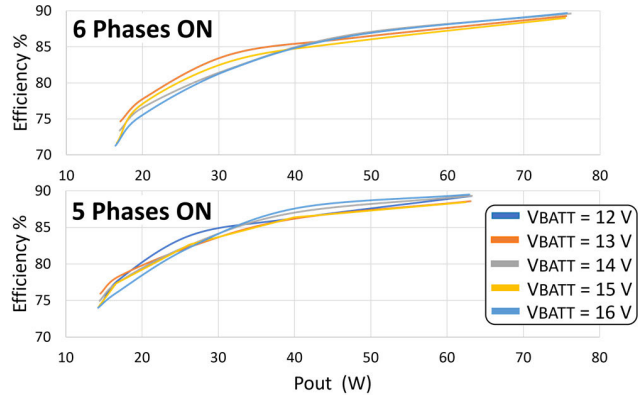

FIGURE 19. Efficiency results (n+1 hot redundancy): 5 and 6 phases.

place, increasing the duty cycle to the maximum, and forcing the SA to operate close to V_{EOC}. Once the MPPT control loop reacts, the SA moves towards the MPP and all phases provide full power from independent MPPT circuits.

F. SOLAR ARRAY REGULATOR EFFICIENCY

To conclude, the whole efficiency of the SAR has been measured with six (n+1) and five (n) active phases. Efficiency test have been performed with an input voltage of 26.7 V (VMPPT at 1.25 AU) and with an output power sweep. The efficiency has been obtained by dividing the converter output power by the converter input power. Fig. 19 shows the

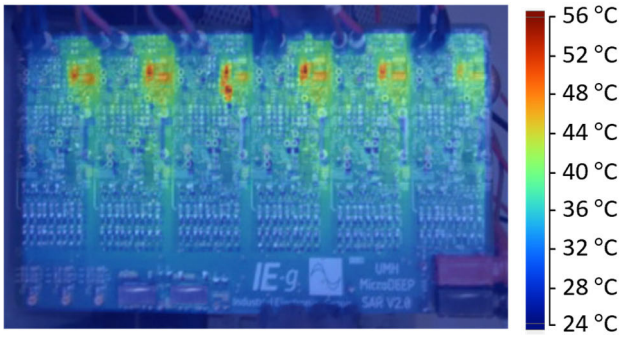

FIGURE 20. SAR thermal capture.

efficiency results measured as a function of the SAR output power and the battery voltage.

The results show that the highest efficiency obtained is slightly less than 90% at full power, which is consistent with the expected efficiency claimed in LT3845's datasheet under similar operating conditions.

The efficiency measurements have been complemented with a thermal image shown in Fig. 20, taken at a controlled ambient temperature of 24°C. Losses are mainly located in the switching section, output diodes and shunt resistors. Maximum temperature reached is less than 60 °C.

V. CONCLUSION

The design of a highly reliable and highly integrated MPPT solar array regulator for microsatellites has been presented. A fully functional (TRL4) prototype has been implemented following the ESA standards and requirements, and its operation has been validated under different conditions covering the whole operating range. The results show that the different control loops operate properly, working the buck converters on the MPP of the SAs when the batteries are not fully charged and regulating the VEOC output voltage when they are 100% charged.

N+1 hot redundancy scheme is considered, so that only five of the six available converters are needed to provide all the power required. As the battery is non-segregated and a critical part of the power subsystem, a redundant (triple majority voted) overvoltage protection circuit has been implemented individually for all phases. As a result, the design approach is tolerant to the failure of any of its components, as required by many space missions, including deep space missions. In a real mission, in addition, a reliability analysis will be needed to assure the high reliability of the presented design, but to perform this reliability analysis a detailed information of the mission, satellite structure and working conditions, printed circuit board layout and components used will be needed.

Despite the low power and the redundancy and fault-tolerant approach, the efficiency is close to 90% at full power, which is very remarkable. Finally, special care has been taken to provide a solution that accepts a fully space-qualified version using equivalent rad-hard components.

REFERENCES

[1] M. N. Sweeting, "Modern small satellites-changing the economics of space," *Proc. IEEE*, vol. 106, no. 3, pp. 343–361, Mar. 2018, doi: 10.1109/JPROC.2018.2806218.

[2] M. Shao, H. Zhou, S. G. Turyshev, C. Zhai, N. Saini, and R. Trahan, "A constellation of MicroSats to search for NEOs," *Proc. SPIE*, vol. 10769, Sep. 2018, Art. no. 107690K, doi: 10.1117/12.2322414.

[3] M. Yaqoob, A. Lashab, J. C. Vasquez, J. M. Guerrero, M. E. Orchard, and A. D. Bintoudi, "A comprehensive review on small satellite microgrids," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12741–12762, Oct. 2022, doi: 10.1109/TPEL.2022.3175093.

[4] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014, doi: 10.1109/TPEL.2014.2304561.

[5] N. W. van Onno and B. R. Doyle, "Design considerations and verification testing of an SEE-hardened quad comparator," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1859–1864, Dec. 2001.

[6] C. Torres, J. M. Blanes, A. Garrigós, D. Marroquí, and J. A. Carrasco, "Single point failure free interleaved synchronous buck converter for microsatellite electrolysis propulsion," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5371–5380, Oct. 2022, doi: 10.1109/JESTPE.2022.3174358.

[7] J.-E. Park, J.-K. Han, K.-B. Park, B.-H. Lee, and G.-W. Moon, "A new direct charging control for electrical power systems in low Earth orbit satellites," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 59, no. 3, pp. 2566–2578, Jun. 2023, doi: 10.1109/TAES.2022.3218495.

[8] M. Langer and J. Bouwmeester, "Reliability of CubeSats—Statistical data, developers' beliefs and the way forward," in *Proc. AIAA/USU Conf. Small Satell.*, Logan, UT, USA, Aug. 2016.

[9] M. Wirthlin, "High-reliability FPGA-based systems: Space, high-energy physics, and beyond," *Proc. IEEE*, vol. 103, no. 3, pp. 379–389, Mar. 2015, doi: 10.1109/JPROC.2015.2404212.

[10] A. Capel, D. O'Sullivan, and J.-C. Marpinard, "High-power conditioning for space applications," *Proc. IEEE*, vol. 76, no. 4, pp. 391–408, Apr. 1988, doi: 10.1109/5.4425.

[11] J. Bouwmeester and J. Guo, "Survey of worldwide pico- and nanosatellite missions, distributions and subsystem technology," *Acta Astronaut.*, vol. 67, nos. 7–8, pp. 854–862, Oct. 2010.

[12] A. Edpuganti, V. Khadkikar, H. Zeineldin, M. S. E. Moursi, and M. A. Hosani, "Comparison of peak power tracking based electric power system architectures for CubeSats," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2758–2768, May 2021.

[13] K. Yao, M. Ye, M. Xu, and F. C. Lee, "Tapped-inductor buck converter for high-step-down DC–DC conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 775–780, Jul. 2005.

[14] J. Faujdar, D. K. Gautam, and V. Verma, "A new converter for common mode noise reduction for EPS of a nano satellite," in *Proc. IEEE 1st Int. Conf. Smart Technol. Power, Energy Control (STPEC)*, Sep. 2020, pp. 1–6.

[15] O. Garcia, P. Alou, J. A. Oliver, D. Diaz, D. Meneses, J. A. Cobos, A. Soto, E. Lapena, and J. Rancano, "Comparison of boost-based MPPT topologies for space applications," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 49, no. 2, pp. 1091–1107, Apr. 2013.

[16] Y.-K. Chen, Y.-C. Lai, W.-C. Lu, and A. Lin, "Design and implementation of high reliability electrical power system for 2U NutSat," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 57, no. 1, pp. 614–622, Feb. 2021, doi: 10.1109/TAES.2020.3028488.

[17] O. Mourra, A. Fernandez, and F. Tonicello, "Buck boost regulator (B2R) for spacecraft solar array power conversion," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Palm Springs, CA, USA, Feb. 2010, pp. 1313–1319, doi: 10.1109/APEC.2010.5433399.

[18] C. Torres, J. M. Blanes, A. Garrigós, D. Marroquí, C. Orts, and J. A. Carrasco, "High-reliability solar array regulator proposal for harsh environments," in *Proc. IEEE 21st Medit. Electrotech. Conf. (MELECON)*, Jun. 2022, pp. 698–702, doi: 10.1109/MELECON53508.2022.9842931.

[19] A. Barchowsky, A. Amirahmadi, C. Stell, E. Merida, G. Bolotin, A. Ulloa-Severino, and G. Carr, "A class of GaN-based, radiation-hardened power electronics for Jovian environments," in *Proc. Eur. Space Power Conf.*, Juan-les-Pins, France, 2019.

[20] W. Denzinger, "Electrical power system of globalstar," in *Proc. Eur. Space Power Conf.*, 1995.

[21] W. Denzinger and W. Dietrich, "Generic 100 V/high power bus conditioning," in *Proc. 7th Eur. Space Power Conf.*, 2005.

[22] A. F. Boehringer, "Self-adapting DC converter for solar spacecraft power supply," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-4, no. 1, pp. 102–111, Jan. 1968, doi: 10.1109/TAES.1968.5408938.
[23] A. Garrigós, J. L. Lizan, J. M. Blanes, and R. Gutierrez, "Exploring the use of the LT3480 (RH3480) circuit as low-power, low-voltage solar array regulator," in *Proc. 10th Eur. Space Power Conf.*, vol. 719, 2014, p. 35.
[24] N. Zhang and D. Li, "Loop Response considerations in peak current mode buck converter design," Texas Instrum., Dallas, TX, USA, Appl. Rep. SLVAE09B, Apr. 2018.
[25] A. Kuperman, M. Sitbon, S. Gadelovits, M. Averbukh, and T. Suntio, "Single-source multi-battery solar charger: Analysis and stability issues," *Energies*, vol. 8, no. 7, pp. 6427–6450, Jun. 2015, doi: 10.3390/en8076427.
[26] M. Sitbon, J. Leppäaho, T. Suntio, and A. Kuperman, "Dynamics of photovoltaic-generator-interfacing voltage-controlled buck power stage," *IEEE J. Photovolt.*, vol. 5, no. 2, pp. 633–640, Mar. 2015, doi: 10.1109/JPHOTOV.2014.2379094.
[27] W. Knorr, "Power system of METEOSAT second generation," in *Proc. 5th Eur. Space Power Conf.*, Noordwijk, The Netherlands, 1998.
[28] *Electrical and Electronic*, Standard ECSS-E-ST-20C Rev.2, Apr. 2022.
[29] *Derating—EEE components*, Standard ECSS-Q-ST-30-11C Rev.2, Jun. 2021.
[30] T. R. Wellawatta and S. -J. Choi, "Regulated incremental conductance (r-INC) MPPT algorithm for photovoltaic system," *Korean Inst. Power Electron. J. Power Electron.*, vol. 19, no. 6, pp. 1544–1553, 2019, doi: 10.6113/JPE.2019.19.6.1544.
[31] *SAFT MP174865xlr Rechargeable Li-Ion Cell—Datasheet*. Accessed: Aug. 1, 2023. [Online]. Available: https://www.saftbatteries.com/products-solutions/products/mp-vl-batteries-launchers
[32] *Azurspace 3G30C Triple Junction Solar Cells—Datasheet*. Accessed: Aug. 1, 2023. [Online]. Available: http://www.azurspace.com/images/0003429-01-01_DB_3G30C-Advanced.pdf

CRISTIAN TORRES was born in Elche, Spain, in 1993. He received the B.Sc. degree in telecommunications technology engineering and the M.Sc. degree in telecommunication engineering from the Miguel Hernández University of Elche (UMH), Elche, in 2019 and 2020, respectively, where he is currently pursuing the Ph.D. degree in industrial technologies, thanks to a grant from the European Social Fund and Generalitat Valenciana.

He spent a research period with the Centre for Research on Microgrids, Aalborg University, Denmark, in 2021, as a Predoctoral Researcher. His main research interests include space power systems and industrial electronics.

JOSÉ M. BLANES was born in Elche, Spain, in 1974. He received the M.Sc. degree in telecommunication engineering from Universidad Politécnica de Valencia, Valencia, Spain, in 1998, and the Ph.D. degree in industrial technologies from the Miguel Hernández University of Elche (UMH), Elche, in 2011. He is currently an Associate Professor with the Department of Materials Science, Optics, and Electronics Technology, UMH. His main research interests include space power systems and industrial electronics.

AUSIÀS GARRIGÓS (Senior Member, IEEE) was born in Xixona, Spain, in 1976. He received the M.Sc. degree in electronic engineering from the University of Valencia, Valencia, Spain, in 2000, and the Ph.D. degree in space power electronics from the Miguel Hernández University of Elche (UMH), Elche, Spain, in 2007. He spent research periods with CERN, Switzerland, from 2002 to 2004; the ESA, The Netherlands, in 2008; and the University of Strathclyde, U.K., in 2015. He is currently a Professor with the Department of Electronics Technology, UMH. He participated in more than 30 research and technology transfer projects and coauthored around 90 international publications. Most of them related to power electronics. His main research interests include space power electronics and their ancillary electronic systems.

DAVID MARROQUÍ was born in Elche, Spain, in 1990. He received the M.Sc. degree in industrial engineering and the Ph.D. degree in industrial technologies from the Miguel Hernández University of Elche (UMH), Elche, in 2015 and 2020, respectively. He spent a research period with the Center of Reliable Power Electronics, Aalborg University, Denmark, in 2018, as a Predoctoral Researcher, and another period with the European Space Agency, Noordwijk, The Netherlands, during 2021–2022, as a Postdoctoral Researcher. He is currently an Assistant Professor with the Department of Materials Science, Optics, and Electronics Technology, UMH. His research interests include space power systems, industrial electronics, and electronics reliability.

JOSÉ A. CARRASCO received the M.Sc. degree in physics and the Ph.D. degree in electronics engineering from Universidad de Valencia, Valencia, Spain, in 1991 and 1996, respectively.

After a period of two years as a Power Electronics Researcher with the European Space Agency, European Space Research and Technology Centre, Noordwijk, The Netherlands, he joined Universidad de Valencia as a Lecturer, in 1993, and the Miguel Hernández University of Elche, Spain, in 1998, as a Professor. In 2005, he co-founded the company Embedded Instruments and Systems, where he is the CEO. He currently holds a Full Professorship in the electronics technology area. He has participated in several projects on power electronics, mixed (analog/digital) designs, and instrumentation for space applications, including four in-orbit technology and scientific demonstrations. His research interests include robust electronics for power, instrumentation, and control systems in aerospace applications.