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RESEARCH ARTICLE

High Current Density Vertical Nanowire TFETs With $I_{60} > 1\,\mu A/\mu m$

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ABSTRACT We present experimental data for a vertical, 22-nm-diameter InAs/(In)GaAsSb nanowire Tunnel Field-Effect Transistor that exhibits the highest reported I_{60} of 1.2 μA/μm, paving the way for low power applications. The transistor reaches a minimum subthreshold swing of 43 mV/dec at $V_{DS} = 300$ mV with a sub-60 mV/dec operation over a wide current range. Combined with a high transconductance of 205 μS/μm, the ON-current for the same device is 18.6 μA/μm at $V_{DS} = 300$ mV for I_{OFF} of 1 nA/μm.

INDEX TERMS Vertical nanowires, III-V, TFETs, steep-slope, source engineering.

I. INTRODUCTION

TFETs employ band-to-band tunneling (BTBT) and operate with subthreshold swing (SS) below 60 mV/dec, a physical limitation for MOSFETs. The associated possibility to operate at reduced voltage makes TFETs a viable alternative to MOSFETs in low power applications [1], [2], [3]. A variety of material systems, including Si, strained Si, SiGe, carbon nanotubes, and III-V materials have been utilized to demonstrate TFETs [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. Among them, III-V heterostructure semiconductors have emerged as the most promising, due to their low effective mass, direct bandgap, and flexible band engineering supporting detailed heterostructure design at the source-channel junction [14], [15], [16]. For implementation, the gate-all-around architecture (GAA) provides the best electrostatic control and combined with the ease of growing vertical III-V heterostructure nanowires with small footprint and excellent scalability, vertical III-V nanowire TFETs emerge as strong contenders for MOSFETs at low power levels [17], [18].

In the recent international roadmap for devices and systems (IRDS), GAA and vertical III-V nanowire TFETs are considered candidates for extending Moore's law [19]. The report notes two constraints for TFETs as MOSFET replacement, namely, the inability to exhibit SS < 60 mV/dec for a wide range of current levels and the on-state current being too low for reasonable performance. In this regard, I_{60} (defined as the highest current level where the subthreshold characteristics exhibit a transition from sub- to super-60 mV/decade behavior) is a key metric. For MOSFETs, the current at threshold voltage is around 1 μA/μm [20]. Thereby, for TFETs to be competitive against MOSFETs in low-power applications, I_{60} of 1-10 μA/μm is needed and further efforts are required to balance the on-state and off-state performance. Despite the potential of compound semiconductors for achieving high I_{60} and sharp switching behaviour, their practical demonstration has so far been hindered by the challenges of obtaining high-quality gate-dielectrics and defect-free tunnel junctions [2].

In this work, we demonstrate an enhancement-mode vertical InAs/(In)GaAsSb nanowire TFET by carefully engineering the heterostructure band alignment with the introduction of an InAsSb segment and source doping selection. Measured device performance demonstrates record I_{60} of 1.2 μA/μm at V_{DS} of 500 mV and is favorably compared with other TFETs, showing a clear improvement in device characteristics. Furthermore, at V_{DS} of 0.1 V, the device shows three orders of current with SS < 60 mV/dec, with a minimum achieved SS of 43 mV/dec at V_{DS} of 0.3 V. The ON-current (I_{ON}) of the device is 18.6 μA/μm at $V_{DS} = 300$ mV and 40 μA/μm at

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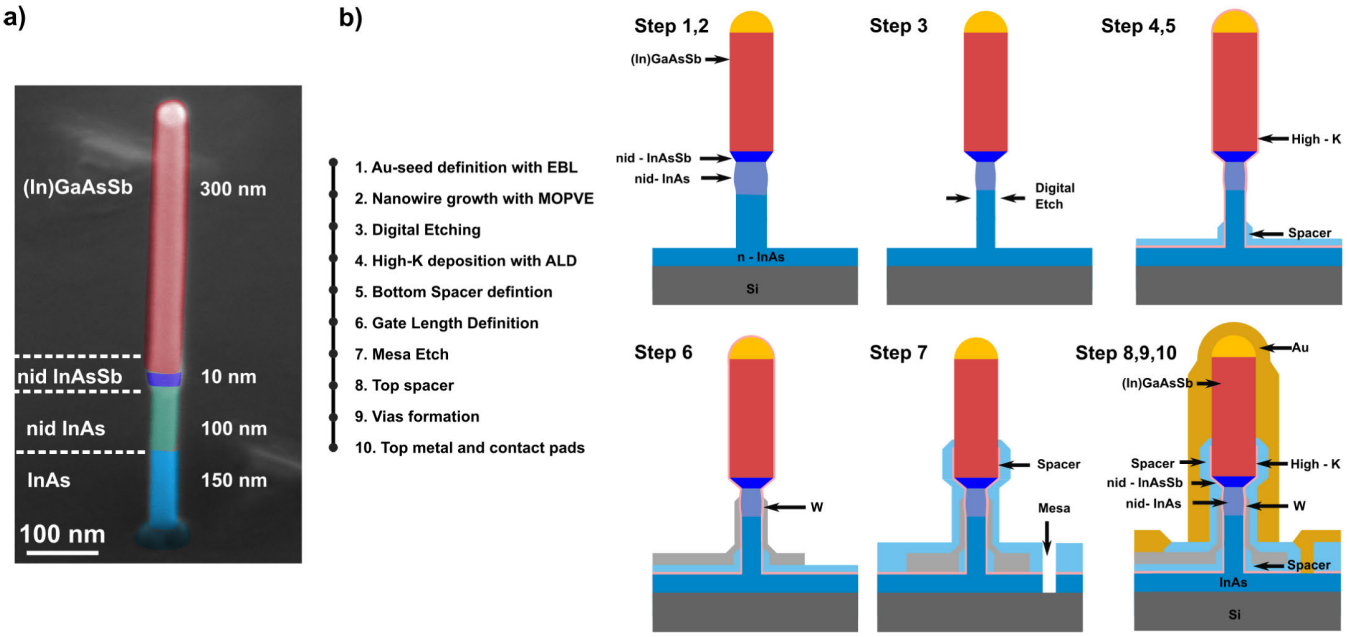

FIGURE 1. **(a) SEM image of vertical III-V nanowire used for TFET fabrication (b) Flow chart of processing with schematic illustration of device cross section at different process steps indicated by the numbers above the illustrations.**

V_{DS} = 500 mV for off-current (I_{OFF}) of 1 nA/μm, showing a very good on-state performance.

II. FABRICATION

A flow chart of processing along with schematic diagram of device at key process steps are shown in Fig 1 (b).The starting substrate was highly resistive Si (111) substrate ($\rho > 12k\Omega m$) integrated with 260 nm n^+-InAs buffer layer grown on top. Au dots with 24-nm diameter were prepatterned on the InAs layer by electron beam lithography (EBL) and polymethyl methacrylate-based lift-off. The InAs/(In)GaAsSb nanowires were grown at 470 °C using the Au dots with metal-organic vapor phase epitaxy (MOVPE) based on vapor-liquid-solid (VLS) process. First, 150-nm-long n-doped InAs nanowires were grown as the drain material using precursors of trimethylindium (TMIn) and arsine (AsH_3). Tetraethyltin (TESn) was used for Sn doping with a ratio of TESn/TMIn = 5, corresponding to an estimated doping of 1×10^{19} cm^{-3} [15]. Non-intentionally doped (nid) InAs channels with a length of 100 nm were subsequently grown, with an estimated background doping of 1×10^{17} cm^{-3}. This was followed by 300-nm-long p-doped (In)GaAsSb source segments using precursors of trimethylgallium (TMGa), trimethylantimony (TMSb), and arsine (AsH_3) with a gas phase composition of $AsH_3/(AsH_3+TMSb)$ = 0.18. Here, diethylzinc (DEZn) was utilized as the p-type dopant in the source material with an estimated doping of 1.4×10^{19} cm^{-3}.

A SEM image of the nanowire with different segments and the positions of the heterostructure is shown in Fig. 1 (a). A significant modification of the source segment was done on the presented TFET structure from our previous work [21], [22]. GaSb was removed from the source segment and a nid-InAsSb segment is introduced as part of the channel between the source and the InAs segment. This is achieved by delaying the Zn dopant introduction in the source by 8s (corresponding to an increase of ∼10 nm in length from the heterostructure). In addition, the nominal Zn doping is increased by 40% from 1×10^{19} cm^{-3} to 1.4×10^{19} cm^{-3}. The change in both Zn doping position and concentration lowers the valence and conduction band in the source adjacent to the tunnel junction and thus reduces the effective tunnel barrier and increases the tunneling energy window, thereby increasing the tunnelling transmission probability [23], [24]. Fig. 2 compares the bulk band-edge simulation of the heterostructure presented in this work along with our previous generation device at V_{DS} of 300 mV [21]. The simulation shows that the modification to the heterostructure results in the tunneling energy window, ΔE, being increased while the tunnelling length has been reduced by more than 30% (Z_1 (6.1 nm) < Z_2 (9.1 nm) in Fig. 2). This is expected, as InAsSb has narrower bandgap in comparison to InAs and thereby it reduces the tunneling length. Similar design has been utilized in Esaki diodes as well, where the incorporation of a narrow bandgap material in between the p and n segments increases the current density [25]. Furthermore, due to Fermi level pinning close to the conduction band edge of InAs in our previous device, the threshold voltage observed in those InAs channel TFETs were negative, leading to a depletion mode device. We mitigated the Fermi level pinning by switching part of the channel material to InAsSb and observe a positive threshold voltage and an enhancement mode for the new devices. The removal of the GaSb segment decreased the thermal budget of the growth as well.

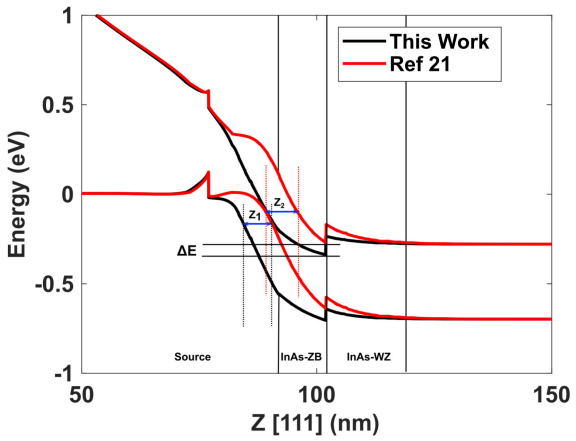

FIGURE 2. Bulk band-edge simulation of heterostructure presented in this work compared with our previous generation device [21] at V_{DS} of 300 mV.

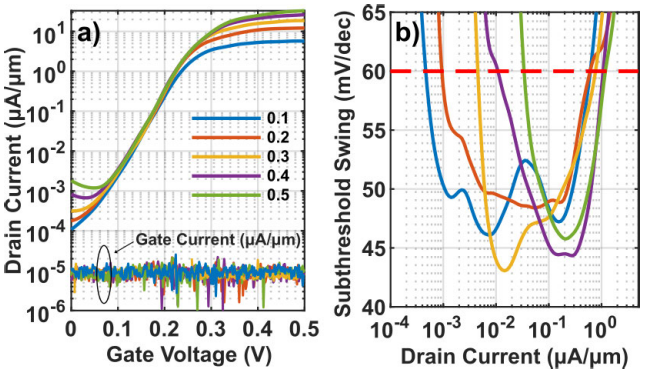

FIGURE 3. (a) Measured transfer characteristics of the device for V_{DS} of 0.1 to 0.5 V with steps of 0.1 V and (b) respective subthreshold swing vs drain current. The lowest slope is 43 to 48 mV/dec for V_{DS} of 0.1 to 0.5 V, respectively.

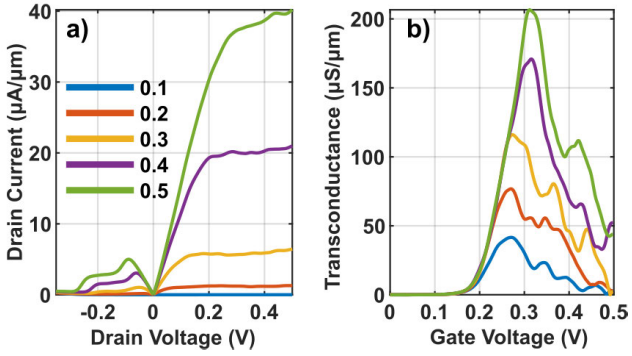

FIGURE 4. (a) Output characteristics of the device. The maximum current of 40 $\mu A/\mu m$ was obtained at $V_{DS} = V_{GS} = 0.5$ V. (b) The transconductance of transistor for V_{DS} of 0.1 to 0.5 V with steps of 0.1 V, reaching a maximum of 205 $\mu S/\mu m$ at $V_{DS} = 0.5$ V.

After the growth, three successive cycles of digital etching with ozone oxidation and reduction in citric acid were performed selectively to reduce the InAs segment diameter from 40 nm to the desired diameter of 22 nm. After digital etching, a trilayer of 1 nm Al_2O_3/ 3 nm HfO_2/ 30 nm Al_2O_3 were deposited using atomic layer deposition (ALD) at temperatures of 300 °C, 120 °C, and 100 °C respectively. After the trilayer was deposited, S1813 photoresist was spun and etched in RIE with oxygen plasma to define the first spacer height. After this definition, the 30-nm-thick Al_2O_3 is etched away in HF (1:400), leaving 1 nm Al_2O_3/ 3 nm HfO_2 bilayer behind which forms the gate dielectric, with an effective oxide thickness (EOT) of 1 nm. The nanowires were sputtered with 30-nm-thick Tungsten to form the gate layer. The gate length was defined by spin coating the sample with S1813 photoresist and etching the resist back in RIE to the desired gate length. The exposed Tungsten was removed with SF_6/ Ar plasma in RIE. The effective gate length was about 100 nm. In the following step, the gate pad was defined using UV lithography and RIE to remove Tungsten in the exposed areas. A mesa formation step was introduced to etch away the first spacer and the underlying InAs to isolate the individual nanowires. This was followed by ALD deposition of 10 nm Al_2O_3 at 100 °C as a second spacer for isolating the gate from the source.Via-holes were defined with UV lithography and RIE to make contacts. High-k was removed from the via with HF (1:400). Finally, contacts to the nanowires were made by depositing 10 nm Ni and 200 nm Au. The probe pads are defined using UV lithography and wet etching.

III. RESULTS AND DISCUSSION

The transistor is characterized in a common source configuration with the top contact grounded. The currents presented in the paper are normalized to the circumference of the 22 nm diameter InAs segment. Fig. 3(a) shows the transfer characteristics; the device exhibits a good electrostatic control, confirmed by the low drain-induced barrier lowering of 8 mV/V. The gate current is two orders lower than the drain current. Effects of ambipolarity are observed for $V_{GS} < -200$ mV. As seen in Fig. 3(b) the devices achieve SS below 60 mV/dec for current levels between 0.5 nA/μm to 1.2 μA/μm. The lowest SS is 43 mV/dec measured at V_{DS} of 0.3 V. The device shows I_{ON} of 18.6 μA/μm at V_{DS} of 0.3 V for $I_{OFF} = 1$ nA/μm. To confirm the sub-60 operation current levels, we swept the gate bias in both directions. The same I_{60} values was measured regardless of gate sweep direction, indicating that trapping in the gate oxide is not responsible for sub-thermal SS observed. We observe that $I_{60,min}$ increases with the V_{DS} due to increased ambipolar current and slight increase in source-drain leakage current. The fluctuations seen in Fig. 3(b) is attributed to oxide defects [26].

Fig. 4(a) shows the output characteristics of the device, exhibiting a superlinear behaviour. The presence of negative differential resistance (NDR) with peak to valley current ratio (PVCR) of 11.1 at V_{GS} of 0.5 V, confirms the presence of a high-quality tunneling junction within the TFET. The slight fluctuations in the drain current are attributed to discrete charge trapping in oxide and interface defects present in the nanowire [26]. The saturation current reaches a maximum

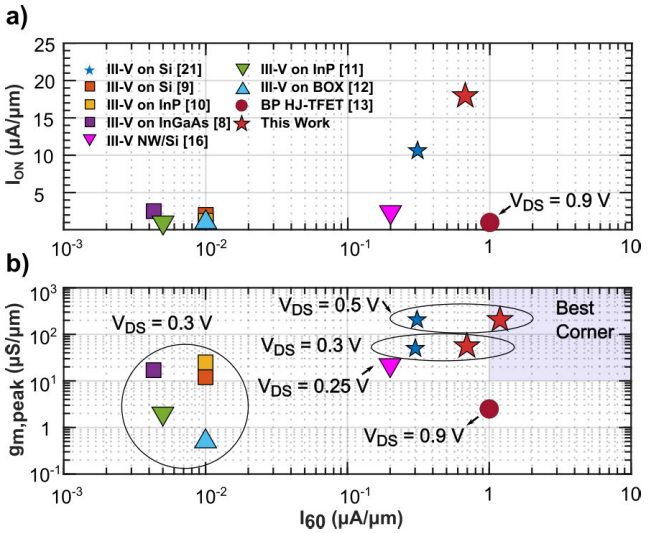

FIGURE 5. a) I_{ON} versus I_{60} at V_{DS} of 0.3 V unless stated otherwise and b) peak transconductance versus I_{60} used for different types of state-of-the-art TFET based on both homo- and heterojunction designs. Among the presented devices, our TFET features the highest I_{60}.

of 40 $\mu A/\mu m$ at $V_{DS} = 0.5$ V, while R_{ON} is evaluated to be 12 $k\Omega\mu m$ with a maximum transconductance (g_m) of 205 $\mu S/\mu m$ at $V_{DS} = 0.5$ V (Fig. 3(b)).

Our previous generation device achieved a minimum SS of 48 mV/dec at V_{DS} of 300 mV and I_{60} of 0.31 $\mu A/\mu m$ at V_{DS} of 500 mV [21]. In comparison, we improve minimum SS by 5 mV/dec and increase I_{60} by 0.89 $\mu A/\mu m$. A reduction of 5 mV/dec in SS increases the gate voltage range under which device remains in subthermal operation by 44 mV. Alternatively, by quadrupling the I_{60} from 0.31 $\mu A/\mu m$ to 1.2 $\mu A/\mu m$, we increase the gate voltage window by 30 mV. Based on this observation, we recommend improving minimum SS of TFETs targeting voltage mode circuit operation while improving I_{60} might be more important for current mode circuit operation utilizing the improved transconductance efficiency.

For benchmarking, we consider the balance between the on- and off-state, highlighted by the I_{ON}, g_m and SS. A low SS is a result of high energy filtering of the Fermi-Dirac exponential tail of the carrier distribution in the source. With higher source doping, part of this exponential tail is no longer filtered and thereby deteriorates SS, although it leads to higher g_m and I_{ON}. The minimum SS depends on the bandgap, V_{DD} and I_{OFF}, which are determined by the targeted application [20], [24]. Therefore, to compare various TFET configurations presented in literature, we use I_{60}, which is independent to V_{DD}, I_{OFF} or the gate work function. Fig. 5(a) shows the benchmark of I_{ON} vs I_{60} for different state-of-the-art TFETs at V_{DS} of 0.3 V, unless stated otherwise. I_{ON} is dependent on the maturity level of technology, thereby we find derivatives of transfer characteristics in the on-state to be more appropriate metric than ON currents [27]. Fig. 5(b) shows peak g_m vs I_{60}. Among the devices presented here, the reported TFET exhibits the highest I_{60}, I_{ON} and peak g_m, demonstrating great promise for low-power applications. The presented data shows that fine tuning of the device material parameters has the potential to improve the TFET device performance.Additionally, a post-fabrication annealing of drain and source contacts could further improve the device's performance [28].

IV. CONCLUSION

We have demonstrated a vertical InAs/(In)GaAsSb nanowire TFET with the ability to operate below 60 mV/decade over a wide current range. By optimizing the source material selection, we achieved the highest I_{60} of 1.2 $\mu A/\mu m$ at V_{DS} of 0.5 V. The combination of high I_{60} and minimum SS current of 0.28 $\mu A/\mu m$ at V_{DS} of 0.5 V with a high transconductance of 205 $\mu S/\mu m$ results in an almost 2x I_{ON} increase and shows promise for low power applications.

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