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RESEARCH ARTICLE

A Hybrid Low Capacitance Modular Multilevel Converter for Medium Voltage PMSM Drive and Its Control Method

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ABSTRACT The main technical challenge of the medium-voltage Permanent Magnet Synchronous Motor (PMSM) drives with Modular Multilevel Converter (MMC) is the serious low-frequency fluctuation on the capacitor voltages. Therefore, a Hybrid Low Capacitance MMC (HLC-MMC) topology based on horizontal sub-module (SM) interconnection is proposed in this paper. Based on the three-phase symmetry of the input fluctuation currents of the sub-modules of the HLC-MMC, a fluctuation current coupling channel is established between the sub-modules with the same horizontal position of the three phases. The fluctuation currents are coupled and cancelled in the interconnection channel, and the amplitude of the fluctuation currents flowing into the sub-module capacitors is reduced. A switch tube in series with the DC bus is turned on and off at a regular frequency. The average DC voltage component in the bridge arm voltage is reduced and the voltage ripple of the capacitor is reduced. Then, a new control method is proposed for the HLC-MMC topology, where the energy is equalized between the upper and lower bridge arms of each stage by adjusting the fundamental frequency current components. The switching frequency of the series switches on the DC bus is controlled by duty cycle, and the measured average voltage of the control sub-module capacitors is equal to the reference voltage value. The overall energy of the system is balanced and the sub-module capacitor voltage ripple is further reduced. The correctness and effectiveness of the topology and the proposed control method are verified by simulation.

INDEX TERMS Capacitor voltage ripple suppression, hybrid low capacitance topology, low-frequency operation, modular multilevel converter, medium voltage PMSM drives.

I. INTRODUCTION

Modular Multilevel Converter (MMC) has attracted much attention due to its low harmonic distortion rate of the output voltage waveform, easy scalability and redundant design [1], [2], [3]. Compared with the cascaded H-bridge type motor drive system, the MMC motor drive system does not need to be equipped with a large phase-shifting transformer and can realize four-quadrant operation of the motor, which is more suitable for medium voltage high-power motor drives.

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However, one of the main technical challenges of MMC-based motor drives is the problem of sub-module capacitance voltage fluctuations during low-frequency operation [4]. During low-speed operation or start-up operation of MMC motor drive systems, lower operating frequencies can lead to large fluctuations in the MMC capacitor voltage, exacerbating the internal power imbalance of the MMC, which can lead to equipment damage when the fluctuations are severe [5], [6].

The fluctuation of the MMC sub-module capacitor voltage grows inversely proportional to the output frequency [7], making it difficult for the MMC to drive constant torque motors during low-speed. It is more suitable for fan or

blower type loads, which usually require high starting torque to overcome motor static friction. Therefore, in order to provide sufficient torque in the low-speed range, methods must be used to attenuate the SM capacitor voltage ripple. Direct injection of high-frequency common-mode voltage into the three-phase modulating wave of the MMC, along with indirect injection of high-frequency circulating current into the phase bridge arm of the MMC, coordinated with common-mode voltage of the same frequency, is by far the most effective method of capacitor voltage fluctuation suppression. The injected voltage and current create a high-frequency power exchange between the upper and lower bridge arms, allowing the SM capacitor to charge and discharge more frequently, thus reducing voltage fluctuations. However, the injected common-mode voltage increases the insulation stress in the motor windings and generates leakage currents through the motor bearings, which can seriously harm the motor. In addition, the injected circulating current can significantly increase the current stress of the switching devices and increase the losses of the system.

In recent years, scholars at home and abroad have conducted some degree of research on the problem of sub-module capacitor voltage fluctuation during low frequency operation of MMC motor drive systems. In [8], an improved circulating current injection method was proposed, which cannot completely eliminate the capacitor voltage ripple but limits the voltage ripple to a certain range. In [9], a hybrid injection method based on a quasi-resonant controller for a full-bridge MMC is proposed to obtain better injection performance with circulating current tracking. In [10], the error between the reference current and the actual circulating current is evaluated and an additional parameter is introduced in the reference circulating current to enhance the suppression of the MMC sub-module capacitor voltage fluctuations. In [11], a low-speed and start-up coordination strategy for MMC-based motor drives is proposed to optimally coordinate the injected common-mode voltage and the circulating current with the average capacitance voltage, improving the safety margin of the device.

In addition, some scholars have addressed the problem of capacitor voltage fluctuation under low-frequency operation of MMC from the perspective of improving the topology. In [12], a novel back-to-back type MMC solution is proposed. The net-side MMC is controlled as a DC current source, and the ripple magnitude of the sub-module capacitor voltage is basically constant when the MMC frequency is reduced. In [13], a novel device combining a thyristor-based six-pulse controllable rectifier with a waveshaper-based MMC (WS-MMC) is proposed. Each phase of the converter consists of a WS and a director valve, and the phases are connected in series to form a common direct current path. The capacitor voltage ripple at low frequency is stayed within the specified limit. In [14], additional circuitry is added between the sub-modules of the adjacent bridge arms of the MMC to construct energy channels, and the fluctuating power of the bridge arms can be fully decoupled by bi-directional power transfer between the adjacent bridge arms, and the amount of fluctuation of the sub-module capacitance voltage is reduced. The improved topology adds some cost compared to the optimized modulation, but avoids the injection of circulating and common mode voltages [15], [16].

In order to solve the problem of large capacitor voltage ripples under low frequency operation conditions in modular multilevel permanent magnet synchronous motor drive systems, a Hybrid Low Capacitance MMC (HLC-MMC) topology based on horizontal SM interconnections and its control method are proposed in this paper. The proposed HLC-MMC topology and its control method can effectively reduce the MMC capacitor voltage ripple and output current harmonics under low-frequency operation. The rest of this paper is described as follows. In Section II, the topology and control method of the conventional MMC motor drive system are presented. In Section III, the topology of HLC-MMC motor drive system is proposed and its working principle is analyzed. In Section IV, the capacitor voltage fluctuations of conventional MMC and HLC-MMC are analyzed in detail. In Section V, the control scheme of the HLC-MMC motor drive system is presented. In section VI, the simulation results are analyzed. Finally, in Section VII, the article is briefly summarized.

II. CONVENTIONAL MMC MOTER DRIVE SYSTEM

A. TOPOLOGY

The topology of a conventional three-phase MMC motor drive system is shown in Fig. 1 [17]. Each phase of the three-phase MMC (a, b, and c represent phases A, B, and C, respectively) contains two bridge arms, each bridge arm contains N identical sub-modules and a bridge arm inductor L_m, which are connected in series. The AC side has a three-phase permanent magnet synchronous motor and a half-bridge sub-module, which consists of two switches $Q1$, $Q2$, and a sub-module capacitor C.

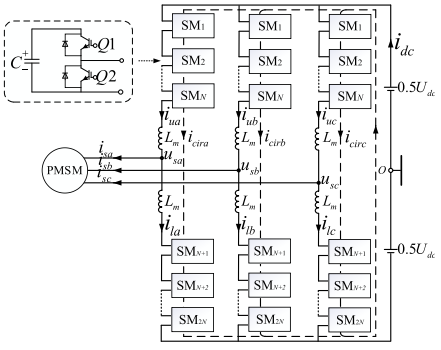

FIGURE 1. Conventional MMC motor drive system topology.

B. CONTROL STRATEGY

The overall control block diagram of the conventional three-phase MMC motor drive system is shown in Fig. 2.

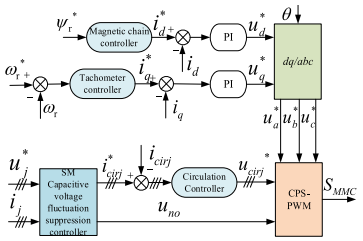

FIGURE 2. Control block diagram of conventional MMC motor drive system.

The reference signals and of the current inner loop are generated by the speed outer loop with the given magnetic chain, and then the three-phase modulating waves, and required for MMC control are generated by the control of the current inner loop in the d-q coordinate system, which is modulated by the CPS-SPWM to generate the switching control signal S_{MMC} to realize the normal drive of the motor.

In order to suppress the sub-module capacitance voltage fluctuation of the MMC, the suppression strategy of injecting common mode voltage and circulating current is used to generate the modulating wave correction amount and circulating current reference value from the three-phase modulating wave and three-phase output current, and then the subsequent circulating current control is used to finally achieve the purpose of suppressing the sub-module capacitance voltage fluctuation.

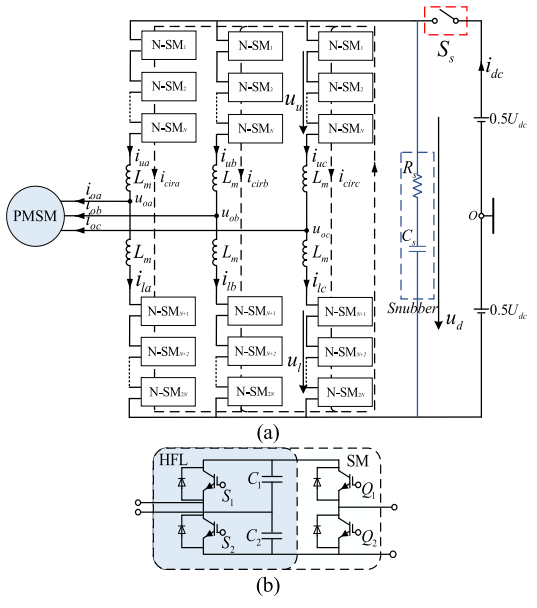

FIGURE 3. HLC-MMC motor drive system topology: (a)Main topology (b)N-SM structure.

III. HLC-MMC PERMANENT MAGNET SYNCHRONOUS MOTER DRIVE SYSTEM

A. HLC-MMC TOPOLOGY

The HLC-MMC motor drive system topology proposed in this paper is shown in Fig. 3(a), where a series switch S_s is inserted between the conventional MMC and the DC voltage source to connect or disconnect the MMC from the DC power supply. Since the switching of the series switch S_s causes a discontinuous DC current, an RC buffer circuit is added in parallel with the MMC to filter the switching voltage harmonics. The capacitor equivalent of the half-bridge type sub-module is replaced with two capacitors in series and a new half-bridge circuit is added to form a new type of sub-module (N-SM), as shown in Fig. 3(b), where three N-SMs in the same horizontal position of each phase of the MMC are interconnected together through the three side windings of a high frequency transformer (HFT) with a 1:1:1 ratio of the HFT. The newly added half-bridge circuit in the N-SM forms a high frequency link (HFL) circuit with the HFT, providing a channel for the fluctuating current coupling of the three-phase sub-module.

B. WORKING PRINCIPLE OF HLC-MMC

Regarding the hybrid low capacitance MMC circuit, each phase of which consists of two bridge arms, upper and lower, connected by two bridge arm inductors L_m. Each bridge arm is composed of N N-SMs, u_d is the buffer circuit terminal voltage, u_{oj} and i_{oj} are j-phase output phase voltages and currents, u_{uj}, i_{uj} and u_{lj}, i_{lj} denote j-phase voltages and currents of the upper and lower bridge arms, respectively, and the subscripts $j = a, b, c$. U_{dc} is the DC supply voltage and i_{dc} is the DC supply current. U_{cj} is the average voltage of the capacitors in the sub-module, derived from $U_{cj} = U_{dc}/N$. According to Kirchhoff's voltage law, the following voltage relations exist:

$$\begin{cases} u_{oj} = \dfrac{1}{2}(u_{lj} - u_{uj} - L\dfrac{di_{oj}}{dt}) \\ u_{dj} = u_{lj} + u_{uj} + 2L\dfrac{di_{cirj}}{dt} \end{cases} \tag{1}$$

where $i_{cirj}(j = a, b, c)$ is defined as the phase circulation current, which is obtained from $i_{cirj} = 1/2(i_{uj} + i_{lj})$. In addition, the DC supply current i_{dc} can be calculated by summing the three phase circulating currents, and the output current i_{oj} of the MMC is equally distributed to the upper and lower bridge arms. Combining the circulating current components i_{cirj}, the j-phase current through the upper and lower bridge arms can be expressed as:

$$\begin{cases} i_{uj} = i_{cirj} + 1/2 i_{oj} \\ i_{lj} = i_{cirj} - 1/2 i_{oj} \end{cases} \tag{2}$$

According to [18], The j-phase output AC voltage and current can be written as:

$$u_{oj} = U_{ojm}\cos(\omega t) \tag{3}$$

$$i_{oj} = I_{ojm}\cos(\omega t - \varphi) \tag{4}$$

where U_{ojm} and I_{ojm} are the amplitude, ω is the output angular frequency, and φ is the phase lag angle. The output voltage amplitude U_{ojm} can also be expressed as:

$$U_{ojm} = 1/2 mU_{dc} \tag{5}$$

where m denotes the modulation index that varies from 0 to 1.

In a motor drive system, a constant m/ω ratio is always maintained. Assuming $m = 1$ at rated motor speed, the modulation index at any motor speed can be expressed as:

$$m = \omega/\omega_{rated} \tag{6}$$

If the series switch S_s remains closed, u_d equals U_{dc}. The j-phase average bridge arm voltage can be approximated as:

$$\begin{cases} u_{uj} = 1/2 U_{dc}(1 - m\cos(\omega t)) \\ u_{lj} = 1/2 U_{dc}(1 + m\cos(\omega t)) \end{cases} \tag{7}$$

Series switch S_s conducts and turns off at the frequency of f_h, where $f_h = 1/T_h$, and T_h is the S_s switching period. When S_s conducts, u_d equals U_{dc} and the loop current i_{cirj} is $1/3 I_{dc(rated)}$, therefore, i_{dc} equals $I_{dc(rated)}$. when S_s turns off, u_d is controlled as $2U_{ojm}$, when i_{cirj} and i_{dc} are 0. The current i_{dc} can be expressed as:

$$i_{dc} = \begin{cases} I_{dc(rated)} & \text{if}(S_s{=}1) \\ 0 & \text{if}(S_s{=}0) \end{cases} \tag{8}$$

According to equation (5), u_d can be expressed as:

$$u_d = \begin{cases} U_{dc} & \text{if}(S_s{=}1) \\ mU_{dc} & \text{if}(S_s{=}0) \end{cases} \tag{9}$$

The average voltage of u_d is:

$$\overline{U}_d = DU_{dc} + (1 - D)mU_{dc} \tag{10}$$

where D is the duty cycle that controls the on and off frequencies of S_s.

The j-phase bridge arm voltage of the HLC-MMC can be expressed as:

$$\begin{cases} u_{uj} = 1/2 u_d - 1/2 mU_{dc}\cos(\omega t) - \Delta u_d \\ u_{lj} = 1/2 u_d + 1/2 mU_{dc}\cos(\omega t) - \Delta u_d \end{cases} \tag{11}$$

where Δu_d is used to drive the circulating current i_{cirj}. Due to the controllability of the current, zero-current switching of the series switch S_s is possible. Compared to (7), the AC voltage component in the bridge arm voltage remains unchanged. However, the average DC voltage component is reduced, resulting in a smaller SM capacitor voltage ripple.

The power balance must be ensured in the HLC-MMC, which gives $U_{dc}I_{dc(rated)}D = 3/2 U_{ojm}I_{ojm}\cos\varphi$. D is designed to be equal to 1 at rated output power and rated motor speed, which gives:

$$D = \frac{mI_{ojm}}{I_{ojm(rated)}} \tag{12}$$

IV. CIRCUIT ANALYSIS

A. ANALYSIS OF CAPACITANCE VOLTAGE FLUCTUATION OF CONVENTIONAL MMC

Based on equations (2) and (7), the instantaneous power absorbed by each bridge arm of the conventional MMC can be expressed as:

$$\begin{cases} P_{uj} = u_{uj}i_{uj} = (1/2 U_{dc} - u_{oj})(i_{cirj} + 1/2 i_{oj}) \\ P_{lj} = u_{lj}i_{lj} = (1/2 U_{dc} + u_{oj})(i_{cirj} - 1/2 i_{oj}) \end{cases} \tag{13}$$

Integrating and simplifying (13), the energy change for each bridge arm can be derived as:

$$\begin{cases} w_{uj} = \int_0^t P_{uj}dt \\ \quad = \underbrace{\frac{1}{\omega}\frac{U_{dc}I_{ojm}}{4}\sin(\omega t - \varphi)}_{1stterm} - \underbrace{\frac{m^2}{\omega}\frac{U_{dc}I_{ojm}\cos\varphi}{8}\sin(\omega t)}_{2nd\ \ term} \\ \quad\quad - \underbrace{\frac{m}{\omega}\frac{U_{dc}I_{ojm}\sin(2\omega t - \varphi)}{16}}_{3rd\ \ term} \\ w_{lj} = \int_0^t P_{lj}dt \\ \quad = -\underbrace{\frac{1}{\omega}\frac{U_{dc}I_{ojm}}{4}\sin(\omega t - \varphi)}_{1stterm} + \underbrace{\frac{m^2}{\omega}\frac{U_{dc}I_{ojm}\cos\varphi}{8}\sin(\omega t)}_{2nd\ \ term} \\ \quad\quad - \underbrace{\frac{m}{\omega}\frac{U_{dc}I_{ojm}\sin(2\omega t - \varphi)}{16}}_{3rd\ \ term} \end{cases} \tag{14}$$

In a motor drive system that always keeps a constant m/ω, while U_{dc} is fixed and I_{ojm} remains constant if driving a constant torque load [19], [20]. the first part of the above equation becomes larger when the motor speed decreases. the second part becomes smaller. and the third part remains constant. Therefore, at low motor speeds, the first part of the energy change term is the dominant part, and the last two terms can be neglected, so the peak-to-peak energy change of each bridge arm can be approximated as:

$$\Delta w_{uj} \approx \Delta w_{lj} \approx \frac{U_{dc}I_{ojm}}{2\omega} \tag{15}$$

This energy change needs to be buffered by the SM capacitor in each bridge arm, i.e.

$$\frac{U_{dc}I_{ojm}}{2\omega} = N(1/2 CU^2_{cj(\max)} - 1/2 CU^2_{cj(\min)}) = NCU_{cj}\Delta U_{cj(pp)} \tag{16}$$

where $\Delta U_{cj(pp)}$ is the peak-to-peak SM capacitor fluctuation voltage.

Due to $NU_{cj} = U_{dc}$, equation (16) can be simplified as:

$$\Delta U_{cj(pp)} = \frac{I_{ojm}}{2\omega C} \tag{17}$$

Equation (17) expresses that the capacitor voltage ripple of conventional MMC is proportional to the output torque and inversely proportional to the motor speed. Therefore, the capacitor voltage fluctuations will be too large for high torque requirements at low speeds.

B. ANALYSIS OF CAPACITANCE VOLTAGE FLUCTUATION OF CONVENTIONAL HLC-MMC

The cause of the fluctuation of the sub-module capacitor voltage is first analyzed. Since the internal circulating current of the HLC-MMC is dominated by the 2-frequency component, the harmonic component of the bridge arm current above 2-frequency is ignored in the analysis. Because of the three-phase symmetry of the HLC-MMC, the analysis of its A-phase is illustrated here as an example. Fig. 4 shows the A-phase equivalent model of the HLC-MMC. The series sub-module of each bridge arm can be equated to a controlled voltage source, and the positive direction of each electrical quantity of the HLC-MMC is defined according to the direction in Fig. 4.

According to [21], The relationship between the sub-module capacitance voltage and the fluctuating current injected into the sub-module is given by:

$$\begin{cases} u_{Cua} = u_{Cua}(t_0) + \dfrac{1}{C_{sm}} \displaystyle\int_{t_0}^{t} i_{Cua} dt \\ u_{Cla} = u_{Cla}(t_0) + \dfrac{1}{C_{sm}} \displaystyle\int_{t_0}^{t} i_{Cla} dt \end{cases} \tag{18}$$

where u_{cua} and u_{cla} are the instantaneous values of the individual sub-module capacitor voltages of the upper and lower bridge arms of phase A, respectively. i_{cua} and i_{cla} are the fluctuation currents of the individual sub-modules of the upper and lower bridge arms of phase A, respectively. and C_{sm} is the sub-module capacitor capacitance value of the MMC.

The HLC-MMC sub-module fluctuation current is the product of the sub-module switching function and the bridge arm current. According to [22], the fluctuation current expressions of the upper and lower bridge arm sub-modules are obtained as:

$$\begin{cases} i_{Cua} = F_{ua} i_{ua} = \dfrac{1}{6} I_{dc} - \dfrac{1}{8} m I_a \cos(\varphi) \\ \quad - \dfrac{1}{6} m I_{dc} \cos(\omega t + \theta_a) \\ \quad + \dfrac{1}{4} I_a \cos(\omega t + \varphi + \theta_a) - \dfrac{1}{4} m I_{2a} \cos(\omega t - \theta_a + \theta_{2a}) \\ \quad - \dfrac{1}{8} m I_a \cos(2\omega t + \varphi + 2\theta_a) + \dfrac{1}{2} I_{2a} \cos(2\omega t + \theta_{2a}) \\ \quad - \dfrac{1}{4} m I_{2a} \cos(3\omega t + \theta_a + \theta_{2a}) \\ i_{Cla} = F_{la} i_{la} = \dfrac{1}{6} I_{dc} - \dfrac{1}{8} m I_a \cos(\varphi) \\ \quad + \dfrac{1}{6} m I_{dc} \cos(\omega t + \theta_a) \\ \quad - \dfrac{1}{4} I_a \cos(\omega t + \varphi + \theta_a) + \dfrac{1}{4} m I_{2a} \cos(\omega t - \theta_a + \theta_{2a}) \\ \quad - \dfrac{1}{8} m I_a \cos(2\omega t + \varphi + 2\theta_a) + \dfrac{1}{2} I_{2a} \cos(2\omega t + \theta_{2a}) \\ \quad + \dfrac{1}{4} m I_{2a} \cos(3\omega t + \theta_a + \theta_{2a}) \end{cases} \tag{19}$$

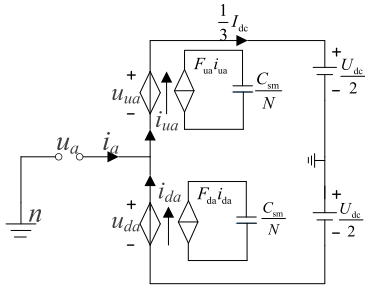

FIGURE 4. HLC-MMC single-phase equivalent model.

where F_{ua} and F_{la} are the switching functions of the upper and lower bridge arms of phase A, respectively. i_{ua} and i_{la} are the instantaneous currents of the upper and lower bridge arms of phase A, respectively. I_{dc} is the HLC-MMC DC-side current. I_a is the A-phase phase current amplitude of the HLC-MMC. ω is the angular frequency of the HLC-MMC AC measurement voltage. θ_a is the initial phase angle of phase A. I_{2a} is the A-phase 2-frequency loop current amplitude of the HLC-MMC. θ_{2a} is the initial phase angle of the A-phase 2-frequency loop current.

According to (18) and (19), it can be seen that the direct cause of the sub-module capacitance voltage fluctuation is the fluctuation current injected into the sub-module. In the steady-state operating state of the HLC-MMC, the sub-module fluctuation current contains the fundamental, 2-frequency, and high-frequency AC components. From the studies in [23] and [24], it is clear that the fundamental and 2-frequency components dominate the fluctuation current, and the content of the 3-frequency and higher frequency components is small and negligible. Each frequency component of the fluctuating current is a function of the associated angular frequency, which has the nature of three-phase symmetry. From (19), it can be seen that the dominant fundamental frequency component in the SM current presents three-phase positive-order symmetry, and the 2-frequency component presents three-phase negative-order symmetry, as shown in Fig. 5.

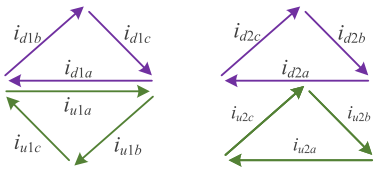

FIGURE 5. Three-phase fluctuation current relationship diagram.

In Fig. 5: i_{u1a}, i_{u1b}, i_{u1c}, i_{l1a}, i_{l1b} and i_{l1c} represent the fundamental frequency components of the fluctuation currents of the three-phase upper and lower bridge arm sub-modules, respectively. i_{u2a}, i_{u2b}, i_{u2c}, i_{l2a}, i_{l2b} and i_{l2c} represent the 2-fold frequency components of the fluctuation currents of the three-phase upper and lower bridge arm sub-modules, respectively.

For the proposed HLC-MMC, the above analysis is the theoretical basis for the coupling offset of fluctuation currents. The vector sum of the low-frequency components of the three-phase fluctuation currents are all zero, and their coupling can be achieved by constructing a coupling channel between the three-phase sub-modules, so that the fluctuation current amplitude flowing into the sub-module capacitor is smaller, and thus the fluctuation of the sub-module capacitor voltage can be effectively suppressed.

It is unique in that it can significantly reduce the SM capacitor voltage fluctuation. Since the I_{ojm} is determined by the load torque, the way to avoid energy variations is to reduce the DC component of the bridge arm voltage. In the HLC-MMC, this operation is achieved by regularly interval switching off the DC supply and generating the bridge arm voltages shown in (11). As a result, the average DC bridge arm voltage component can be reduced to $1/2U_d$.

According to the above analysis, the energy change of each bridge arm of the HLC-MMC can be expressed as:

$$\Delta w_{uj} \approx \Delta w_{lj} \approx \frac{(D+(1-D)m)U_{dc}I_{ojm}}{2\omega} \tag{20}$$

Therefore, the j-phase capacitor voltage fluctuation is expressed as:

$$\Delta U_{cj(pp)} = \frac{(D+(1-D)m)I_{ojm}}{2\omega C} \tag{21}$$

Inserting (6) and (12) into (21) yields:

$$\Delta U_{cj(pp)} = \frac{\left[I_{ojm(rated)} + (1-\frac{\omega}{\omega_{rated}})I_{ojm}\right]I_{ojm}}{2\omega_{rated}I_{ojm(rated)}C} \tag{22}$$

For the constant torque load case of $I_{ojm} = I_{ojm(rated)}$, (22) can be further simplified as:

$$\Delta U_{cj(pp)} = \left(2-\frac{\omega}{\omega_{rated}}\right)\frac{I_{ojm(rated)}}{2\omega_{rated}C} \tag{23}$$

C. HFL FLUCTUATION CURRENT OPTIMIZATION

In order to realize the fluctuation current coupling of the three-phase SMs in the MMC, the half-bridge circuit in the HFL circuit needs to control the transmission of the fluctuation current to the remaining two phases, and then realize the coupling of the fluctuation current. Therefore, the half-bridge circuits in the HFL circuit all use exactly the same 0.5 duty cycle open-loop synchronous control signal S_{HFL}. That is, at any moment, the fluctuation current on the three side windings of the HFL are isotropic, after passing through the HFL, the fluctuating currents are coupled and offset by superposition. To simplify the analysis of the HFL circuit, the parameters of the HFL circuit connected to each sub-module are assumed to be the same, and the effect of the HFT excitation branch is ignored, and each HFL module is considered as a separate linear system.

Since the switching frequency of the HFL circuit is orders of magnitude higher than the carrier frequency of the MMC, the HFL circuit can be analyzed while ignoring the switching action on the MMC side, and the pre-stage circuit of each HFL sub-module is considered as a current source. Because the switching states of the three half-bridge circuits that make up the HFL circuit are identical and the current direction of each winding of the HFT is the same, the HFL circuit can be equivalently simplified to obtain a simplified equivalent circuit as shown in Fig. 6.

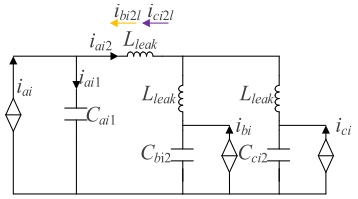

FIGURE 6. HFL simplified equivalent circuit.

In any switching state of the HFL circuit, the sub-module fluctuation currents i_{ai} in accordance with the analysis of equation (19), where the part flowing into the sub-module capacitor is set to i_{ai1} and the part flowing through the HFL is set to i_{ai2}. Their magnitudes are related to the impedance distribution of the HFL circuit. Taking the HFL$_{ia}$ sub-module S_{ai1} open and S_{ai2} disconnected states as an example, a brief analysis of the impedance and the estimation of the coupling current are as follows:

The value of the branch impedance through which the wave current i_{ai1} flows is recorded as Z_1, and the value of the branch impedance through which i_{ai2} flows is recorded as Z_2. Their expressions are:

$$\begin{cases} Z_1 = \dfrac{1}{j\omega C} \\ Z_2 = \dfrac{j3\omega L_{leak}}{2} + \dfrac{1}{j2\omega C} \end{cases} \tag{24}$$

where C is the capacitance of one of the series capacitors of the sub-module. L_{leak} is the leakage inductance of each winding of HFT.

If only the input current of phase A sub-module is considered and the input currents of phase B and C sub-modules are not considered, the fluctuating current values i_{ai1_a} and i_{ai2_a} of the two branches are:

$$\begin{cases} i_{ai1\_a} = \dfrac{Z_2}{Z_1+Z_2}i_{ai} = \dfrac{1-3\omega^2 L_{leak}C}{3-3\omega^2 L_{leak}C}i_{ai} \\ i_{ai2\_a} = \dfrac{Z_1}{Z_1+Z_2}i_{ai} = \dfrac{2}{3-3\omega^2 L_{leak}C}i_{ai} \end{cases} \tag{25}$$

After considering the input currents i_{bi} and i_{ci} of the B and C phase sub-modules respectively, by the three-phase symmetry and according to the superposition theorem. The currents i_{bi21} and i_{ci21} flowing from the B and C phases into the A phase are:

$$\begin{cases} i_{bi21} = \dfrac{Z_2}{Z_1+Z_2}i_{ai} = \dfrac{1}{3-3\omega^2 L_{leak}C}i_{bi} \\ i_{ci21} = \dfrac{Z_1}{Z_1+Z_2}i_{ai} = \dfrac{1}{3-3\omega^2 L_{leak}C}i_{ci} \end{cases} \tag{26}$$

In the MMC steady-state condition, the DC component of the sub-module fluctuation current is 0, which contains only the AC component. Therefore, according to (25) and (26), the superposition theorem and the three-phase symmetry, the actual fluctuation current i_{ai1} flowing into the sub-module capacitor is:

$$i_{ai1} = i_{ai1\_a} + i_{bi21} + i_{ci21} = \frac{-\omega^2 L_{leak} C}{1 - \omega^2 L_{leak} C} i_{ai} \tag{27}$$

According to (27), it can be seen that for each frequency component of the sub-module fluctuation current, the frequency is different, so the proportion of their shunt flow into the capacitor is also different, and the HFL circuit has a better absorption coupling effect on the low-frequency fluctuation current. Since the fluctuation current is dominated by low-frequency components, the value of L_{leak} is of order μH and the value of C is of order mF, so the portion of the fluctuation current flowing into the sub-module capacitor is much smaller than the portion flowing into the HFL, and the low-frequency pulsation of the sub-module voltage is eliminated. From the study in [25], it is clear that the bridge arm circulation is subsequently eliminated.

V. SYSTEM CONTROL SCHEME

This section presents the control scheme applicable to the HLC-MMC motor drive system, as shown in Fig. 7. The control system consists of the following five main components: overall energy balance control, phase energy balance control, bridge arm energy balance control, loop current control and SM capacitor voltage balance related pulse width modulation control.

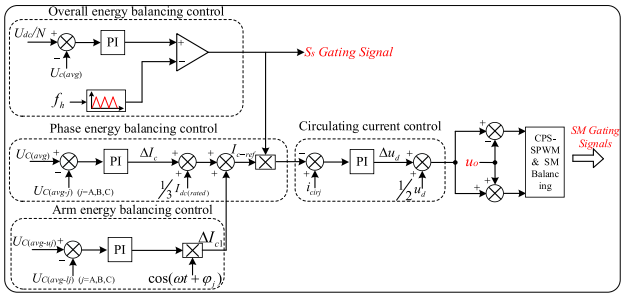

FIGURE 7. Control block diagram of HLC-MMC.

In order to achieve stable operation of the hybrid low capacitance MMC, the power balance between the DC input and AC output must be maintained. The input-output power difference affects the capacitor energy storage, so an overall energy balance control is used to make the measured average voltage $U_{c(avg)}$ of all SM capacitors equal to the reference value U_{dc}/N by adjusting the duty cycle D. Phase energy balance control is used to control the measured average capacitor voltage $U_{c(avg-j)}$ per phase equal to $U_{c(avg)}$ by a DC current regulating element ΔI_c to ensure a uniform distribution of the total energy among the three phases.

In addition, the bridge arm energy balance control is used to maintain an equal distribution of energy between the upper and lower arms for each stage. This is achieved by adjusting the fundamental frequency current components ΔI_{c1}. These current regulation components are then summed with $1/3I_{dc(rated)}$ to generate $I_{c-ref} = 1/3I_{dc(rated)} + \Delta I_c + \Delta I_{c1}$. I_{c-ref} is then multiplied with the duty cycle D to obtain the circulating current reference. The purpose of using the circulating current control is to make the actual circulating current follow I_{c-ref}, where the controlled variable is Δu_d. Reference values for the bridge arm voltages u_u and u_l can be obtained according to (11).

Finally, reference values u_u and u_l are sent to the PWM generator to synthesize the stepped switching voltage waveform. To reduce the output voltage harmonics and increase the equivalent switching frequency, a phase-shifted carrier pulse width modulation with uniform distribution of the carrier waveform is used. In addition, a voltage balancing scheme based on the reference signal adjustment is used to keep the SM capacitor voltages in each bridge arm balanced.

The PMSM control part of this paper adopts the SPWM vector control. The control block diagram is shown in Fig. 8. d-axis current reference value is set to 0. The speed reference value ω_e^* is compared with the measured value ω_e and then passed through the PI regulator to get the q-axis current reference value i_q^*. The comparison result is controlled by the deadbeat current controller to get the predicted voltage values of d-axis and q-axis. The pulse signals S_a, S_b, S_c required to control the HLC-MMC are then generated by the coordinate transformation and the CPS-SPWM module.

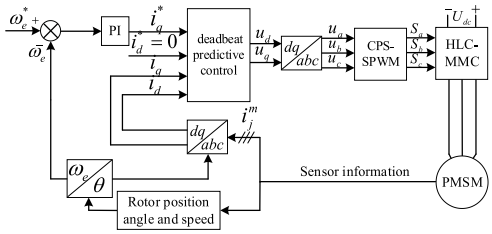

FIGURE 8. Motor control block diagram.

VI. SIMULATION ANALYSIS

In order to verify the correctness and effectiveness of the proposed HLC-MMC topology and the control scheme of the PMSM drives, a simulation model of the 1.2MW/8kV HLC-MMC PMSM drive system is established in the Matlab/Simulink environment. The simulation parameters are shown in Table 1.

In the application of PMSM drives, the low frequency operation of the motor as well as the heavy load or full load operation conditions will lead to large sub-module capacitance voltage fluctuations in the MMC. Therefore, 10Hz low-frequency and full load operation conditions are considered in the simulation condition design in this paper.

TABLE 1. HLC-MMC motor drive system simulation parameters.

Parameter		Value	Unit
HLC-MMC	DC-source voltage	8000	V
	Number of bridge arm SMs	10	Number
	Rated capacitance voltage	800	V
	Rated output frequency	50	Hz
	Bridge arm inductance	10	mH
	SM equivalent capacitance	750	μF
	Snubber resistance	200	Ω
	Snubber capacitance	1	μF
RL load	Load resistance	14	Ω
	Load inductance	2	mH
PMSM	Rated active power	1.2	MW
	Number of pole pairs	4	Pairs
	Rated speed	750	Rpm
	Rated torque	15200	N·m

Fig. 9 shows the simulation waveform of the transient process of the motor running at 10Hz low-frequency condition and the load torque increasing suddenly from 12000N·m to the rated torque (15200N·m) under the proposed HLC-MMC topology and its control method. The system can transition to the steady state smoothly after the load torque increases suddenly at 1.0s, the HLC-MMC three-phase output current waveform is good before and after the sudden change of torque. The HLC-MMC motor drive system has good dynamic characteristics, and the voltage ripple of the capacitor of the sub-module is maintained within 2.0%.

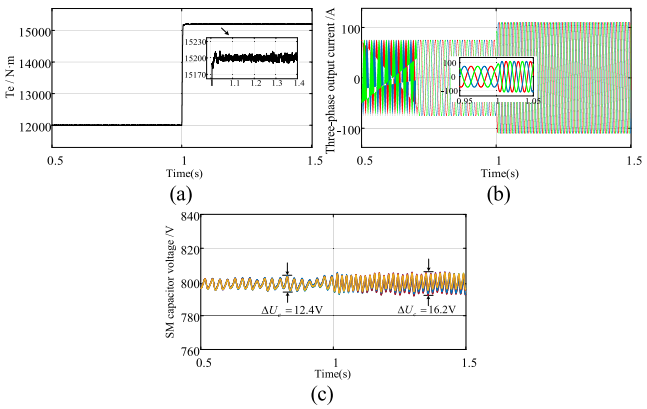

FIGURE 9. Simulation waveform of the system with sudden change of load torque under 10Hz low-frequency operation: (a) Torque (b) Stator current (c) A-phase upper bridge arm sub-module capacitor voltage.

When the motor is running at 50Hz rated condition, the simulation waveform of the transient process of the load torque suddenly increasing from 12000N·m to rated torque (15200N·m) is shown in Fig. 10. The system can smoothly transition to steady state after the sudden increase of load torque at 1.0s, the three-phase output current waveform is good before and after the sudden change of torque, the sub-module capacitor voltage ripple is maintained at about 1.6%, and the system keeps stable operation. The system has good temporary steady-state characteristics and good anti-interference ability.

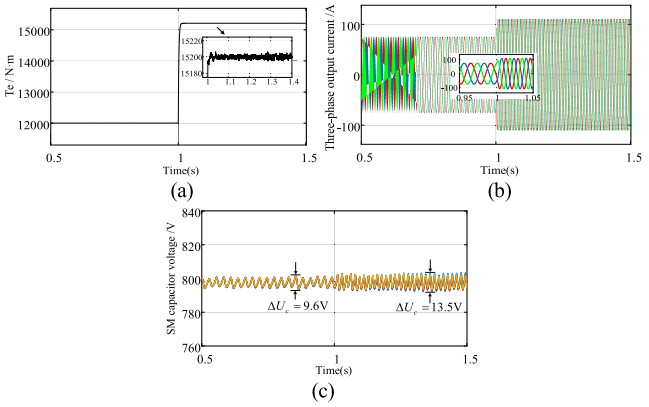

FIGURE 10. Simulation waveform of the system with sudden change of load torque under 50 Hz rated working condition: (a) Torque (b) Stator current (c) A-phase upper bridge arm sub-module capacitor voltage.

In order to illustrate the suppression effect of the proposed HLC-MMC topology and its control method on capacitor voltage ripple, the capacitor voltage ripple comparison is performed under 100% load torque of the motor and 50Hz rated operating conditions. The equivalent capacitance of the sub-module is set to 4.7mF because of the large capacitance requirement of the conventional MMC. Fig. 11(a) shows the simulated waveform of sub-module capacitor voltage under the conventional MMC topology and conventional control method, and the ripple rate is 2.95%. Fig. 11(b) shows the simulated waveform of sub-module capacitor voltage under the proposed HLC-MMC topology and conventional control method, and the ripple rate is 2.01%. Fig. 11(c) shows the simulated waveform of sub-module capacitor voltage under the proposed HLC-MMC topology and the proposed control method, and the ripple rate is 1.65%. The comparison results show that the proposed topology and its control method are effective in suppressing the capacitor voltage fluctuation under the rated operating condition of 50Hz motor.

When the motor is running at 100% load torque and 10Hz low-frequency, the simulated sub-module capacitor voltage waveforms are compared as follows: Fig. 12(a) shows the simulated sub-module capacitor voltage waveforms under the traditional MMC topology and traditional control method, and the ripple rate is 3.72%. Fig. 12(b) shows the simulated sub-module capacitor voltage waveforms under the proposed HLC-MMC topology and traditional control method, and the ripple rate is 2.15%. Fig. 12(c) shows the simulated waveform of sub-module capacitor voltage under the proposed HLC-MMC topology and the proposed control method, and the ripple rate is 1.69%. The comparison results show that the proposed topology and its control method have obvious suppression effect on the capacitor voltage fluctuation under the low-frequency condition of 10Hz motor, which is consistent with the theoretical analysis mentioned above.

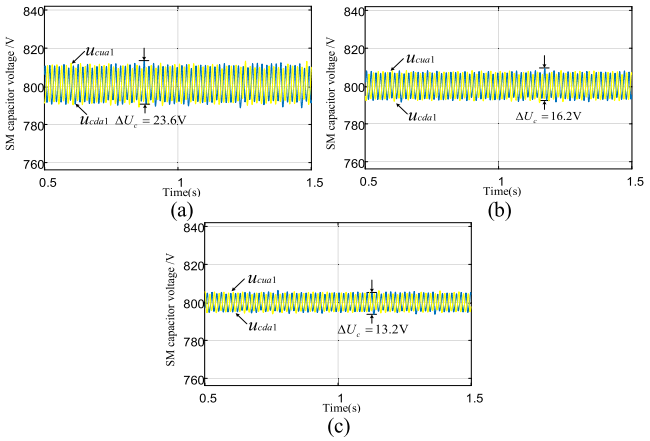

FIGURE 11. Simulation waveform of MMC capacitor voltage ripple comparison under rated operating condition of motor running at 50 Hz: (a) MMC and conventional control method (b) HLC-MMC and conventional control method (c) HLC-MMC and the proposed control method.

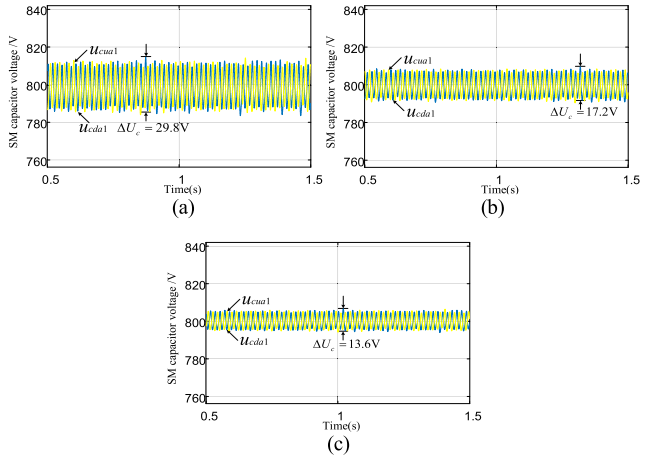

FIGURE 12. Simulation waveform of MMC capacitor voltage ripple comparison under low-frequency operating condition of motor running at 10Hz: (a) MMC and conventional control method (b) HLC-MMC and conventional control method (c) HLC-MMC and the proposed control method.

To illustrate the effect of the proposed HLC-MMC topology and its control method on output current harmonics suppression, a comparison of output current THD at 50Hz rated operating condition under 100% load torque of the motor is performed. Fig. 13(a) shows the output current THD under the conventional MMC topology and the conventional control method with the value of 4.36%. Fig. 13(b) shows the output current THD under the proposed HLC-MMC topology and the conventional control method with the value of 2.11%. Fig. 13(c) shows the output current THD under the proposed HLC-MMC topology and the proposed control method with the value of 1.87%. By comparing the output current THD, it can be seen that the proposed topology and its control method have obvious suppression effect on the MMC output current harmonics under the rated condition of the motor, which is consistent with the theoretical analysis mentioned above.

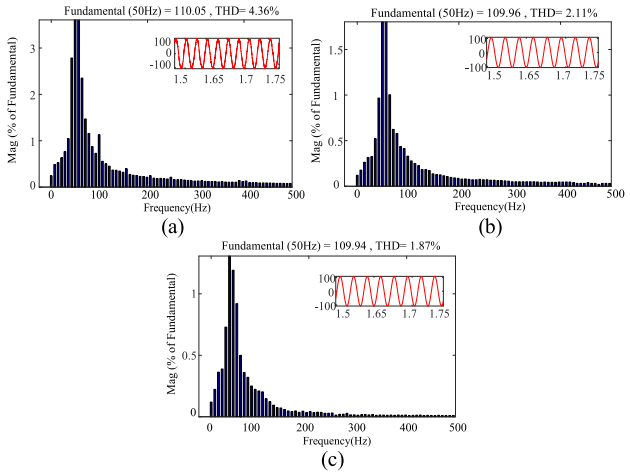

FIGURE 13. Comparison of MMC output current THD under rated operating condition of motor running at 50 Hz: (a) MMC and conventional control method (b) HLC-MMC and conventional control method (c) HLC-MMC and the proposed control method.

The output current THD comparison is performed at 10Hz low-frequency operating condition under 100% load torque of the motor. As shown in Fig. 14(a), the output current THD is 4.62% under the conventional MMC topology and conventional control method. as shown in Fig. 14(b), the output current THD is 2.35% under the proposed HLC-MMC topology and conventional control method. as shown in Fig. 14(c), the output current THD is 2.18% under the proposed HLC-MMC topology and proposed control method. The comparison of output current THD shows that the proposed topology and control method have a certain degree of output current harmonic suppression ability at low-frequency operation of the motor.

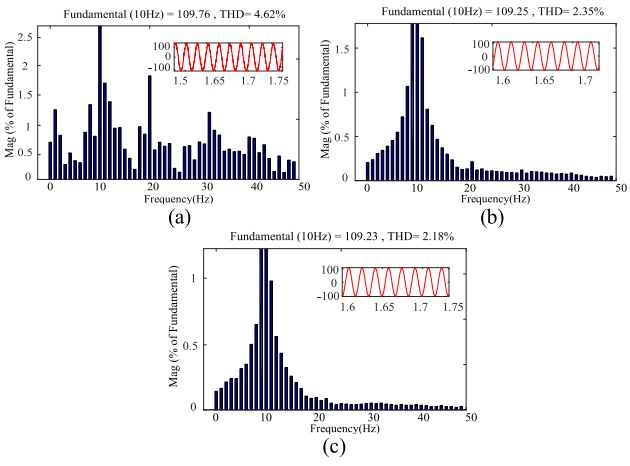

FIGURE 14. Comparison of MMC output current THD under low-frequency operating condition of motor running at 10Hz: (a) MMC and conventional control method (b) HLC-MMC and conventional control method (c) HLC-MMC and the proposed control method.

VII. CONCLUSION

In order to solve the problem of large sub-module capacitor voltage ripple at low-frequency operating conditions of

modular multilevel permanent magnet synchronous motor drives, a new HLC-MMC topology and its control method are proposed in this paper. The following conclusions are obtained through theoretical analysis and simulation results:

1) In the proposed control method applicable to the HLC-MMC topology, the energy is equalized between the bridge arms of each phase by adjusting the fundamental frequency current component. The measured average voltage of the control sub-module capacitor is equal to the reference voltage and the overall energy of the system is equalized.
2) A motor control method applicable to the HLC-MMC topology is proposed to incorporate integral regulation in the motor deadbeat current control. The design of the control system is simplified and has good transient steady-state characteristics.
3) Compared with the conventional MMC topology and the conventional control method, the proposed HLC-MMC topology and the proposed control method reduce the capacitor voltage ripple from 3.72% to 1.69% at low-frequency operating conditions and from 2.95% to 1.65% at rated operating conditions. Sub-module capacitor voltage ripple is effectively suppressed.
4) Compared with the conventional MMC topology and the conventional control method, the proposed HLC-MMC topology and the proposed control method reduce the MMC output current THD from 4.62% to 2.18% at low-frequency operating conditions and from 4.36% to 1.87% at rated operating conditions. The MMC output current harmonics are effectively suppressed.

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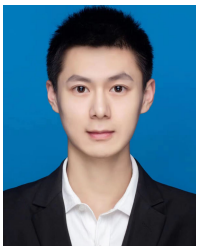

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