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APPLIED RESEARCH

# Increasing Light Load Efficiency in Phase-Shifted, Variable Frequency Multiport Series Resonant Converters

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**ABSTRACT** Multiport power conversion topologies provide the capability of multiple independent converters with a single transformer having multiple windings (i.e., ports) potentially increasing power densities and enabling flexible (and bidirectional) power routing. In automotive onboard charger (OBC), the multiport approach combined with symmetrical series resonant circuits, the so-called multiport series resonant converter (MSRC), allows for a galvanic isolated connection between all ports: the grid-side converter (i.e., usually an AC/DC power factor correction (PFC) stage), vehicle's main and the auxiliary low-voltage (LV) battery. The variation of the battery voltage significantly affects the MSRC operation, particularly for light loads at a low state-of-charge, and high losses can be experienced since zero-voltage-switching (ZVS) conditions are lost. In addition to the conventional control approach of the MSRC, where the power flow is set with a phase-shift between the individual full bridges or by changing the switching frequency, this paper proposes a novel and coordinated approach, including the manipulation of both and the additional modulation of the duty cycle as a function of the DC-link voltages, aiming to introduce a zero-voltage interval on the full bridge output voltages. A full mathematical description of the adopted converter topology is provided, including accurate simulation models that allow a comparison between the proposed *duty cycle* mode and the conventional control strategy. A detailed description of achieving ZVS within the connected full bridges is also included. Experimental results validate the proposal and demonstrate significant efficiency improvements compared to standard control approaches.

**INDEX TERMS** Multiport series resonant converter, modulation scheme, light load efficiency, DC/DC converter, battery chargers, energy and power routing, automotive converters.

## I. INTRODUCTION

Transformers are common elements of modern power converters as they offer the galvanic isolation needed to satisfy safety and leakage current requirements in many commercial applications, as well as a convenient passive voltage conversion via the turns ratio for applications with widely different input and output voltages [1], [2], [3], [4]. Despite the space consumption and inevitable power losses introduced by the transformer, it is still possible to build highly compact and efficient converters by leveraging these inherent benefits together with higher switching frequencies and effective modelling of the transformer and surrounding power electronics during the design and control development phase [5],

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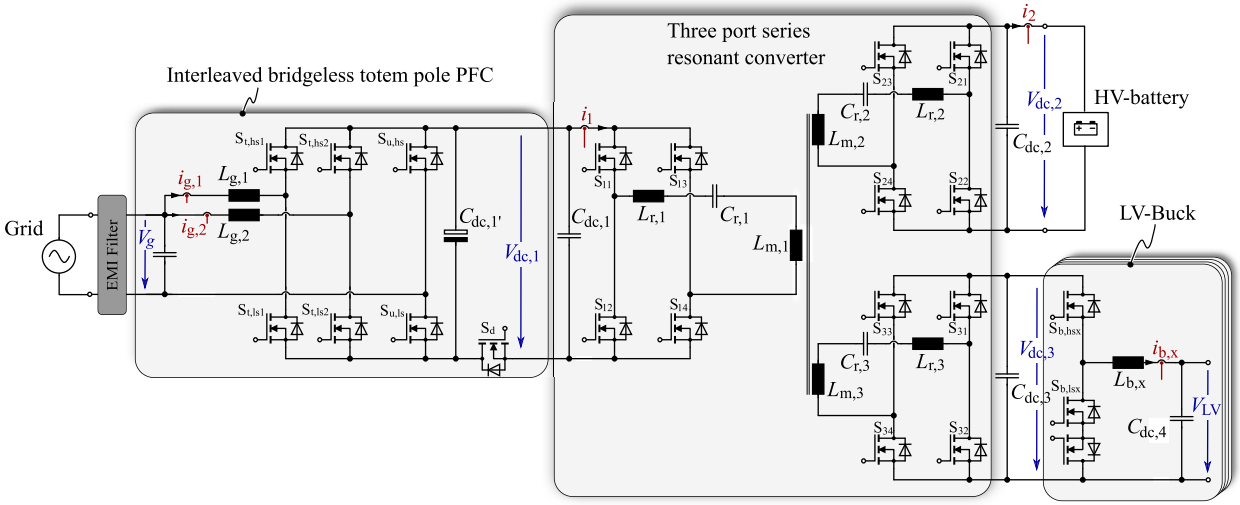


**FIGURE 1.** Topology for a single-phase on-board charger with an integrated DC/DC converter for supplying the high-voltage (HV) and the auxiliary battery. The grid interface consists of an interleaved, bridgeless totem pole PFC connected to a three port series resonant converter connected to a HV battery and an intermediate stage followed by interleaved buck converters connected to the auxiliary LV battery.

[6], [7]. Furthermore, converter topologies with a multiport transformer can provide the functionality of multiple converters but with just one magnetic structure via additional coupled windings. Despite the more sophisticated magnetic design needs, the multiport approach can often offer higher power density in applications where several single (two-port) transformers or parallel power converters would otherwise be needed [8]. Indeed, each transformer port can be supplemented with a similarly dimensioned LC tank for a series resonant converter (SRC) characterized by a high transformer magnetizing inductance with resonant energy storage concentrated in the LC tanks [6], which makes the MSRC approach attractive for exploiting the benefits offered by a multiport transformer since the physical design of the transformer is simplified by not having a need for a low and precisely dimensioned magnetizing inductance. Indeed the SRC topology has already been shown to offer full multi-directional power flow as an MSRC capable of high efficiency in certain operating conditions [9]. Other topologies like an LLC or popular multiport topologies such as a triple-active-bridge are typically made with comparatively low transformer magnetizing inductance where ZVS can be achieved independently of switching frequency and thus high efficiency can be achieved in a wide range of operating conditions. However the typical triple-active-bridge does not have inherent DC-saturation blocking (due to the lack of a series resonant capacitor) while the LLC may not offer as complete multi-directional power flow without a resonant tank and active switches on the output side port(s) and the transformer design can be more sensitive and complex [10], [11], [12]. An improved control/modulation approach for extending the high efficiency range of the MSRC topology so it can compete with such rival topologies, especially in light load conditions with varying port DC-link voltages [13], is the subject of this paper.

With conventional modulation strategies, high efficiency can be achieved with the MSRC when reactive power flow is minimized - i.e. when the voltages on each port are equal w.r.t. the turns ratio(s), and when the switching frequency is above the resonant frequency for operation in the inductive region of the resonant tank for zero-voltage-switching [14]. Power flow modelling and calculation of an MSRC using phase shift control with constant switching frequency can be found in [15] and [16] where, in effect, the amount of phase shift determines the real power transferred from the leading to the lagging port(s) with ubiquitous 50% duty cycle switching. Although such a simple control scheme is one benefit of the MSRC, the lack of energy storage in a magnetizing inductance leads to difficulty in maintaining ZVS in all load cases because the phase angle needed for the power flow may not align with the direction of the resonant current required to discharge the relevant switch parasitic output capacitance(s); which depends on the resonant tank impedance and output impedance [14]. However the control approach was expanded in [17] where the switching frequency was also varied (in a similar manner to an LLC, [18] or for a dual-active-bridge (DAB), [19], [20]) while still using phase shift control with a decoupling network to distribute power flow among the output ports. This additional freedom gives two benefits: the effective impedance of the resonant tank networks can be varied to extend the ZVS region for lower loads, and the control could continually "perturb and disturb" to find the best balance of switching and magnetic losses by ensuring that, as long as the port voltages were similar, ZVS was achieved with the smallest switching frequency possible.

A recent application of this concept is given in [9] whereby a 7 kW automotive OBC was made using the power topology shown in **Fig. 1** (a photo of the resulting hardware design is shown in **Fig. 2** and **Fig. 3**). This example uses a

three-port SRC for its DC-DC stage; connecting the PFC to both HV (400 V) and integrated LV (12 V, 2.4 kW) battery outputs where galvanic isolation was required between all ports and the possibility of an inherent voltage step down via the multiport transformer turns-ratio was exploited for the LV port. This led to a high power density (3.6 kW/L) hardware demonstrator where a peak efficiency of 98.5 % was achieved in the three-port SRC DC-DC stage [9]. The concept was expanded in [7] and shown to offer a reduction of DC-link capacitance in three-phase AC applications [9] using a five-port SRC where a power pulsation mode provides even higher power density (4.0 kW/L) compared to the convectional approach [21]. However, although an OBC with integrated LV output seems to benefit well from the advantages of a MSRC (isolation, voltage/turns-ratio, power density etc…), the OBC application also reveals two compounding weaknesses of the MSRC that are the main topics of this paper:

1) low efficiency in light load operation, &
2) losing ZVS across a wide output voltage range.

Firstly, for bi-directional OBCs there are scenarios where low power transfer is needed: for example, vehicle-to-grid (V2G) where a small amount of power is used for stabilizing the grid and more critically, in the case of an integrated LV output, the power transfer for supplying a car's LV systems while driving (i.e. power from HV to LV batteries) is also much less than the OBC's rated power [22]. Such scenarios can bring out poor performance from the switching frequency control given in [17] since it operates the MSRC partly like an LLC where low load power flow is achieved with higher switching frequencies and thus generally lower efficiency due to the risk of higher AC magnetic component losses and other switching related losses. Secondly, this poor light-load efficiency due to high switching frequency is compounded when port voltage ratios diverge from the transformer turns-ratio and thus uniform ZVS is no longer achieved. For example, in **Fig. 1**, while the PFC controller defines the voltage at the DC-link on port 1 (where the voltage boundaries are given by the sinusoidal grid voltage and the rating of the DC-link capacitors), and an intermediate buck/boost converter stage regulates the voltage on port 3, the port 2 voltage in contrast is not actively controlled and is effectively determined by the state-of-charge of the HV battery instead. This means that, with state-of-the-art control schemes either all port voltages would need to move with the voltage of the HV battery to maintain symmetrical port voltages and ZVS, or efficiency needs to be further sacrificed.

Clearly, these two compounding phenomena can occur with an MSRC based OBC during low battery state-of-charge and low load power flow as the switching frequency will be high and ZVS will not be achieved.

To mitigate this effect while keeping all the advantages offered by the MSRC, this paper proposes a further augmentation of the switching-frequency and phase control from [17]. Specifically, this paper shows how super-imposing symmetrically aligned "duty cycle" modulation (later

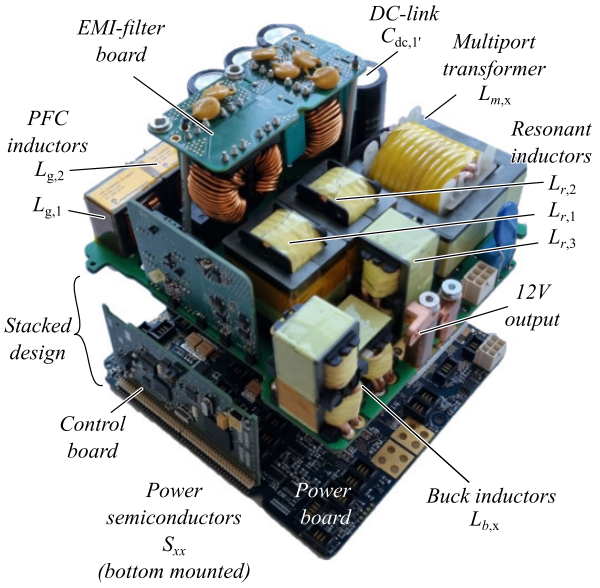


**FIGURE 2.** Exploded view of the Tiny Power Box Automotive demonstrator with annotated components but without housing and cold plates. The illustration contains the topology given in **Fig. 1**.

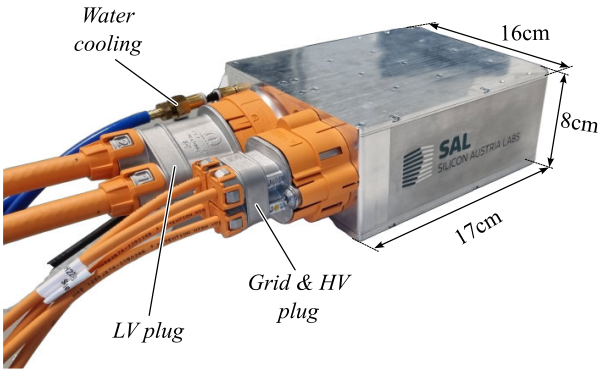


**FIGURE 3.** Tiny Power Box automotive demonstrator with housing, connected water cooling and HV and LV connectors containing the hardware shown in **Fig. 2**.

referred to as duty cycle mode) together with the phase angle and switching frequency control, can both *improve light load efficiency* (via reduced switching frequency and resonant currents) and *widen the ZVS region* for given power flow conditions (thus reducing switching losses). The duty cycle mode is achieved by adding a zero voltage time in the switching period, the extent of which is related to the extent of the voltage divergence from the lowest port voltage aiming for a nearly equal voltage time area in each port w.r.t. the transformer turns-ratios. For example, in the case of an OBC with a HV battery charged to 250 V, it's respective port full-bridge will hold 50 % duty cycle while the other ports reduce the duty cycle until the effective voltage time area applied by each full bridge is similar w.r.t. the multiport transformer turns-ratios.

Expanding the ZVS region with the duty cycle mode has already been shown using a multiport triple-active-bridge topology in [23] and more recently in [24] for an EV onboard

charger application, where a closed loop control ensured constant voltage-time integrals for all ports. No literature has been found where all three control parameters (phase angle, switching frequency, duty cycle) have been used to both *reduce reactive power* and *provide additional ZVS space forming*, while simultaneously allowing the frequency related power losses to be minimized. Such a control strategy truly expands the applicability of the MSRC into applications where light load operation and wide port voltage ranges are needed, without the addition of any power hardware or control sensors.

The analytic justification and explanation of the circuit modelling for this proposed concept will be given in Section II, including an expansion of the MSRC admittance model given in [17] for a general N-port MSRC, plus an alternative state-space model of the converter. These models will be used to predict power flow for the range of control parameters and Section III will explain how the state-space model is used to predict if ZVS is possible for any given operating condition and modulation strategy, resulting in the ''ZVS maps'' for the example application of the 7kW OBC shown in **Fig. 1**. Section IV will explain the proposed duty cycle mode control in detail, including both simulation based analysis and laboratory measurements made using the hardware demonstrator shown in **Fig. 2** and **Fig. 3**. The exact efficiency gain from the proposed modulation scheme will be given along with examples of ZVS maps for both the conventional and proposed control methods in Section IV-C. Finally, discussion on the benefits and practical limits of the concept will be given in Section V followed by an outlook for further work.

## II. ANALYTICAL MODELLING OF THE MSRC

To analyze the widest relevant parameter space possible, mathematical models of the MSRC were developed whereby the modulation scheme variables could be quickly yet thoroughly assessed. These models have been used to calculate power flow and current waveforms in order to investigate the impact of the state-of-the-art frequency-phase based MSRC modulation approach compared to when further super-imposing the proposed duty cycle mode. The end-purpose of the models is then to compare the modulation schemes on switching related losses across the whole load range, but in particular in the light-load conditions with varying port DC-link voltages.

For evaluating any given discrete operating point (defined as an unique combination of DC-link voltages and control parameters), two approaches for analytically modelling the MSRC have been considered in this paper: firstly an admittance model that combines with a Fourier decomposition of the square-wave switch node voltages, and secondly a differential equation based state space model. These two methods offer mirrored pros and cons for analyzing different modulation schemes: the admittance model offers fast evaluation of any given operating point but accuracy is lost during the Fourier decomposition of the voltage excitation and the model only gets more complex when adding a higher number of harmonics. However this admittance model approach has been shown to be sufficiently accurate for reliable closed loop power flow control of a three port SRC in [17] and the average power flow estimation generally corresponds well with more accurate methods like the state space model. In contrast, the state space model is computationally more demanding but yields more precise transient waveform evaluation such as the shape of the resonant current waveforms. Although this added precision does not yield any benefits when predicting the overall power flow for a given operating point, more detailed insight into the switching transients is key when predicting ZVS and other switching related loss mechanisms. In this paper, the state space model is primarily used in order to generate ZVS maps of the whole space of operating points for each modulation scheme. However the authors use the admittance approach for quickly generating power flow for operating points and for closed loop control. This section explains the principles of the mathematics behind both approaches and contrasts the predictions made to measurements from the laboratory.

### A. ADMITTANCE MODEL

An admittance matrix model combining resonant tanks and mutual inductances on each winding of the N-port transformer is used to determine the power flow in a MSRC. A Fourier series decomposition of the rectangular port voltages, imposed by the full-bridges, as derived in [17] has been considered. The Fourier coefficients $b_{\mathrm{x,k}}$ of the fundamental and its harmonics are based on Eq. (1) where x refers to an individual port and k to the harmonic order of the Fourier coefficient. For the MSRC the fundamental and harmonics of the port voltages are combined to the voltage vector corresponding to Eq. (3) where $j$ is the imaginary unit, $f_{\mathrm{s}}$ is the switching frequency of the whole system whereas $\varphi_{\mathrm{x}}$ refers to each port's phase angle relative to one another, and $V_{\mathrm{DC,x}}$ is each port's independent DC-link voltage. The formula for calculating the Fourier coefficient is

$$b_{\mathrm{x,k}} = \frac{1}{\pi}\int_{\omega t=0}^{\pi} V_{\mathrm{DC,x}} \cdot \sin(k\omega t)dt - \frac{1}{\pi}\int_{\pi}^{2\pi} V_{\mathrm{DC,x}} \cdot \sin(k\omega t)dt = \frac{4}{k\pi}V_{\mathrm{DC,x}}. \quad (1)$$

The single entries of the vector are derived by

$$V_{\mathrm{x}}(\omega_{\mathrm{k}}) = b_{\mathrm{x,k}}e^{jk\varphi_{\mathrm{x}}} \quad (2)$$

which results in

$$V(\omega_{\mathrm{k}}) = \begin{pmatrix} \frac{4}{k\pi}V_{\mathrm{DC,1}} \cdot e^{jk\varphi_1} \\ \frac{4}{k\pi}V_{\mathrm{DC,2}} \cdot e^{jk\varphi_2} \\ \vdots \\ \frac{4}{k\pi}V_{\mathrm{DC,N}} \cdot e^{jk\varphi_{\mathrm{N}}} \end{pmatrix}, \quad \omega_k = 2\pi k f_{\mathrm{s}} \quad (3)$$

If a pulse width overlap of two converter-legs (resulting in a "zero voltage time" $t_0$ across the switch nodes) is to be considered, a factor of $\cos(\omega_k t_0/2)$ can be added to Eq. (2), which decreases the effective magnitude; this can be seen in **Fig. 10b** and **c**.[1]

The power transfer between the ports can be calculated by multiplying the voltage and current vectors as

$$S = P + jQ = \frac{V \cdot I'}{2} = \sum_{k=1}^{\infty} \frac{1}{2} V(\omega_k)^T \mathbf{Y_k}' V'(\omega_k) \quad (4)$$

$\mathbf{Y}_k$ is the admittance matrix for the k–th harmonic of the MSRC transformer ports and resonant tank(s), $S$ is the apparent power, $P$ real power, $Q$ the reactive power and symbol $'$ represents the conjugate complex operator. The admittance matrices have the following shape: (the matrix entries can be read like this: $Y_{k,xy}$, where k is the order of the harmonic and x and y represents the row and column in the matrix)

$$\mathbf{Y}_k = \begin{pmatrix} Y_{k,11} & Y_{k,12} & \cdots & Y_{k,1N} \\ Y_{k,21} & Y_{k,22} & \cdots & Y_{k,2N} \\ \vdots & & \ddots & \vdots \\ Y_{k,N1} & Y_{k,N2} & \cdots & Y_{k,NN} \end{pmatrix} \quad (5)$$

For calculating the admittance matrix, the impedance of the mutual inductance and the resonant tanks have to be calculated before. The transfer ratio between the mutual inductances $L_{m,x}$ is defined as

$$u_{xy} = \sqrt{\frac{L_{m,x}}{L_{m,y}}} = \frac{N_x}{N_y} \quad (6)$$

with $N_x$ denoting the number of turns. The impedance of the resonant tank is given by

$$Z_{r,x,k} = j\omega_k L_{r,x} + \frac{1}{j\omega_k C_{r,x}} + R_{r,x} \quad (7)$$

whereby $L_{r,x}$ represents the sum of external and leakage inductance, $R_{r,x}$ the sum of ohmic components within the circuit and the corresponding mutual impedance can be expressed as

$$Z_{m,x,k} = \frac{j\omega_k L_{m,x} R_{m,x}}{j\omega_k L_{m,x} + R_{m,x}} \quad (8)$$

which is a parallel connection of the magnetizing inductance $L_{m,x}$ and the resistance $R_{m,x}$ representing the iron core losses. If the assumption $R_{m,x} \gg \omega_k L_{m,x}$ is used, then the mutual impedance is almost equal to

$$Z_{m,x,k} = j\omega_k L_{m,x} \quad (9)$$

[1] Alternatively, to regard a zero voltage time, cosine terms with corresponding coefficients $a_{x,k}$ could be introduced. To minimize computational effort this was avoided in this paper but is a point for future work.

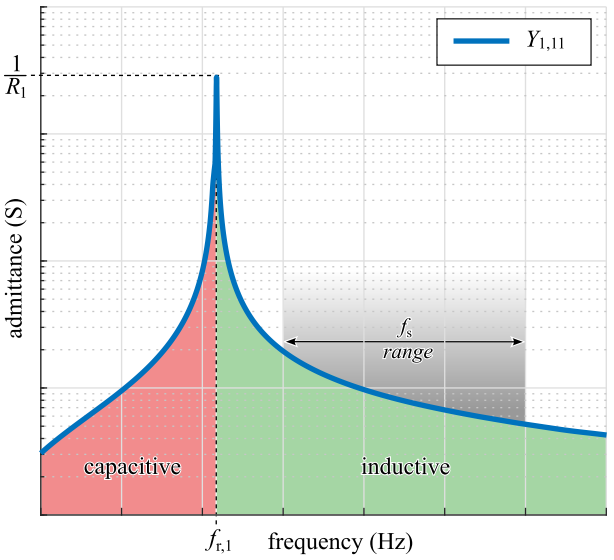


**FIGURE 4.** Admittance $Y_{1,11}$ versus switching frequency $f_s$ with the highlighted regions for capacitive, inductive behaviour and the switching frequency range typically used for SRC. At the resonance frequency $f_{r,1}$ the ohmic component of the port is defining the peak value of the admittance.

The admittance matrix $\mathbf{Y}_k$ for a MSRC with its elements can be written as

$$\begin{pmatrix} \frac{1}{Z_{r,1}} - \frac{1}{Z_{r,1}^2 \zeta_1} & -\frac{1}{Z_{r,1} Z_{r,2} \zeta_1 u_{12}} & \cdots & -\frac{1}{Z_{r,1} Z_{r,N} \zeta_1 u_{1N}} \\ -\frac{1}{Z_{r,2} Z_{r,1} \zeta_2 u_{21}} & \frac{1}{Z_{r,2}} - \frac{1}{Z_{r,2}^2 \zeta_2} & \cdots & -\frac{1}{Z_{r,2} Z_{r,N} \zeta_2 u_{2N}} \\ \vdots & & \ddots & \vdots \\ -\frac{1}{Z_{r,N} Z_{r,1} \zeta_N u_{N1}} & -\frac{1}{Z_{r,N} Z_{r,2} \zeta_N u_{N2}} & \cdots & \frac{1}{Z_{r,N}} - \frac{1}{Z_{r,N}^2 \zeta_N} \end{pmatrix} \quad (10)$$

(due to space limitations, $k$ was neglected) whereby the coefficients $\zeta_x$ are

$$\begin{aligned} \zeta_{1,k} &= \frac{1}{Z_{m,1,k}} + \sum_{i=1}^{N} \frac{1}{Z_{r,i,k} u_{1i}^2} \\ \zeta_{2,k} &= \frac{1}{Z_{m,2,k}} + \sum_{i=1}^{N} \frac{1}{Z_{r,i,k} u_{2i}^2} \\ &\vdots \\ \zeta_{N,k} &= \frac{1}{Z_{m,N,k}} + \sum_{i=1}^{N} \frac{1}{Z_{r,i,k} u_{Ni}^2} \end{aligned} \quad (11)$$

A demonstration of how the admittance values of one port typically varies over frequency is given in **Fig. 4**. It can be seen, that the admittance is highly dependent on the frequency. Above the resonance frequency the resonant circuit is behaving like an inductor and below like a capacitor. The

shown resonance frequency can be calculated by

$$f_{\mathrm{r,x}} = \frac{1}{2\pi}\frac{1}{\sqrt{L_{\mathrm{r,x}}C_{\mathrm{r,x}}}} \tag{12}$$

### B. STATE-SPACE MODEL

An alternative mathematical representation of the MSRC can be obtained by developing the differential equations of the system. From this, a state-space model can be derived, which is commonly used for simulation or for the direct development of an appropriate control strategy.

The inductances in one port can be summed up to

$$L_{\mathrm{x}} = L_{\mathrm{r,x}} + L_{\mathrm{m,x}} \tag{13}$$

The basic differential equations for one port x in a MSRC are

$$\frac{di_{\mathrm{r,x}}}{dt}L_{\mathrm{x}} + \sum_{y=1,y\neq x}^{N}\frac{di_{\mathrm{r,y}}}{dt}M_{\mathrm{xy}} + i_{\mathrm{r,x}}R_{\mathrm{x}} + V_{\mathrm{c,x}} = V_{\mathrm{x}}$$
$$\frac{dV_{\mathrm{c,x}}}{dt}C_{\mathrm{r,x}} = i_{\mathrm{r,x}} \tag{14}$$

whereby $i_{\mathrm{r,x}}$ denote the port currents and $V_{\mathrm{x}}$ are the applied port voltages. The mutual inductance $M_{\mathrm{xy}}$ is defined as

$$M_{\mathrm{xy}} = k_{\mathrm{xy}}\sqrt{L_{\mathrm{x}}L_{\mathrm{y}}} = \sqrt{L_{\mathrm{m,x}}L_{\mathrm{m,y}}} \tag{15}$$

and $k_{\mathrm{xy}}$ is the magnetic coupling factor between the individual mutual inductances. The equations for a MSRC can be written as:

$$\begin{aligned}
&\dot{i}_{\mathrm{r,1}}L_1 + \dot{i}_{\mathrm{r,2}}M_{12} + \cdots + \dot{i}_{\mathrm{r,N}}M_{1\mathrm{N}} = V_1 - i_{\mathrm{r,1}}R_1 - V_{\mathrm{c,1}}\\
&\qquad\qquad\vdots\\
&\dot{i}_{\mathrm{r,N}}L_{\mathrm{N}} + \dot{i}_{\mathrm{r,1}}M_{\mathrm{N1}} + \cdots + \dot{i}_{\mathrm{r,N}}M_{\mathrm{N(N-1)}} = V_{\mathrm{N}} - i_{\mathrm{r,N}}R_{\mathrm{N}} - V_{\mathrm{c,N}}
\end{aligned} \tag{16}$$

and

$$\begin{aligned}
\dot{V}_{\mathrm{c,1}}C_{\mathrm{r,1}} &= i_{\mathrm{r,1}}\\
&\vdots\\
\dot{V}_{\mathrm{c,N}}C_{\mathrm{r,N1}} &= i_{\mathrm{r,N}}.
\end{aligned} \tag{17}$$

In **Fig. 5** the equivalent circuit model for a three port SRC is given.

The differential equations in Eqs. (16) and (17) can be represented as descriptor model, which is in general shaped as

$$\mathbf{F}\dot{x} = \mathbf{A}x + \mathbf{B}u \tag{18}$$

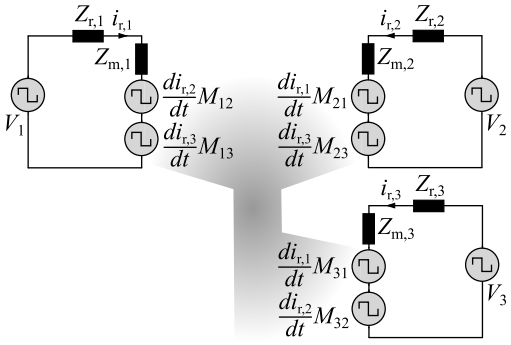


**FIGURE 5.** Equivalent circuit model for the 3-port SRC shown in Fig. 1.

The vectors and matrices from Eqs. (16) and (17) in descriptor representation are

$$\mathbf{F} = \begin{bmatrix}
L_1 & M_{12} & \cdots & M_{1\mathrm{N}} & 0 & 0 & \cdots & 0\\
M_{21} & L_2 & \cdots & M_{2\mathrm{N}} & 0 & 0 & \cdots & 0\\
\vdots & & \ddots & & \vdots & \vdots & \ddots & \vdots\\
M_{\mathrm{N1}} & M_{\mathrm{N2}} & \cdots & L_{\mathrm{N}} & 0 & 0 & \cdots & 0\\
0 & 0 & \cdots & 0 & 1 & 0 & \cdots & 0\\
0 & 0 & \cdots & 0 & 0 & 1 & \cdots & 0\\
\vdots & & \ddots & \vdots & \vdots & & \ddots & \vdots\\
0 & 0 & \cdots & 0 & 0 & 0 & \cdots & 1
\end{bmatrix} \tag{19}$$

$$\mathbf{A} = \begin{bmatrix}
-R_1 & 0 & \cdots & 0 & -1 & 0 & \cdots & 0\\
0 & -R_2 & \cdots & 0 & 0 & -1 & \cdots & 0\\
\vdots & & \ddots & & \vdots & \vdots & \ddots & \vdots\\
0 & 0 & \cdots & -R_{\mathrm{N}} & 0 & 0 & \cdots & -1\\
\frac{1}{C_{\mathrm{r,1}}} & 0 & \cdots & 0 & 0 & 0 & \cdots & 0\\
0 & \frac{1}{C_{\mathrm{r,2}}} & \cdots & 0 & 0 & 0 & \cdots & 0\\
\vdots & & \ddots & \vdots & \vdots & & \ddots & \vdots\\
0 & 0 & \cdots & \frac{1}{C_{\mathrm{r,N}}} & 0 & 0 & \cdots & 0
\end{bmatrix} \tag{20}$$

$$\mathbf{B} = \begin{bmatrix}
1 & 0 & \cdots & 0\\
0 & 1 & \cdots & 0\\
\vdots & & \ddots & \vdots\\
0 & 0 & \cdots & 1\\
0 & 0 & \cdots & 0\\
0 & 0 & \cdots & 0\\
\vdots & & \ddots & \vdots\\
0 & 0 & \cdots & 0
\end{bmatrix};\quad x = \begin{pmatrix}
i_{\mathrm{r,1}}\\ i_{\mathrm{r,2}}\\ \vdots\\ i_{\mathrm{r,N}}\\ V_{\mathrm{c,1}}\\ \vdots\\ V_{\mathrm{c,N}}
\end{pmatrix};\quad u = \begin{pmatrix}
V_1\\ V_2\\ \vdots\\ V_{\mathrm{N}}
\end{pmatrix}. \tag{21}$$

If the matrix $\mathbf{F}$ is not singular, then the descriptor system can be transformed to a state space model with the transformation by

$$\dot{x} = \mathbf{F}^{-1}\mathbf{A}x + \mathbf{F}^{-1}\mathbf{B}u \tag{22}$$

### C. PRELIMINARY VALIDATION AND COMPARISON

Preliminary validation and comparison of admittance and state-space models have been done in simulation, the results being reported in **Fig. 6**. The time waveforms are generated by numerical integration and in case of the admittance model the superposition of the calculated waveforms for the fundamental up to the 7–th harmonic have been considered. The used circuit parameters are listed in **Tab. 1** which correspond to the hardware demonstrator shown in **Fig. 2**.

The different modelling approaches show similar average power in the considered operating conditions, as detailed in the figure caption. The maximum absolute difference between average powers in the two models, i.e., **Fig. 6a.iii** and **Fig. 6b.iii**, is about 250 W. The admittance model is more efficient regarding calculation, which of course reduces with increasing number of added harmonics or added terms for $a_{\mathrm{x,k}}$, whereby the state-space model shows better time resolution for the waveforms. Due to the importance of better time resolution, the state-space model was used for all further investigations. As a simplification, the bride output voltage during a switching period's interlock or dead-time was assumed to be 0 V for the state-space model in order to minimize computation time, even though in reality the direction of the current flow during the dead-time would define the value of the bride output voltages. The authors believe that to incorporate this into the calculation would introduce significant computational effort but with negligible benefit toward the objectives of this paper: i.e. to show the relative improvement to the ZVS region possible with "duty cycle" modulation, rather than the exact precise boundaries of the ZVS region. Similarly, the dead-time duration is typically order(s) of magnitude smaller than switching period and therefore negligible when calculating overall power flow.[2] Should more precise estimation of the ZVS region boundaries be needed, a more accurate modelling approach could be used whereby the calculations are split into more time intervals each with a dedicated state space models as shown in [25].

### D. EXPERIMENTAL VALIDATION

Using the measured hardware parameters given in **Tab. 1**, validation of the state-space model was done by comparing simulated waveforms to corresponding measured waveforms using the same operating conditions (frequency and phase angles etc…).[3] An example of this is shown via side-by-side plots in **Fig. 7** where significant agreement of the waveforms in **a** and **b** can be seen with only a small mismatch for the magnitude of the measured current. This mismatch is due to the aforementioned assumption of 0 V full-bridge output voltage during the dead-time. **b** reveals the effect of the current direction during the dead time; non-zero voltage caused by body diode conduction shifting the potential towards that of the DC-link voltage. This results in an effective phase shift of $V_2$ in contrast to simulation where the port voltages are perfectly aligned with 0 V in the switching transition.

[2]The dead time used for calculations in this paper was 200ns.

[3]The verification was performed at half of the rated voltage.

**TABLE 1. Component values for the hardware demonstrator.**

| Design. | Description | Value |
|---|---|---|
| $C_{\mathrm{dc},1}$ | DC-link capacitor port 1 | 2.35 mF |
| $C_{\mathrm{dc},2}$ | DC-link capacitor port 2 | 10 µF |
| $C_{\mathrm{dc},3}$ | DC-link capacitor port 3 | 70 µF |
| $C_{\mathrm{r},1}$ | resonant capacitor port 1 | 386 nF |
| $C_{\mathrm{r},2}$ | resonant capacitor port 2 | 383 nF |
| $C_{\mathrm{r},3}$ | resonant capacitor port 3 | 4.68 µF |
| $L_{\mathrm{r},1}$ | resonant inductance port 1 | 17.40 µH |
| $L_{\mathrm{r},2}$ | resonant inductance port 2 | 17.40 µH |
| $L_{\mathrm{r},3}$ | resonant inductance port 3 | 1.35 µH |
| $L_{\mathrm{m},1}$ | transformer main inductance port 1 | 1 mH |
| $L_{\mathrm{m},2}$ | transformer main inductance port 2 | 1 mH |
| $L_{\mathrm{m},3}$ | transformer main inductance port 3 | 40 µH |
| $R_1$ | parasitic resistance port 1 | 18.30 mΩ |
| $R_2$ | parasitic resistance port 2 | 18.30 mΩ |
| $R_3$ | parasitic resistance port 3 | 4.20 mΩ |
| $n_{12}$ | transformer winding ratio port 1 to 2 | 1 |
| $n_{13}$ | transformer winding ratio port 1 to 3 | 5 |
| $n_{23}$ | transformer winding ratio port 2 to 3 | 5 |
| $k$ | transformer coupling factor | 0.9998 |

**TABLE 2. Power semiconductors and its characteristic values.**

| Design. | Description | $Q_{\mathrm{oss,x,eq}}$ | $C_{\mathrm{oss,x,lin}}$ |
|---|---|---|---|
| $\mathrm{S_{1x}}$, $\mathrm{S_{2x}}$ | IMBG65R022M1H [28] | 158 nC | 262 pF |
| $\mathrm{S_{3x}}$ | BSC040N10NS5SC [29] | 150 nC | 1.26 nF |

## III. DETERMINATION OF SWITCHING LOSSES

For ensuring most efficient operation of the MSRC for a wide HV battery range, investigations about the losses have to be performed. While the conduction losses could be simply determined by adding the on-resistance to the used calculation model, the switching losses have to be calculated differently due to the influence on the overall losses of the SRC. The switches placed at the individual ports are listed in **Tab. 2** and show that Si and SiC based semiconductors are used simultaneously in the LV and HV ports respectively, making an individual loss calculation necessary.

To improve the model detail and accuracy it is mandatory to determine how the commutation of the switched currents will be done, because this is influencing the losses of the individual switches. Especially the energy dissipated during a forced commutation of the current during turn-on sequence (hard switching/commutation) is higher compared to a turn-off sequence with natural commutation to the opposing switch. Therefore, implementing ZVS turn-on switching is the preferred choice to reduce switching losses in total [26]. Note: Although full ZVS could be reached, still a small amount of switching losses is still present ($C_{\mathrm{oss}}$ related + gating losses), described in [27].

### A. TURN-OFF SWITCHING LOSSES CALCULATION

Considering that the SRC will be operated at ZVS only, the turn-off losses can be calculated using a lookup table or an

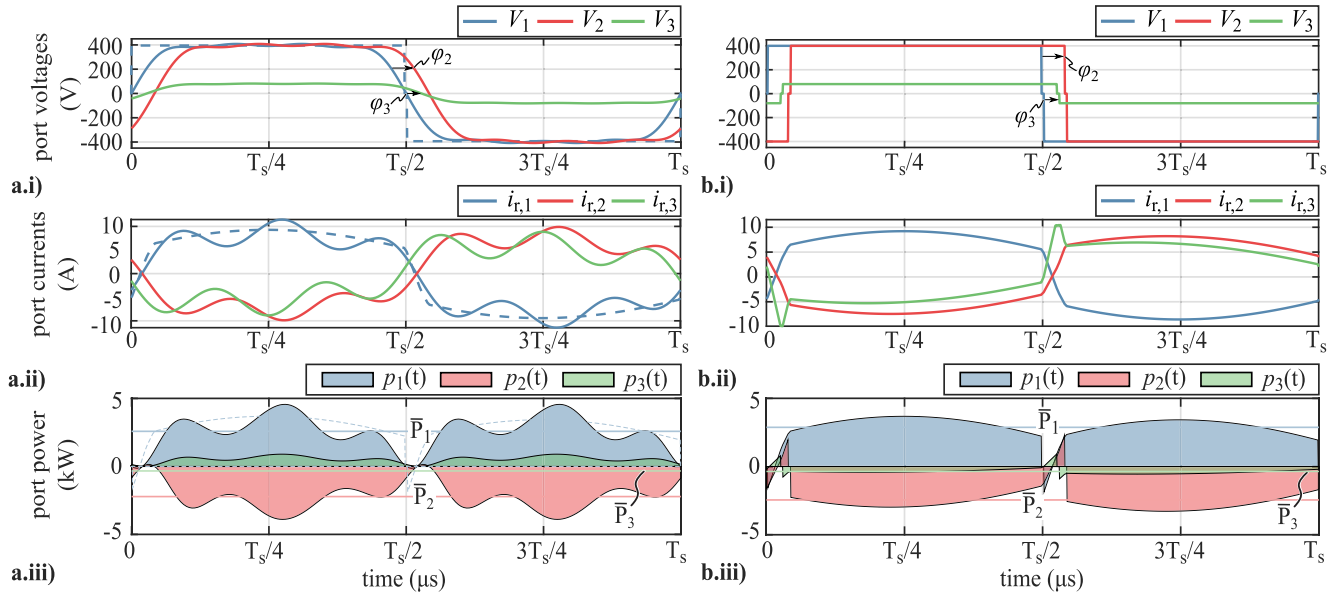


**FIGURE 6.** Comparison of voltage, current and power waveforms between the state-space model and the admittance model generated waveforms for a used switching frequency of $f_s = 100$ KHz and DC-link voltages of $V_{dc,1} = 400$ V, $V_{dc,2} = 400$ V and $V_{dc,3} = 80$ V and phase shifts ($\varphi_1$ serves as reference and is always 0) $\varphi_2 = 15°$ and $\varphi_3 = 10°$. Simulated waveforms based on the admittance model showing **a.i** voltage waveforms **a.ii** current waveforms and **a.iii** power waveforms. The state space model based waveforms showing **b.i** voltage waveforms, **b.ii** current waveforms and **b.iii** power waveforms. The dashed lines in **a** are the equivalent waveforms of the first port from **b**. The admittance model uses the fundamental up to the 7–th harmonic for this comparison.

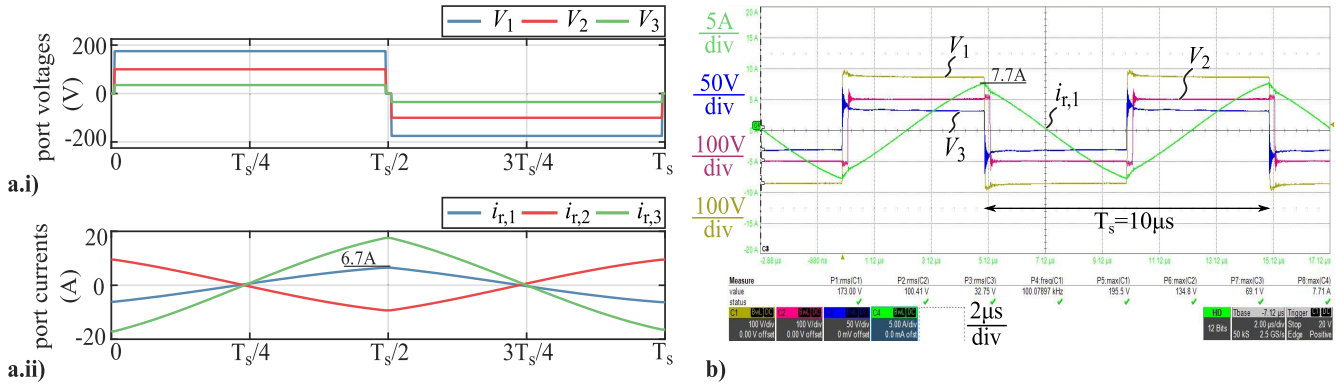


**FIGURE 7.** State-space model based simulated waveforms and corresponding hardware measurements for a switching frequency of $f_s = 100$ KHz, phase angles $\varphi_1 = \varphi_2 = \varphi_3 = 0$, and DC-link voltages of $V_{dc,1} = 175$ V, $V_{dc,2} = 100$ V and $V_{dc,3} = 35$ V. Simulated waveforms show the port voltages in **a.i** and resonant circuit currents of each port in **a.ii**. Measured waveforms in **b** show the three port voltages and the current flowing from port 1 into its resonant circuit with its peak current highlighted. The peak value of the resonant current from port 1 is annotated for both simulation and measurement.

equation which correlates the turned off current to energy dissipation during this event. To make the loss calculation model independent from actual device parameters a linear representation of the losses as a function of the commuted current divided by the nominal peak current could be used. To improve accuracy a more sophisticated method is shown in [27] for SiC devices including a comprehensive analysis. This paper is giving an indication of the turn-off current behaviour and the improvement one can get from the proposed modulation strategy shown in Section IV, even though a detailed model is not considered but could be considered in future investigations.

The results reported in **Fig. 8** are aimed at showing the effect of the modulation strategy on the turn-off current for given operating conditions of the three port converter; specifically, a low battery state-of-charge (low voltage) on port 2 of the converter and light load. The bridge output voltages, resonant currents and powers are provided in **a** and **c** diagrams for standard control and the proposed duty cycle control (as presented and discussed in Section IV), respectively. Diagrams **b** and **d** show the corresponding turn-off currents for the full-bridge on port 2 (constant current contours) as a function of the power in port 2 and 3 (yellow star marker). The representation of the switched turn-off current is given in

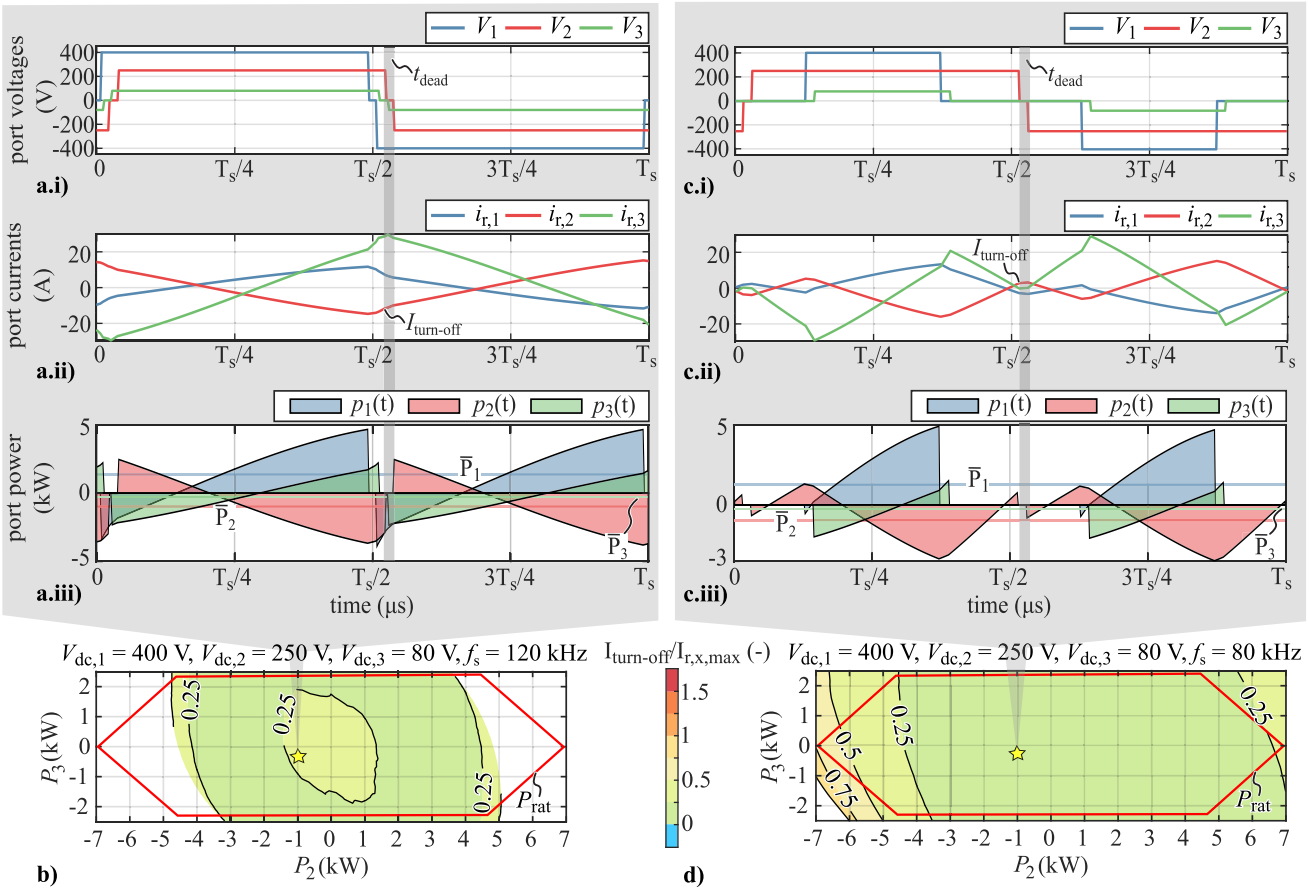


**FIGURE 8.** Illustration of the different turn-off currents for the full-bridge on port 2, which is connected to the HV battery and shown for $V_{dc,1} = 400$ V, $V_{dc,2} = 250$ V and $V_{dc,3} = 80$ V, which corresponds to a low state-of-charge of the HV battery. The corresponding waveforms for the normal operation with its a.i voltages a.ii currents and a.iii power. In b the map for the turn-off currents over the whole operation range in normal operation is given. The corresponding waveforms for the duty cycle mode operation with its c.i voltages c.ii currents and c.iii power. In d the map for the turn-off currents over the whole operation range in duty cycle operation is given. The waveforms in a and c are given for a transferred power of $P_2 = -1$ kW and $P_3 = -250$ W.

per unit form, i.e., its absolute value is divided by the nominal peak current of the individual ports[4] The comparison between **b** and **d** shows that, although the modulation is aiming at ZVS at turn-on, the turn-off current can be decreased at light load operation, which is also beneficial for the efficiency of the converter.

### B. IDENTIFYING ZVS CONDITION AT TURN-ON

ZVS condition at turn-on requires that the output capacitance seen from each leg output node has to be discharged before switching. The dominant component is due to the output capacitance of the power semiconductors, being highly non-linear with respect to the switched voltage. The corresponding $Q_{oss}$ charge and the linearized capacitance $C_{oss,x,lin}$ are used for calculating the equivalent capacitance $C_{oss,x,eq.}$ adopted in the simulation model. The considered equation is

$$C_{oss,x,eq} = (Q_{oss,x,eq} + (V_{dc,x} - V_{lin})C_{oss,x,lin})/V_{dc,x} \quad (23)$$

[4]Maximum current ratings for the components within the resonant circuit: $I_{r,1,max} = 45$ A, $I_{r,2,max} = 45$ A and $I_{r,3,max} = 55$ A.

The adopted power devices from Infineon with its corresponding data is given in **Tab. 2**. It is worth noticing that two devices are always connected in parallel at port 3 for ensuring the proper current and power capabilities. The adopted linearization voltages $V_{lin}$ for the port 1, 2 and 3 are 400 V, 400 V and 50 V, respectively.

The method for identifying if ZVS condition at turn-on is achieved or not is based on the charge stored in the output capacitance of the power semiconductors devices of the individual legs, as calculated with the following equation:

$$Q_{oss,x} = 2C_{oss,x,eq}V_{dc,x} \quad (24)$$

It is worth noticing that if both legs are switched at the same time, then a factor of 4 can be applied instead of 2 to calculate the charge of the whole full-bridge. At the turn-off instant of the opposite switch within each individual leg, the current in the resonant circuit is integrated over the dead time interval $t_{dead}$, as given in Eq. (25). The obtained charge value is compared to the one stored in the considered leg and their ratio $Q_{ind,x}/Q_{oss,x}$ is calculated. Based on the resulting value the commutation condition is estimated, i.e., if $\geq 1$ or

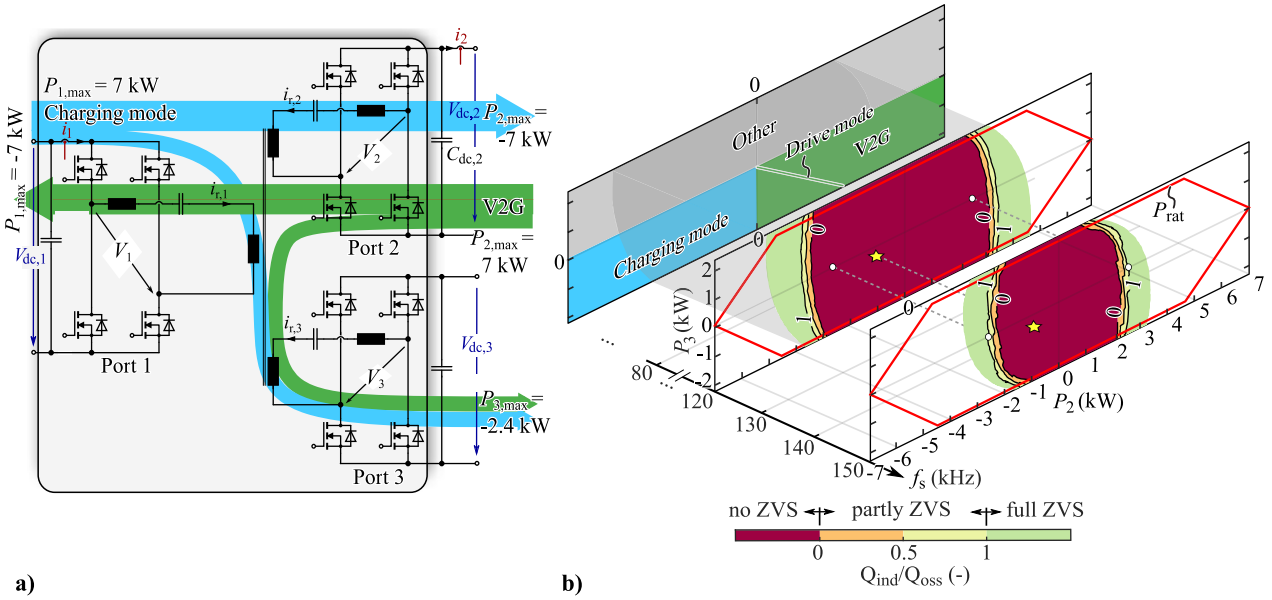


**FIGURE 9.** The three port series resonant converter with a its highlighted power flow directions for charging, vehicle-to-grid and drive mode. **b** The ZVS map given with the corresponding areas for charging and V2G including the drive mode for a low state of charge of the HV battery with the DC-link voltages of $V_{dc,1} = 400\,V$, $V_{dc,2} = 250\,V$ and $V_{dc,3} = 80\,V$.

between 1 and 0 full or partial ZVS is attained, respectively, whilst if below 0 hard commutation is experienced.[5]

$$Q_{ind,x} = \int_{\tau}^{\tau+t_{dead}} i_{r,x}(t)dt \tag{25}$$

Due to the operation above the resonance frequency the energy is stored in the resonant inductor, which explains the labelling for the given charge as $Q_{ind}$.

### C. ZVS MAPS FOR TURN-ON

Main operation modes of the converter are based on the direction of the power flow, i.e., the charging, V2G and drive mode, this last being a sub mode of the V2G mode whereby no power is transferred to port 1 (i.e., power is drawn from the HV battery to feed the LV stage). The situation is graphically resumed in **Fig. 9a**. The maximum (absolute value) power of port 1 and 2 is $P_{1,max} = 7\,kW$ and $P_{2,max} = 7\,kW$, whilst port 3 is limited by $P_{3,max} = 2.4\,kW$. A constraint is however needed, given by the following equation

$$\sum_{x=1}^{3} P_x + P_{loss} = 0 \tag{26}$$

e.g., in the charging mode the LV stage has to be supplied with 2.4 kW, then the HV battery can only be charged with 4.6 kW due to the power limit of port 1, being also valid for the V2G operation.

All other modes, as highlighted in **Fig. 9b** are not relevant for a permanent operation. An example for another operation mode is the pre-charging of the DC-link capacitors, mainly interesting for the DC-link capacitor connected to port 1. Due to the SRCs full bi-bidirectionallity pre-charing from the HV or LV battery could be implemented as shown in [22] and [31].

Evaluation of the area where ZVS turn-on is achieved or not is of paramount importance to understand the feasible operating range of the converter and any room to widen it and/or to improve the efficiency by a proper control strategy within certain operating regions.

An example is reported in **Fig. 9b**, where the operating point $V_{dc,1} = 400\,V$, $V_{dc,2} = 250\,V$ and $V_{dc,3} = 80\,V$ (which corresponds to a low state-of-charge of the HV battery) and light load operation have been considered, as previously highlighted. The different modes are reported in the top left diagram as a function of the port power levels. The ZVS maps have been drawn at two switching frequencies, namely 120 kHz and 150 kHz, as shown in the two additional diagrams. The red polygon encircles the operating range, limited by the ports maximum power capability of 7 kW. It is easy to verify that with a smaller switching frequency (i.e., close to the resonant frequency) the ZVS region is pushed to the outside allowing a higher power transfer region, and with increasing switching frequency the ZVS region shrinks, leading to a lower power transfer region. The trade-off for the control for achieving best efficiency is to decrease the switching frequency and linked to that decreasing the frequency dependent losses within the magnetic components while still maintaining ZVS for all full bridges, which was introduced in [17] but without investigations into ZVS operation. The determination if full, partly or no ZVS is achieved is done by evaluating $Q_{ind,x}/Q_{oss,x}$, as already mentioned.

## IV. DUTY CYCLE MODE

A substantial amount of circulating reactive power can occur in a MSRC (and thus poor efficiency) when the required volt-

[5]Note: the relation in case of hard commutation is not regarding the reverse recovery charge $Q_{rr}$, which might lead to an error [30].

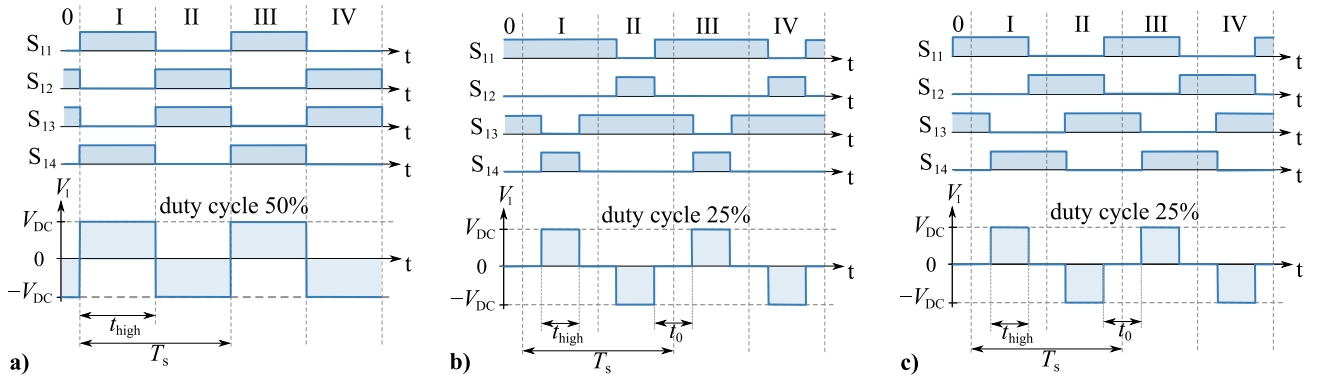


**FIGURE 10.** Comparison of the different modulation schemes and the possible combinations for the normal mode and the duty-cylce mode shown for the full bridge of port 1. **a** Pulse pattern for normal operation, whereby the duty cycle of the port voltage is fixed to 50%. **b** Pattern generated by a duty cycle change of the individual half bridges. The port voltage shows an example for a duty cycle of 25%. In **c** the pattern for the full bridge is shown maintained by a phase shift of the individual half bridges resulting again in a duty cycle of 25% for the port voltage. Note: The influence of the dead time is neglected in these illustrations.

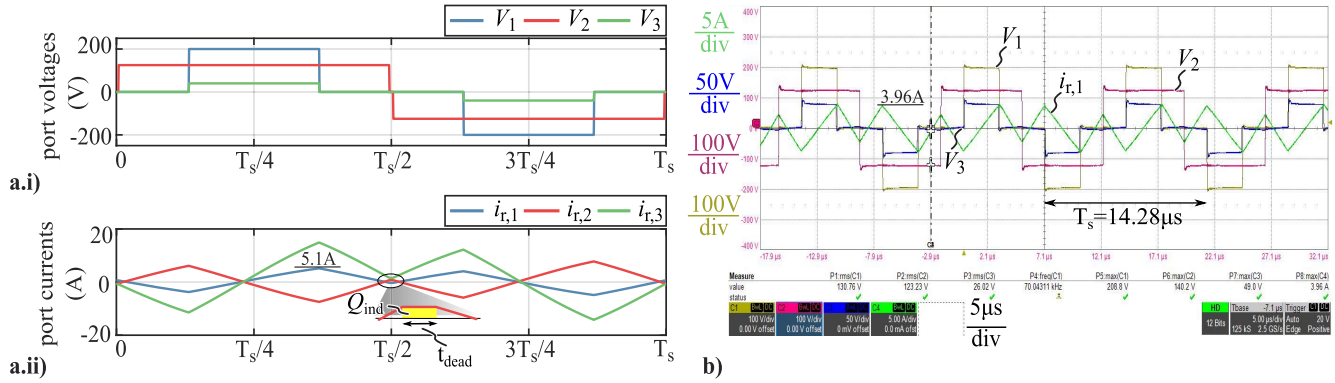


**FIGURE 11.** State-space model based simulated waveforms for the proposed duty cycle modulation using a switching frequency of $f_s = 100$ KHz and DC-link voltages of $V_{dc,1} = 200$ V, $V_{dc,2} = 125$ V and $V_{dc,3} = 45$ V, showing **a.i** the port voltages and **a.ii** port currents, flowing in the resonant circuit. Indicated is the peak value of the resonant current from port 1 **b** shows the corresponding verification measurement of the three port voltages and the current flowing from port 1 into its resonant circuit with its highlighted peak current.

age gain between any two ports is unfavorable, i.e., widely diverging from the turns ratio of the transformer. Additionally, when using "normal mode" modulation in light load operation, a high switching frequency $f_s$ is needed which can compound the poor efficiency with higher switching (frequency) related losses, especially if ZVS is not achieved. The method proposed in this paper to improve the efficiency of the converter in such operating conditions is to modify the full-bridge output waveform by introducing zero voltage intervals, thus reducing the peak value of the fundamental of the fed voltage to the resonant network of each port. This is achieved by manipulating the effective duty cycle of ports with higher DC-link voltages in order to equalize the voltage-time-area on all ports,[6] on top of the frequency and phase angle control given in recent MSRC literature. The advantage of the proposed method is that the modulation can be implemented without any additional sensing or measuring electronics. Furthermore, the applied switching frequency can be lower compared to the normal mode operation in the same operating conditions thus reducing the higher switching (frequency) related losses incurred with conventional normal mode operation in light load conditions. For the example application used in this paper (and described in Section I), the proposed superposition of duty cycle control is shown to improve efficiency up to 30 % rated load (approx. 2 kW) before the normal mode modulation gets more efficient.

In the next sub-sections the duty cycle mode is introduced and main implementation strategies shortly presented and discussed. The preliminary validation of the simulation model against the experimental system is also reported. Detailed comparison of the two modes in the simulation model is then considered, demonstrating that ZVS operating conditions can be achieved with the proposed modulation strategy in the low power range. Finally, experimental validations are reported by showing the efficiency gain that can be attained.

### A. MODULATION AND MODEL VALIDATION

The normal mode operation of the full-bridge driving signals and the corresponding output voltage are shown in **Fig. 10a**. 50 % duty cycle is adopted in both legs and rectangular voltage is therefore obtained at the output. Reduction of the peak

[6]For a safety-margin and to maximize the ZVS region, the duty cycle on the ports with higher DC-link voltage (w.r.t the turns-ratios) was decreased slightly beyond what is theoretically needed; resulting in a smaller voltage time area than the other ports.

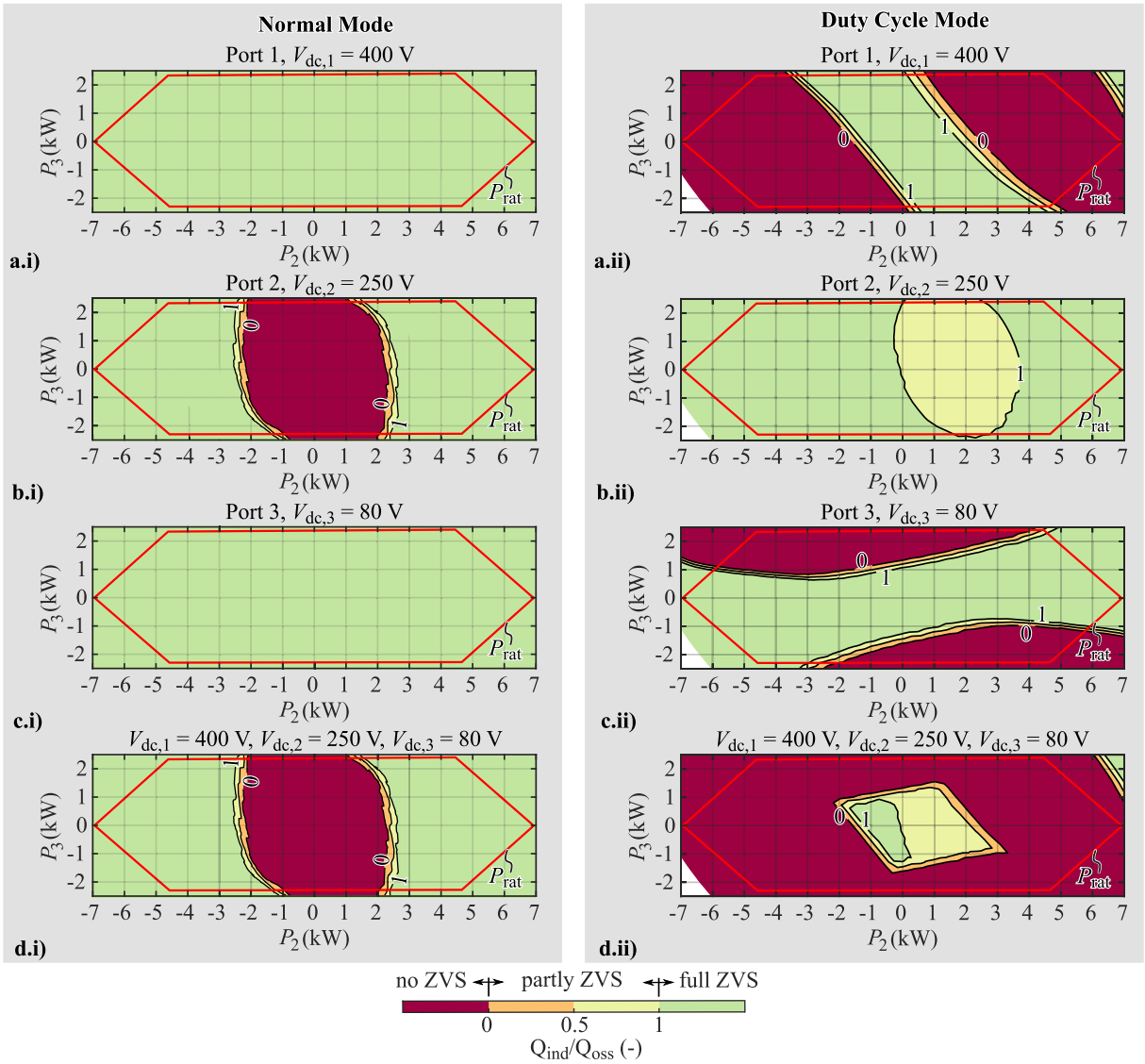


**FIGURE 12.** ZVS maps comparison for the normal (left) and the duty cycle (right) mode operations: maps for port 1, 2 and 3 in a, b, c respectively; ***superposition*** of all ports in d.

value of the fundamental voltage can be achieved by reducing the active intervals, i.e., introducing zero voltage intervals. This can be accomplished in two ways, i.e., by either modifying the duty cycle of each leg, **Fig. 10b**, or introducing a phase shift between them (as normally done with triple phase shift control of DAB, [19], [20]), **Fig. 10c**. It is clearly visible that they lead to the same shape of the output voltage waveform. The duty cycle of the individual ports is defined as $d_x = t_{high,x}/T_s$ and the resulting port voltage time area is

$$\int_{\tau}^{\tau+T_s/2} |V_x(t)|dt = V_{DC,x} d_x \tag{27}$$

(neglecting $t_{dead}$). The Fourier coefficient for (as calculated in Eq. (1) for normal mode operation) could be applied also for duty cycle mode, which yield in

$$b_{x,k} = \frac{4}{k\pi} V_{DC,x} \cos\left(\omega_k \frac{t_0}{2}\right) \tag{28}$$

with $t_0$ being the "zero voltage time".

A preliminary validation of the duty cycle mode has been performed by comparing the results of the simulated state-space model, and the actual measurements in the same operating conditions, as reported in **Fig. 11**. The voltage signals in **a.i** show an equal voltage time area for a low state-of-charge for the HV battery.[7] The calculated currents are given in **a.ii** and show that the resonant current $i_{r,2}$ changes its polarity close to the switching instant which enables building up the charge within the resonant inductor to fully discharge the

[7]The verification was performed at half of the rated voltage.

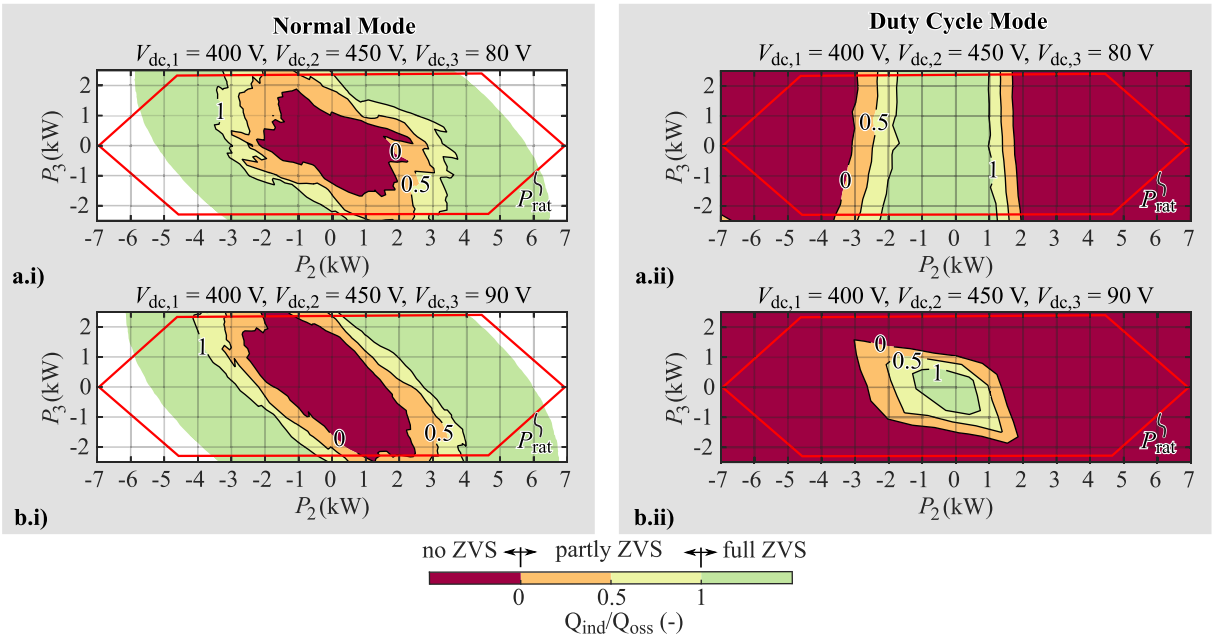


**FIGURE 13.** ***Superposition*** **of all ports ZVS maps for the normal (left; using $f_s$ = 120 kHz and 150 kHz) and the duty cycle (right; using $f_s$ = 80 kHz) mode operations, and two different values of the LV DC-link voltage (high state-of-charge of the HV battery for all results).**

switches output capacitance yielding in ZVS turn-on. A good correlation can be verified by comparing the simulated and measured waveforms, even though the peak values show a small deviation due to the simplified modeling of the dead time effects. However, the achieved precision is still sufficient for all further investigations.

### B. COMPARISONS BETWEEN THE TWO MODES

The results of the comparison of normal and duty cycle mode for a low state-of-charge of the HV battery ($V_{dc,1}$ = 400 V, $V_{dc,2}$ = 250 V and $V_{dc,3}$ = 80 V) are reported in **Fig. 12**. The left plots **x.i** are referred to the normal mode operation and the right plots **x.ii** to the duty cycle mode. The *superposition* of all ports, i.e., the minimum values of the ratio $Q_{ind,x}/Q_{oss,x}$ for all the ports, is then reported in **d.i** and **d.ii**, respectively. The duty cycle mode is operated at $f_s$ = 80 kHz and the normal mode with $f_s$ = 120 kHz to 150 kHz, as already discussed in **Fig. 9b**. (Whereby the 120 kHz define the operation for higher and 150 kHz is used for the smaller reference values). One can see that with the normal mode the port with the lowest DC-link voltage, i.e., port 2, is not achieving ZVS for the light load operation area. With the suggested duty cycle modulation the non-ZVS area is shifted towards the other ports, but achieving ZVS in the light load operation area. Another advantage of this modulation scheme is that the operation with lower switching frequency is possible compared to the normal mode, which suffers from exceeding the current rating if the switching frequency is selected too small.

In **Fig. 13** a high state-of-charge condition for the HV battery has been considered and the comparison of the ZVS maps

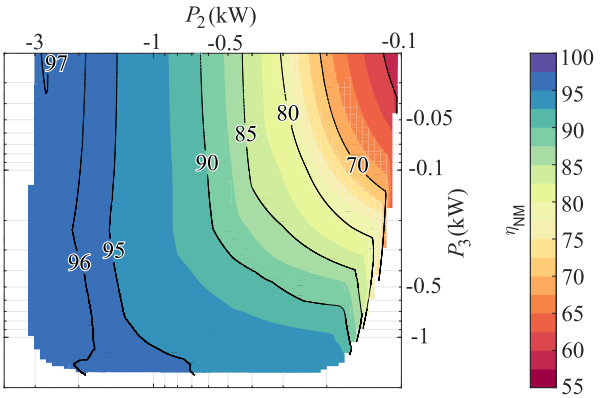


**FIGURE 14.** **Efficiency map adopting the normal mode operation for the DC-link voltages of $V_{dc,1}$ = 400 V, $V_{dc,2}$ = 250 V and $V_{dc,3}$ = 70 V.**

for normal (in ·**.i**) and duty cycle (in ·**.ii**) modes, and for two different values of the LV DC-link voltage ($V_{dc,3}$ = 80 V in **b.i** and $V_{dc,3}$ = 90 V in **b.ii**) is reported. Similar result can be verified in both operating conditions, which show increased light load efficiency adopting duty cycle mode operations. The DC-link voltage $V_{dc,3}$ on port 3 is connected to the subsequent buck converter connected to the 12 V auxiliary battery output, as shown in **Fig. 1**. $V_{dc,3}$ could be varied between 12 V and approximately 90 V, whereby the upper limit is defined by the maximum voltage rating of the power semiconductors and a margin which regards the voltage overshoot during switching operation. A proper snubber network, which is explained in detail in [32], was applied for ensuring a safe operation within the actual circuit layout. Note: The DC-link

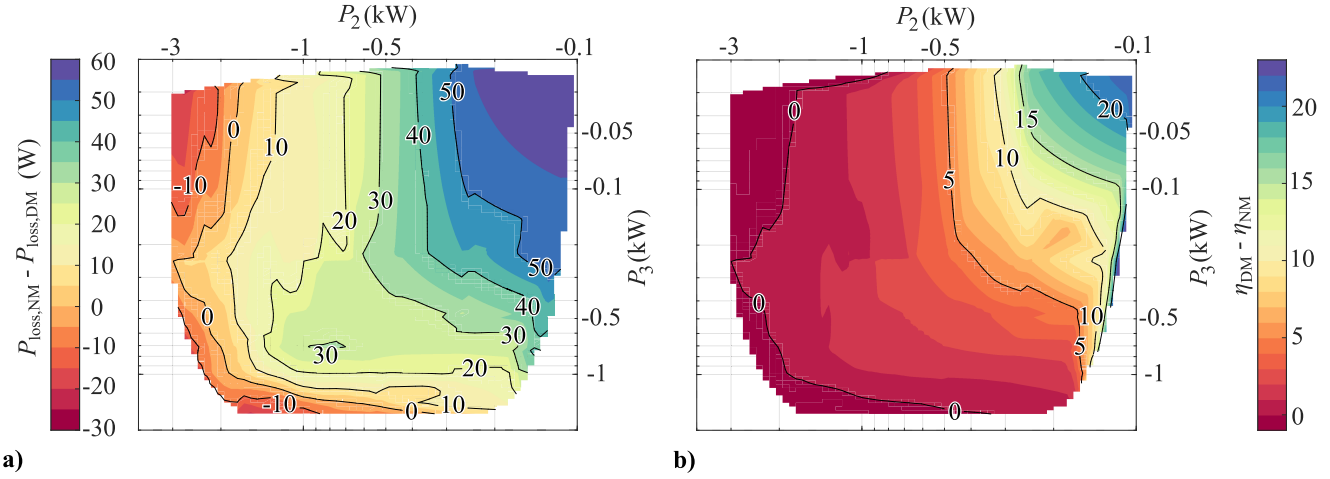


**FIGURE 15.** Comparison of measurements results for normal versus duty cycle mode for an operation point of $V_{dc,1} = 400\,V$, $V_{dc,2} = 250\,V$ and $V_{dc,3} = 70\,V$, which corresponds to a low state-of-charge for the HV battery. In a the difference of the losses for both modes is given and in b the difference in efficiency is shown. (NM ... normal mode, DM ... duty cycle mode).

voltage on port 3 not only influences the efficiency of the Multiport SRC but also the subsequent Buck converter.

### C. EXPERIMENTAL RESULTS AND EFFICIENCY GAIN

Experimental validation of the efficiency gains which can be achieved by the proposed modulation approach in the light load operation has been performed using a Yokogawa WT5000 power analyzer. The operating point has been considered, which corresponds to a low state-of-charge for the HV battery (quite similar operating point as in **Fig. 12** with a slightly reduced DC-link voltage at port 3). The results of the efficiency measurements applying normal mode operation are reported in **Fig. 14**. The generated map consists out of 86 measurement points and linear interpolation is adopted to refine the graph. The axis at the plot are scaled logarithmic to highlight the light load operation area. The measured efficiency is between 55 % and 97 %, which is obviously unsatisfactory for the light load operation range.

The comparison with respect to duty cycle mode operation is reported in **Fig. 15** and it is based on the same set of measurement points. The difference between the losses and the efficiency gain are reported in the two subplots. The saved losses are going up to nearly 60 W, which corresponds to an increase of efficiency of nearly 22 %. The overall efficiency for the duty cycle mode can simply be calculated by adding the values of **b** to **Fig. 14**, leading to a worst efficiency of 77 %, significantly higher than with the normal mode modulation.

## V. CONCLUSION AND FUTURE ACTIVITIES

In this paper a three port SRC for an OBC use case has been considered and a novel control proposal for the efficiency improvement in the light load operation of the converter has been proposed and validated.

The multiport approach combined with symmetrical series resonant circuits enable the required galvanic isolated connection from the grid-side PFC stage to both the main HV traction and the auxiliary LV batteries of the vehicle, allowing to achieve increased power densities and enabling a flexible (and bidirectional) power routing among the different ports.

A detailed literature review about the same or similar topologies and/or explaining corresponding control designs and requirements was provided.

Two modelling approaches were introduced and validated against experimental measurements, whereby the admittance approach provides benefits regarding computation and the state-space model regarding time resolution vs. simulation time ratio. They represent the basis for the calculation method of ZVS maps, adopted to verify whether ZVS conditions are achieved or not in the whole operating range of the converter applying different control approaches.

One of the drawbacks of the SRC is in fact low efficiency in light load operation mainly due to the lack of ZVS, especially if the DC-link voltages of the three ports do not follow the turns ratio of the transformer.

A possible solution for increasing the light load efficiency was introduced and validated, based on the full utilization of all three control parameters: the phase shift, which is controlling the actual power flow, the switching frequency, which is changed based on power reference values aiming at ZVS operation in all the full bridges, and the duty cycle according to the DC-link voltages.

A potential limitation of the duty cycle mode is limited power transfer due to the deceased voltage-time area in some of the ports, which in fact depends heavily on the switching frequency used. Nevertheless, in this application, this was not an issue because of the target region, which is light-load operation using a switching frequency close to the resonance frequency. In duty cycle mode, the same amount of power is transferred, but there is less voltage time area available, which requires a higher current. At a certain point, this makes normal mode more efficient. Additionally, MSRC's duty

cycle generates higher frequency components in the currents, however, these have a limited impact on the active power transfer.

The experimental validation of the proposed control strategy was performed by using the hardware demonstrator shown in **Fig. 2**, featuring a high power density [9]. The results highlight a gain in efficiency up to 22 %, with a loss saving of up to 55 W, as well as significant average efficiency improvements with respect to standard control approaches.

In the light load operation it is expected that overheating of the magnetic components is not an issue, whereas power semiconductors could heat up due to high switching losses, their reduction by changing the switching frequency and/or the duty cycle is also going into the direction of higher system reliability. Therefore it is also beneficial to use the duty cycle modulation done via phase shift, proposed in **Fig. 10c** due to the equal turn-on time of the individual switches resulting in a more equal heat distribution.

A possible future extension of the presented workflow is the complete and more accurate modelling of loss sources, including power semiconductor and passive component (as suggested in [33]), also including the behavior during the dead times (which has been neglected in the present analysis), aiming at achieving an overall optimization by a Pareto front analysis. Another possibility would be to use the provided modelling approach for N ports, which is especially interesting for three-phase modular AC/DC applications [9], [21].

## REFERENCES


[1] J. Yuan, L. Dorn-Gomba, A. D. Callegaro, J. Reimers, and A. Emadi, "A review of bidirectional on-board chargers for electric vehicles," *IEEE Access*, vol. 9, pp. 51501–51518, 2021.

[2] Y. Cao, M. Ngo, N. Yan, D. Dong, R. Burgos, and A. Ismail, "Design and implementation of an 18-kW 500-kHz 98.8% efficiency high-density battery charger with partial power processing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7963–7975, Dec. 2022.

[3] H. Kim, J. Park, S. Kim, R. M. Hakim, H. Belkamel, and S. Choi, "A single-stage electrolytic capacitor-less EV charger with single- and three-phase compatibility," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6780–6791, Jun. 2022.

[4] A. Khaligh and M. D'Antonio, "Global trends in high-power on-board chargers for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3306–3324, Apr. 2019.

[5] Y.-K. Tran, F. D. Freijedo, and D. Dujic, "Open-loop power sharing characteristic of a three-port resonant LLC converter," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 2, pp. 171–179, Jun. 2019.

[6] K. T. Manez, Z. Zhang, and Y. Xiao, "Three-port series-resonant converter DC transformer with integrated magnetics for high efficiency operation," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 5622–5629.

[7] F. Vollmaier, A. Connaughton, T. Langbauer, and K. Krischan, "Exploiting a multi-port transformer for minimal DC-link capacitance for an automotive onboard charger," in *Proc. 22nd Eur. Conf. Power Electron. Appl. (EPE ECCE Eur.)*, Sep. 2020, pp. 1–8.

[8] J. Schäfer, D. Bortis, and J. W. Kolar, "Multi-port multi-cell DC/DC converter topology for electric vehicle's power distribution networks," in *Proc. IEEE 18th Workshop Control Modeling Power Electron. (COMPEL)*, Jul. 2017, pp. 1–9.

[9] F. Vollmaier, A. Connaughton, I. Recepi, T. Langbauer, M. Pajnic, W. Konrad, and C. Mentin, "Tiny power box–exploiting multiport series resonant topologies for very high power density onboard chargers," in *Proc. PCIM Eur., Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2022, pp. 1–9.

[10] R. L. Steigerwald, R. W. De Doncker, and H. Kheraluwala, "A comparison of high-power DC–DC soft-switched converter topologies," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1139–1145, Sep./Oct. 1996.

[11] B. Li, F. C. Lee, Q. Li, and Z. Liu, "Bi-directional on-board charger architecture and control for achieving ultra-high efficiency with wide battery voltage range," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2017, pp. 3688–3694.

[12] J. Deng, S. Li, S. Hu, C. C. Mi, and R. Ma, "Design methodology of LLC resonant converters for electric vehicle battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1581–1592, May 2014.

[13] O. Bay, M. Tran, M. El Baghdadi, S. Chakraborty, and O. Hegazy, "A comprehensive review of GaN-based bi-directional on-board charger topologies and modulation methods," *Energies*, vol. 16, no. 8, p. 3433, Apr. 2023.

[14] B. S. Nathan and V. Ramanarayanan, "Analysis, simulation and design of series resonant converter for high voltage applications," in *Proc. IEEE Int. Conf. Ind. Technol.*, Jan. 2000, pp. 688–693.

[15] H. Krishnaswami and N. Mohan, "Three-port series-resonant DC–DC converter to interface renewable energy sources with bidirectional load and energy storage ports," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2289–2297, Oct. 2009.

[16] C. Zhao and J. W. Kolar, "A novel three-phase three-port UPS employing a single high-frequency isolation transformer," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Jun. 2004, pp. 4135–4141.

[17] T. Langbauer, A. Connaughton, F. Vollmaier, M. Pajnic, and K. Krischan, "Closed-loop control of a three-port series resonant converter," in *Proc. IEEE 22nd Workshop Control Modeling Power Electron. (COMPEL)*, Nov. 2021, pp. 1–7.

[18] B. McDonald and F. Wang, "LLC performance enhancements with frequency and phase shift modulation control," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 2036–2040.

[19] F. Jauch and J. Biela, "Combined phase-shift and frequency modulation of a dual-active-bridge AC–DC converter with PFC," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8387–8397, Dec. 2016.

[20] M. F. Fiaz, S. Calligaro, and R. Petrella, "Analytical modelling and control of dual active bridge converter considering all phase-shifts," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2020, pp. 5984–5991.

[21] T. Langbauer, D. Menzi, V. Marugg, F. Vollmaier, J. Azurza, M. Kasper, and J. W. Kolar, "Third-harmonic-type modulation minimizing the DC-link energy storage requirement of isolated phase-modular three-phase PFC rectifier systems," *IEEE Access*, vol. 11, pp. 34359–34371, 2023.

[22] M. Kumar, P. M. Barbosa, J. M. Ruiz, J. Minli, and S. Hao, "Isolated three-port bidirectional DC–DC converter for electric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2022, pp. 2000–2007.

[23] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-coupled multiport ZVS bidirectional DC–DC converter with wide input range," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 771–781, Mar. 2008.

[24] L. Zhu, H. Bai, A. Brown, and L. Keuck, "A current-fed three-port DC/DC converter for integration of on-board charger and auxiliary power module in electric vehicles," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Jun. 2021, pp. 577–582.

[25] D. Neuner and M. Hartmann, "Analytical model for LLC resonant converters in operation below resonance," *E I Elektrotechnik und Informationstechnik*, vol. 140, no. 1, pp. 34–44, 2023.

[26] S. Tiwari, J. K. Langelid, O.-M. Midtgård, and T. M. Undeland, "Hard and soft switching losses of a SiC MOSFET module under realistic topology and loading conditions," in *Proc. 19th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2017, pp. P.1–P.10.

[27] M. Haider, J. A. Anderson, N. Nain, G. Zulauf, J. W. Kolar, D. Xu, and G. Deboy, "Analytical calculation of the residual ZVS losses of TCM-operated single-phase PFC rectifiers," *IEEE Open J. Power Electron.*, vol. 2, pp. 250–264, 2021.

[28] *IMBG65R022M1H, 650V CoolSiC M1 SiC Trench Power Device*, Infineon Technologies AG, Neubiberg, Germany, 2021. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IMBG65R022M1H-DataSheet-v02_00-EN.pdf?fileId=8ac78c8c7ddc01d7017e49799d240d74

[29] *BSC040N10NS5SC, OptiMOS 5 Power-Transistor, 100V*, Infineon Technologies AG, Neubiberg, Germany, 2022. [Online]. Available: https://www.infineon.com/dgdl/Infineon-BSC040N10NS5SC-DataSheet-v02_01-EN.pdf?fileId=5546d462712ef9b701712f7dd8030083

[30] A. Huang, "Hard commutation of power MOSFET OptiMOS FD 200V/250V," Infineon, Neubiberg, Germany, Appl. Note AN201403, 2014, pp. 1–13.
[31] T. Langbauer, A. Connaughton, F. Vollmaier, and K. Krischan, "Pre-charging of a DC-link capacitor from a high voltage battery," in *Proc. IEEE 21st Workshop Control Modeling Power Electron. (COMPEL)*, Nov. 2020, pp. 1–6.
[32] F. Vollmaier, T. Langbauer, K. Krischan, and R. Petrella, "The impact of DC-bus impedance on the switching performance of low-voltage silicon power MOSFETs," *E I Elektrotechnik Und Informationstechnik*, vol. 140, no. 1, pp. 82–94, Feb. 2023.
[33] A. Connaughton and T. Langbauer, "Fast estimation of best achievable inductor power density in circuit simulation (with DC-bias effects)," in *Proc. IEEE Design Methodolog. Conf. (DMC)*, Jul. 2021, pp. 1–6.

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