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RESEARCH ARTICLE

Design and Analysis of a Single-Stage Simultaneous Charging Converter Using a SiC-Based Quasi-Z-Source Resonant Converter for a Wide Output Voltage Range

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ABSTRACT Simultaneous charging with the individual voltage-fed LLC resonant converters has the drawback of two-stage conversion losses and increased cost, volume, and control complexity. This work presents an isolated Quasi-Z-Source Inverter (QZSI) combined with an LLC resonant converter for a simultaneous charging system in a single-stage conversion at different voltage levels to overcome these issues. The dual tank resonant circuit (DTRC) design structure and required magnetizing inductance are detailed to achieve simultaneous charging. Moreover, the influence of the equivalent magnetizing inductance-to-inductance ratio on power sharing and efficiencies is analyzed. This analysis uses SiC MOSFETs with double-leg shoot-through PWM (DLST PWM) at the constant switching frequency. Simulations and experimental results are evaluated for the proposed converter with a prototype of 200 *W* on each HFT in the upper and lower circuits in the laboratory using the dSPACE1104 platform. This work has analyzed simultaneous charging at equal and unequal voltage levels. It offers a novel, efficient topology with simple control and a smaller size.

INDEX TERMS QZSRC, simultaneous charging system, a dual-tank resonant circuit, double-leg shoot-through PWM.

NOMENCLATURE

EVs	Electric vehicles.
QZSRC	Quasi-Z-Source Resonant Converter.
DLST PWM	Double-leg shoot-through pulse- width modulation.
SLST PWM	Single-leg shoot-through pulse- width modulation.
DTRC	Dual tank resonant circuit.
ZSI	Z source inverter.
QZSI	Quasi-z-source Inverter.
ZCS	Zero Current Switching.
ZVS	Zero Voltage Switching.
OBC	On-board or Off-board charging system.
T_{act}	Active state.
T_{act1}	Active state-1.
T_{act2}	Active state-2.
T_{st}	shoot-through state.
T_s	One switching cycle time.
HFTs	High Frequency Transformers.
QZSN	Quasi z source network.
L_1, L_2	QZSN inductors.
C_1, C_2	QZSN Capacitors.
i_{L1}, i_{L2}	Current through inductors in QZSN.
L_r	Inductance of the resonant inductor.
C_{rp}	Resonant capacitor.
V_H	Voltage of H-bridge.
v_{p1}	Primary voltage of upper HFT.
i_{p1}	Primary current of upper HFT.
v_{s1}	Secondary voltage of upper HFT.
i_{s1}	Secondary current of upper HFT.
v_{p2}	Primary voltage of lower HFT.

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i_{p2}	Primary current of lower HFT.
v_{s2}	Secondary voltage of lower HFT.
i_{s2}	Secondary current of lower HFT.
L_{m1}	Lower magnetizing inductance of HFT.
L_{m2}	Higher magnetizing inductance of HFT.
L_{m_equ1}	Lower equivalent magnetizing inductance of HFT combinations.
L_{m_equ2}	Higher equivalent magnetizing inductance of HFT combinations.
L_{m_equ3}	Moderate equivalent magnetizing inductance of HFT combinations.
L_{lk1}	Leakage inductance of the lower magnetizing inductance of HFT.
L_{lk2}	Leakage inductance of the higher magnetizing inductance of HFT.
L_{rp1}	Sum of lower magnetizing inductance, HFT leakage inductance, and the inductance of the resonant inductor ($L_{lk1}+L_r$).
L_{rp2}	Sum of higher magnetizing inductance, HFT leakage inductance, and the inductance of the resonant inductor ($L_{lk2}+L_r$).
L_{rp_equ1}	Equivalent resonant inductance of the lower magnetizing inductance of HFT combinations (L_{rp1} // L_{rp1}).
L_{rp_equ2}	Equivalent resonant inductance of the higher magnetizing inductance of HFT combinations (L_{rp2} // L_{rp2}).
L_{rp_equ3}	Moderate equivalent resonant inductance of the lower and higher magnetizing inductances of HFT combinations (L_{rp1} // L_{rp2}).
M_1	Equivalent magnetizing inductance-to - equivalent resonant inductance ratio of the lower magnetizing inductance of HFT combinations (L_{mequ1} / L_{rpequ1}).
M_2	Equivalent magnetizing inductance-to - equivalent resonant inductance ratio of the lower magnetizing inductance of HFT combinations (L_{mequ2} / L_{rpequ2}).
M_3	Equivalent magnetizing inductance-to - equivalent resonant inductance ratio of the lower magnetizing inductance of HFT combinations (L_{mequ3} / L_{rpequ3}).
i_{Lrp1}, i_{Lrp2}	Current through inductors in the upper circuit and lower circuit in DTRC.
i_{LM1}	Current through the magnetizing inductor in the lower HFT combinations.
i_{LM2}	Current through the magnetizing inductor in higher HFT combinations.
i_{LM3}	Current through the magnetizing inductor in higher and lower HFT combinations.
S_1, S_2, S_3, S_4	Switches.
$D_1 - D_8$	Diodes.
v_{p1}, v_{p2}	Voltage at primary sides of upper HFT and lower HFT.
v_{s1}, v_{s2}	Voltage at secondary sides of upper HFT and lower HFT.
V_{in}	Input DC voltage.
V_{pn}	DC link voltage.
v_{c1}, v_{c2}	QZS capacitor voltages.
C_{o1}, C_{o2}	Output side capacitors.
V_{out1}, V_{out2}	Output voltages of upper and lower circuits.
i_{out1}, i_{out2}	Output currents of upper and lower circuits.
P_{out1}, P_{out2}	Output powers in upper and lower circuits.
$D_{st} = D_0$	Shoot-through duty cycle.
$D_{stmax} = D_{0max}$	Maximum shoot-through duty cycle.
FHA	First harmonic approximation.
f_{prLLC}	Peak resonant frequency of LLC.
f_{srLLC}	Switching resonant frequency of LLC.
f_{lrLLC}	Lower resonant frequency of LLC.
f_n	Normalized frequency.
f_{max}	Maximum frequency.
Q	Quality factor.
R_{ac}	AC equivalent load.
G_{max}	Maximum voltage gain.
G_{min}	Minimum voltage gain.
V_{in_nom}	Nominal input DC voltage.
V_{in_min}	Minimum input DC voltage.
V_{in_max}	Maximum input DC voltage.
M_{nom}	Nominal voltage gain.

I. INTRODUCTION

Due to fossil fuel depletion and global warming, many countries are giving more attention to electric vehicles (EVs). The development of EV charging infrastructure has given isolated topologies more favour as the number of EVs has increased [1]. Additional charging stations are required to meet the energy needs of the growing number of EVs. It can be achieved with grid support or integrated with multiple sources like renewable energy sources and energy storage systems to charge multiple EVs with individual converters [2], [3], [4], [5], [6]. Using individual power converters for multi-port charging systems has more components, relatively higher cost, and increased control complexity. As an alternative system, a single converter with a multi-port charging system was proposed in [7], [8].

In an isolated DC-DC converter, the HFTs facilitate energy transfer from sources to loads, either in a single port [9] or a multi-port charging system [9]. Among the isolated DC-DC converters, LLC resonant converters are one promising candidate for EV charging systems. They offer good efficiency and high power density, utilize the advantages of soft switching techniques (ZVS and ZCS), and are employed in conventional off-board and on-board charging (OBC) systems [10], [11]. Several studies have concentrated on the single converter with a single tank and dual tank resonant circuit, which uses the

two HFTs to charge a single port charging system [12], [13], [14], [15]. For wide input voltage applications, Hu et al. [12] have proposed the single tank LLC resonant circuit, which achieves the input voltage range by limiting the magnetizing currents in the main HFT by adding a second HFT in series with it.

Furthermore, Du and Bhat [13] proposed a single converter with dual tank LCL-type series resonant converters using two HFTs with low magnetizing inductance. Hua et al. [14] have proposed a half-bridge single tank LLC resonant circuit with two HFTs operated in parallel with equal magnetizing inductance for wide output voltage applications. This idea was used for the full bridge dual tank LLC resonant circuit using the two HF transformers operated in parallel with unequal magnetizing inductance [15]. These converters, however, performed multi-stage power conversion. A single-stage power conversion employing LLC resonant converters was presented in [13], [16], [17], [18], and [19]. These can be integrated with a front-end power factor conversion circuit and become inexpensive. It is observed that the single-stage PFC-integrated topology has higher conduction loss, works at 50% duty cycle, and adjusts switching frequencies to manage the appropriate voltage. However, these topologies cannot use a duty cycle beyond 50%.

In [20], [21], single-stage power conversion topologies were proposed, namely ZSI and QZSI. They are capable of converting both AC to DC and vice versa and have the following advantages: (i) operation in buck-boost mode, (ii) lower failure rate, (iii) no effect of the shoot-through on EMI, (iv) a lower degradation rate, and (v) enhanced reliability. Thus, the advantages of ZSCs have attracted researchers to employ these topologies for power conversions in various applications like PV grids [22], EV drives [23], and EV chargers [24], [25], [26]. For the first time, combinations of ZSI with traditional LLC resonant circuits for DC-DC conversions and enhanced switches capable of withstanding short-circuit and open-circuit conditions were introduced by Cha et al. [27]. Based on the concept of this topology, researchers extended the advantages of the ZSI with LLC for power factor corrections [24] and load regulations with various PWM techniques to the single-port EV charging system [25], [26].

A modified ZSI for the multiport EV charging system from multiport inputs like PV, grid, and battery on the primary side in single-stage operation using two isolated HF transformers for simultaneous charging systems was proposed in [28], [29]. Similarly, isolated multiport converters used with renewable energy and stored energy devices are proposed to charge multiple batteries simultaneously on the secondary side of HFTs [30]. However, the control of power flow in each converter is complex and requires the addition of control circuits for each converter. In [7], a multiport charging system (a tri-port charging system) uses three winding transformers. Which has two secondary windings to charge two batteries simultaneously in the combination of a dual active bridge and bridge rectifier. Recently, a SEPIC-Ćuk combined topology has been proposed for the simultaneous charging of two batteries [31]. It uses a single switch at the primary side of two HFTs. The two batteries have a common node between them, which could cause battery-to-battery power flow. The proposed topology is suitable for low-power EVs, such as electric bikes.

However, prior works did not address the influence of equivalent magnetizing inductance-to-inductance ratio on power sharing and efficiency in parallel-operated HFTs for the simultaneous charging system with a single-stage power conversion by a single converter. In this regard, the objective of the present study is to propose a new topology for the simultaneous charging systems and report the issues on power sharing in the parallel operated HFTs under different magnetizing inductance-to-inductance ratios. This paper is organized as follows: Section II discusses the operation of the proposed QZSRC under steady-state conditions for dual-leg shoot-through PWM. Section III describes the design of a dual-tank resonant circuit. Section IV presents the simulations and hardware results. Conclusions and future scope are drawn in Section V.

II. PROPOSED QZSRC

A. STRUCTURE OF PROPOSED TOPOLOGY

The proposed simultaneous charging converter, shown in Fig. 1, has four impedance elements interfaced between the source and the Full-Bridge Inverter (FBI). This FBI shares the primary side of two isolated high-frequency transformers and two resonant elements (L_{rp1} $C_{rp1} = L_{rp2}$ $C_{rp2} = L_{rp}$ C_{rp}) in upper and lower circuits. Two sets of full bridge diode rectifiers are connected on the secondary side in parallel. The equivalent circuit of the proposed converter is given in Fig. 2. In this topology, two isolated HFTs are operated at the same DC link voltage and switching frequency.

B. OPERATING PRINCIPLE AND STEADY-STATE ANALYSIS

The QZSI has a symmetrical impedance network ($L_1 = L_2$ and $C_1 = C_2$) between the source and H bridge circuits. It can operate in two modes: active states (non-shoot-through states) and shoot-through states. During the non-shoot-through states, the power is transferred from the DC source to the AC side dual resonant circuit through switches of combinations S_1-S_2 and S_3-S_4. No power was transferred from the source to the resonant tank circuits when operating in the shoot-through state due to the DC link voltage going to zero.

1) ACTIVE STATES (T_{act})

In one switching cycle interval (T_s), two active states are achieved by the switching of diagonal switches S_1- S_2 (T_{act1}) and anti-diagonal switches S_3-S_4 (T_{act2}) alternatively. In both these states, a diode is forward-biased. The sum of the resonant currents (i_{Lrp1} + i_{Lrp2}) at the resonant frequency is supplied by the capacitors and inductors. In one switching cycle, ($T_s - 2 \cdot T_{st}/2$) is the active state time. During this

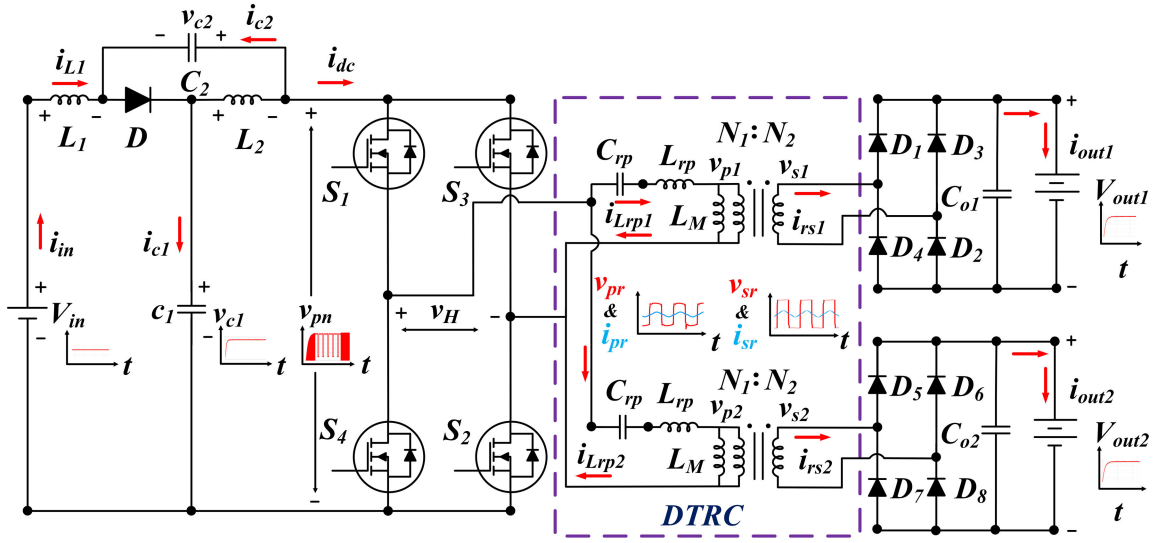


FIGURE 1. Proposed quasi-z-source resonant converter for the simultaneous charging system.

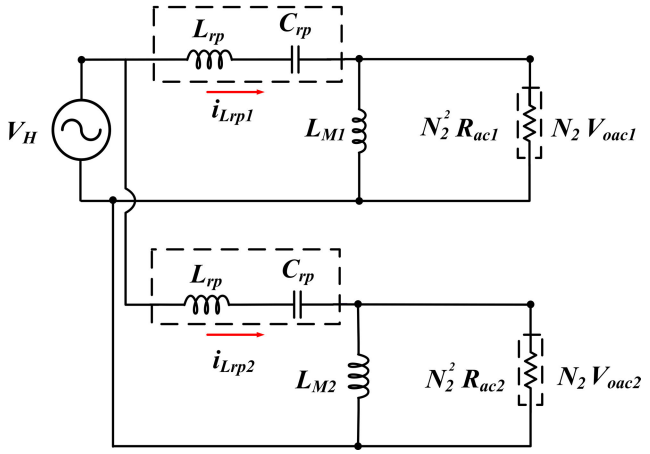


FIGURE 2. Equivalent circuit.

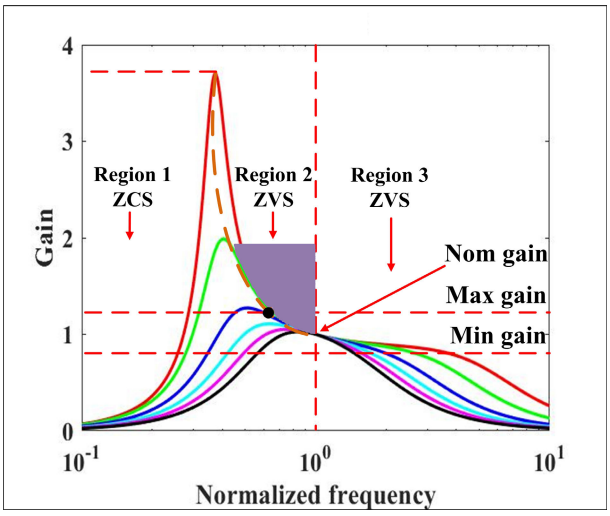


FIGURE 3. Operating regions of LLC.

interval, the voltage across inductors, diode, and H bridge is given by (1).

$$\begin{aligned} v_{L1} &= V_{in} + v_{c1} \\ v_{L2} &= -v_{c2} \\ v_H &= v_{c1} + v_{c2} \\ v_{diode} &= 0 \end{aligned} \tag{1}$$

The current through the diode and capacitors is expressed in terms of the inductor and dc-link currents by (2).

$$\begin{aligned} i_{diode} &= i_{iL1} + i_{L2} - i_{dc} \\ i_{c1} &= i_{iL1} - i_{dc} \\ i_{c2} &= i_{iL2} - i_{dc} \end{aligned} \tag{2}$$

Representing the equations (1) and (2) in matrix form and state-space equations of the impedance network is given by (4)

$$\frac{dx}{dt} = \dot{X} = A_1 X(t) + B_1 U(t) \tag{3}$$

where,

$$X(t) = [i_{L1} \quad i_{L2} \quad v_{C1} \quad v_{C2}]^T, U(t) = [i_{dc} \quad v_{in}]^T$$

$$A_1 = \begin{bmatrix} -\frac{R}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & \frac{R}{L} & 0 & -\frac{1}{L} \\ -\frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{R}{L} & \frac{1}{L} \\ \frac{R}{L} & 0 \\ -\frac{1}{C} & 0 \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & \frac{R}{L} & 0 & -\frac{1}{L} \\ -\frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_{c2} \end{bmatrix}$$

$$+\begin{bmatrix} \frac{R}{L} & \frac{1}{L} \\ \frac{R}{L} & 0 \\ -\frac{1}{C} & 0 \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ V_{in} \end{bmatrix} \tag{4}$$

2) SHOOT-THROUGH STATES (T_{st})

In one switching cycle of interval (T_s), shoot-through states can be achieved in two ways, i.e., by switching two switches in the same leg (SLST PWM) and switching all four switches in both legs (DLST PWM), respectively. In the SLST PWM, the shoot-through current flows only through the switches in any one leg (S_1 and S_4 or S_3 and S_2), and in the other leg, both switches (S_3 and S_2 or S_1 and S_4) are opened. So the stress on the switches is high in the short-circuited leg. In DLST PWM (waveforms shown in Fig. 6), the shoot-through current is divided equally among all switches (S_1, S_2, S_3 and S_4) in both legs and the stress on the switches is reduced compared to the SLST PWM technique. In shoot-through states, the HFTs offer higher impedance, so no current flows on the primary side of the HFTs. Even during the shoot-through time, continuous current flows to the load at the secondary side of the HFTs due to energy stored in the HFTs, and it has been demonstrated in simulation Fig. 5 and experimentally in the Fig. 10b. During this interval, the voltage across inductors, diode, and H bridge is given by (5).

$$\begin{aligned} v_{L1} &= V_{in} + v_{c2} \\ v_{L2} &= v_{c1} \\ v_H &= 0 \\ v_{diode} &= -(v_{c1} + v_{c2}) \end{aligned} \tag{5}$$

The current through the diode is zero due to it being reverse-biased; capacitors and output currents are expressed by (6).

$$\begin{aligned} i_{diode} &= 0 \\ i_{c1} &= -i_{iL2} \\ i_{c2} &= -i_{L1} \\ i_{dc} &= i_{iL1} + i_{iL2} \end{aligned} \tag{6}$$

Representing the equations (5) and (6) in matrix form and at shoot-through state-space equations of the impedance network is given by (4)

$$\frac{dx}{dt} = \dot{X} = A_2 X(t) + B_2 U(t) \tag{7}$$

where,

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{c1}}{dt} \\ \frac{dv_{c2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & \frac{1}{L} \\ 0 & -\frac{R}{L} & \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} & 0 & 0 \\ -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_{c2} \end{bmatrix}$$

$$+\begin{bmatrix} 0 & \frac{1}{L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{dc} \\ V_{in} \end{bmatrix} \tag{8}$$

3) STATE-SPACE AVERAGING

To obtain average state-space for the quasi-z source network by multiplying the active state matrix (A_1) with (D_1 or compliment of $D_1 = (1 - D_0)$) and the shoot-through matrix (A_2) with (D_0).

$$\begin{aligned} \dot{X} &= AX + BU \\ Y &= CX + DU \end{aligned} \tag{9}$$

where, $A = D_1 A_1 + D_0 A_2$

i.e. $A = (1 - D_1)A_1 + D_0 A_2$

$$A = \begin{bmatrix} -\frac{R}{L} & 0 & \frac{D_0 - 1}{L} & \frac{D_0}{L} \\ 0 & -\frac{R}{L} & \frac{D_0}{L} & \frac{D_0 - 1}{L} \\ \frac{1 - D_0}{C} & -\frac{D_0}{C} & 0 & 0 \\ -\frac{D_0}{C} & \frac{1 - D_0}{C} & 0 & 0 \end{bmatrix}$$

$$B = (1 - D_1)B_1 + D_0 B_2$$

$$B = \begin{bmatrix} \frac{(1 - D_0)R}{L} & 1 \\ \frac{(1 - D_0)R}{L} & 0 \\ \frac{(D_0 - 1)}{C} & 0 \\ \frac{(D_0 - 1)}{C} & 0 \end{bmatrix}, C = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}, D = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

In order to get to equation (10), from steady state equation (9) the voltage across the capacitors and the current via the inductors are therefore inferred [21].

$$\begin{aligned} v_{c1} &= \frac{1 - D}{1 - 2D} \cdot v_{in} \\ v_{c2} &= \frac{D}{1 - 2D} \cdot v_{in} \end{aligned} \tag{10}$$

Current through the inductors is given by (11), and the peak voltage across DC-Link is given by (12).

$$i_{L1} = i_{L2} = \frac{1 - D}{1 - 2D} \cdot i_{dc} \tag{11}$$

$$v_{pn} = \frac{1}{1 - 2D_{\text{stmax}}} \cdot v_{in} \tag{12}$$

The waveforms represent the current entering the H-bridge as i_{dc} (or i_{pn}).

Modes of operation of the proposed QZSRC with the DLST PWM are shown in Fig. 4. Fig. 4a and 4b show the active states, and Fig. 4c shows the shoot-through state.

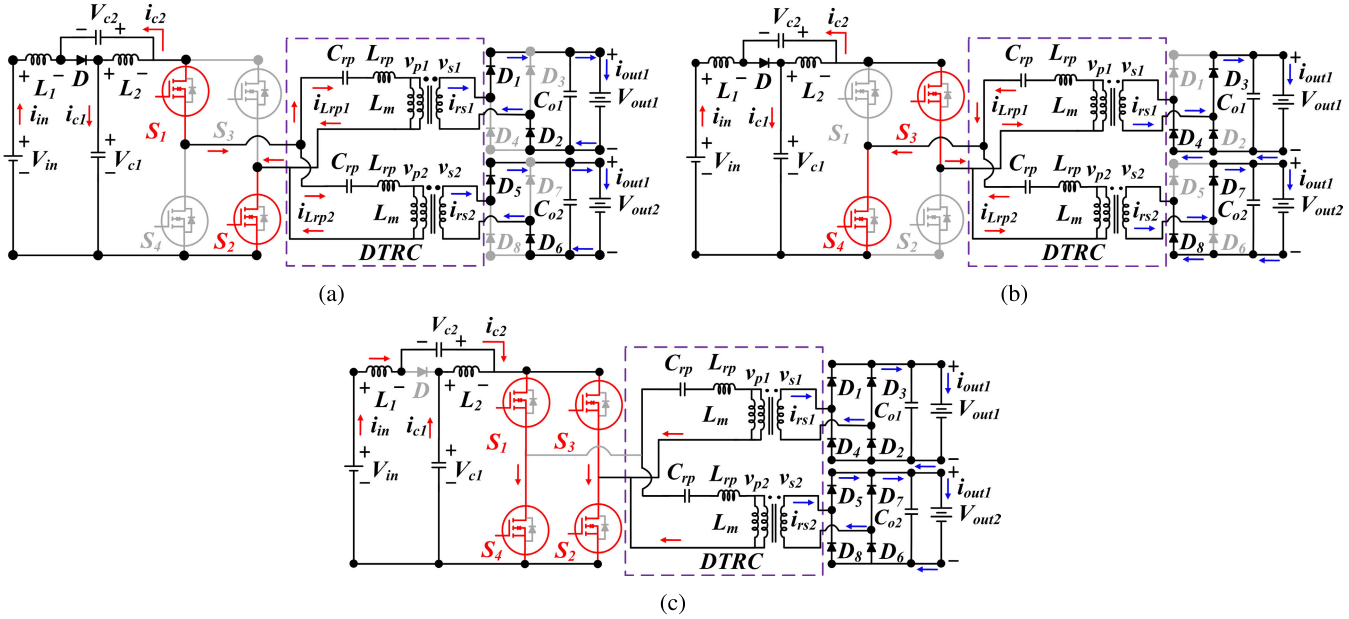


FIGURE 4. Modes of operational (a) Active state - 1 (S_1 - S_2), (b) Active state - 2 (S_3 - S_4), and (3) Shoot-through state (S_1 - S_4, S_3 - S_2).

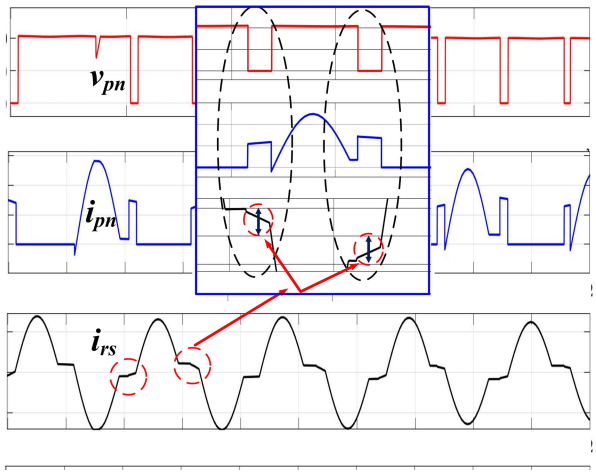


FIGURE 5. Simulation results of current flows at the load side during the shoot-through.

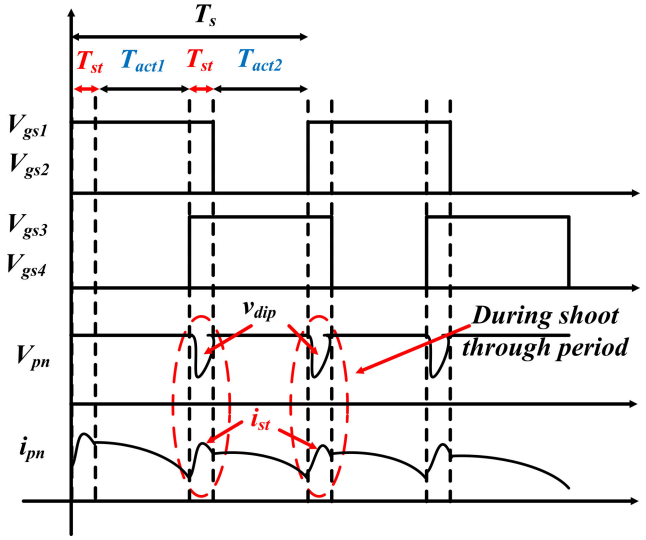


FIGURE 6. Double-leg shoot-through PWM.

III. DESIGN OF DUAL TANK RESONANT CIRCUITS

The detailed design procedure of a resonant network for simultaneous charging is explained in this section. The following are the assumptions made for a selection of HF transformers; i

1) Both HFTs are made of the same type of core materials.
2) Both HFTs operated at the resonant frequency.
3) Both HFTs have the same primary turns.

A. FHA

The proposed simultaneous charging using QZSRC is shown in Figure 1. For analysis, using the FHA technique, its ac equivalent circuit has been shown in Fig.2, [32], [33]. The LLC circuit has two resonant frequencies: the peak resonant frequency is at f_{prLLC}, and it is determined by L_{rp} and C_{rp} as given by (13); the lower frequency is determined at f_{lrLLC} due to the addition of the magnetizing inductance L_m with L_{rp} and C_{rp}, as given by (14).

$$f_{prLLC} = \frac{1}{2\pi\sqrt{L_{rp} \cdot C_{rp}}} \tag{13}$$

$$f_{lrLLC} = \frac{1}{2\pi\sqrt{(L_{rp} + L_m) \cdot C_{rp}}} \tag{14}$$

Fig. 3 shows that the LLC can operate in three regions. Region 1 is a resonant tank working in the capacitive

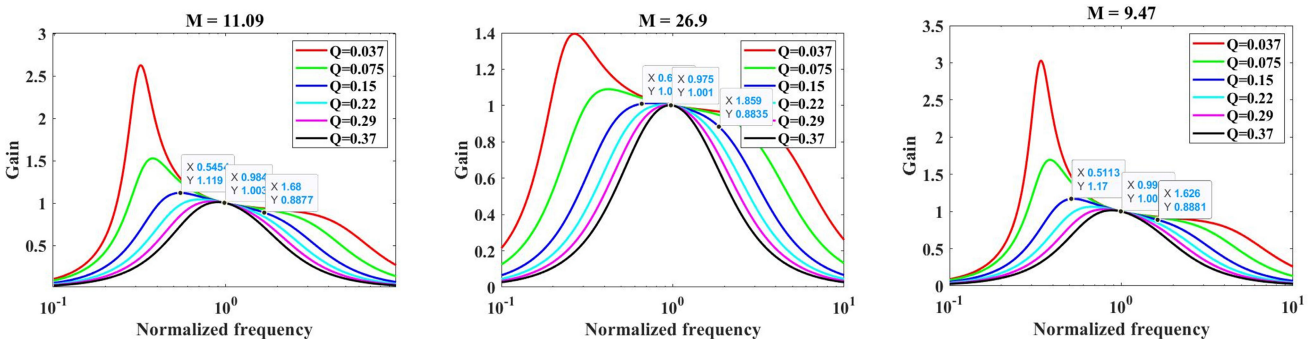


FIGURE 7. Voltage gain vs switching frequency variation under combinations of the of (a) M_1 (b) M_2 and (c) M_3.

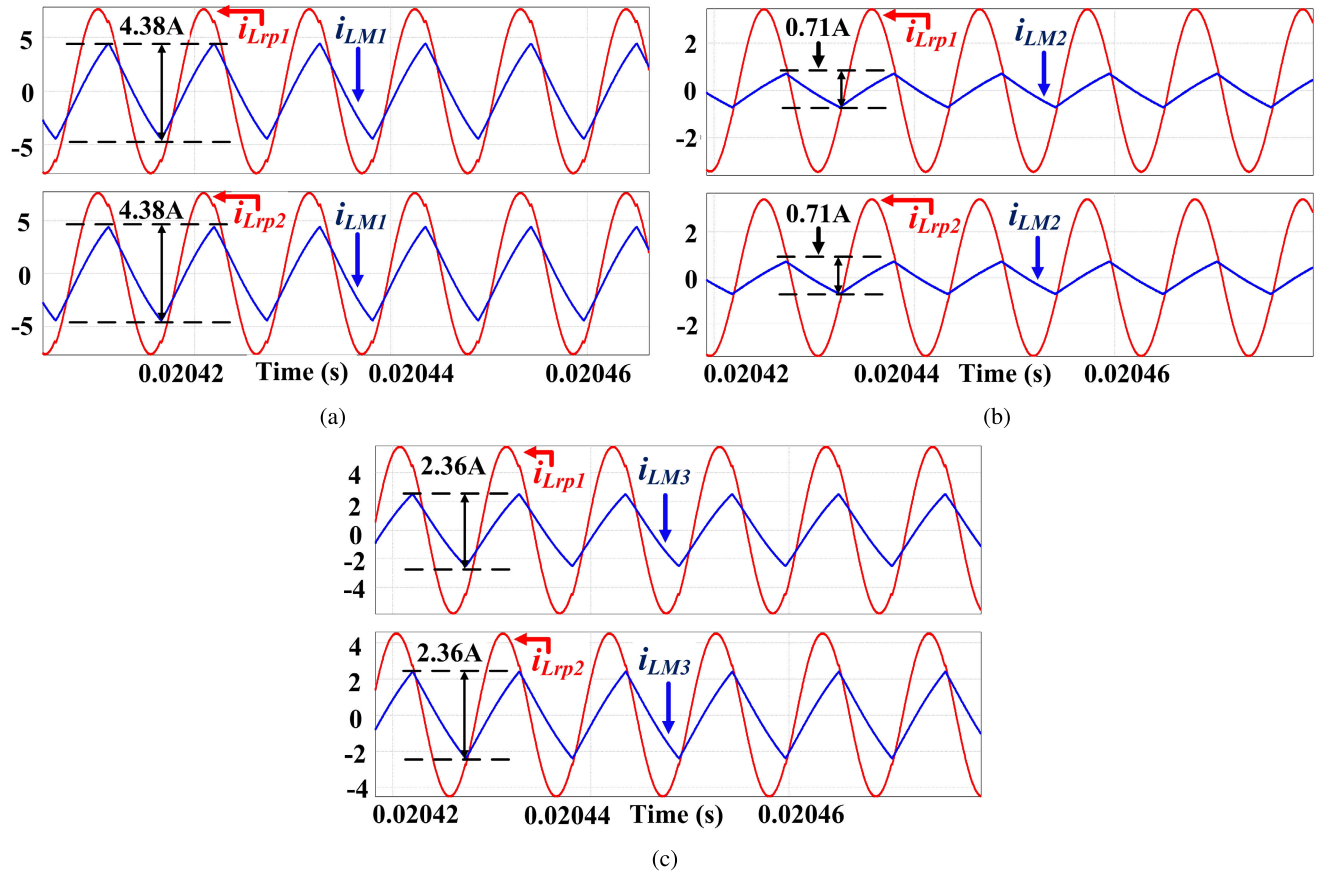


FIGURE 8. Simulation results showing the inductor and magnetizing current of the combinations of (a) M_1 (b) M_2 and (c) M_3.

impedance: this region will not be preferred due to device failure and high reverse recovery loss; regions 2 and 3 operate in the inductive impedance. In region 2, ZVS at the primary side switches and ZCS at the secondary side can be easily achieved with maximum voltage gain between the switching frequencies of $f_{lrLLC} < f_{srLLC} < f_{prLLC}$. In region-3, it loses the ZCS at rectifier diodes but still holds the ZVS at primary side switches above resonant frequency $f_{srLLC} > f_{prLLC}$.

In Regions 1 and 2, the effects of L_m will be there on the resonant elements (L_{rp} and C_{rp}) but will not be there on the resonant elements in Region 3. Higher efficiencies can be achieved by operating in Region 2 when compared to Regions 1 and 3. Thus, keeping the switching frequency near the resonant frequency makes for negligible impedance in the resonant tank and helps reduce the circulating current. Also, switching at a higher frequency can reduce the size of the energy storage elements [14], [33].

TABLE 1. Set of parallel combinations HFT.

EMIIRC*	Parallel HFT combinations	Value
M_1	Lower (L_{m1}) - HFT	L_{m1} = 165 μH || L_{m1} = 165 μH
M_2	Higher (L_{m2}) - HFT	L_{m2} = 776 μH || L_{m2} = 776 μH
M_3	Moderate (L_{m2} and L_{m1}) - HFT	L_{m2} = 776 μH || L_{m1} = 165 μH

*EMIIRC = Equivalent magnetizing inductance-to-inductance ratio combinations

Therefore, SiC MOSFETs and LLC resonant converters operate in the inductive region near the resonant frequency in this analysis. Its voltage gain G and quality factor Q are obtained from (17, 18) and (15).

$$G(Q, M, f_r) = \frac{V_{in}}{V_{out}} = \frac{f_n \cdot (m-1)}{\sqrt{a^2 + b^2 \cdot (m-1)^2 \cdot Q^2}} \quad (15)$$

where,

$$a = (M \cdot f_n^2 - 1)^2, \qquad b = f_n^2 \cdot (f_n^2 - 1)^2$$
$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}}, \qquad R_{ac} = \frac{8 \cdot N_p^2 \cdot V_{out}^2}{\pi^2 \cdot N_s^2 \cdot P_{out}}$$
$$M = \frac{L_m + L_r}{L_r}, \qquad f_n = \frac{f_s}{f_r}$$

The same HFT ratio is used in both the simulation and hardware implementation of the proposed converter. In the proposed converter, two step-up HFTs are connected in parallel to charge two batteries simultaneously. Both HFTS have different magnetizing inductance (L_{m1} and L_{m2}). The DTRC has the same resonant (LC) parameters in upper and lower circuits. The design procedure for the DTRC elements and the magnetizing inductance for both HFTs is explained in sections III-C3 and III-C4. Table 1 shows the combinations of HFTs considered for the analysis in both simulations and experimental work. First, the proposed topology has been tested with equal equivalent magnetizing inductance-to-inductance ratios of the parallel-operated M_1, and next, M_2 combinations, and, finally, with unequal equivalent magnetizing inductance-to-inductance ratios of the parallel-operated HFT M_3 combinations. The maximum voltage gains of both transformers are G_{max}, G_{min}, and the quality factor Q are 1.17, 0.88, and 0.15, respectively, for all combinations in the analysis. The voltage gain curves vs frequency for different Qs are shown in Fig. 7 for M_1, M_2, and M_3.

B. EFFECT OF MAGNETIZING INDUCTANCE IN PARALLEL OPERATION OF HFTs

In step-up applications, higher current flows onto the primary side of the LLC resonant converter compared to the secondary side. This primary current comprises the referred load current and magnetizing current, which supply the conduction loss and core losses. These conduction losses and the magnetizing currents can be minimized by operating in ZVS and ZCS conditions and with suitable resonant parameters, respectively.

The simulated results of the resonant inductor currents i_{Lrp1} and i_{Lrp2} in the upper and lower circuits for all combinations are shown in Figures 8a, 8b and 8c. The magnetizing currents are, i_{LM1}, i_{LM2}, and i_{LM3} of the M_1, M_2, and M_3 of the HFT combinations, respectively. In the M_1 combinations, the effect of the lower equivalent magnetizing inductance results in high core losses in both HFTs due to more circulating current. In the M_2 combinations, higher equivalent magnetizing inductance significantly reduces core losses in both HFTs due to less circulating current. However, in the M_3 combinations, the effect of equivalent magnetizing inductance results causes moderate core loss. Fig. 7 shows the voltage gain vs frequency for various load conditions for combinations M_1, M_2, and M_3. All these combinations of analysis and voltage gain are considered to be between 0.88 and 1.17.

C. DESIGN OF DUAL TANK

1) INITIAL DESIGN PARAMETERS FOR SIMULTANEOUS CHARGING SYSTEM

For a simultaneous charging system, the input voltage ranges, output voltage ranges, and maximum output power value have to be initially defined. In this work, the input voltage ranges from 85 to 115 V, with a nominal value of 100 V for the DC link voltage. The output voltage range is between 85 and 115 V, with a nominal output voltage of 100 V for the first charging system, and from 250 V to 350 V, with a nominal value of 300 V for the second charging system. The maximum power on each transformer is 250 W.

2) TRANSFORMER TURNS RATIO CALCULATIONS

After finalizing the input and output voltage specifications, both transformers' turn ratios are calculated using (16). Both transformers have the same minimum and maximum voltage gain, which can be calculated using (17) and (18), respectively. The nominal voltage gain (M_{nom}) is considered 1 for both transformers [34].

$$\frac{N_p}{N_s} = \frac{V_{in\_nom} \cdot M_{nom}}{V_{out}} \quad (16)$$

$$G_{min} = \frac{V_{in\_nom} \cdot M_{nom}}{V_{in\_max}} \quad (17)$$

$$G_{max} = \frac{V_{in\_nom} \cdot M_{nom}}{V_{in\_min}} \quad (18)$$

3) DUAL TANK RESONANT ELEMENTS CALCULATIONS

The equivalent resistances (R_{ac1} and R_{ac2}) for both transformers, as primary sides, and the resonant elements on the same quality factor have been calculated. Fig. 7 shows the voltage gain vs. f_n graph. After many iterations, Q was finalized at 0.15, and with this value of Q, DTRC parameters (LC) are calculated by using (13) and (15) to the 38 AWG of Litz wire at the switching frequency of 100 kHz. In this work, resonant

parameters for the upper and lower resonant circuits of a dual resonant tank construction operating at a constant frequency were designed.

The equivalent resistances (R_{ac1} and R_{ac2}) are expressed by equations (III-A)

$$\begin{aligned} R_{ac1} &= \left(\frac{8 \cdot N_p^2 \cdot V_{out}^2}{\pi^2 \cdot N_s^2 \cdot P_{out}}\right) \\ &= \left(\frac{8 \cdot 1^2 \cdot 100^2}{\pi^2 \cdot 250}\right) \\ &= 32.4\Omega \end{aligned} \tag{19}$$

$$\begin{aligned} R_{ac2} &= \left(\frac{8 \cdot N_p^2 \cdot V_{out}^2}{\pi^2 \cdot N_s^2 \cdot P_{out}}\right) \\ &= \left(\frac{8 \cdot 0.111^2 \cdot 300^2}{\pi^2 \cdot 250}\right) \\ &= 32.4\Omega \end{aligned} \tag{20}$$

Therefore, resonant capacitors are expressed by (21) and resonant inductors are expressed by (22).

$$\begin{aligned} C_{rp} = C_{r1} = C_{r2} &= \frac{1}{Q \cdot f_{sw} \cdot \sqrt{2\pi}} \\ &= \frac{1}{0.15 \cdot 100,000 \cdot \sqrt{2\pi}} \\ &= 0.15\mu F \end{aligned} \tag{21}$$

and

$$\begin{aligned} L_{rp} = L_{r1} = L_{r2} &= (Q \cdot R_{ac})^2 \cdot C_{rp} \\ &= (0.15 \cdot 32.4)^2 \cdot 0.15\mu F \\ &= 7.79\mu H \end{aligned} \tag{22}$$

4) DESIGN OF MAGNETIZING INDUCTANCE (L_m)

There is a trade-off for the design of magnetizing inductance (L_m) between the reduction of switching or conduction losses. In order to reduce conduction losses, it is necessary to design a higher value of L_m. In contrast, L_m needs to be small enough to guarantee a narrow switching frequency region, which equates to a modest input impedance and circulating current. Based on the above trade-off, the design of L_{m1} and L_{m2} should satisfy equation (23) in the selections of the HFTs to operate in parallel for simultaneous charging systems. Based on the above design specifications, the required maximum magnetizing inductance of L_{m1} and L_{m2} for both HFT is calculated from the (23) to obtain 265 μH and 804.82 μH, respectively [14], [33].

$$L_m \leq \frac{t_{dead} \cdot n \cdot V_{0\_max}}{8 \cdot C_{oss} \cdot V_{in\_min} \cdot f_{max}} \tag{23}$$

where, C_{oss} is the output of the capacitance of SiC-MOSFET, t_{dead} is the dead time, n is the voltage gain, and f_{max} is the maximum switching frequency. The C_{oss} including parasitic capacitance of HFTs, is $220pF$, and the dead time is $100nS$.

$$\begin{aligned} L_{m1} &\leq \frac{100 \cdot 10^{-9} \cdot 0.86 \cdot 115}{8 \cdot 220 \cdot 10^{-12} \cdot 85 \cdot 250000} \\ &= 265\mu H \end{aligned} \tag{24}$$

and

$$\begin{aligned} L_{m2} &\leq \frac{100 \cdot 10^{-}9 \cdot 0.86 \cdot 350}{8 \cdot 220 \cdot 10^{-12} \cdot 85 \cdot 250000} \\ &= 804.82\mu H \end{aligned} \tag{25}$$

$$\begin{aligned} L_{m\_equ1} &\leq \frac{L_{m1} \cdot L_{m1}}{L_{m1} + L_{m1}}; \\ L_{m\_equ2} &\leq \frac{L_{m2} \cdot L_{m2}}{L_{m2} + L_{m2}}; \\ L_{m\_equ3} &\leq \frac{L_{m1} \cdot L_{m2}}{L_{m1} + L_{m2}}; \end{aligned} \tag{26}$$

D. DESIGN AND SELECTION OF COMPONENTS

The proposed converter's components should be with-stand in order to make the most of its performance under DLST shoot-through PWM. The selection of components is detailed in this section.

1) INDUCTOR DESIGN

The average current through the inductors are calculated by (27).

$$I_{\text{avg}} = \frac{P_{\text{out}}}{V_{\text{in}}} = \frac{500}{90} = 5.55\,A \tag{27}$$

The inductors required in the quasi-z source network to meet the necessity condition of continuous conduction mode (CCM) and peak to peak ripple is considered as 15 % [35]. The experimental analysis has considered the above theoretical value.

$$\begin{aligned} L_1 = L_2 &\leq \frac{R_L \cdot 0.0858}{f_{sw}} \leq \frac{450 \cdot 0.0858}{93562} \\ &= 412\mu H \end{aligned} \tag{28}$$

2) CAPACITOR DESIGN

In the design of the capacitor, 5% voltage ripple is considered for both QZSN capacitors and output-side capacitors. The required capacitance is calculated by (29). Therefore, a $50\mu F$ capacitor is considered in the experiment.

$$\begin{aligned} C_1 = C_2 &= \frac{i_{\text{L}} \cdot D_{st}}{2 \cdot \Delta v_{\text{c1}} \cdot f_{\text{s}}} \\ &= \frac{6.38 \cdot 0.06}{2 \cdot 0.05 \cdot 93562} \\ &= 40.92\mu F \end{aligned} \tag{29}$$

3) SELECTION OF DIODE AND SWITCHES

The peak current through the diode is 12.78 A because, at conventional zero states, the diode's peak current is twice as high as the inductor's peak current. Therefore, SiC-Diode IDH20G120C5 (20 A) is selected. While selecting switches a maximum DC link voltage of 700 V can get from a minimum input voltage of 85 V is considered for maximum shoot-through duty of 0.44. Therefore, SiC-MOSFET AIMW120R045M1(1200 V) is selected.

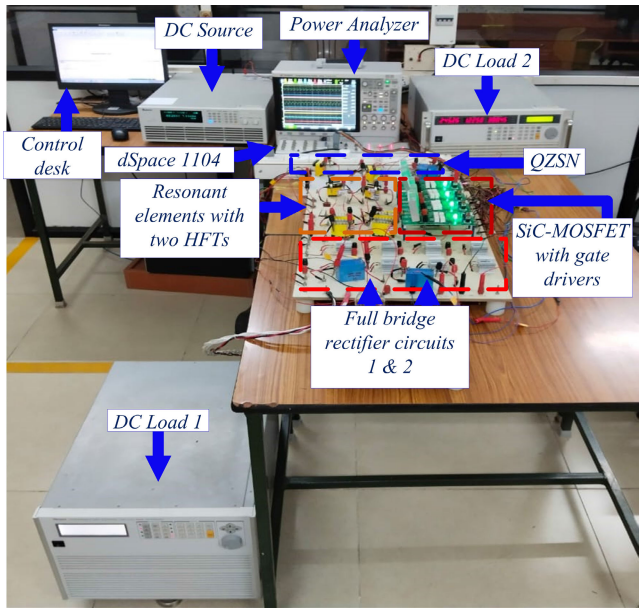


FIGURE 9. Experimental work setup.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation was performed in the MATLAB and SIMULINK environment, and the gate pulse logic for the switches in hardware was implemented using the dSPACE1104 platform. The experimental setup is shown in Fig. 9, which has Chroma programmable DC power supply 62050H600S (600 V and 8 A) used as a DC source, and results have been taken using the Keysight IntegraVision PA2203A Power Analyzer. This power analyzer can measure four voltages, currents, and powers simultaneously. A prototype of 200W on each HFT in both upper and lower circuits was tested with the designed output voltage ranges mentioned in subsection III-C1 for simultaneous charging systems.

Tables 2 and 3 show the hardware specifications and components, respectively. All experimental verification was done at a constant frequency of $f_{sw} = f_{sr} = 93.52\ kHz$ and a constant duty cycle. Three cases were considered during hardware validation:

(a) influence of lower equivalent magnetizing inductance - to - inductance ratio (M_1)
(b) influence of higher equivalent magnetizing inductance - to - inductance ratio (M_2)
(c) influence of moderate equivalent magnetizing inductance - to - inductance (M_3)

Figures 10 to 12 show the experimental waveforms of the proposed system. In the top section of the waveform, the input voltage (V_{in}), DC link voltage (V_{pn}), and output voltages (V_{out1}, V_{out2}) are shown. The middle section shows the input current (i_{in}), DC link current (i_{pn}), and output currents (i_{out1}, i_{out2}). The bottom section shows the upper and lower circuits' input power (P_{in}) and output powers of simultaneous charging systems (P_{out1}, P_{out2}) for the above three cases.

TABLE 2. Parameters and Values.

Parameters	Symbol	Value
Input voltage	V_{in}	$80 - 100V$
DC link voltage	V_{pn}	$100V$
Output voltages	V_{out}	$100V$ and $300V$
Transformers Turns ratio	$N_1 : N_2$	$1:1$ and $1:3$
Magnetizing inductances of HFT	L_{m1} and L_{m2}	165μH and 776μH
Leakage inductances of HFT	L_{lk1} and L_{lk2}	2.5μH and 8μH
Inductance of resonant inductors	$L_{rp1} = L_{rp2}$	7.5μH
Resonant capacitors	$C_{rp1} = C_{rp2}$	0.15μF
Resonant frequency	f_{srLLC}	$93.52kHz$
Maximum switching frequency	f_{max}	$250kHz$

TABLE 3. Components list for the hardware prototype.

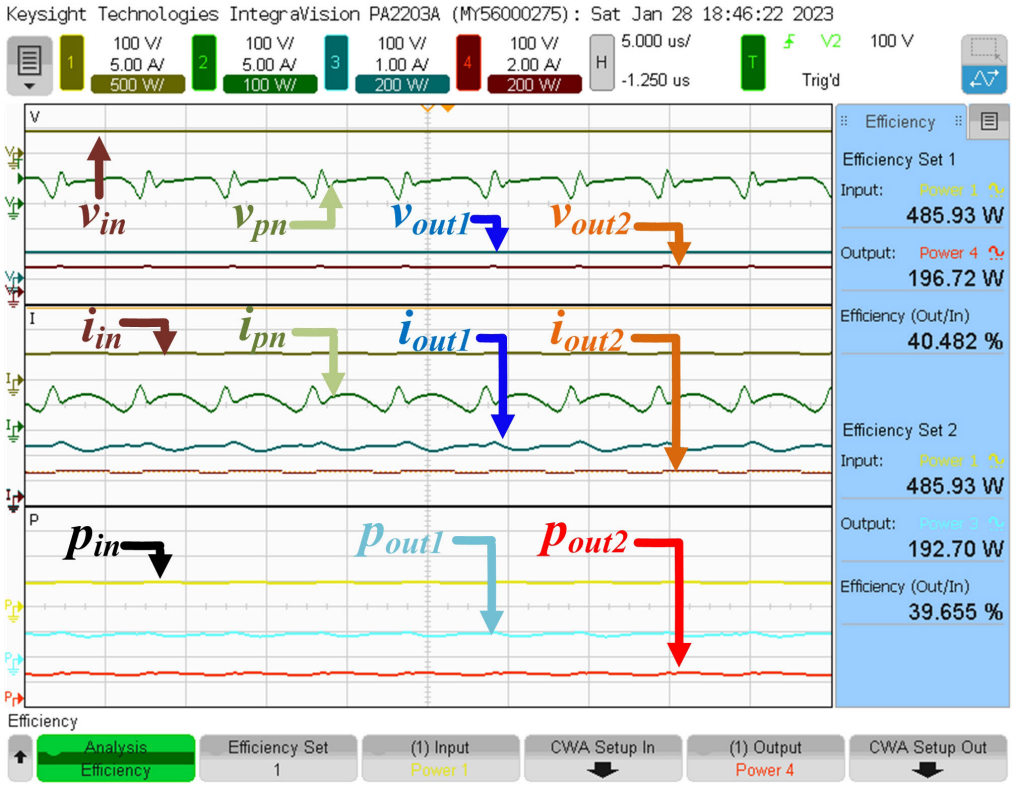
Component	Rating	Part No.
QZSI inductors	500μH, $10A$	ETD44
QZSI capacitors	50μF, $800V$	MKP
Resonant inductors	7.5μH, $800V$	ETD44
Resonant capacitors	4×0.068nF, $450V$	MPP
Full bridge SiC - MOSFETs	$1200V, 52A$	AIMW120R045M1
Full bridge SiC - Diodes	$1200V, 20A$	IDH20G120C5
Output capacitors	50μF, $800V$	MKP
Transformer core Type	500 W and 500 W	ETD44

TABLE 4. Data sheet parameters for loss calculations.

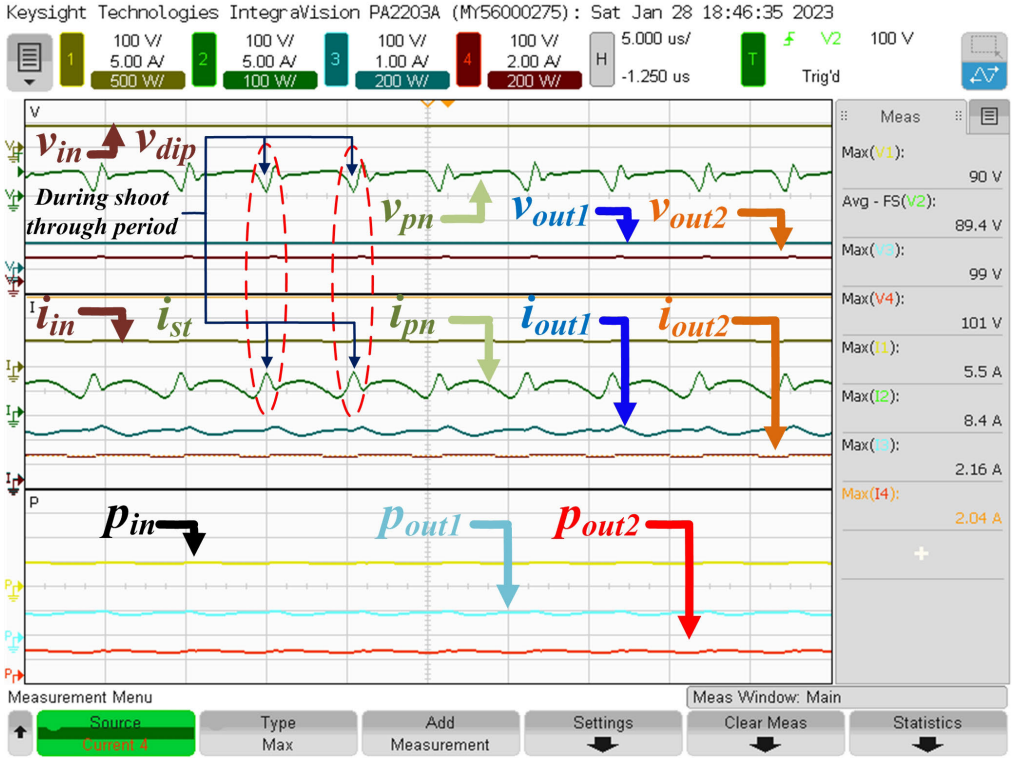
Name	Symbol	Value
MOSFET Gate source capacitance	C_{gs}	$2.12 \cdot 10^{-9} F$
MOSFET Gate source voltage	V_{gs}	$7.8V$
Rise time and Fall time	t_r and t_f	$32nS$ and $13nS$
MOSFET on-state resistance	R_{ds}	$45m\Omega$
Diode on-state resistance	R_d	$20m\Omega$
Diode forward voltage drop	V_F	$1.4V$
Core loss coefficients	K_h, n	$5.597 \cdot 10^{-4}$, 2.85
	m	1.43
Mass of core	M_{core}	$1Kg$
Flux density of core	B_h	$15Wb$
Transformers (1:1)	R_{ac_prim}	0.5Ω
	R_{ac_sec}	0.5Ω
Transformers (1:3)	R_{ac_prim}	0.25Ω
	R_{ac_sec}	0.6Ω
ESR of MKP Capacitor	R_{ESR}	$3.5m\Omega$
Resonant Inductor resistance	R_{ind}	0.35Ω
QZSN Inductor resistance	R_{qzsn}	0.5Ω
Wiring resistance	R_{wire}	1.35Ω

A. EXPERIMENTAL RESULTS OF THE RATIO M_1

Figures 10a and 10b show the experimental waveforms of the power-sharing with efficiencies, voltages, and currents in the upper and lower circuits of the M_1 case. In these combinations, the input power $P_{in} = 485W$ s was observed to be equally shared between the two loads. The output powers of $P_{out1} = P_{out2} \simeq 200W$, output currents of $i_{out1} = i_{out2} = 2.16\ A$, and nominal voltages of $V_{out1} = V_{out2} = V_{nom} = 100\ V$ are maintained on both upper and lower circuit circuits. The efficiency of the upper circuit is equal to that of the lower circuit, and the overall efficiency of the simultaneous charging system is around 80%. Fig. 10b shows a voltage dip that occurs two times in one cycle due to DLST PWM, which causes an increase in current through the switches.

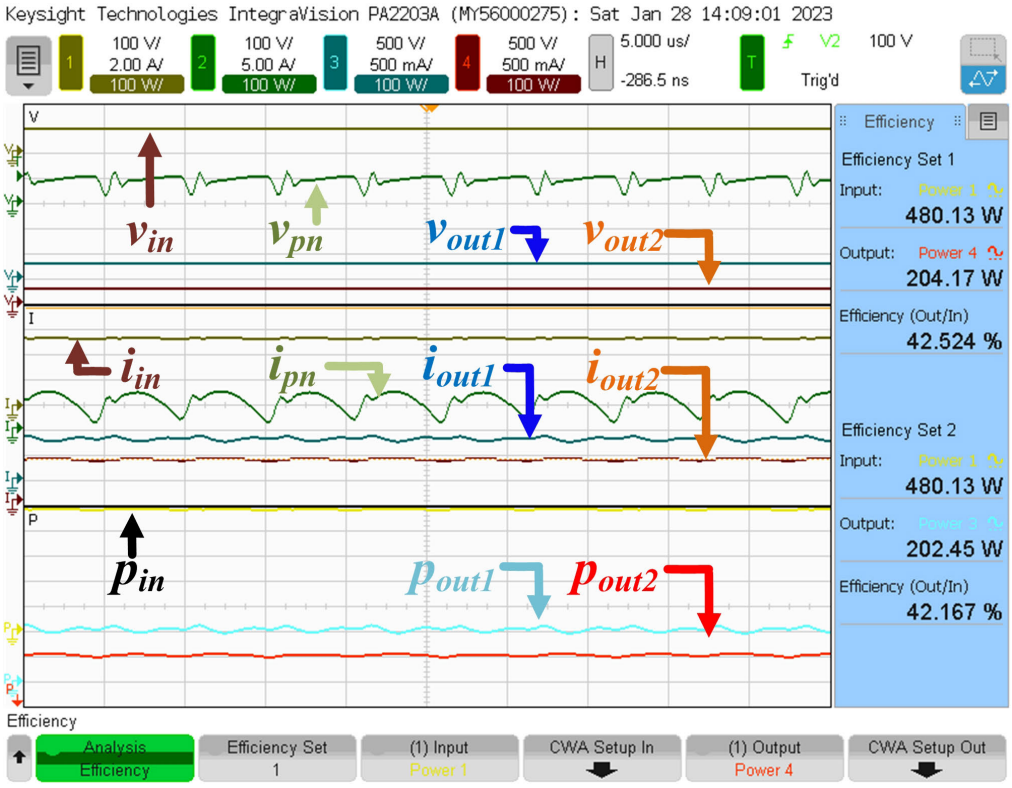


(a)

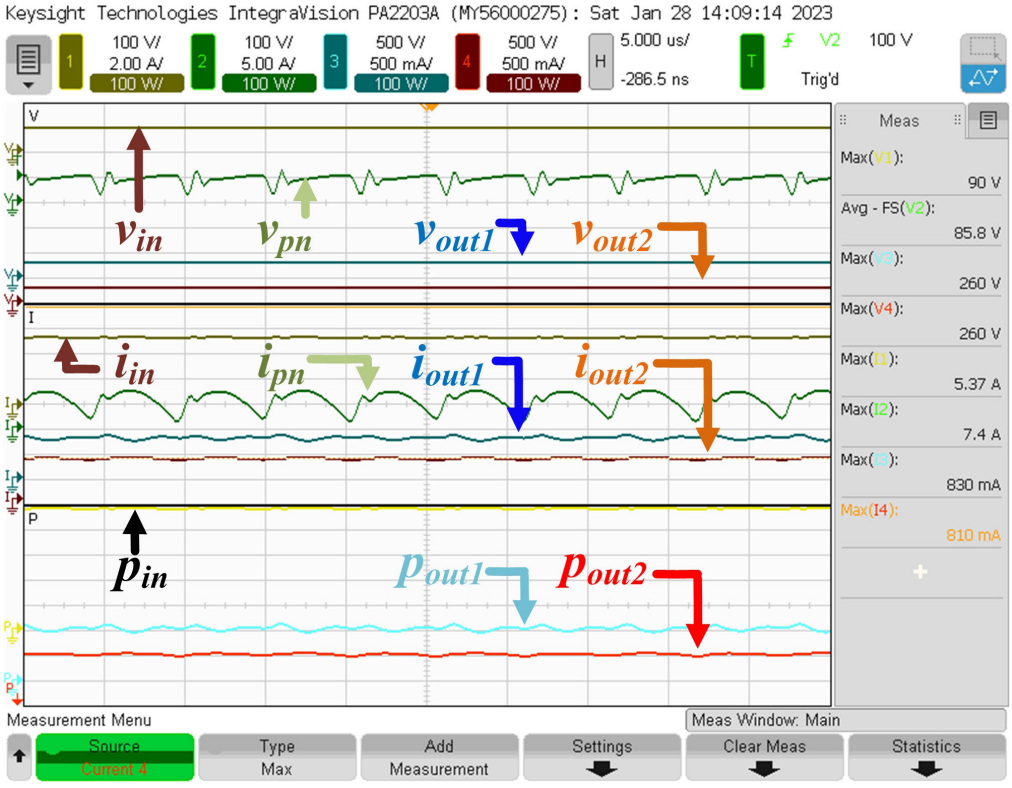


(b)

FIGURE 10. Experimental waveforms of the M_1 combination of the HFTs simultaneously charging at full load condition of 200 W on each HFTS (a) power sharing and efficiencies and (b) voltages and currents waveforms.

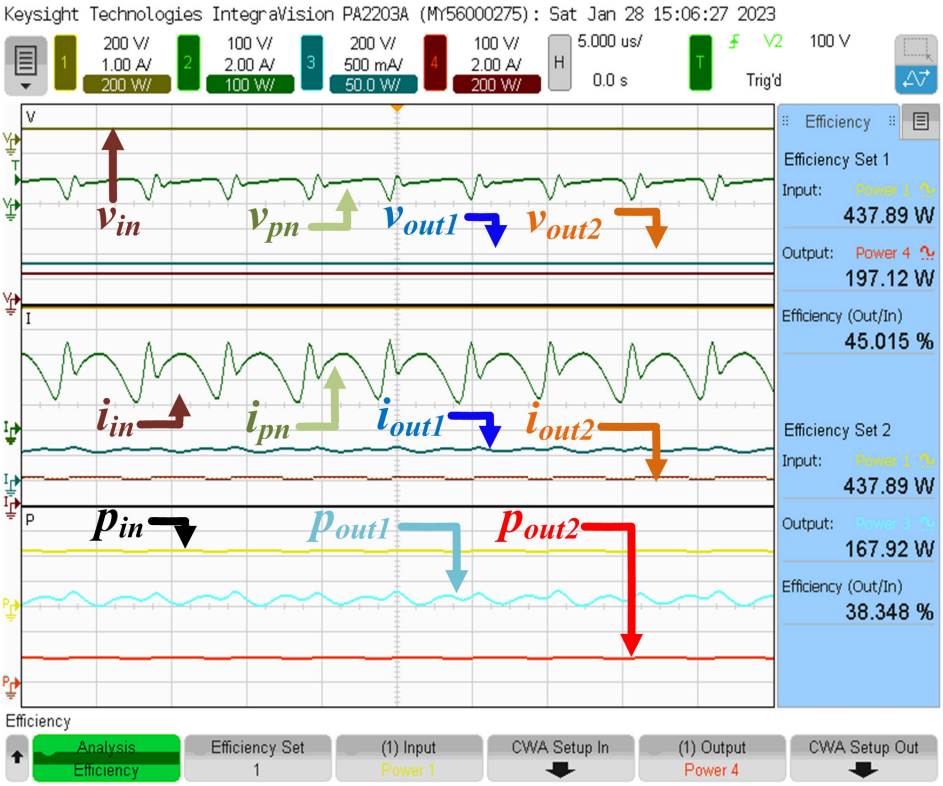


(a)

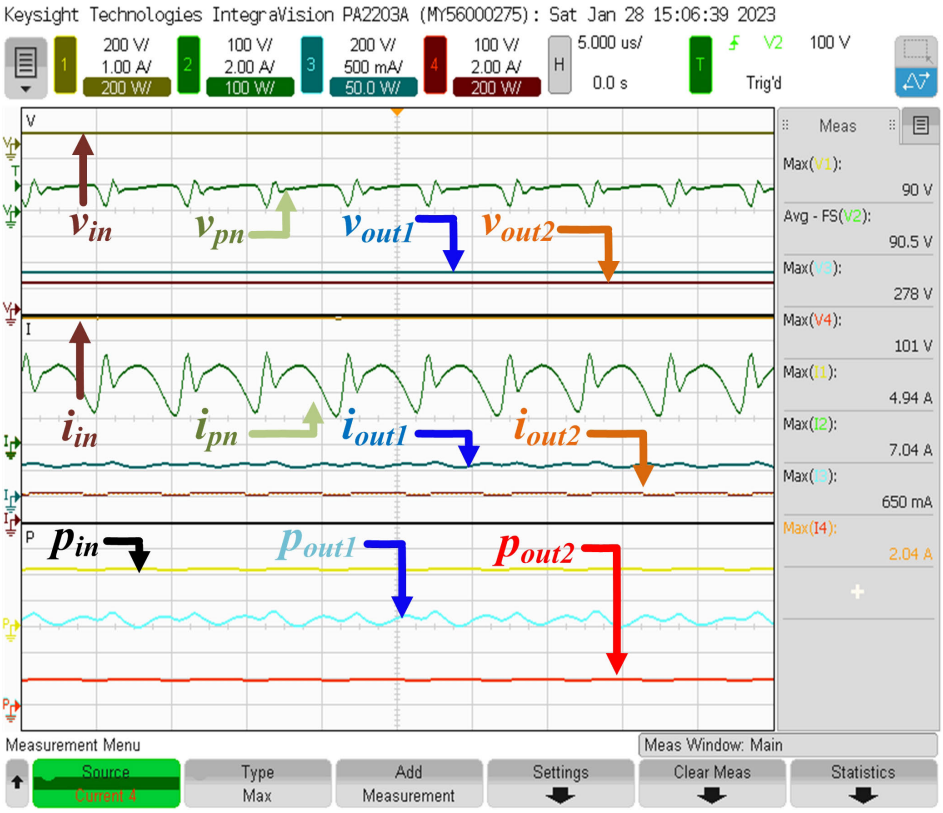


(b)

FIGURE 11. Experimental waveforms of the M_2 combination of the HFTs simultaneously charging at full load condition of 200 W on each HFTS (a) power sharing and efficiencies and (b) voltages and currents waveforms.

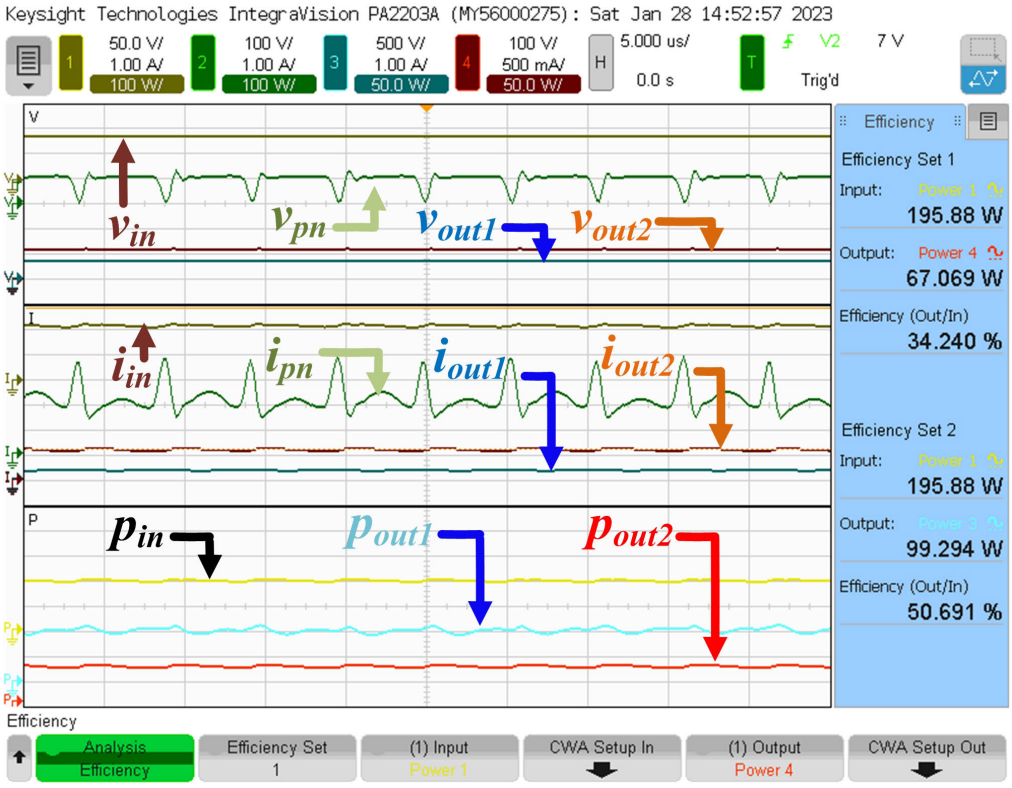


(a)

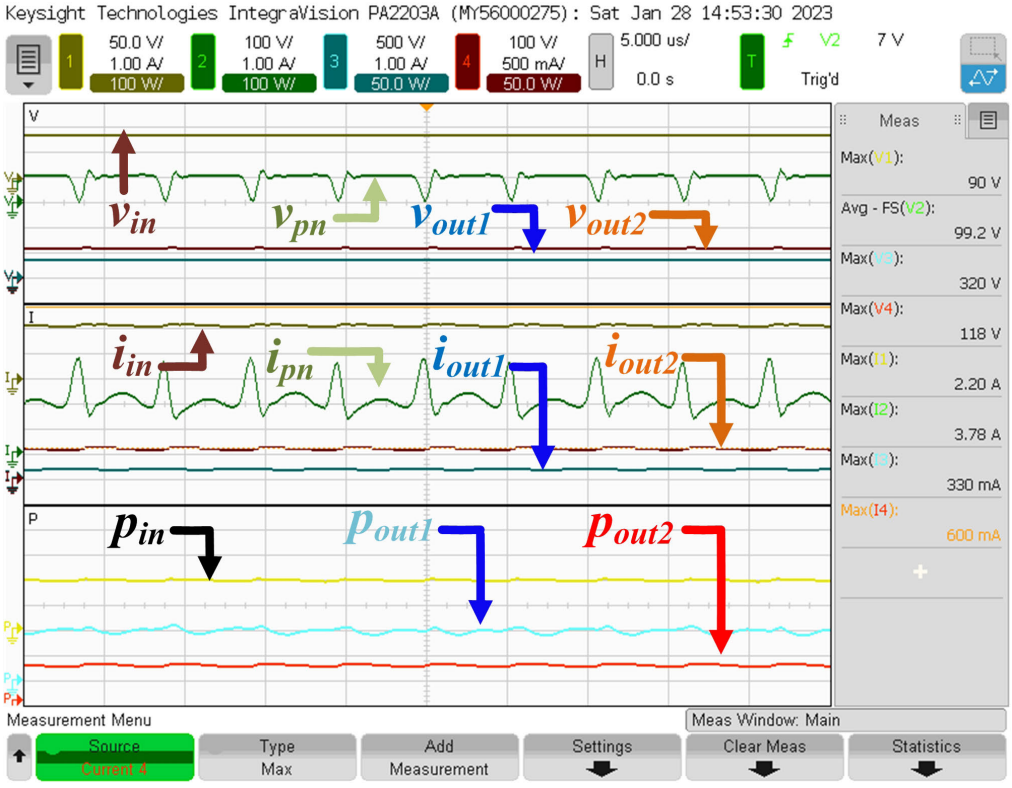


(b)

FIGURE 12. Experimental waveforms of the M_3 combination of the HFTs simultaneously charging at full load condition of 200 W on each HFTS (a) power sharing and efficiencies and (b) voltages and currents waveforms.

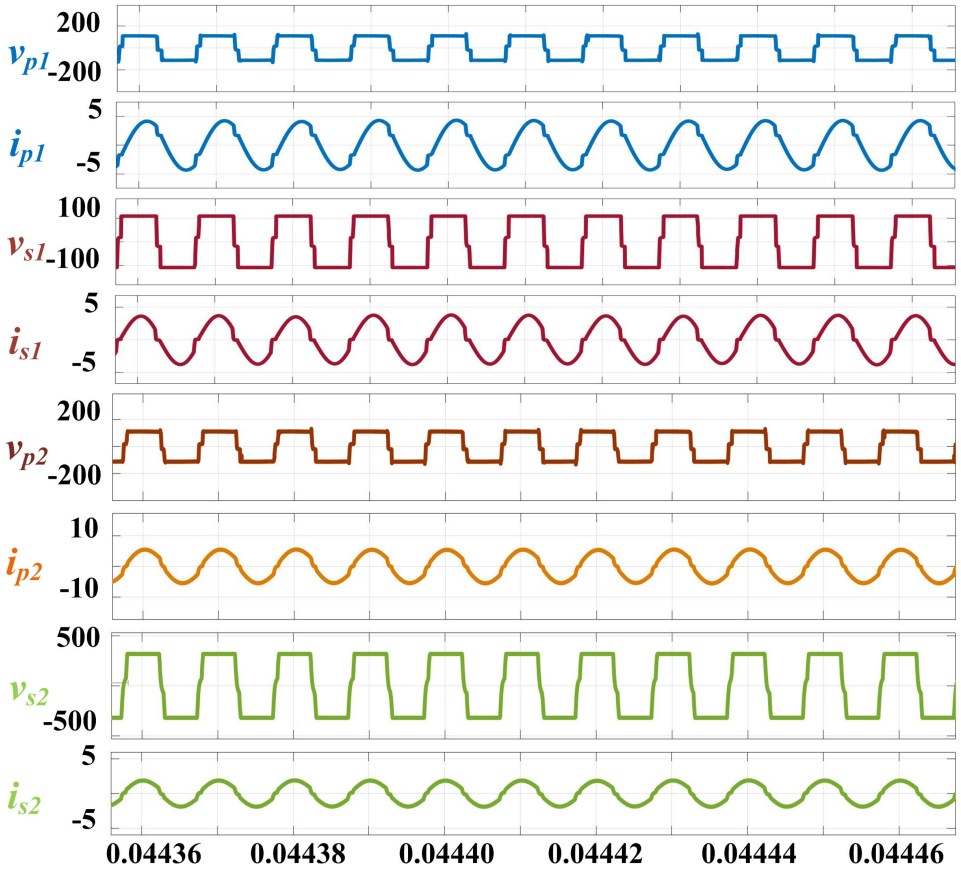


(a)

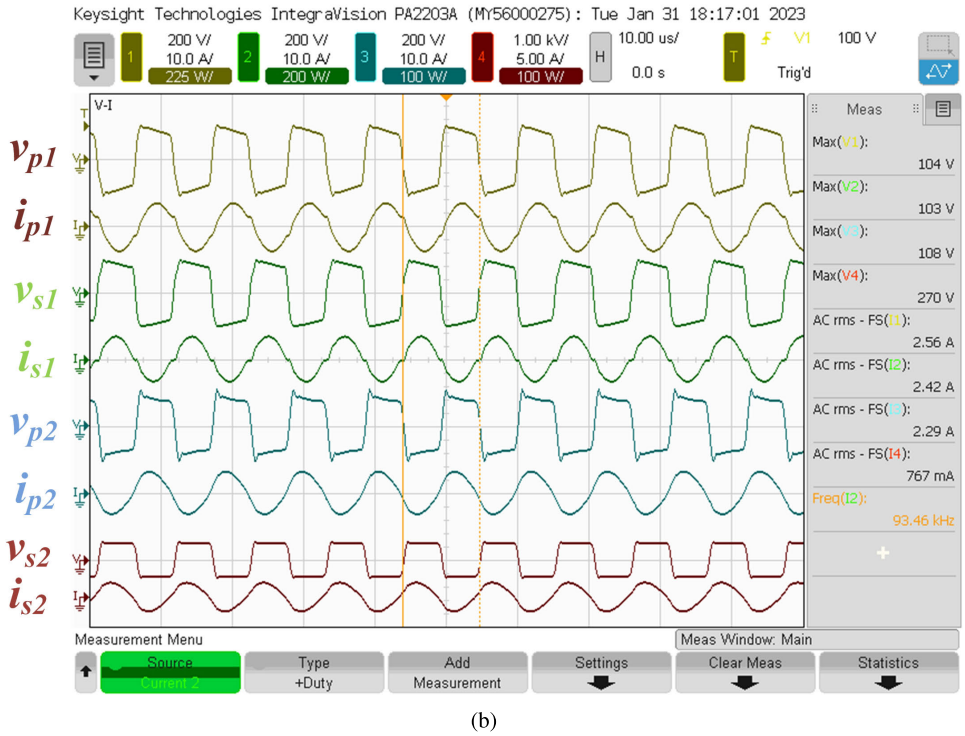


(b)

FIGURE 13. Experimental waveforms of the M_3 combination of the HFTs for simultaneously charging at half load condition of 100 W on each HFTS (a) power sharing and efficiencies and (b) voltages and currents waveforms.



(a)



(b)

FIGURE 14. (a) Simulations and (b) Experimental waveforms of the primary sides - voltages, currents, and a secondary side - voltages, currents of the M_3 combination of the HFTs simultaneously charging at full load condition.

TABLE 5. Theoretical loss calculations in different components of the proposed QZRC in the M_1, M_2, and M_3 combinations.

Components of QZSRC	Types of losses	Loss calculations formulae	M_1	M_2	M_3
MOSFETS	Driving losses (mW)	$P_{drive} = 4 \cdot (\frac{1}{2} \cdot C_{gs} \cdot V_{gs}^2) \cdot f_{sw}$	0.28	0.28	0.28
	Turn-off loss (W)	$P_{tf} = 4 \cdot (\frac{f_{sw} \cdot v_i \cdot i_i \cdot (t_r + t_f)}{2})$	6.37	5.61	5.38
	Conduction loss (W)	$P_{con\_mos} = 4 \cdot (i_{mos\_rms}^2 \cdot R_{ds} + i_{mos\_st}^2 \cdot R_{ds})$	18.1	15.3	14.5
Transformers	Core loss (mW)	$P_{core} = 2 \cdot K_h \cdot f_{ds}^m + B_{ac}^m \cdot M_{core}$	0.146	0.146	0.146
	Copper loss (W)	$P_{cu} = 2 \cdot (i_{prim\_rms}^2 \cdot R_{ac\_prim} + i_{sec\_rms}^2 \cdot R_{ac\_sec})$	12.60	5.45	7.01
Rectifier diodes	Conduction loss (W)	$P_{diode} = 8 \cdot (\frac{1}{2} \cdot \frac{P_0}{V_0} \cdot V_F + i_{diode\_rms}^2 \cdot R_d)$	13.1	4.3	4.28
Inductor loss	Conduction loss (W)	$P_{ind\_core} = 2 \cdot (i_{plr\_rms}^2 \cdot R_{ind}) + 2 \cdot (i_{qzsn\_rms}^2 \cdot R_{qzsn})$	27.70	27.70	27.72
Capacitor loss	Ohmic loss (W)	$P_{cap} = 2 \cdot (i_{cr\_rms}^2 \cdot R_{ESR}) + 2 \cdot (i_{qzsn\_rms}^2 \cdot R_{ESR})$	0.388	0.0788	0.153
Wiring losses	Conduction loss (W)	$P_{wire} = i_{wire}^2 \cdot R_{wire}$	9.83	8.84	9.17
		Total losses (W) (P_{TL_Mx})	88.88	67.4	68.1

*(P_{TL_Mx}) = Theoretical power losses in all combinations of M_x.

TABLE 6. Theoretical and experimental results validate the M_1, M_2, and M_3 combinations.

EMIIRC*	Parallel HFT combinations	P_{in} (W)	P_{Loss_Mx} (W)		P_{out} (W)	Efficiency %
			Theoretical	Experimental		
M_1	Lower (L_{m1}) - HFT	485	88.88	96.51	P_{out1} = 197 P_{out2} = 193	80
M_2	Higher (L_{m2}) - HFT	480	67.40	73.51	P_{out1}= 204 P_{out2} = 202	85
M_3	Moderate (L_{m2} and L_{m1}) - HFT	437	68.1	72.85	P_{out1} = 197 P_{out2} = 168	83

B. EXPERIMENTAL RESULTS OF THE M_2

Figures 11a and 11b show the experimental waveforms of the power-sharing with efficiencies, voltages, and currents in the upper and lower circuits of the M_2 case. In these combinations, it was observed that the input power of $P_{in} = 480W$ is equally shared between the loads to obtain $P_{out1} = P_{out2} = \simeq 200W$, output currents of $i_{out1} = i_{out2} = 0.83\ A$, and voltage gains achieved within the designed limits. However, the nominal voltage level of 300 V is not maintained in both the upper and lower circuit charging systems due to high magnetizing inductance. The efficiency is equal for both upper and lower circuits, and the overall efficiency of the simultaneous charging system for this case is around 85%.

C. EXPERIMENTAL RESULTS OF THE M_3

1) AT FULL LOAD CONDITION

Figures 12a and 12b shows the experimental waveforms of moderate equivalent magnetizing inductance-to-inductance ratio M_3 case. In these combinations, the input power of $438W$ is unequally shared with the loads to obtain $P_{out1} = \simeq 200W$ and $P_{out2} = \simeq 168W$, with output currents $i_{out1} = 0.65\ A$ and $i_{out2} = 2.0\ A$ respectively. At full load conditions, voltage gains are achieved within the design limits. Figures 12b and 11b, show that the voltages of the higher L_{m2} HFT charging circuit increased from 260 V to 278 V.

At full load, in M_3 combinations, the efficiency of the upper circuit charging system (high L_{m2} of HFT) is high compared to the lower circuit charging system (low L_{m1} of HFT).

2) AT HALF LOAD CONDITION

From Figures 13a and 13b, the efficiency of the low magnetizing inductance ($L_{m1} = 165\ \mu$H) of the HFT is seen to be higher than that of the high magnetizing inductance ($L_{m2} = 775\ \mu$H) of HFT in the upper circuit efficiency when the load was varied from light load to half load, and with unequal power distribution in the upper and lower circuits. Figures 14a and 14b show the waveforms of the voltages and

TABLE 7. Dual tank converters topologies comparisons.

Toplogies	[39]	[40]	[15]	[14]	Proposed Topology
Modulations	PWM	Magnetic control	PWM	PFM	PWM
Number of MOSFETS	9	2	9	4	4
Number of diodes	4	9	9	8	9
Number of transformers	2	2	2	2	2
Input voltage (V)	390	$340-380$	$380-420$	400	$85-115$
Output voltage (V)	$100-400$ $100-400$	$120-160$	$250-420$	$36-48$	$85-115$ $250-350$
Power level (W)	1600	$32-320$	3300	700	500
Switching frequency	Fixed	Fixed	Fixed	Variable	Fixed
No. of battery	1	1	1	1	2

TABLE 8. Comparisons of Non-isolated and isolated topologies.

References	Converter	Isolation	No. of components *S/*D/*L/*C	Voltage gains	*NB
[41]	Step-up DC-DC Converter	Non-isolated	3/4/2/3	High	*NM
[42]	TS-TM step-up DC-DC	Non-isolated	3/4/2/4	High	*NM
[38]	TS-TM step-up DC-DC	Non-isolated	3/4/2/3	High	*NM
[43]	Ladder resonant switched-capacitor converters	Non-isolated	2/4/1/5	Medium	*NM
Proposed Topology	QZSRC	Isolated	4/9/4/3	Low	2

*TS-TM= Triple Switch Triple Mode; *S = Switches; *D=Diodes; *L= Coupled Inductors; *C = Capacitors;*ND= No. of diode; *NB= No. of batteries;*NM = Not Mentioned

currents on the primary and secondary sides of the upper and lower M_3 combinations of the simulations, and experiments.

Figures 14a and 14b the simulation and experimental results of the primary and secondary side voltages and currents of both HFTs, respectively. The shoot-through condition does not affect the voltages and sinusoidal currents at the primary and secondary sides. Fig. 15 shows the variation of efficiency as a function of power in the proposed converter for the combinations of M_1, M_2, and M_3 from light to maximum loads. These values were obtained experimentally using the setup shown in Fig. 9.

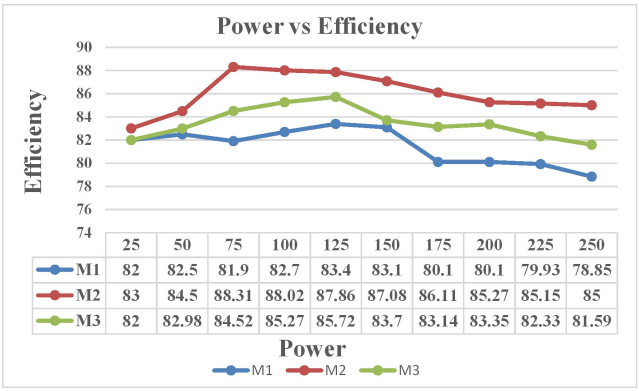


FIGURE 15. Power vs. efficiency plots of combinations of M_1, M_2, and M_3.

D. LOSS ANALYSIS

The power loss is primarily caused by the conduction losses driving losses, and switching losses of four MOSFETs, the conduction losses of nine rectifier diodes; the copper losses; and the core losses of two transformers. The required data for the loss calculations are listed in table 4 , and the theoretical loss calculations for the different components are shown in the table 5 for all three cases. Finally, all the combinations of theoretical and experimental results are tabulated in table 6, [36], [37], [38]. In Table 7, a comparative analysis of dual tank-based topologies with proposed topology has been carried out. This comparison is done regarding Modulations, number of switches, number of diodes, number of HFTs, output voltage variations, power level, switching frequency,

and number of batteries charged using tank circuits. In table 8 comparison is done with the non-isolated topologies.

V. CONCLUSION AND FUTURE SCOPE

The proposed single-stage simultaneous charging system using QZSRC has been tested at the constant resonant frequency with the DLST-PWM technique with a prototype of 200 *W* on each HFT in the upper and lower circuits. Based on the simulation and experimental results, the observations made are summarized here:

(a) For simultaneous charging systems at equal voltage levels with an equal equivalent magnetizing inductance - to - inductance ratio in the HFTs, it is observed that the power is equally distributed in both the upper and lower circuits from light load to full load conditions. The total efficiency is the sum of the efficiencies of both upper and lower circuits. In the lower and higher equivalent magnetizing inductance-to-inductance ratio combinations of the HFTs, the overall efficiencies of the simultaneous charging system are around 80% and around 85%, respectively.

(b) At lower values of the equivalent magnetizing inductance-to-inductance ratio combination in the HFTs, the circulating current is high compared to the circulating current at higher values of the equivalent magnetizing inductance-to-inductance ratio combination in the HFTs. Due to the high circulating currents, the power flow and efficiency capability are fairly reduced.

(c) Due to the moderate equivalent magnetizing inductance - to - inductance ratio, the effect on power sharing and efficiencies will vary from light load to full load conditions for the simultaneous charging system at unequal voltage levels. At light load conditions, power flowing through lower L_{m1} - HFT gives a higher efficiency of around 50% compared to that higher L_{m2} - HFT, which has an efficiency of around 38%. At full load conditions,power flowing through higher L_{m2} - HFT has a higher efficiency of 45% compared to that lower L_{m1} - HFT, which has an efficiency of around 38%. However, the overall efficiency of the simultaneous charging systems is constant at 83% when the load varies from light to full.

The results of the equivalent magnetizing inductance - to - inductance ratio of the HFT in all combinations cases have demonstrated that the proposed topology can be used for the various voltage levels of the charging systems. Comparison of the pattern of voltage and the current waveforms on the primary and secondary sides obtained in LLC Resonant converters (as seen in literature) and those in the proposed converter employing the DLST-PWM technique show that the waveforms are similar. It can therefore be concluded that the proposed converter has additional advantages of low EMI and variable duty to obtain the required output voltage at a fixed frequency.

The proposed converter is able to charge batteries simultaneously while operating at a fixed frequency with a combination of QZSN and LLC elements. It holds good efficiency even at low output power levels in M_2 and M_3 combinations. With this proposed converter, various analyses provide a platform for the selection of HFTs for simultaneous charging of different charging levels of batteries.

The future scope of the work includes testing at higher power levels, testing with EV batteries, applying the phase-shift PWM technique, and optimizing the inductance ratio to obtain higher efficiency.

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