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RESEARCH ARTICLE

An Automatic I/Q Calibrated RF Down-Converter IC With Full-Band 48–55 dB Image Rejection and 150% Fractional IF Bandwidth for SATCOM Applications

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ABSTRACT This article presents a fully-integrated Ku-band CMOS down-converter for the low earth orbit satellite user downlink applications. To receive satellite signals adequately, a wideband receiver is presented with an automatic in-phase and quadrature (I/Q) mismatch calibration to carry out above 40 dB image rejection ratio (IRR) to the interferences within 2 GHz span concurrently. During the I/Q signal phase adjustment, the proposed wideband I/Q interpolator (IQI) exhibits almost a constant group delay over the wide IF signal bandwidth, which alleviates the iterative calibration between multiple frequency points in a wideband system. Also, the proposed wideband IQI has apparently less influence on signal amplitude than the reported phase interpolator and delay cell while calibrating I/Q phase imbalance. This work utilizes polyphase filters to fulfill on-chip image-rejection integration and exploits logarithmic power detector to realize I/Q mismatch indication in automatic calibration. The receiver delivers a peak measured conversion gain of 37.8 dB, an averaged noise figure of 6 dB, and below ±1.5 dB gain variation within the full signal band. Above all, the down-converter achieves not only high IRR performance but broad bandwidth at the IF frequencies from 0.3 to 2.35 GHz (48–55 dB IRR, 150% fractional IF bandwidth) without any external control, tuning, or assistance. The closest frequency proximity is no more than 0.6 GHz between the received satellite signal and image. To the best of authors' knowledge, this work demonstrates the highest fractional IF bandwidth among the reported wideband CMOS receivers with high image rejection (IRR > 40 dB).

INDEX TERMS CMOS, low earth orbit (LEO) satellites, high image rejection, integrated circuit (IC), RF down-converter, auto calibration, wideband, BIST, satellite communication (SATCOM).

I. INTRODUCTION

Low earth orbit satellite (LEO) is emerging as an essential technology to provide lower latency, higher throughput, and more flexible capacity than traditional geostationary orbit (GEO) satellite in global broadband internet access. Owing to the closeness and the short data paths, LEO-based networks show a similar latency to the existing terrestrial networks, which makes it possible to provide users fiber quality connectivity over a wide area through deploying satellite constellation [1]. The system operators choose Ka-band for gateway communications (17.8–19.3 GHz and 27.5–30 GHz for downlink and uplink, separately). As shown in Fig. 1, Ku-band is used for user links (10.7–12.7 GHz and 14–14.5 GHz for downlink and uplink, respectively) [2], [3]. The satellite RF signals can also be polarized into right-handed circular polarization (RHCP) and left-handed circular polarization (LHCP). This work focuses on the user downlink application

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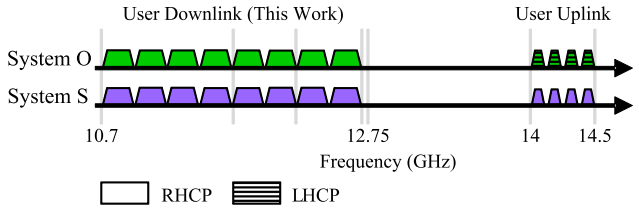

FIGURE 1. Frequency allocation of LEO satellite user link.

and the full signal band includes eight of 250 MHz channels. In addition to wide bandwidth, satellite receivers need to suppress out-of-band interferers effectively. Since the out- of-band interferers can be very large especially at 10–16 GHz due to the Ku-band satellite transmitters, high power point-to-point backhaul systems, and radar systems, the Ku-band satellite system requires at least 40 dB IRR to assure the received signal quality for data demodulation [4], [5], [6]. One way for the interferer suppression is to use off-chip passive filters. Nevertheless, this increases the system cost and the filter loss adds to the system noise figure. Therefore, it is better to design a wideband receiver with integrated high image rejection as addressed in this article.

Wideband integrated receivers with a substantial image rejection (IRR $>$ 40 dB) have been reported [7], [8], [9], [10], [11]. Most wideband receivers employ the fixed and narrowband intermediate frequency (IF) architecture to achieve wide bandwidth by changing the local oscillator (LO) frequency. Choosing a high IF frequency improves the image filtering response in front-end circuit design. However, this architecture makes it difficult to concurrently receive different satellite channels due to the narrow IF bandwidth. Another disadvantage is the image-reject receivers requiring high IF up to 8–16 GHz will demand a high-quality factor (Q) channel-select filtering, which therefore increases the subsequent demodulation circuit complexity. In [12], a published wideband receiver integrates image rejection with a wider and lower IF choice (IF: 2–5 GHz). The transformer-based calibration-free receiver front-end utilizes cascaded transformers for wideband high-precision quadrature LO generation, and a two-stage RC-CR polyphase filter (PPF) is used to complete the image rejection at the IF frequency. Nevertheless, the reported receiver cannot satisfy the minimal IRR of 40 dB within the full IF bandwidth.

This paper, which is an expanded edition of [13], presents a low-IF wideband receiver with high image rejection. By selecting suitable operating frequencies for the LO and IF (LO: 10.4 GHz, IF: 0.3–2.35 GHz), the image can be apparently suppressed after I/Q mismatch calibration without using external filtering. The proposed wideband I/Q interpolator greatly simplifies the wideband IF mismatch calibration. The measured 150% fraction IF bandwidth (IRR $>$ 40 dB) is better than those of other reported wideband receivers with high image rejection. This paper is organized as follows. Section II presents the proposed image-reject receiver architecture. The detailed circuit operation principles and implementation are described in Section III. Section IV provides the measurement results, and Section V concludes this work.

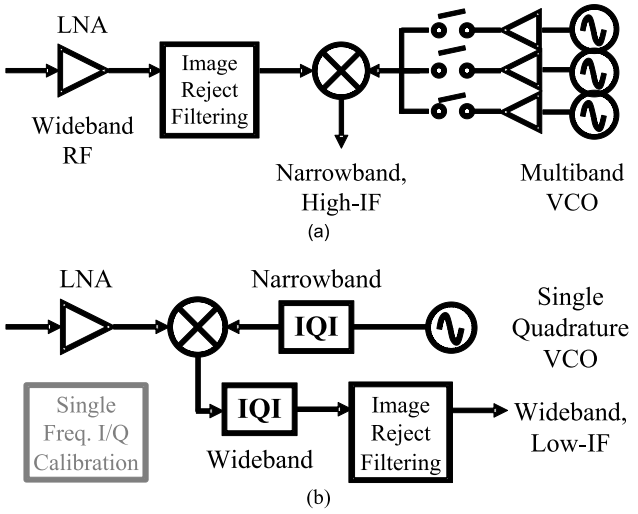

FIGURE 2. Topologies of wideband receivers with high image rejection. (a) Traditional narrowband IF method. (b) Proposed wideband IF method.

II. RECEIVER ARCHITECTURE

Fig. 2(a) presents the traditional monolithic receiver architecture with a RF image-reject filtering. By choosing a high-IF (8–16 GHz), the wideband receiver can integrate the filtering within the low-noise amplifier (LNA) or the mixer and achieves high IRR with minimum noise figure (NF) impact. This topology requires the use of multi-band voltage-controlled oscillator (VCO) to maintain the fixed IF. For several GHz tuning range applications, a capacitor bank can be added to VCO for a wide capacitance range. Nevertheless, this method may occupy a large area and, together with the on-resistance of the bank switches, result in a decreased tank Q of the oscillator. Since most satellite systems adopt the enhanced phase-shift keying (PSK) modulation schemes such as 16APSK or 32APSK, low LO phase noise is essential for accurate signal demodulation. Also, the operating frequency necessitates a higher IF-filter order for better Q in channel selection. As shown in Fig. 2(b), a low-IF receiver with wide IF bandwidth is proposed. An IF from 0.3 GHz to 2.35 GHz is selected together with a wideband IF I/Q interpolator (IQI) and a wideband integrated PPF for image-reject filtering. The proposed IF IQI not only adjusts the signal amplitudes but manipulates the signal phases over a wide bandwidth. The mismatches of wideband down-converted I/Q signals can be largely reduced after just single-frequency calibration, which improves the circuit complexity and results in the following PPF to sustain a good image rejection. A single-band quadrature VCO (QVCO) of 10.4 GHz and narrowband LO I/Q interpolator provide the receiver LO signals. The PPF in IF sustains a high image rejection if the input I/Q signals are balanced after calibration. Moreover, in the proposed architecture, the IF is below 3 GHz and the demodulator operating frequency and the IF- filter order can be relaxed.

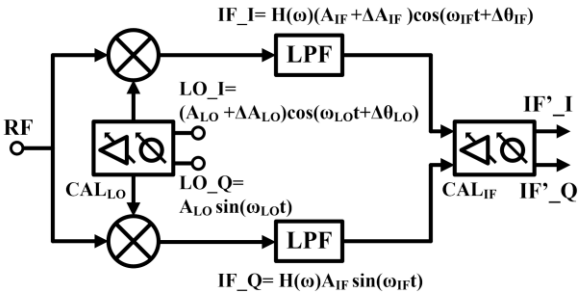

FIGURE 3. Quadrature mixing with I/Q imbalance and compensation.

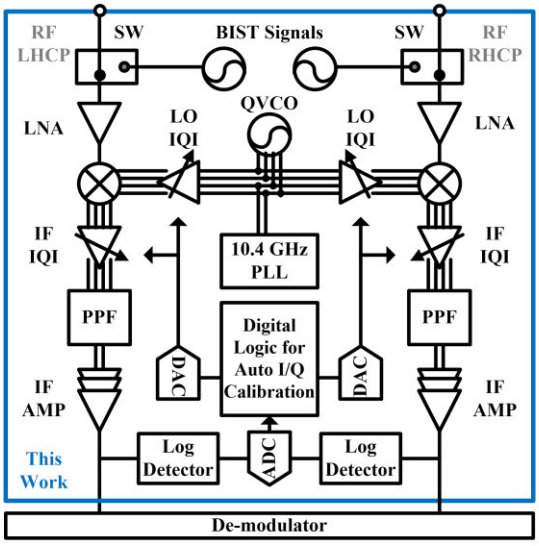

FIGURE 4. Block diagram of the proposed Ku-band down-converter with automatic I/Q calibration.

The IRR formula in [14] considers the I/Q errors of both LO and IF ports in quadrature mixing. Fig. 3 depicts the model to calculate the effects of the LO and IF compensation on IRR. $\Delta A_{LO}/\Delta\theta_{LO}$ and $\Delta A_{IF}/\Delta\theta_{IF}$ represent the uncompensated amplitude/phase imbalances in LO and IF, respectively. The compensated IRR, defined by the average power ratio of signal and image, can be derived as

$$\mathrm{IRR} = \frac{1 + (1+\Delta A')^2 + 2\left(1+\Delta A'\right) cos(\Delta\theta')}{1 + (1+\Delta A')^2 - 2\left(1+\Delta A'\right) cos(\Delta\theta')} \quad (1)$$

where

$$\Delta A' = \left(\frac{\Delta A_{LO}}{A_{LO}} - \frac{\Delta A_{CAL\_LO}}{A_{LO}}\right)\left(\frac{\Delta A_{IF}}{A_{IF}} - \frac{\Delta A_{CAL\_IF}}{A_{IF}}\right) \quad (2)$$

$$\Delta\theta' = \left(\Delta\theta_{LO} - \Delta\theta_{CAL\_LO}\right) + \left(\Delta\theta_{IF} - \Delta\theta_{CAL\_IF}\right) \quad (3)$$

In (1), $\Delta A'$ is the compensated I/Q amplitude mismatch from LO and IF, while $\Delta\theta'$ is the compensated I/Q phase mismatch. According to (2) and (3), the I/Q imbalance of the low-IF receiver can be improved by properly selecting the calibration parameters from the calibration circuits, where the amplitude/phase compensation parameters of LO and IF calibration circuits are denoted as $\Delta A_{CAL\_LO}/\Delta\theta_{CAL\_LO}$ and $\Delta A_{CAL\_IF}/\Delta\theta_{CAL\_IF}$, separately. To have IRR above 40 dB with margin, the resulting amplitude and phase mismatch of 50 dB IRR shall be within ±0.05 dB and ±0.5° according to [15]. Besides the stringent resolution of calibration, another design challenge is to provide wideband compensation. The reported calibration methods have limited performances for wideband receivers to satisfy both high image rejection (IRR > 40 dB) and broad bandwidth requirements [16], [17], [18], [19].

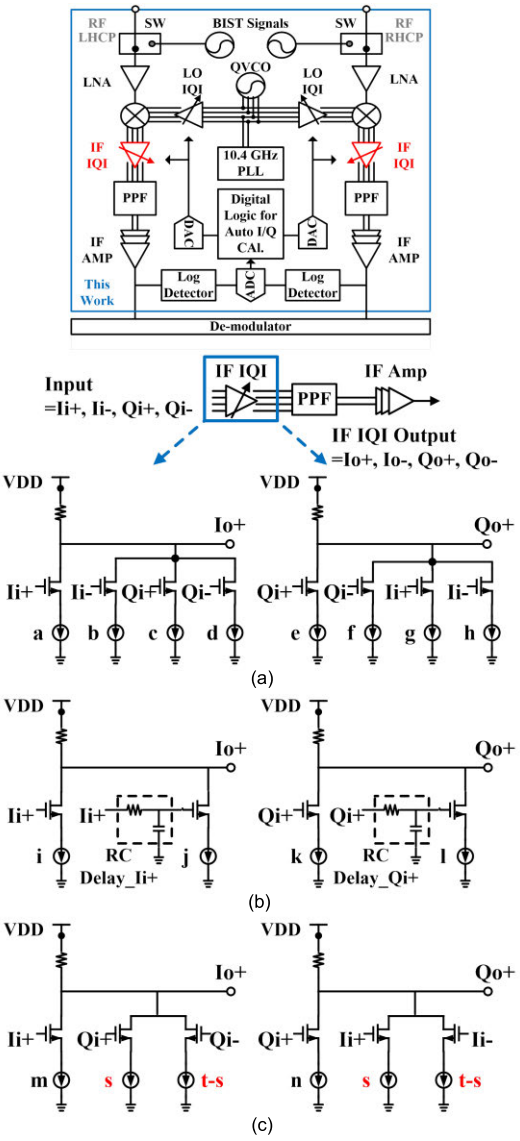

FIGURE 5. IF chain block diagram. (a) Conventional PI, (b) conventional delay cell, and (c) proposed IQI topologies for IF I/Q phase calibration.

Fig. 4 illustrates the block diagram of the proposed wideband image-reject RF down-converter IC with automatic I/Q mismatch calibration. To satisfy a diversity of system applications, this work can independently receive satellite signals of two polarizations, RHCP and LHCP. In each polarization path, the receiver comprises a single-ended LNA, an active mixer, and a 6th-order wideband image-reject PPF followed

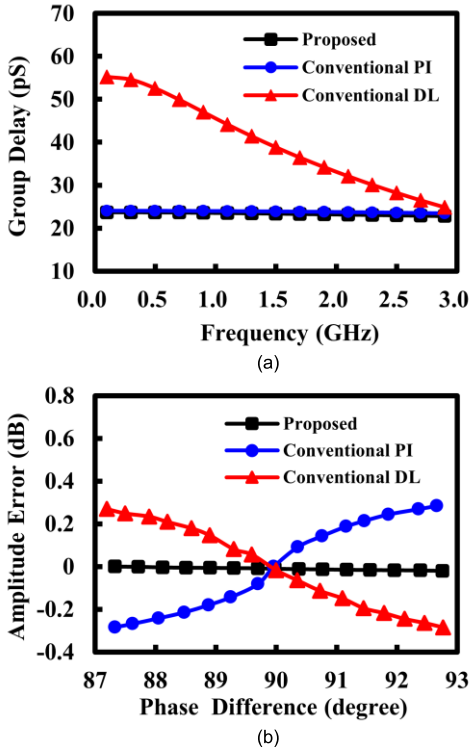

FIGURE 6. (a) Simulated group delay. (b) Simulated I/Q amplitude imbalance versus I/Q phase difference after phase adjustment.

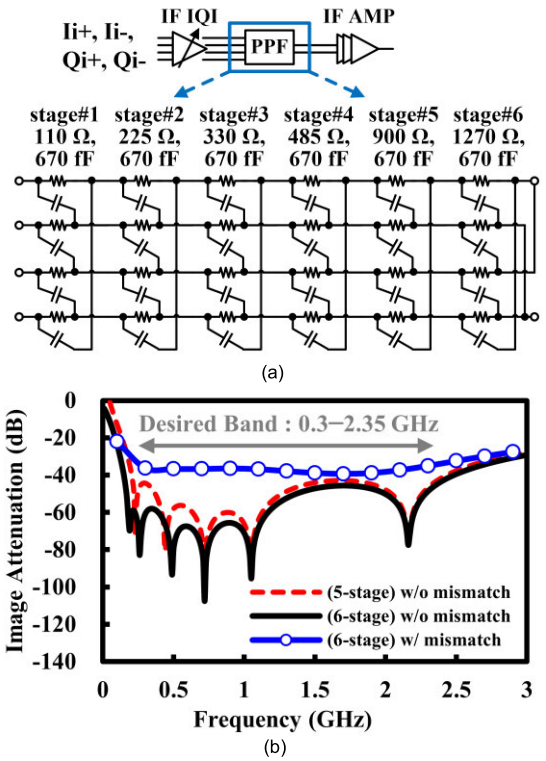

FIGURE 7. The IF polyphase filter. (a) Schematic and component values. (b) Simulated image attenuation.

by a three-stage IF amplifier (AMP). A dual calibration scheme composed of LO and IF compensation is used in this work. The proposed IF IQI features a high-resolution wideband adjustment within the full IF span while the proposed narrowband LO IQI combines accurate mismatch compensation and LO buffer function moderately. The I/Q mismatch detection in automatic calibration is realized by generating a built-in self-test (BIST) RF signal internally, rectifying the IF test signal in log detector, and finally processing the output indicator in the digital circuitry. The wideband IF compensation and mismatch indication can largely reduce the circuit and computation complexity. An integer-N phase-locked loop (PLL) constitutes the 10.4 GHz LO generation with a 50 MHz reference frequency. This reference frequency is derived from the chip reference clock generated by an internal crystal oscillator (XOSC). Based on the coupling of the two LC-tank VCOs, the coupled-oscillators implement the QVCO in this work to generate quadrature LO phases. The cascode-based coupling technique is used to improve the I/Q phase ambiguity [20].

III. CIRCUIT DESIGN

A. CALIBRATION BUILDING BLOCKS

1) IF IQI

The IF IQI plays a vital role in IF calibration and is responsible to interpolate the wideband IF inputs and provide PPF balanced I/Q signals for image-reject filtering. I/Q mismatch calibration includes phase mismatch and amplitude mismatch calibration. To adjust signal phase in calibration, the conventional phase interpolator (PI) and delay cell (DL) can be used and are shown in Fig. 5(a) and Fig. 5(b), respectively. The conventional PI has the advantage of wide phase range (0° to 360°) by utilizing quadrature phase mixing [21], [22]. The phase interpolation can be expressed as a weighted summation of the four I/Q signals. The weighting factors of I/Q signal paths are realized by adjusting current sources of the in-phase signal path (a,b,c,d) and current sources of the quadrature signal path (e,f,g,h) separately. Conversely, the conventional variable delay cell features its simplicity by steering the fast signal current sources (i and k) and slow signal current sources (j and l) [23]. Phase control is accomplished by making the output phase a summation of the phase delays in the fast and slow paths. Nevertheless, the disadvantage of the above two reported designs is their output swing will change under different phase control choices, which necessitates a limiter to solve the swing imbalance. As illustrated in Fig. 5(c), the proposed design takes the complementary form of both phase control signal sources (Io^+: Qi^+/Qi^- and Qo^+: Ii^+/Ii^-) and phase control current sources (s and t-s). The current sources of m and n are reserved for amplitude mismatch calibration. $\Delta\varphi$ and ϵ denote the interpolated I/Q signal phase difference and amplitude mismatch of the proposed IQI, separately. In (4), $\Delta\varphi$ is independent of frequency and suitable for wideband IF signal phase adjustment. The interpolated I/Q signal phase difference depends on the choice of the phase control current

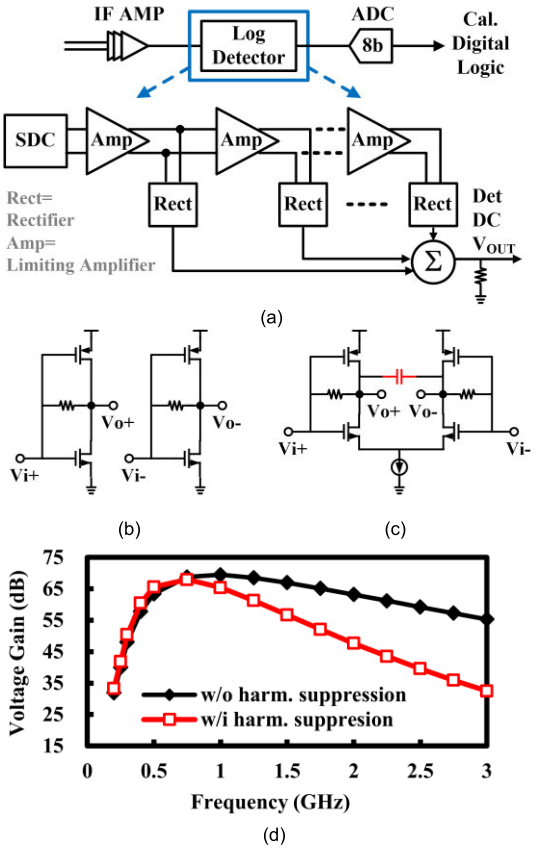

FIGURE 8. The power detector for ISSI. (a) The detector architecture. (b) The conventional and (c) the proposed limiting amplifier units. (d) The simulated detector voltage gain.

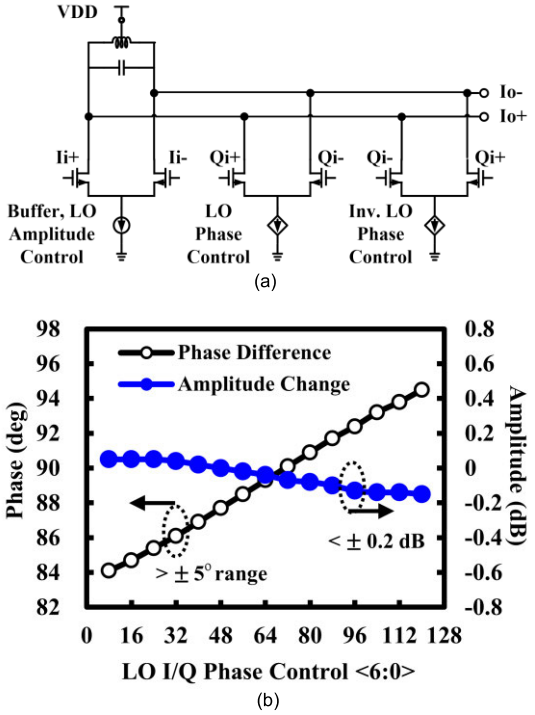

FIGURE 9. (a) The simplified schematic and (b) the simulated phase difference and amplitude change versus phase control of the LO IQI.

source complements of t-s and s for a given m and n. According to (5), ϵ is insensitive to the resulting difference of phase control sources (t-2s and 2s-t) during phase interpolation.

$$\Delta\varphi = \frac{\pi}{2} + tan^{-1}\left(\frac{t-2s}{n}\right) - tan^{-1}\left(\frac{2s-t}{m}\right) \quad (4)$$

$$\epsilon = 10\log\left[\frac{(n^2+(t-2s)^2)}{(m^2+(2s-t)^2)}\right] \quad (5)$$

Phase shifting of a broadband signal needs to provide a constant group delay over the signal bandwidth. As shown in Fig. 6(a), the simulated group delays of the proposed IF IQI and conventional PI show flat frequency responses, less than 0.8 pS deviation within the desired 2 GHz IF bandwidth. On the contrary, the conventional DL finds a group delay deviation of 27.5 pS performance from 0.3 GHz to 2.35 GHz. Fig. 6(b) provides the simulated amplitude error at different phase interpolation values. Under a similar I/Q signal phase range from 87° to 93°, the proposed IF IQI achieves no more than 0.02 dB amplitude difference while the performances of the conventional PI and DL are 0.28 dB and 0.29 dB, respectively. At the supply voltage VDD of 1.6 V, under a perfect I/Q balance assumption ($\Delta\varphi = 90°$), the sizes of phase control current sources (s and t-s) and amplitude control current sources (m and n) are 115 μA and 1150 μA, respectively. To meet high IRR requirement, the resolutions of phase and amplitude interpolation in the wideband IF calibration are set to 0.1° and 0.03 dB, separately.

2) IF PPF

Besides the proposed IF IQI, the integrated PPF is essential to obtain a wideband and high IRR performance in the IF signal chain. The pole splitting technique by cascading several RC-CR networks can separate the generated poles, smooth the frequency response, and extend the achievable bandwidth [24]. As depicted in Fig. 7(a), six RC-CR sections are used and cascaded in this work. To alleviate the desired signal attenuation, the resistors in the latter stages are chosen larger than those in the former. Fig. 7(b) shows the simulated performance of the proposed IF PPF. For the ideal balanced quadrature inputs, the 6-stage polyphase filter design exhibits better image attenuation at 0.3 GHz than the 5-stage filter by 16.5 dB within the desired band. The former is preferred due to the limited image filtering of front-end circuit and the input imbalance effect on PPF. The LC-tuned integrated LNA has little suppression to the image signal under close frequency proximity of 600 MHz. To place PPF poles at the head of the desired band can compensate the lack of RF image filtering. Taking the mismatch into consideration, the 6-stage PPF fails to meet the required image rejection of 40 dB if imperfect filter inputs contain the amplitude mismatch of 0.1 dB and the phase difference of 1°. The IRR degradation not only coheres to the proposed IQI resolution but manifests the importance of mismatch calibration.

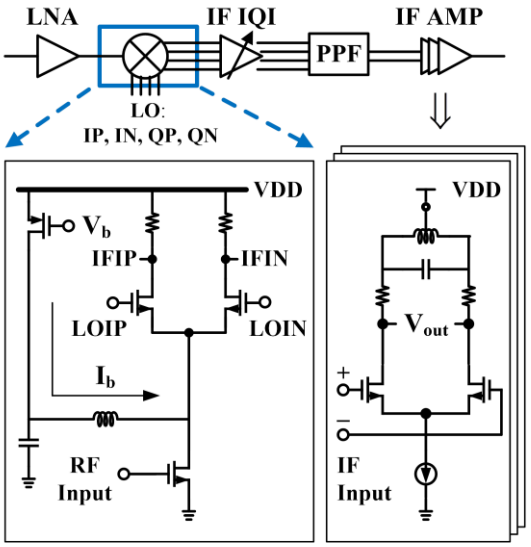

FIGURE 10. Receiver chain blocks and building block topology.

3) IF LOG DETECTOR

The automatic I/Q mismatch calibration in this work relies on the close-loop control of the mismatch cancellation and the image signal strength indication (ISSI). The former is implemented by the I/Q signal amplitude and phase adjustment. The function of ISSI is to quantitatively demonstrate the existing imbalance condition in a receiver by using a built-in self-test image signal. The challenge of ISSI lies in the ability to indicate the difference even if the signal power level is quite low in high image rejection condition. As illustrated in Fig. 8(a), this work uses a logarithmic power detector to convert the IF signal level to a DC voltage. The detector performs the single-to-differential conversion (SDC) in the first stage and cascades limiting amplifiers and rectifiers for a wide detection range. The IF test frequency is set to 500 MHz after a frequency response comparison since the log detector presents higher gain performance and hence better linear dynamic range. The operation details of the complete ISSI are as follows. At the beginning of the automatic I/Q calibration, a RF image test signal is generated by the 9.9 GHz on-chip inverter-based ring oscillator and fed to the input of LNA. The log detector rectifies the down-converted IF image test signal and an 8-bit ADC generates a digital output code. The control signal is conclusively obtained with the digital circuitry.

Nevertheless, some undesired harmonics are accompanied by the imperfect sinusoidal test signal and therefore the additional power inputs interfere with the regular strength indication. Fig. 8(b) shows the conventional resistive-feedback inverters (RFIs). The RFI is composed of a NMOS transistor, a PMOS transistor, and a shunt feedback resistor. Under a low supply voltage, the RFI has higher transconductance and better gain performance than a common-source stage. Also, the RFI architecture provides a good driving ability and is suitable for receiver output stage design [25]. Fig. 8(c) is the proposed amplifier unit with harmonic suppression. Compared with the conventional RFI, the proposed fully-differential design not only improves the rejection to the common-mode spurious signals but integrates the low pass filtering made up of the low-cost metal-insulator-metal (MIM) capacitor. Fig. 8(d) shows the simulated power detector voltage gain. In comparison with the detector design without low pass filtering, the proposed detector has better third and fifth harmonic suppression by 10 dB and 20 dB, respectively. In this work, the simulated detection range of 500 MHz with ±3 dB nonlinearity reaches 65 dB, from -10 dBm to -75 dBm.

4) LO IQI

Placed at 10.4 GHz QVCO output, the LO IQI compensates the mismatch of quadrature LO signals and acts as a buffer stage to the subsequent down-conversion mixer. As illustrated in Fig. 9(a), the LO IQI is similar to the aforementioned IF IQI in circuit configuration but makes use of a parallel LC circuit as its load. The existing LO in-phase and quadrature signals and complementary current control are utilized to simplify the phase adjustment. Different from the addition of quadrature signals in the LO phase difference compensation, a straight operating current selection of the LO amplitude control stage compensates the LO amplitude mismatch. In this work, a 7-bit current-mode digital-to-analog converter (DAC) implements the high-resolution compensation current control. Fig. 9(b) provides the simulated LO I/Q signal phase difference and amplitude change at different phase control values. The simulated phase difference presents almost linear characteristic in response to the phase control. The phase tuning resolution at 10.4 GHz in simulation reaches 0.1°, and more important, the resulting amplitude variation is less than 0.004 dB per phase tuning step. The maximum amplitude change among the full phase tuning range of 12.5° is no more than ±0.15 dB. The power consumption of the full LO phase control circuitry adds up to only 5 mW. For the narrow-band LO phase interpolation in this work, the proposed LO IQI design demonstrates a high-resolution low-complexity design.

The I/Q path mismatch compensation is performed in the following sequence: LO phase → LO amplitude → IF amplitude → IF phase. The LO signal path is solved first since more layout sensitivity results from the operating frequency. The amplitude adjustment resolution of the LO IQI is 0.07 dB and larger than that of the IF IQI since the active mixer is less sensitive to the swing mismatch of quadrature signals than the IF PPF in this work. A sequential search is used here. Calibration will stop while the strength indicator minimum of the down-converted test image signal is found.

B. RECEIVER CHAIN

Fig. 10 illustrates the receiver chain block diagram and building block schematics. As for the receiver front-end (RXFE) circuit, a single-ended input, cascode common-source LNA is followed by a single-balanced active mixer. The mixer utilizes the inductor-based current-bleeding technique to insert

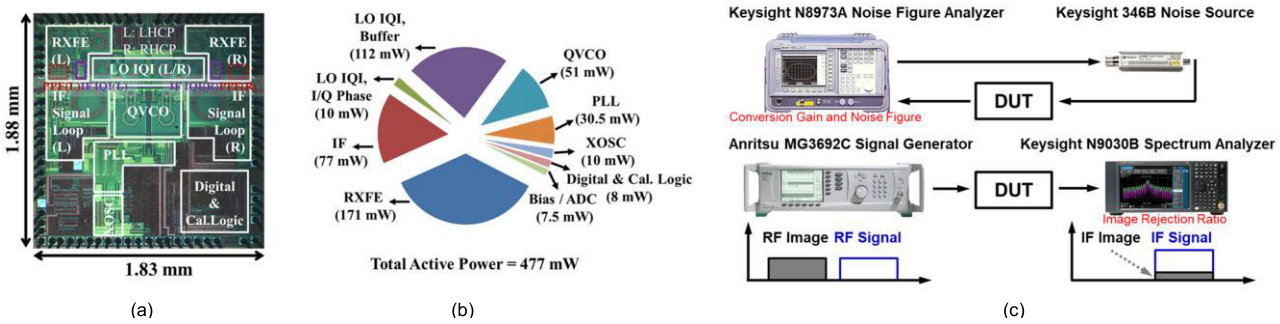

FIGURE 11. (a) Die photograph. (b) Power consumption chart. (c) Measurement setup.

a current source helper (I_b) [26]. This addition alleviates the conflicting requirements of the input transistor current (high enough for noise and linearity) and the load resistor current (low enough for large resistors and thus high gain). More importantly, the resulted low LO leakage not only improves the receiver gain desensitization in IF but suppresses an interference to log detector while ISSI runs. The mixer provides the simulated conversion gain of 10.5 dB at an expense of the operating current of 8.3 mA. The corresponding load resistor current is only 0.43 mA. After down-conversion, the IF signal flows through an IF IQI and a PPF to the three-stage IF amplifier. Composed of a differential pair with a LC tank load, the first stage of IF AMP cooperates with the RF front-end to obtain a wideband receiver gain response by means of stagger-tuning principle [27]. The gain slope of this stage is also controlled by the load resistor. Next, the IF AMP performs differential to single-ended conversion by using the current mirror source as an active load in the second stage. Driving an external low resistance instrument loading, the final output stage is implemented with a RFI topology in this work.

C. POWER PLAN

In system applications, the system operating voltage ranges from 11 V to 19 V. An on-board DC/DC switching converter IC is a widely-used regulator choice to convert the high voltage to a lower one [28]. This arrangement can have high system efficiency but results in the occurrence of the supply voltage ripples in blocks. Hence, the CMOS-based low dropout (LDO) regulators are placed in this work and regarded as voltage buffers to suppress the ripples. Thus, the proposed down-converter IC operates at 1.8 V nominally while the true supply voltages for analog and digital circuitries are regulated to 1.6 V and 1.2 V, respectively.

IV. MEASUREMENT

The proposed Ku-band down-converter IC is fabricated in a standard 110-nm CMOS technology. Fig. 11(a) shows the die micrograph. The total chip size is 3.45 mm^2, which supports two independent polarized RF signal down-conversion paths. Compared with published wideband receivers with high image rejection (IRR > 40 dB), this work is the first one to integrate both the LO source and BIST mismatch detection. The proposed ISSI detection blocks for automatic I/Q calibration occupy an area of less than 0.15 mm^2, which is area efficient. Additionally, the cell size of each 6-stage IF PPF in this work is no more than 0.017 mm^2, resulting in just 0.5% of the total chip area consumption. Furthermore, the dimensions of the proposed IF IQI are compact and each IF IQI size is as low as 140 μm × 75 μm.

The down-converter IC consumes 477 mW under 1.8V operating voltage. Fig. 11(b) shows the power consumption of blocks. In this chart, the consumed powers of RXFE, IF, and

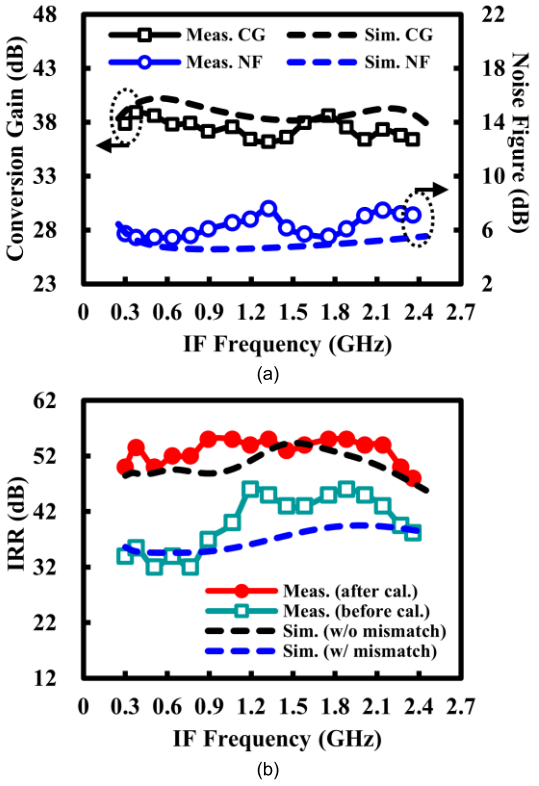

FIGURE 12. Measured and simulated (a) conversion gain, noise figure, and (b) image rejection ratio.

TABLE 1. Performance summary and comparison of the reported wideband receiver and mixer with high image rejection.

	[8] ISSCC'22	[9] JSSC'22	[10] JSSC'19		[11] TMTT'20	[12] JSSC'20	[14] Access'20	**This Work**
IF BW[#] (GHz)	Single-point and fixed IF frequency				15–17	3.1–4.6	0.65–2.5[$]	**0.3–2.35**
Fractional IF BW (%)	Single-point and fixed IF frequency				12.5	39	117[$]	**150**
IRR (dB)	> 52	30–50	> 30	> 25	75–84	32–56	33–36	**48–55**
CG (dB)	14–19	25–29	33	26.5	25–28.5	35	-12.8	**37**
NF (dB)	4.6–8	7.5–11	5.7	8.5	3.3–5	3.2–6.1	n.a.	**5.5–7.6**
Architecture	High-IF	Low-IF	Low-IF		High-IF	Low-IF	Low-IF	**Low-IF**
Image Proximity (GHz)	16	6	0.06		30	6.2	2	**0.6**
RF BW[#] (GHz)	24.3–54	22–26	28–28.5	37.3–38	20–44	24–33[†]	17.1–20.6[$]	**10.7–12.75**
RXFE P_{DC}[##] (mW)	32–75[$$]	35	85		30	60	12	**85.5**
External LO Source	Yes	Yes	Yes		Yes	Yes	Yes	**No**
Self-Test for IRR	No	No	No		No	No	No	**Yes**
Die Area (mm^2)	4.48	1.15[††]	4.5		1.8	0.77	1.22	**3.45**
Process	65 nm CMOS	28 nm CMOS	65 nm CMOS		22 nm CMOS SOI	45 nm CMOS SOI	90 nm CMOS	**110 nm CMOS**
Integration	RXFE+ IF PPF+ LO Tri-phase Generator	RXFE+ IF AMP+ LO/IF Hybrid Coupler	RXFE+ LO PPF+ Manual I/Q Calibration		RXFE+ IF AMP+ RF High-pass Filtering	RXFE + IF PPF+ IF AMP+ Quad. LO Generator	Mixer+ IF PPF+ IF AMP+ Quad. LO Generator	**RXFE+ IF PPF+ IF AMP+ QVCO+ Auto I/Q Cal.**

[#]IRR > 40 dB. [##]Each RF path. [$]IRR > 30 dB. [$$]Operation freq. dependent. [†]IF is fixed at 3.5 GHz. [††]Include up converter. Quad.: Quadrature

LO IQI add up two receiver chains. The power consumption of each IF is 38.5 mW including an IF IQI and a three-stage IF AMP, exclusive of passive PPF. LO IQI consumes only 5 mW in performing the proposed LO I/Q phase interpolation but needs more than 55 mW in buffering QVCO since the in-phase and quadrature LO signals have their own buffer stages and hence the power consumption is doubled from a viewpoint of a conventional fully-differential amplifier. The down-converter IC is tested on-board in a QFN40 package. RO4350 PCB is used to reduce dielectric loss at high frequency.

Fig. 11(c) illustrates the measurement setup. A Keysight N8973A noise figure analyzer is cascaded with a Keysight 346B noise source to verify the receiver conversion gain and noise figure performance. The N8973A has the ability to characterize not only amplifiers but also frequency translating devices and offers simultaneous noise figure and gain measurements. Next, to test IRR, a continuous-wave signal at desired band (10.7–12.75 GHz) and also a RF tone at image band (8.05–10.1 GHz) are generated by an Anritsu MG3692C signal generator and separately sent to the down-converter input. The receiver output spectrum is recorded and used to calculate IRR with a Keysight N9030B spectrum analyzer.

As shown in Fig. 12(a), the measured receiver presents 37.8 dB peak conversion gain, averaged 6 dB noise figure, and less than ±1.5 dB full-band gain flatness. The measured upper and lower 3-dB frequencies are above 2.4 GHz and below 0.25 GHz, respectively. The wide IF bandwidth and low IF frequency advantages make the concurrent full-band satellite signal demodulation feasible. Fig. 12(b) shows the measured IRR performance. A 48–55 dB IRR is achieved among the full IF signal band (0.3–2.3 GHz) after automatic I/Q calibration. The image rejection improvement reaches 20 dB maximally without any external control, on-board element, or additional filtering. It is observed experimentally that the I/Q phase difference obviously reduces from > 3° to below 1° after the proposed calibration. The I/Q amplitude mismatch improves from >0.5 dB to less than 0.1 dB after automatic tuning.

More importantly, the proposed down-converter IC presents a wideband and substantial image rejection even if the RF signal is close to its image by no more than 0.6 GHz. The resulting fractional IF bandwidth with high image rejection (IRR > 40 dB) is up to 150%, which is the highest performance according to the literature. Additionally, the rejection performance of this work is superior to other

reported IRR results of monolithic wideband image-reject receivers under similar image proximity. In comparison with more than 15 GHz IF frequency choice for better image filtering [11], this work largely simplifies the required demodulation circuit complexity. The proposed receiver architecture also demonstrates better conversion gain and noise figure performance than the receivers exploiting mixer-first topology to have wideband image rejection [29], [30].

Table 1 summarizes the measurement results of this work and makes a comparison with the state-of-the-art. The automatic I/Q calibrated receiver in this article achieves the best performance in terms of integration and fractional IF bandwidth with high image rejection.

V. CONCLUSION

A Ku-band automatic I/Q-calibrated bulk-CMOS down-converter IC for wideband satellite communication with high image rejection (IRR $>$ 40 dB) is presented in this paper. The proposed IF I/Q interpolator features almost a constant group delay within the full IF desired band and exerts less influence on signal amplitude than the published phase interpolator and delay cell while compensating the I/Q signal phase mismatch. Additionally, the used logarithmic power detector in this work demonstrates a better harmonic suppression, thereby realizing a wide I/Q mismatch indication range in automatic calibration. Delivering the conversion gain, noise figure, and gain flatness adequately, the measured receiver achieves the state-of-the-art 150% fractional IF bandwidth with substantial image rejection (48–55 dB IRR, 0.3–2.35 GHz) with no external filtering. Thus, the proposed down-converter IC develops a high-IRR, wide-IF bandwidth, and low-cost work for SATCOM applications.

REFERENCES

[1] M. Giordani and M. Zorzi, "Non-terrestrial networks in the 6G era: Challenges and opportunities," *IEEE Netw.*, vol. 35, no. 2, pp. 244–251, Mar. 2021.
[2] *Space Exploration Holdings*, LLC, FCC, Washington, DC, USA, 2018.
[3] I. del Portillo, B. G. Cameron, and E. F. Crawley, "A technical comparison of three low Earth orbit satellite constellation systems to provide global broadband," *Acta Astronautica*, vol. 159, pp. 123–135, Jun. 2019.
[4] *Ku-Band Satellite Low-Noise Block, dCSS Series Datasheet*, Microelectronics Technology, Inc., Hsinchu, Taiwan, 2016.
[5] *Ku-Band Satellite Low-Noise Block, DTVGD Series Datasheet*, Wistron NeWeb Corp., Hsinchu, Taiwan, 2023.
[6] *Ku-Band Satellite Low-Noise Block, PLL LO 10.75 Series Datasheet*, Universal Microwave Technology, Inc., Keelung, Taiwan, 2023.
[7] Q. Ma, H. Chung, and G. M. Rebeiz, "A 35–105 GHz high image-rejection-ratio IQ receiver with integrated LO doubler and > 40 dB IRR," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 595–598.
[8] J. Pang, Y. Zhang, Z. Li, M. Tang, Y. Liao, A. A. Fadila, A. Shirane, and K. Okada, "A power-efficient 24-to-71 GHz CMOS phased-array receiver utilizing harmonic-selection technique supporting 36dB inter-band blocker rejection for 5G NR," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 434–436.
[9] F. Quadrelli, D. Manente, D. Seebacher, F. Padovan, M. Bassi, A. Mazzanti, and A. Bevilacqua, "A broadband 22–31-GHz bidirectional image-reject up/down converter module in 28-nm CMOS for 5G communications," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 1968–1981, Jul. 2022.
[10] S. Mondal and J. Paramesh, "A reconfigurable 28-/37-GHz MMSE-adaptive hybrid-beamforming receiver for carrier aggregation and multi-standard MIMO communication," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1391–1406, May 2019.
[11] L. Gao, Q. Ma, and G. M. Rebeiz, "A 20–44-GHz image-rejection receiver with >75-dB image-rejection ratio in 22-nm CMOS FD-SOI for 5G applications," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2823–2832, Jul. 2020.
[12] M.-Y. Huang, T. Chi, S. Li, T.-Y. Huang, and H. Wang, "A 24.5–43.5-GHz ultra-compact CMOS receiver front end with calibration-free instantaneous full-band image rejection for multiband 5G massive MIMO," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1177–1186, May 2020.
[13] C.-C. Ma, K.-Y. Hsu, C.-Y. Huang, and C.-N. Kuo, "A 48–55 dB full-band image rejection RF down-converter IC with automatic I/Q self-test calibration for LEO satellite communications," in *Proc. IEEE 22nd Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2022, pp. 55–57.
[14] M.-H. Wu, J.-H. Tsai, and T.-W. Huang, "Ka-band calibration-free high image-rejection up/down mixers with 117% fractional IF bandwidth for SATCOM applications," *IEEE Access*, vol. 8, pp. 182133–182145, 2020.
[15] F. Piri, M. Bassi, N. Lacaita, A. Mazzanti, and F. Svelto, "A >40dB IRR, 44% fractional-bandwidth ultra-wideband mm-wave quadrature LO generator for 5G networks in 55nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 368–370.
[16] Y. Aoki, M. T. Dao, K. Min, Y. Hwang, Y. Kim, and S.-G. Yang, "1.4-GHz bandwidth frequency-dependent I/Q imbalance calibration for 5G mmWave communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 626–629.
[17] S. Kawai, "An 802.11ax 4×4 high-efficiency WLAN AP transceiver SoC supporting 1024-QAM with frequency-dependent IQ calibration and integrated interference analyzer," *IEEE J. lid-State Circuits*, vol. 53, no. 12, pp. 3688–3699, Dec. 2018.
[18] A. Rezola, J. F. Sevillano, I. Gurutzeaga, D. del Rio, R. Berenguer, and I. Vélez, "Built-in-self-calibration for I/Q imbalance in wideband millimeter-wave gigabit transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4758–4769, Nov. 2017.
[19] X. Huang, Y. J. Guo, and J. A. Zhang, "Transceiver I/Q imbalance self-calibration with phase-shifted local loopback for multichannel microwave backhaul," *IEEE Trans. Wireless Commun.*, vol. 15, no. 11, pp. 7657–7669, Nov. 2016.
[20] S. Li, I. Kipnis, and M. Ismail, "A 10-GHz CMOS quadrature LC-VCO for multirate optical applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1626–1634, Oct. 2003.
[21] R. Kreienkamp, U. Langmann, C. Zimmermann, T. Aoyama, and H. Siedhoff, "A 10-Gb/s CMOS clock and data recovery circuit with an analog phase interpolator," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 736–743, Mar. 2005.
[22] R. K. Nandwana, T. Anand, S. Saxena, S.-J. Kim, M. Talegaonkar, A. Elkholy, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A calibration-free fractional-N ring PLL using hybrid phase/current-mode phase interpolation method," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 882–895, Apr. 2015.
[23] L. Der and B. Razavi, "A 2-GHz CMOS image-reject receiver with LMS calibration," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 167–175, Feb. 2003.
[24] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, Jun. 2001.
[25] J.-H. Tsai, "Design of 1.2-V broadband high data-rate MMW CMOS I/Q modulator and demodulator using modified Gilbert-cell mixer," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1350–1360, May 2011.
[26] S. G. Lee and J. K. Choi, "Current-reuse bleeding mixer," *Electron. Lett.*, vol. 36, no. 8, pp. 696–697, Apr. 2000.
[27] Z. Deng, J. Chen, J. Tsai, and A. M. Niknejad, "A CMOS Ku-band single-conversion low-noise block front-end for satellite receivers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 135–138.
[28] *24V Step-Down Switching Converter, MP2314 Series Datasheet*, Monolithic Power Systems, Inc., Kirkland, WA, USA, 2014.
[29] A. Ahmed, M.-Y. Huang, D. Munzer, and H. Wang, "A 43–97-GHz mixer-first front-end with quadrature input matching and on-chip image rejection," *IEEE J. Solid-State Circuits*, vol. 56, no. 3, pp. 705–714, Mar. 2021.
[30] P. Song and H. Hashemi, "Mm-wave mixer-first receiver with selective passive wideband low-pass filtering," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1454–1463, May 2021.

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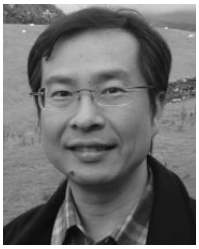

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