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RESEARCH ARTICLE

Development of a High-Gain Step-Up DC/DC Power Converter With Magnetic Coupling for Low-Voltage Renewable Energy

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ABSTRACT There exists an extensive range of applications for elevated gain DC/DC converters, as numerous low-voltage resources are exploited for power supply. Therefore, this study introduces a groundbreaking magnetically coupled DC/DC converter specifically designed for resources with low voltage, including micro PV or fuel cell systems. By enduring low current and voltage stresses, the power devices in this converter ensure remarkable efficiency while maintaining proven voltage ratio capability. The operational principles of the converter are thoroughly discussed and supported by the implementation of a 200W-400V prototype. In order to confirm the effectiveness of the converter, a range of experimental tests were carried out in different scenarios, confirming its dependable functionality. This novel converter opens up new possibilities for harnessing the potential of low-voltage resources, offering an efficient and reliable solution for power conversion. The research yields a substantial advancement in renewable energy systems, showcasing the practicality and efficiency of the proposed converter in real-life scenarios, with the suggested converter achieving a remarkable 94.3% maximum efficiency during voltage transfer. The MATLAB software serves as the principal tool for conducting primary simulations and formulating the design equations for the circuit.

INDEX TERMS DC/DC converter, elevated gain, low input current, magnetically coupled.

NOMENCLATURE

A_e	Effective cross-section of magnetic core.
A_p	Product areas of magnetic core.
A_w	Effective window area of magnetic core.
B_{max}	Maximum flux density of core.
C_S	Snubber capacitor.
CS_Q	Maximum current stress of MOSFETs.
D	Duty cycle.
f_s	Switching frequency.
G	Voltage transfer ratio.
G_{1or2}	Gating signals.
I_g	Input current.
$i_L(t)$	Instantaneous current of inductor.
I_{L1}, I_{L2}	Primary current of transformers 1 and 2.
I_{out}	Output current.
I_{pk}	Peak of inductor current.
I_{rms}	Effective current of transformer primary windings.
J	Current density.
L_1 *and* L_2	Inductance of transformer 1 and 2.
l_e	Effective length of flux path in magnetic core.
n	Turn ratio of transformers.

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n_{1or2}	Primary or secondary turns of winding.
P_{core}	Power loss of magnetic core.
P_D	Power loss of diodes.
P_L	ESL power loss of inductors.
P_{out}	Output power.
P_{QC}	Conducting power loss of MOSFETs.
P_{QS}	Switching power loss of MOSFETs.
R_L	Load resistance.
r_{L1or2}	Equivalent primary resistance of transformer 1 and 2.
r_{Q1or2}	On-state resistance of the MOSFET 1 and 2.
R_S	Snubber resistor.
T_{f1or2}	Falling time of MOSFETs 1 and 2.
t_{r1or2}	Rising time of MOSFETs1 and 2.
T_s	Switching period.
$v_c(t)$	Instantaneous voltage of capacitor.
V_{clamp}	Clamp voltage of RCD circuit.
V_{coutx}	Voltage of the xth output Capacitor.
V_{cx}	Voltage of the xth Capacitor.
V_{D1toD8}	Voltage of diodes.
V_g	Input voltage.
V_{L1}, V_{L2}	Primary voltage of transformer 1 and 2.
V_{OR}	Reflected secondary voltage.
V_{out}	Output voltage.
VS_D	Maximum voltage stress of diodes.
VS_Q	Maximum voltage stress of MOSFETs.
$V_{SW1orSW2}$	Voltage of switches 1 and 2.
W_A	Wire cross section.
ΔI	Maximum current ripple of inductor.
ΔV	Maximum voltage ripple of capacitor.
μ_r	Relative magnetic permeability.

I. INTRODUCTION

By ever growing renewable energy exploitation e.g. wind and solar energies, use of power electronic converters have been significantly extended to transform the different current and voltage levels to a desired and a standard level. One popular type of converter, known as DC/DC converters, has found extensive utilization in numerous applications such as photovoltaic (PV) systems, wind turbines, and fuel cells. These converters play a crucial role in transforming an unregulated DC voltage into a regulated DC voltage [1], [2], [3], [4]. In industrial settings, the generated DC voltage level is often considerably lower than what is typically required for regular usage. In this regard, researchers have recently concentrated on proposal of elevated gain boost DC/DC converters [5], [6], [7], [8].

Elevated gain step-up DC/DC converters can be categorized based on several different aspects including number of active switches, isolation status, efficiency levels, boosting techniques, etc., [9], [10], [11], [12], and [13]. Various recent studies have focused on employing transformers with high-turn ratio to prepare an elevated gain converter for renewable energy [14], [15]. However, vital issues such as high switch stress, higher leakage inductance, winding losses and lower efficiency have been touched on [16]. Some costly and complex controlling algorithms as well as additional active switches for active clamping have been considered to tackle these problems in [17], [18], [19], and [20]. As an example in [21], Sigma converter has been proposed for reducing voltage stress in the active semiconductors at the expense of increasing the number of active switches. High frequency transformers in switching converters have been employed in order to increase the voltage conversion ration while isolation can be guaranteed. In addition to the isolated high-gain converters, non-isolated converters may employ different techniques to reach a desired voltage ratio conversion for ultra-low-voltage applications [10]. Some topologies including the coupled inductor-based and switched capacitor based have been significantly used in designing high gain DC/DC converters [1], [22]. Single-, dual-coupled inductor along with different boosting algorithms including voltage multiplier, and clamp circuits have been extensively used in DC/DC converters [23]. Although high gain capability occurs with these techniques, input discontinuous or large ripple current makes them encounter the accelerated failure or aging due to the large current stresses in the power semiconductor [24], [25]. In this regard, Effective solutions originating from current feeding techniques have been sought to mitigate this problem in high gain DC/DC converter [26], [27]. A soft switching included technique with a single switch structure has been proposed in [28]. Elevated voltage ratio, high efficiency, and low ripple input current have been achieved. However, the topology may not be a featured circuit for higher power applications in which the power devices should endure high current stresses leading to lower efficiency. The cross coupled inductors, as a solution, has been adopted to optimize the current stresses of the switches by applying additional power semiconductor [29]. In this structure, the current stresses can be minimized at the expense of the considerable source current ripple which may directly affect the converter's electromagnetic compatibility.

Not only does exploiting the interleaved topologies suppress the ripple of the input current, but increases the capability of the transferring higher power by diminishing the input current stresses [30]. Furthermore, magnetic component size will be decreased which subsequently lead to power density increase [31]. The quantity of components in transformer-based interleaved topologies is a significant disadvantage that contributes to increased converter costs and larger size.

This paper presents a novel structure for achieving high voltage ratios in boost DC/DC power converters, leveraging the benefits of various boosting techniques to enhance overall performance. The proposed converter introduces several key contributions that set it apart from previous methods.

Firstly, the converter incorporates a two-phase interleave inductor configuration, along with quasi switched capacitor and voltage multiplier stages. This combination enables the

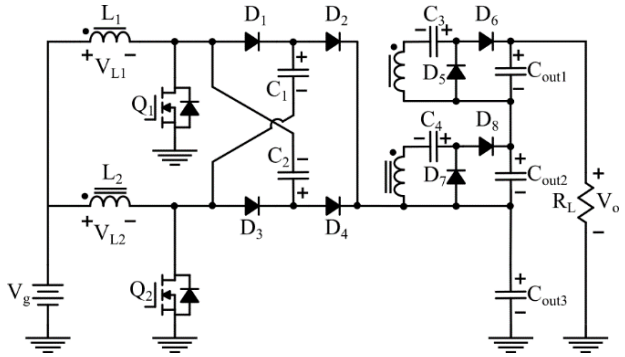

FIGURE 1. Schematic of the proposed elevated boost DC/DC power converter using multiphase input for suppressing the input current ripple with 180o phase shifted gate signals.

converter to achieve elevated voltage ratio conversion, surpassing the capabilities of conventional approaches.

Secondly, the interleaved technique contributes to reducing the input current ripple. By mitigating pulsating power drawn from the input source, this feature significantly extends the useful lifetime of the input source.

Another noteworthy advantage of the proposed converter is its utilization of a common ground among the input, output, and active switches. This configuration results in lower common noise and improved gate driving, enhancing the overall stability and performance of the converter.

In summary, the main contributions of this paper lie in the development of a new structure that enables high voltage ratio conversion, the incorporation of interleaved techniques for reduced input current ripple, and the utilization of a common ground for improved noise performance and gate driving. These advancements highlight the superiority of the proposed method and pave the way for more efficient and reliable high voltage ratio step-up DC/DC power converters.

Within the confines of this study, it is imperative to acknowledge two prominent limitations: the absence of an in-depth exploration into cost implications and the omission of a comprehensive reliability assessment. However, it is vital to underscore that our research impetus emanates from the innovative proposition of a novel topology, characterized by its remarkable efficiency and exceptional voltage ratio, thereby encompassing a broader aspiration within the realm of high-gain step-up DC/DC power converters tailored for low-voltage renewable energy applications.

The following sections of the paper are as follows: Section II deals with an explanation of the fundamental operating principle of the converter of interest. Section III focuses on the circuit design aspects, while Section IV presents the experimental results obtained from the implemented converter. The paper concludes with a summary and concluding remark in the last section.

II. OPERATION PRINCIPLE

Fig. 1 demonstrates the schematic of the introduced high voltage transfer ratio DC/DC converter. As it can be seen,

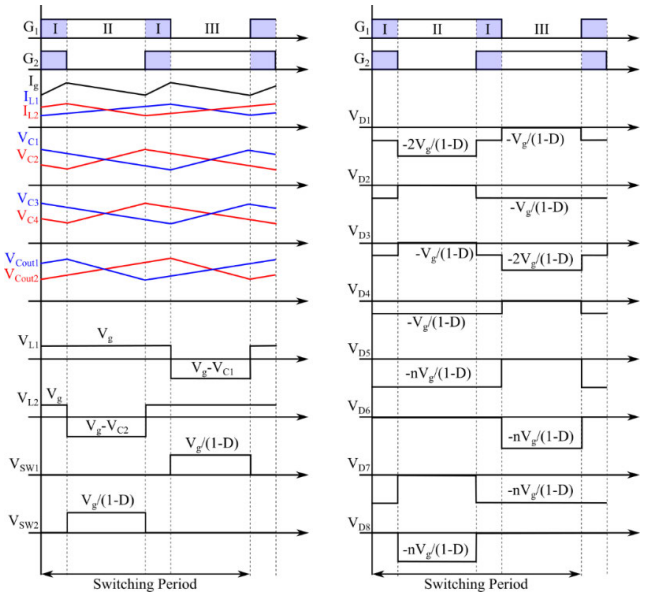

FIGURE 2. The essential waveforms of the DC/DC converter are as follows. Both active switches operate with an equal duty cycle but are phase-shifted by 180^o degrees to leverage the advantages of the interleaved technique. There exist three different operating modes.

there exist two parallel input paths which finally reach each other in series via different stepping up techniques. In order to optimize the impact of the magnetic circuit on enhancing the output voltage, a pair of coupled inductors has been utilized. The turn ratio is defined as $n=n_2/n_1$. Two capacitors i.e. C_1 and C_2 have been employed to constitute the switched capacitor method. As the last stage of voltage gaining, a voltage multiplier is supplied through the secondary side of the coupled inductors. The components indices and their polarities are indicated in the figure.

A. OPERATION STATE

The proposed converter has been controlled with phase shifted gate controlling signal for reducing the input current ripple. The steady state operation waveforms for a specific operating point is depicted in **Fig. 2**. The first two traces in this figure are related to the binary activation signals of Q1 and Q2 as the main active power semiconductors. The PWM gate controlling signals have the same switching frequency (f_{sw}) and duty cycle (D). The difference between the Q1 and Q2 gate signals is the 180^o delay, i.e. $T_{sw}/2$, in Q2 gate signal in order to take the advantage of interleaved pattern for minimizing the input current pulsating. By manipulating the duty cycle of the switches, the converter can attain a desired voltage transfer ratio. As shown in **Fig. 2**, there exist three different operating modes corresponding to the switching state of the active devices. These modes of operating shown in **Fig. 3** are discussed as follows.

Mode I: in this operating mode as illustrated in **Fig. 3a**, both switches turn and keep on (overlapped). Thus, the magnetizing inductors are being charged through the active switches

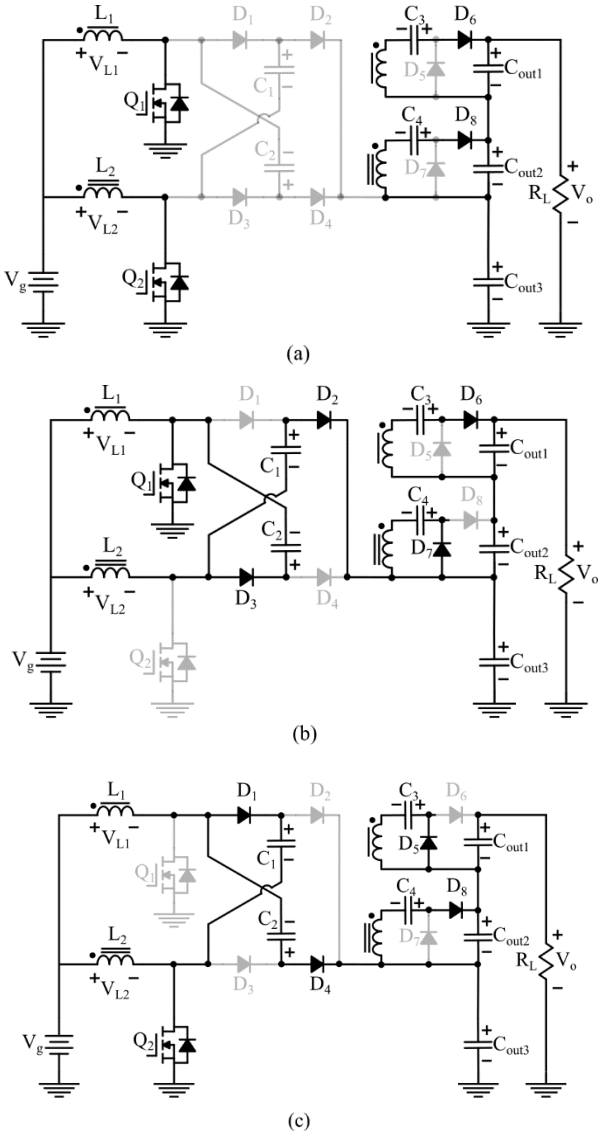

FIGURE 3. The converter of interest can be represented by an equivalent circuit in different operating modes: a) Mode I, b) Mode II, and c) Mode III.

and the input voltage. Since two parallel paths are included at the input, the input power supply may tolerate less pulsating current extraction which can improve its performance and reliability. The output capacitors, namely C_{out1} and C_{out2}, are charged through the capacitors C_3 and C_4 and the secondary windings of their associated coupled inductors, respectively. Simultaneously, the output load is supplied with all three output capacitors at the output. During this specific time period, the charging of capacitors charges through the discharge of capacitors C_3 and C_4.

Mode II: in this mode of operation as illustrated in **Fig. 3b**, Q_1 is continuously on while Q_2 is off. The inductor L_1 continues its charging from the input power supply V_g. However, the inductor L_2 discharges its absorbed energy via two different paths. In the first path, the input voltage as well as the inductor L_2 charge the capacitor C_2 via D_3 and Q_1. In the second path, the input voltage, the inductor L_2 as well as the capacitor C_1 charge the capacitor C_{out3} via D_2. The secondary winding of inductor L^2, facilitated by diode D_7, enables the charging of capacitor C_4. Similarly, the charging of output capacitor C_{out1} charges via the secondary part of inductor L_1 as well as capacitors C_3. Throughout this time interval, all the output capacitors contribute to supplying the output energy.

Mode III: in this operating mode as depicted in **Fig. 3c**, Q_2 turns on while Q_1 turns off. The input power supply V_g continues the inductor L_2 charging. However, the inductor L_1 discharges its absorbed energy via two different paths. In the first path, the input voltage as well as the inductor L_1 charge the capacitor C_1 via D_1 and Q_2. Through the second pathway facilitated by diode D_4, capacitor C_{out3} receives its charge from the input voltage, inductor L_1, and capacitor C_2. Capacitor C_3 gets charged through diode D_5 by inductor L_1. Similarly, the charging of output capacitor Cout2 is achieved through the use of capacitors C_4 and inductor L_2. During this specific time interval, all the output capacitors are actively providing the output energy.

B. VOLTAGE GAIN DERIVATION

In this section, For analyzing the continuous conduction mode (CCM) operation will be discussed. In this case, one can assume that the ripple of the inductor currents are not as high as reaching zero current in their discharging mode. Therefore, **Fig. 2** and **Fig. 3** do not introduce any additional operating modes. With the assumption that output capacitors are high enough to supply the output energy during the normal operating, three states can be defined for describing the circuit as follows.

1) STATE I

In this state, inconsidering the turning off delay of the power MOSFETS (Q_1 and Q_2), both active switches are on. Accordingly, following equations can be derived for the magnetizing inductors voltages:

$$V_{L1} = V_{L2} = V_g \tag{1}$$

where V_g is the input voltage. The capacitors voltages are given as follows in this state:

$$\begin{aligned} V_{Cout1} &= nV_{L1} + V_{C3} = nV_g + V_{C3} \\ V_{Cout2} &= nV_{L2} + V_{C4} = nV_g + V_{C4} \\ V_{out} &= V_{Cout1} + V_{Cout2} + V_{Cout3} \end{aligned} \tag{2}$$

where $n=n_2/n_1$ is the turn ratio of the coupling inductors.

2) STATE II

Switch Q_2 turns off in this state while the switch Q_1 is still on. Regarding **Fig. 2** and **Fig. 3** which are showing the essential waveforms and the equivalent circuit, inductors' voltages are

given by

$$V_{L1} = V_g$$
$$V_{L2} = V_g - V_{C2} \quad (3)$$

The voltages across the capacitors can be determined in the following manner:

$$V_{C3} = n(V_g - V_{C2})$$
$$V_{Cout3} = V_{C1} + V_{C2}$$
$$V_{out} = V_{Cout1} + V_{Cout2} + V_{Cout3} \quad (4)$$

3) STATE III

In this state, switch Q_1 turns off while the switch Q_2 is still on. Regarding **Fig. 2** and **Fig. 3** which are showing the essential waveforms and the equivalent circuit, the inductors' voltages are given by

$$V_{L1} = V_g - V_{C1}$$
$$V_{L2} = V_g \quad (5)$$

The capacitors voltages can be derived as follows:

$$V_{C4} = n(V_g - V_{C1})$$
$$V_{Cout3} = V_{C1} + V_{C2}$$
$$V_{out} = V_{Cout1} + V_{Cout2} + V_{Cout3} \quad (6)$$

Considering the equations mentioned above, one can obtain the voltage transfer ratio by considering the principle of voltage-second balance [1] to the inductors, as shown in equations (1), (3), and (5):

$$DV_g + (1-D)(V_g - V_{C1}) = 0 \rightarrow V_{C1} = \frac{V_g}{1-D}$$
$$DV_g + (1-D)(V_g - V_{C2}) = 0 \rightarrow V_{C2} = \frac{V_g}{1-D} \quad (7)$$

In which D represents the duty cycle of the active devices. Considering a constant voltage for the capacitor and handling (2), (4) and (6), capacitors' voltages yield as follows:

$$V_{C3} = n(V_g - V_{C2}) = nV_g(1 - \frac{1}{1-D}) = \frac{nDV_g}{1-D}$$
$$V_{C4} = n(V_g - V_{C1}) = nV_g(1 - \frac{1}{1-D}) = \frac{nDV_g}{1-D} \quad (8)$$

And

$$V_{Cout1} = nV_g + V_{C3} = nV_g(1 + \frac{D}{1-D}) = \frac{nV_g}{1-D}$$
$$V_{Cout2} = nV_g + V_{C4} = nV_g(1 + \frac{D}{1-D}) = \frac{nV_g}{1-D}$$
$$V_{Cout3} = V_{C1} + V_{C2} = \frac{2V_g}{1-D} \quad (9)$$

The voltage at the output terminal is derived as follows:

$$V_{out} = V_{Cout1} + V_{Cout2} + V_{Cout3} = \frac{2nV_g}{1-D} + \frac{2V_g}{1-D}$$
$$= 2V_g(\frac{1+n}{1-D})$$
$$G = \frac{V_{out}}{V_g} = 2(\frac{1+n}{1-D}) \quad (10)$$

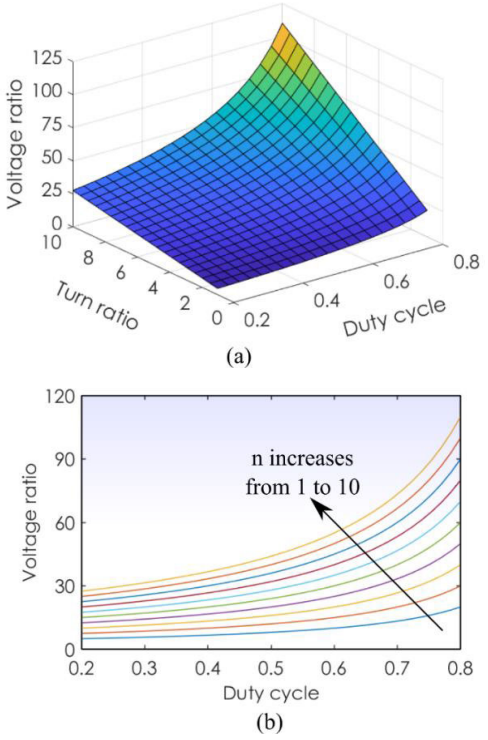

FIGURE 4. The voltage gain of the converter of interest can be represented as a function of two parameters: the turn ratio of the coupled inductor and the duty cycle. This relationship can be visualized through a) a three-dimensional plot, and b) a projected two-dimensional plot.

Regarding the equations mentioned above, output voltage is obviously impressed by two separated parameters i.e. D and n. To provide a clearer understanding, the voltage ratio (VR) is depicted in Fig. 4a, showcasing its dependence on both turn ratio of the magnetically coupled inductors and the duty cycle. The turn ratio (n) plays a key role in considering the value of the voltage transfer ratio in the converter. Regarding the application and the required voltage conversion ratio, $n=n_2/n_1$, can be chosen in the predesign stage of the power converter.

In **Fig. 4b**, the voltage transfer ratio is depicted with the duty cycle variation and with the turn ratio (n) taken into account as a parameter. The voltage gain of the converter of interest demonstrates a significant increase as the duty cycles of the switches are increased. This observation reflects the fact that an increase in duty cycle (D) results in more energy being stored in the input coupled inductors, leading to a higher energy transfer to the load. Moreover, the turn ratio of the inductors directly influences the voltage transfer ratio. A higher turn ratio corresponds to a higher voltage conversion ratio. Since the turn ratio is predetermined as a design parameter, the voltage at the output can be adjusted by manipulating the duty cycles of the active switches (Q_1 and Q_2) while accounting for variations in the load and input voltage. Thus, the duty cycle can be tuned to alleviate for the effects of variations in the input voltage and load.

TABLE 1. Performance comparison of different topologies.

Topology	Voltage conversion ratio (V_o/V_g)	Switch voltage stress (VS/V_g)	No. of components			No. of inductors		Maximum reported efficiency	Input current ripple ($\Delta I_{in}/I_{in}$)	Common ground
			switches	diodes	capacitors	single	Coupled			
Proposed converter	$2(\frac{1+n}{1-D})$	$\frac{G}{2(1+n)}$	2	8	7	0	2	94.1%	28%	Yes
Proposed in [23]	$2\left(\frac{1+n}{1-D}\right)$	$\frac{G}{2+n}$	4	2	4	0	2	95.2%	23%	No
Proposed in [31]	$\frac{2+n}{1-D}$	$\frac{G}{2+n}$	2	4	3	2	1	94.0%	45%	Yes
Proposed in [32]	$\frac{3+5D}{1-D}$	$\frac{1+G}{4}$	2	9	3	4	0	94.1%	37.5%	No
Proposed in [33]	$\frac{3+nD}{1-D}$	$\frac{n+G}{n+3}$	2	4	5	0	1	92.0%	150%	Yes
Proposed in [34]	$\frac{nD}{1-D}$	$\frac{G}{n}$	2	2	6	4	2	91.0%	50%	Yes
Proposed in [35]	$\frac{5+D}{1-D}$	$\frac{1+G}{2}$	1	7	6	4	0	92.2%	200%	No
Proposed in [36]	$2\left(\frac{1+n}{1-D}\right)$	$\frac{G}{2+n}$	4	2	3	0	2	96.1%	32%	Yes
Proposed in [37]	$\frac{4}{1-D}$	$4G$	2	8	6	2	0	93.3%	37.5%	No
Conventional boost Converter	$\frac{1}{1-D}$	G	1	1	1	1	0	98.0%	30%	Yes

C. VOLTAGE AND CURRENT STRESSES

The maximum voltage stress (VS) experienced by the active switches has a crucial role in determining the performance of the switching converter. In the primary design stage, gaining information about the maximum voltage stress is important in MOSFET selection and affects the final cost of the whole system. Secondary, the maximum stress voltage directly impacts the efficiency of the converter. In simpler terms, achieving a lower maximum voltage stress on the active switch leads to higher efficiency. Therefore, it is significant to estimate the maximum voltage stress experienced by the switches. Regarding **Fig. 2** and **Fig. 3**, one can find that that the maximum blocking voltage can be obtained as the following equation:

$$VS_{Q_1,Q_2} = \frac{V_g}{1-D} = V_g\frac{G}{2(1+n)} \tag{11}$$

and for the power diodes are calculated as

$$\begin{aligned} VS_{D_1,D_3} &= \frac{2V_g}{1-D} = V_g\frac{G}{(1+n)} \\ VS_{D_2,D_4} &= \frac{V_g}{1-D} = V_g\frac{G}{2(1+n)} \\ VS_{D_5-D_8} &= \frac{nV_g}{1-D} = V_g\frac{nG}{2(1+n)} \end{aligned} \tag{12}$$

The maximum current stresses (CS) of the active devices, namely Q_1 and Q_2 are important in the MOSFET selection process as the most important active component in DC/DC converter. Based on **Fig. 2** and the aforementioned equations, the current stress on the switches can be determined as follows:

$$\begin{aligned} CS_{Q_1,Q_2(avg)} &= \frac{DGI_{out}}{2} \\ CS_{Q_1,Q_2(rms)} &= \frac{GI_{out}}{2}\sqrt{1+\left(\frac{1}{3}\right)\left(\frac{\Delta i_{L_1,L_2}}{GI_{out}}\right)^2} \end{aligned} \tag{13}$$

D. PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER

Investigation of the various aspects of the converter may be helpful to express its advantages. In this regard, two important factors, namely voltage transfer ratio (G) and maximum voltage stress (VS) of the active devices, will be discussed. Hence, this comparison encompasses diverse elevated DC/DC power converters, as well as the conventional DC/DC boost converter. **Table 1** presents the specifications of these high-gain DC/DC power converters. It is evident that the proposed converter stands out by offering a significantly reduced the input current ripple, thanks to the interleaved technique. Interestingly, some of the converters mentioned in the list exhibit higher input current despite employing a larger number of active switches. In the converters in which single active switch was used, the amount of current ripple at the input stage is significant which finally may accelerate

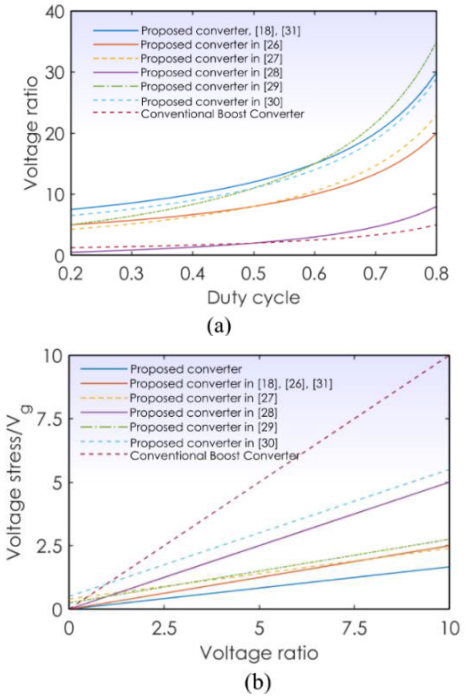

FIGURE 5. Characterization of recent converters including the proposed one, a) voltage ratio, b) voltage stress of the active switches with respect to the input voltage.

the degradation of the input supply. Additionally, the active switches are common ground which make the gate driving circuit as simple as possible. In the high-gain DC/DC converter design that is proposed, two common ground switches are present. When referring to Table 1, it becomes evident that the gain of the converter of interest surpasses that of the majority of other high-gain converters. This observation is further supported by **Fig. 5a**, which visually represents the voltage ratio of the compared high-gain converters. The turn ratio was considered as n=1:2. The proposed converter demonstrates the feasibility of providing high gain transfer ratio compared to other recent topologies. For D<0.6, the converter is leading in regards of voltage transfer ratio, while the proposed converter in [32] shows better performance beyond duty cycle of 0.6. As depicted in **Fig. 5b**, the performance of the converter regarding the induced stress on the devices surpasses that of other recently proposed converters. This indicates that, for a given voltage transfer ratio, the voltage stress on the active switches is minor comparing with others. In other words, one can choose a lower voltage power switch which can significantly decrease the cost. Furthermore, the lower voltage stress of the active devices results in improved efficiency.

III. CIRCUIT DESIGN

Design considerations and equations of power converters are crucial aspects that significantly influence their overall performance. These factors not only impact the converter's efficiency but also play a vital role in mitigating potential issues like electromagnetic interference, which can affect the proper functioning of other electronic devices in the vicinity. In the initial stage of circuit design for power systems, it is essential to take into account the specific application requirements and relevant industry standards. These considerations set the foundation for creating a reliable and effective power converter that meets the desired specifications. One of the critical aspects in designing power converters is determining the appropriate values of inductances and capacitances for various components within the circuit. To achieve this, careful consideration is given to the current ripples for inductors and voltage ripples for capacitors. By analyzing and understanding these ripples, engineers can select suitable inductance and capacitance values that will result in stable and efficient converter operation. Consequently, meticulous design considerations, incorporating equations and an in-depth analysis of current and voltage ripples, are essential in the successful development of power converters.

A. COUPLED INDUCTOR DESIGN

In **Fig. 2**, a particular scenario is depicted, showing the behavior of input inductors during the switch activation period. Understanding these voltage characteristics is crucial as it helps engineers to optimize the performance of the converter during the switching process. By analyzing the voltage behavior of input inductors, designers can make informed decisions regarding component selection and switching strategies, thereby enhancing the converter's overall efficiency and performance. Thus

$$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = V_g \tag{14}$$

Accordingly, one can calculate the inductance of the input inductors as follows:

$$L_1 = L_2 = \frac{V_g D}{f_s \Delta I} \tag{15}$$

where f_s denotes the switching frequency and ΔI represents the maximum allowable inductor current ripple.

Since the values of inductances of the coupled inductors have been determined, it becomes feasible to calculate other crucial parameters essential for their successful design and implementation. One such critical parameter is the number of turns in each coil, particularly the number of primary turns, which significantly influences the overall performance of the coupled inductor. The calculation of the number of primary turns is of great significance as it directly affects the magnetic flux linkage and the transformation ratio of the coupled inductor. To calculate the number of primary turns (n_1) in the coupled inductor, certain design considerations must be taken into account. The primary objective is to achieve the desired inductance and ensure efficient power transfer. The following mathematical relationship is employed for this purpose:

$$n_1 = \frac{L_{1or2} I_{pk}}{A_e B_{\max}} \tag{16}$$

In the context of coupled inductors, the I_{pk} represents the peak current flowing through the primary side of these interconnected inductors, measured in Amperes. The parameters A_e and B_{max} correspond to the effective cross-sectional area of the magnetic core (extracted from core datasheet, here is ETD34/17/11), measured in square meters, and the flux density, and measured in Teslas, respectively. The magnetic permeability of the core can be determined using the following equation:

$$\mu_r = \frac{L_{1or2}\ell_e}{n_1^2 A_e \mu_0}$$
$$\ell_g \cong \frac{\ell_e}{\mu_r} \tag{17}$$

where ℓ_e and ℓ_g denote the effective magnetic path of the core (extracted from core datasheet) and the necessary air gap introduced to prevent saturation. The wire cross section (W_A) can be calculated as

$$W_A = \frac{I_{rms}}{J} \tag{18}$$

where I_{rms} symbolizes the root mean square current flowing through the winding, and J denotes the current density, a parameter taken as 4.5 Amperes per square millimeter. During this critical phase, the suitability of the chosen magnetic core is assessed by calculating the product of areas (A_p). This analysis ensures the coupled inductor design meets the desired performance and efficiency for various applications.

$$A_P = A_e A_w = \frac{L_1 I_{pk} \sum_{i=1}^{2} \frac{n_i}{n_1} I_{rms,i}}{B_{\max} J k} \tag{19}$$

where the filling factor k is assigned a value of 0.7 for this particular design. The calculated product of areas (AP) is then compared to the product areas specified in the datasheet. The design process concludes once the comparison is completed, ensuring that the desired criteria and requirements have been met, namely $A_P^{calculated} < A_P^{datasheet}$.

B. CAPACITOR DESIGN

In the domain of DC-DC converter design, capacitor charge balance analysis emerges as a fundamental and widely applied technique for determining optimal capacitance values while adhering to prescribed constraints. Specifically, this method plays a pivotal role in calculating suitable capacitance values for output capacitors, which are vital components responsible for the reliable supply of output current during their discharging mode. Mathematically, the output capacitor charge balance equations are expressed as follows:

$$C_{out1}\frac{dv_{Cout1}}{dt} = C_{out2}\frac{dv_{Cout2}}{dt} = I_{out}$$
$$C_{out3}\frac{dv_{Cout3}}{dt} = I_{out} \tag{20}$$

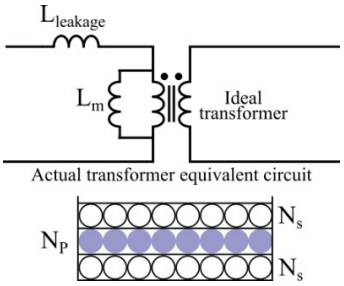

FIGURE 6. A transformer sandwich structure was devised in the design to minimize the leakage inductance of the inductor. This approach aims to address electromagnetic interference (EMI) concerns and reduce voltage ringing on the MOSFET.

Therefore, the computation of the output capacitance is accomplished as follows:

$$C_{out1} = C_{out2} = \frac{P_{out} D}{V_{out} f_s \Delta V}$$
$$C_{out3} = \frac{P_{out}\,(2D-1)}{V_{out} f_s \Delta V} \tag{21}$$

In this context, the term ΔV refers to the acceptable voltage ripple, while P_{out} signifies the output loading power. It becomes evident that as the output power rises, the demand for larger capacitors becomes imperative to effectively deliver the desired output voltage within the permissible voltage ripple limits. The relationship between output power and capacitor size is intricately intertwined with the need to maintain stable voltage levels during load variations. As the output loading power increases, so does the magnitude of the voltage fluctuations. Consequently, larger capacitors are indispensable to counteract these fluctuations and preserve the output voltage within the predefined voltage ripple tolerance.

C. SNUBBER CIRCUIT DESIGN

In the realm of power DC/DC converter design, a critical factor to be mindful of is the configuration of the snubber circuit. The primary objective of this circuit is to alleviate the occurrence of voltage spikes across the MOSFETs, which stem from the accumulation of energy in the leakage inductance of the inductors. The presence of such voltage spikes necessitates the implementation of effective measures to ensure both the proper functionality and reliability of the converter. A paramount approach to address this issue involves the mitigation of the leakage inductance in the inductor. To achieve this, the implementation of a sandwich magnetic structure (as depicted in **Fig. 6**) has been identified as a promising solution. By adopting this methodology, the undesired effects of leakage inductance can be significantly minimized, leading to improved performance and enhanced operational robustness of the DC/DC converter system.

A consolidated approach involving the utilization of an RCD (Resistor-Capacitor-Diode) snubber circuit presents a compelling strategy for dissipating the stored energy stemming from leakage inductance. This method stands in contrast to relying on the parasitic capacitance of the MOSFETs

[38], [39]. The conventional RCD circuit, shown in **Fig. 7** and operating in conjunction with the coupled inductor, effectively facilitates the transfer of stored energy to the appropriately designed RCD circuit, thereby mitigating the occurrence of ringing phenomena across the power MOSFET.

Throughout the conduction phase of the power MOSFETs, both magnetizing and leakage inductances play a role in accumulating energy in a magnetic form. Subsequently, during the off-period of the MOSFETs, the stored energy is transferred to the output windings. To prevent voltage ringing across the power MOSFET, it becomes crucial to dampen the stored energy associated with the leakage inductance. In this scenario, capacitor C_S charges through diode D_S until reaching the clamp voltage (V_{Clamp}). Once this threshold is reached, diode D_S turns off, leading to the discharge of capacitor C_S to resistor R_s.

The determination of optimal values for the snubber parameters becomes instrumental in reducing power consumption in the RCD circuit and the power MOSFET, while simultaneously enhancing the reliability of the power MOSFET [40]. By carefully optimizing these parameters, the consolidated approach ensures a superior performance and increased robustness in the operation of the power DC/DC converter system. Such advancements are crucial in addressing challenges associated with voltage spikes, energy dissipation, and overall system reliability in power electronics applications. Furthermore, it is worth noting that the implementation of the RCD snubber circuit presents an innovative and practical solution that complements the sandwich magnetic structure previously mentioned. Integrating these techniques fosters a comprehensive and sophisticated approach to tackle issues related to leakage inductance and its consequential effects on power converter performance. Continued research and experimentation in this domain hold significant promise for further advancements in power electronics design, paving the way for more efficient, reliable, and stable power DC/DC converters in various industrial and electronic applications. Based on the design procedure in [41] and [42], one can calculate the RCD parameters as follows:

$$R_S = \frac{2V_{clamp}(V_{clamp} - V_{OR})}{L_{leakage} I_{pk}^2 f_s}$$
$$C_S > \frac{V_{clamp}}{\Delta V_{clamp} R_S f_s} \tag{22}$$

where V_{OR}, I_{pk} and f_S are reflected secondary voltage, peak current of coupled inductors and switching frequency, respectively. By using this RCD circuit, the ringing voltage on the power MOSFETs would be decayed and no significant overvoltage would suffer the MOSFETs.

IV. POWER LOSS ANALYSIS

The power dissipation across various components in the proposed DC-DC converter plays a crucial role in determining overall efficiency. To thoroughly assess the converter's performance, a rigorous examination of power loss for each individual device is conducted, and the cumulative losses are then computed. While the capacitors exhibit relatively small voltage ripple, their influence on the total power loss is deemed insignificant. Conversely, the inductors are subject to heating energy dissipation due to their equivalent series resistance, rendering their contribution to power loss more significant. Consequently, a meticulous approach is adopted to account for these individual shares in the comprehensive power loss calculation. Undoubtedly, the active components hold greater responsibility in power loss generation. Understanding the power dissipation characteristics of the active components enables us to optimize their performance and efficiency in the DC-DC converter design. By comprehensively examining power loss contributions from each component, we can identify potential areas for improvement and make informed decisions to enhance overall converter efficiency. As such, the investigation of the proposed topology's efficiency involves the consideration of two primary types of power losses: conducting and switching losses [43], [44]. Analyzing these losses provides valuable insights into the converter's energy efficiency and performance. For the power MOSFETs, the power dissipation formula is expressed as follows:

$$P_{QC} = r_{Q1} I_{rms,Q1}^2 + r_{Q2} I_{rms,Q2}^2$$
$$P_{QS} = \frac{f_s}{2}\left\{V_{Q1} I_{Q1}\left(t_{r1} + t_{f1}\right) + V_{Q2} I_{Q2}\left(t_{r2} + t_{f2}\right)\right\} \tag{23}$$

P_{QC} and P_{QS} represent the conducting and switching power losses, respectively. The on-state resistance and root mean square of power MOSFETs are denoted by r_Q and I_{rms}, respectively, while the falling and rising times of switches are represented as t_f and t_r, respectively.

The power loss arising from the diodes and inductors can be determined using the following calculation:

$$P_D = \sum_{j=1}^{8} \left\{V_{Dj} I_{ave,Dj} + r_{Dj} I_{rms,Dj}\right\} \tag{24}$$
$$P_L = I_{rms,L1}^2 r_{L1-eq} + I_{rms,L2}^2 r_{L2-eq} \tag{25}$$

P_D and P_L are the diodes and inductor power losses. r_D and r_{L-eq} denote the on-state diode resistance and the equivalent resistance of the coupled inductor on the primary side, respectively.

Another important factor in power loss calculation of any converter is the magnetic loss. Core loss refers to the energy dissipation within the magnetic core of an inductor due to alternating magnetic fields generated by the current passing through the windings. It encompasses hysteresis and eddy current losses, impacting the inductor's efficiency and temperature rise during operation. Minimizing core losses is crucial for improving overall inductor performance and efficiency in various electronic applications. Inductor designers consider factors like core material, shape, operating frequency, and magnetic field to optimize designs and reduce losses. The core loss can be extracted from datasheet of core (especially, figure of merit) based on the core type, shape, frequency, maximum flux density, temperature etc. Accordingly,

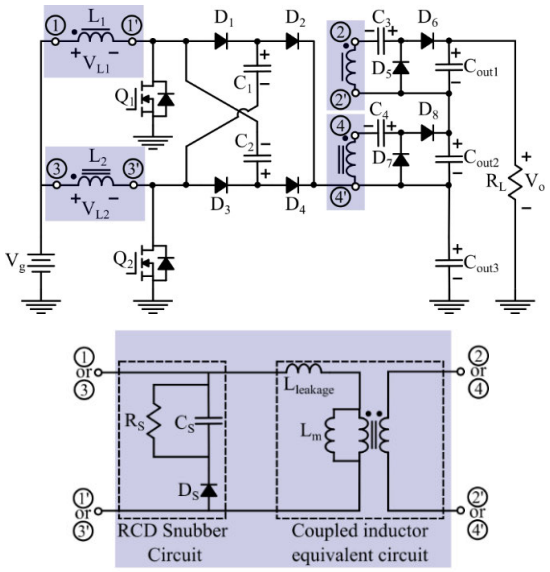

FIGURE 7. RCD snubber circuit connected across the power MOSFETs for suppressing the voltage spike across the MOSFETs originated from the leakage inductance of coupled inductor.

the total power loss can be calculated as

$$P_{Loss} = P_{QC} + P_{QS} + P_D + P_L + P_{core} \tag{26}$$

where P_{core} is the loss dissipated in the magnetic cores of the inductors.

V. EXPERIMENTAL PROCEDURE

To evaluate the converter performance in various aspects, a prototype setup was designed and implemented. The experimental validation utilized a 200W setup, as demonstrated in **Fig. 8**. It is considered to provide the voltage of 400V as the primary interface of a PWM DC-AC inverter for low power application e.g. PV and FC systems. The design of the converter of interest aims to boost the voltage from a range of 20V-30V to 400VDC, specifically for on-grid applications operating at 230Vac. Several aspects including electromagnetic interference (EMI), transformer design, MOSFET power losses, snubber circuit and reliability are practically important in DC/DC power converter designing. As the EMI perspective, numerous parameters including PCB structure and shielded inductors are paramount of importance. In this converter, a sandwich structure was chosen for coupled inductors in order to minimize the EMI effects and leakage inductance as shown in **Fig. 6**. This type of transformer winding reduces the leakage inductance since the magnetic flux generated by two windings are more interfered.

This finally can lead to higher electromagnetic compatibility and mitigating the EMI issues. In addition, the switching frequency may directly affect the EMI in the DC/DC power converter. Accordingly, a switching frequency of 60kHz was selected as a tradeoff between the EMI mitigation and passive components sizes.

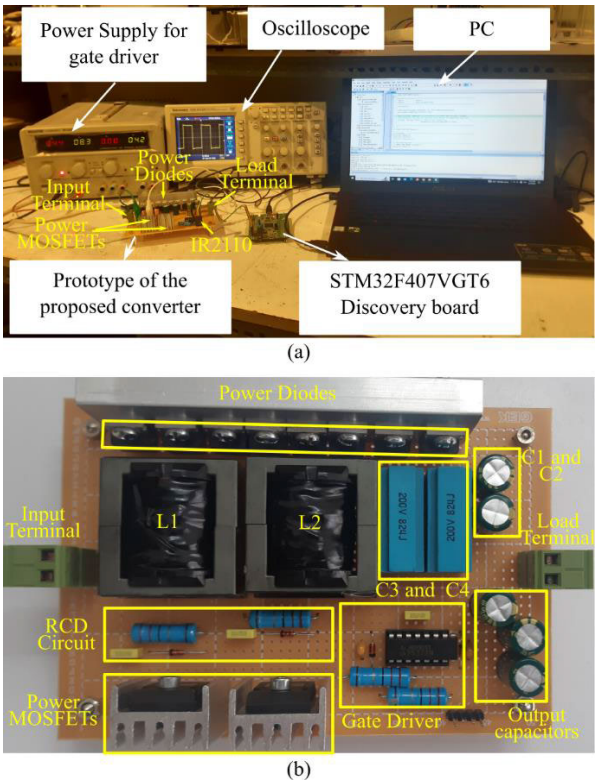

FIGURE 8. Prototype for the proposed elevated gain DC/DC power electronic converter. STM32F407VGT6 discovery board is used for creating the gate signals.

VI. RESULTS AND DISCUSSION

We will discuss the experimental waveforms and values obtained from the prototype that was designed and implemented in the previous section. The converter of interest has been designed to provide a 400V output voltage, serving as the primary interface for a PWM DC-AC inverter in applications requiring low power. The objective is to elevate the voltage from a range of 20V-30V to 400V for 230Vac applications. Based on equation (10), a duty cycle ranging from 0.55 to 0.7 is required to regulate the output voltage across different input voltage ranges and under varying load conditions, assuming a turn ratio of 2 for the coupled inductors. The components of the converter have been designed to limit the inductor current ripple to 0.5A and the capacitor voltage ripple to 2V. The switching frequency has been set at 60kHz, striking a balance between the size of the passive components and EMI considerations. Taking into account these constraints, as well as induced stresses on the power semiconductor, the components for the converter of interest can be designed as listed in **Table 2**.

The experimental essential waveforms of the proposed high gain power converter for different input voltages under full loading conditions are illustrated in **Fig. 9**. It shows the waveforms while input voltage is in its maximum value i.e. $V_g = 30V$. In this condition, the maximum duty cycle namely D=0.55 is required in order to reach 400V at the output

TABLE 2. The following are the specifications of the designed components for the proposed converter.

Component	Type	Rating	Manufacturer	Model/Part Number
Q_1 and Q_2	N-channel, Enhancement	33A, 200V	Infineon Technologies	IRFP250NPBF
D_1-D_8	Schottky	20A, 200V	International Rectifier	MBR20200CT
L_1 and L_2	Transformer	L_m=550uH, 10A N_1=170T W_1=1.6mm^2 N_2=340T W_2=0.5mm^2	-	-
Core	power ferrite material	B_{max}=0.5T H_{max}=14A/m P_{loss}=650 kW/m^3	Magnetics	ETD34/17/11 A_e=96.6mm^2 L_e=79.1mm V_e=7635mm^3
C_1-C_2	Electrolytic	3.3μF, 200V	Jiangxi Jia Wei Cheng Electronic	LF3.3M2GBKJ0812VGN
C_3-C_4	Film	820nF, 200V	Xiamen Faratronic Co	PCM824J
C_{out1}-C_{out3}	Electrolytic	4.7μF, 200V	Jiangxi Jia Wei Cheng Electronic	LF4.7M2GBKJ0812VGN

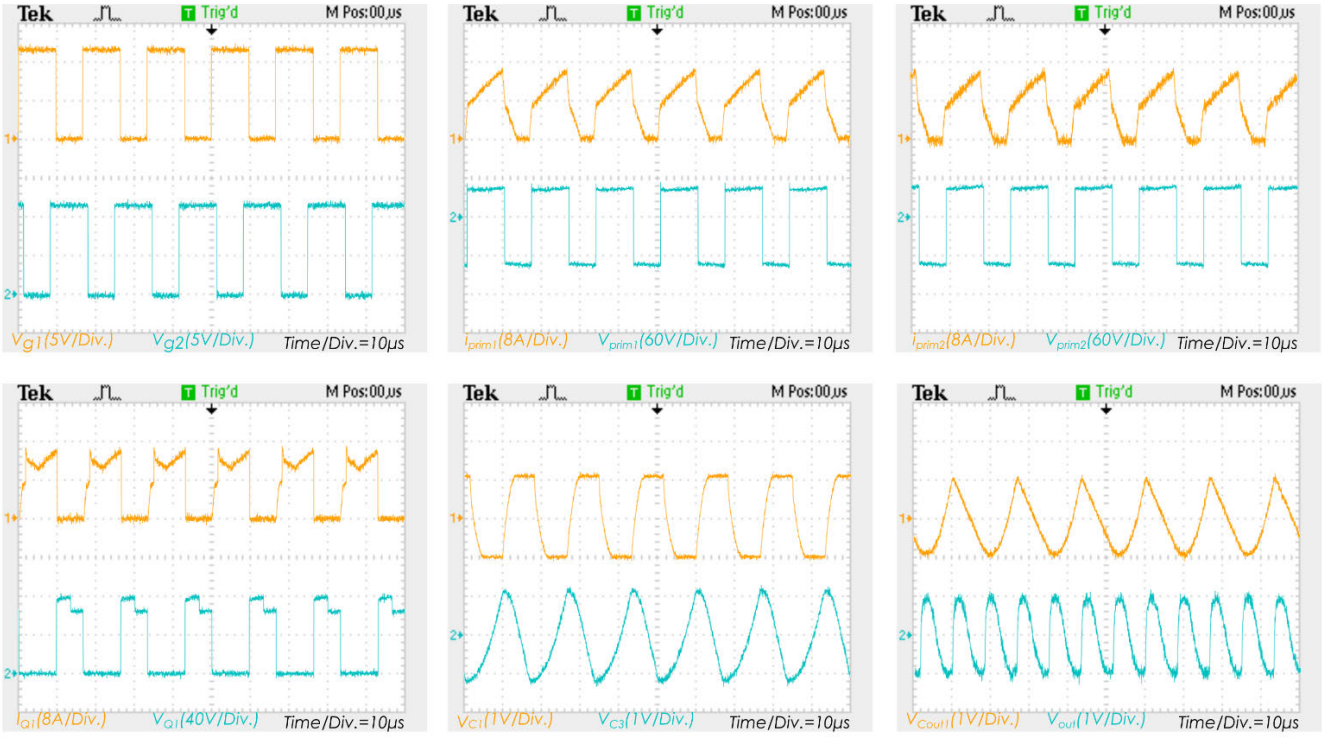

FIGURE 9. Experimental essential waveforms of the proposed converter in the maximum input voltage (Vg=30V).

under full loading conditions. The equivalent load resistance is 800Ω. The gate signals for triggering the MOSFETs are illustrated in **Fig. 9a**. From this figure, one can observe that there exists a half cycle delay between these two gate signals for satisfying the operational characteristics and effectiveness of the proposed power converter. The gate signals are created using a common gate driving circuit in which a 8V power supply is used in order to activate the MOSFETs. Primary voltage and current of coupled inductors (L_1 and L_2) are illustrated in **Fig. 9b** and **Fig. 9c**. The waveforms are similar to each other as expected while there only exists a 180-phase delay. During conducting period, input energy is saving in the coupled inductors via magnetic fields. The upward trajectory of the primary currents in the inductors indicates energy conservation within the magnetic core of the inductors. During the period in which the switches are off, the saved energy transfers to the output. The capacitors voltages are drawn in **Fig. 9e** and **Fig. 9f**. Regarding these waveforms, one can find that the maximum allowable ripples (2V) are occurred during normal working which guarantee the circuit design procedure.

Analysis of the converter's efficiency was conducted to evaluate its performance under various operating conditions. The measurements encompassed different loading scenarios and input voltages, providing valuable insights into the converter's behavior.

Fig. 10 presents the measured efficiency results, which shed light on the converter's performance characteristics. Three distinct input voltages were examined: 20V, 25V, and 30V. To maintain an output voltage of 400V, the duty cycles were adjusted accordingly.

The efficiency of the converter varied across different input voltages, with the highest measured efficiency of 94.2% achieved at the maximum input voltage (Vg=30V), while

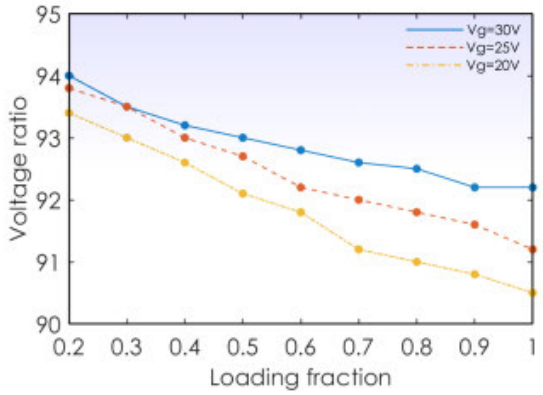

FIGURE 10. The efficiency of energy conversion at an output voltage of 400V, plotted against the output power, for various input voltage levels.

the minimum measured efficiency of 90.5% was observed at the lowest input voltage (Vg=20V). This discrepancy is attributable to the higher duty cycle requirements at lower input voltages, resulting in increased conduction losses within the power MOSFETs.

Furthermore, the efficiency of the converter demonstrated a decreasing trend as the load resistance was increased, indicative of higher loading conditions. This decline in efficiency can be attributed to the elevated current drawn from the input supply, leading to increased losses across both active and passive components. The increased power dissipation in the active switches and the associated losses contribute to the lower overall efficiency.

Taken together, these findings emphasize the importance of considering the interplay between input voltage, loading conditions, and efficiency in the design and optimization of high-gain power converters. While the measured efficiencies fall within an acceptable range, further analysis and fine-tuning may be required to optimize the converter's performance for specific real-time applications, accounting for the desired input voltage range and expected loading conditions.

VII. CONCLUSION

This research paper shows an innovative DC/DC converter with an elevated voltage gain. By integrating switched capacitor and switched inductor energy-saving systems, the proposed converter achieves exceptional performance. Thorough investigations were carried out to gain a comprehensive understanding of the functional principles of the converter of interest. Experimental results confirm the anticipated improvements, including elevated gain voltage conversion, low input current ripple, and high efficiency. Notably, the converter demonstrates maximum efficiency of 94.2% under light load conditions and at the highest input voltage. Comparing it with recent topologies further validates the superior performance of the introduced converter. Based on these findings, the introduced converter emerges as a highly promising solution for various low-power applications, including fuel cell and photovoltaic systems.

In conclusion, this paper presents a state-of-the-art ultra-high voltage transfer ratio DC/DC converter. By incorporating both switched capacitor and switched inductor systems, it achieves remarkable performance. The expected improvements in voltage conversion capability, input current ripple, and efficiency have been validated through the experimental results. Importantly, it should be noted that the converter demonstrates its highest level of efficiency when operating under light load conditions and at the maximum input voltage. The contrast with recent topologies accentuates its exceptional performance, positioning it as a highly capable option for low-power applications including PV and FC systems. The authors are currently focusing on the dynamic assessment of the suggested converter and its control strategy, both of which will be discussed in forthcoming reports.

REFERENCES

[1] V. Samavatian and A. Radan, "A high efficiency input/output magnetically coupled interleaved buck–boost converter with low internal oscillation for fuel-cell applications: CCM steady-state analysis," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5560–5568, Sep. 2015, doi: 10.1109/TIE.2015.2408560.

[2] O. Abdel-Rahim and H. Wang, "A new high gain DC–DC converter with model-predictive-control based MPPT technique for photovoltaic systems," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 2, pp. 191–200, Jun. 2020, doi: 10.24295/CPSSTPEA.2020.00016.

[3] Q. Zhang, Z. Liu, X. Jiang, Y. Peng, C. Zhu, and Z. Li, "Experimental investigation on performance improvement of cantilever piezoelectric energy harvesters via escapement mechanism from extremely low-frequency excitations," *Sustain. Energy Technol. Assessments*, vol. 53, Oct. 2022, Art. no. 102591, doi: 10.1016/j.seta.2022.102591.

[4] Q. Zhang, C. Xin, F. Shen, Y. Gong, Y. Zi, H. Guo, Z. Li, Y. Peng, Q. Zhang, and Z. L. Wang, "Human body IoT systems based on the triboelectrification effect: Energy harvesting, sensing, interfacing and communication," *Energy Environ. Sci.*, vol. 15, no. 9, pp. 3688–3721, 2022.

[5] N. Swaminathan and Y. Cao, "An overview of high-conversion high-voltage DC–DC converters for electrified aviation power distribution system," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 4, pp. 1740–1754, Dec. 2020, doi: 10.1109/TTE.2020.3009152.

[6] A. M. S. S. Andrade, L. Schuch, and M. L. D. S. Martins, "Analysis and design of high-efficiency hybrid high step-up DC–DC converter for distributed PV generation systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3860–3868, May 2019, doi: 10.1109/TIE.2018.2840496.

[7] S. K. Purushothaman, D. Sattianadan, and K. Vijayakumar, "Novel compact design high gain DC–DC step up converter applicable for PV applications," *Sustain. Energy Technol. Assessments*, vol. 51, Jun. 2022, Art. no. 101720, doi: 10.1016/j.seta.2021.101720.

[8] Y. Wang, X. Wen, B. Gu, and F. Gao, "Power scheduling optimization method of wind-hydrogen integrated energy system based on the improved AUKF algorithm," *Mathematics*, vol. 10, no. 22, p. 4207, Nov. 2022.

[9] A. Amir, A. Amir, H. S. Che, A. Elkhateb, and N. A. Rahim, "Comparative analysis of high voltage gain DC–DC converter topologies for photovoltaic systems," *Renew. Energy*, vol. 136, pp. 1147–1163, Jun. 2019, doi: 10.1016/j.renene.2018.09.089.

[10] Y. Guan, C. Cecati, J. M. Alonso, and Z. Zhang, "Review of high-frequency high-voltage-conversion-ratio DC–DC converters," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 4, pp. 374–389, Oct. 2021, doi: 10.1109/JESTIE.2021.3051554.

[11] L. Ge, T. Du, C. Li, Y. Li, J. Yan, and M. Rafiq, "Virtual collection for distributed photovoltaic data: Challenges, methodologies, and applications," *Energies*, vol. 15, no. 23, p. 8783, Nov. 2022.

[12] M. R. Banaei and S. G. Sani, "Analysis and implementation of a new SEPIC-based single-switch buck–boost DC–DC converter with continuous input current," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10317–10325, Dec. 2018, doi: 10.1109/TPEL.2018.2799876.

[13] B. Zhu, F. Ding, and D. M. Vilathgamuwa, "Coat circuits for DC–DC converters to improve voltage conversion ratio," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3679–3687, Apr. 2020.

[14] Y. Hu, J. Wu, W. Cao, W. Xiao, P. Li, S. J. Finney, and Y. Li, "Ultrahigh step-up DC–DC converter for distributed generation by three degrees of freedom (3DoF) approach," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4930–4941, Jul. 2016, doi: 10.1109/TPEL.2015.2487821.

[15] Y. Cao, V. Samavatian, K. Kaskani, and H. Eshraghi, "A novel nonisolated ultra-high-voltage-gain DC–DC converter with low voltage stress," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2809–2819, Apr. 2017.

[16] M. H. Ahmed, A. Nabih, F. C. Lee, and Q. Li, "Low-loss integrated inductor and transformer structure and application in regulated LLC converter for 48-V bus converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 589–600, Mar. 2020, doi: 10.1109/JESTPE.2019.2952878.

[17] S. Sadaf, M. S. Bhaskar, M. Meraj, A. Iqbal, and N. Al-Emadi, "A novel modified switched inductor boost converter with reduced switch voltage stress," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1275–1289, Feb. 2021, doi: 10.1109/TIE.2020.2970648.

[18] F. M. Shahir, E. Babaei, and M. Farsadi, "Voltage-lift technique based nonisolated boost DC–DC converter: Analysis and design," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5917–5926, Jul. 2018, doi: 10.1109/TPEL.2017.2740843.

[19] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high-efficiency fuel-cell power-generation system with active-clamp flyback–forward converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 599–610, Jan. 2012, doi: 10.1109/TIE.2011.2130499.

[20] S. Liu, Z. Song, Z. Dong, Y. Liu, and C. Liu, "Generic carrier-based PWM solution for series-end winding PMSM traction system with adaptative overmodulation scheme," *IEEE Trans. Transport. Electrific.*, vol. 9, no. 1, pp. 712–726, Mar. 2023.

[21] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 48/1V Sigma converter voltage regulator module," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2017, pp. 2207–2212, doi: 10.1109/APEC.2017.7931005.

[22] S. Gao, Y. Wang, Y. Guan, and D. Xu, "A high step up SEPIC-based converter based on partly interleaved transformer," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1455–1465, Feb. 2020, doi: 10.1109/TIE.2019.2910044.

[23] M. Muhammad, M. Armstrong, and M. A. Elgendy, "A nonisolated interleaved boost converter for high-voltage gain applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 352–362, Jun. 2016, doi: 10.1109/JESTPE.2015.2488839.

[24] V. Samavatian, M. Fotuhi-Firuzabad, M. Samavatian, P. Dehghanian, and F. Blaabjerg, "Correlation-driven machine learning for accelerated reliability assessment of solder joints in electronics," *Sci. Rep.*, vol. 10, no. 1, p. 14821, Sep. 2020, doi: 10.1038/s41598-020-71926-7.

[25] U. M. Choi, F. Blaabjerg, S. Jørgensen, F. Iannuzzo, H. Wang, C. Uhrenfeldt, and S. Munk-Nielsen, "Power cycling test and failure analysis of molded intelligent power IGBT module under different temperature swing durations," *Microelectron. Rel.*, vol. 64, pp. 403–408, Sep. 2016, doi: 10.1016/j.microrel.2016.07.020.

[26] M. Forouzesh, K. Yari, A. Baghramian, and S. Hasanpour, "Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation," *IET Power Electron.*, vol. 10, no. 2, pp. 240–250, Feb. 2017.

[27] W. Hassan, D. D. Lu, and W. Xiao, "Single-switch high step-up DC–DC converter with low and steady switch voltage stress," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9326–9338, Dec. 2019, doi: 10.1109/TIE.2019.2893833.

[28] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "High step-up trans-inverse (Tx^{-1}) DC–DC converter for the distributed generation system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4278–4291, Jul. 2016, doi: 10.1109/TIE.2016.2546854.

[29] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2959–2968, Jun. 2014, doi: 10.1109/TPEL.2013.2272639.

[30] H. Wu, T. Mu, H. Ge, and Y. Xing, "Full-range soft-switching-isolated buck–boost converters with integrated interleaved boost converter and phase-shifted control," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 987–999, Feb. 2016, doi: 10.1109/TPEL.2015.2425956.

[31] K.-C. Tseng, C.-A. Cheng, and C.-T. Chen, "High step-up interleaved boost converter for distributed generation using renewable and alternative power sources," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 713–722, Jun. 2017, doi: 10.1109/JESTPE.2016.2611641.

[32] Y. Tang, T. Wang, and D. Fu, "Multicell switched-inductor/switched-capacitor combined active-network converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2063–2072, Apr. 2015, doi: 10.1109/TPEL.2014.2325052.

[33] B. Axelrod, Y. Beck, and Y. Berkovich, "High step-up DC–DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier: Steady state and dynamics," *IET Power Electron.*, vol. 8, no. 8, pp. 1420–1428, Aug. 2015.

[34] V. Bist and B. Singh, "A unity power factor bridgeless isolated Cuk converter-fed brushless DC motor drive," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4118–4129, Jul. 2015, doi: 10.1109/TIE.2014.2384001.

[35] T. Nouri, E. Babaei, and S. H. Hosseini, "A generalized ultra step-up DC–DC converter for high voltage application with design considerations," *Electr. Power Syst. Res.*, vol. 105, pp. 71–84, Dec. 2013, doi: 10.1016/j.epsr.2013.07.012.

[36] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-efficiency high step-up DC–DC converter with dual coupled inductors for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5967–5982, Jul. 2018, doi: 10.1109/TPEL.2017.2746750.

[37] B. Zhu, Q. Zeng, Y. Chen, Y. Zhao, and S. Liu, "A dual-input high step-up DC/DC converter with ZVT auxiliary circuit," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 161–169, Mar. 2019, doi: 10.1109/TEC.2018.2876303.

[38] F. Zhu, F. Liu, W. Liu, K. Feng, and X. Zha, "Performance analysis of RCD and MOV snubber circuits in low-voltage DC microgrid system," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, May 2017, pp. 1518–1521, doi: 10.1109/APEC.2017.7930900.

[39] F. Fiori, "On the use of magnetically coupled resonant snubbers to mitigate the electromagnetic emission of power switching circuits," *IEEE Trans. Electromagn. Compat.*, vol. 64, no. 1, pp. 259–262, Feb. 2022, doi: 10.1109/TEMC.2021.3106769.

[40] C. U-Yaisom, W. Khanngern, and S. Nitta, "The study and analysis of the conducted EMI suppression on power MOSFET using passive snubber circuits," in *Proc. 3rd Int. Symp. Electromagn. Compat.*, 2002, pp. 561–564, doi: 10.1109/ELMAGC.2002.1177495.

[41] M. Mohammadzadeh, E. Akbari, A. A. Salameh, M. Ghadamyari, S. Pirouzi, and T. Senjyu, "Application of mixture of experts in machine learning-based controlling of DC–DC power electronics converter," *IEEE Access*, vol. 10, pp. 117157–117169, 2022, doi: 10.1109/ACCESS.2022.3218667.

[42] R. Parvari, M. Zarghani, and S. Kaboli, "RCD snubber design based on reliability consideration: A case study for thermal balancing in power electronic converters," *Microelectron. Rel.*, vols. 88–90, pp. 1311–1315, Sep. 2018, doi: 10.1016/j.microrel.2018.06.072.

[43] H. Tarzamni, E. Babaei, A. Z. Gharehkoushan, and M. Sabahi, "Interleaved full ZVZCS DC–DC boost converter: Analysis, design, reliability evaluations and experimental results," *IET Power Electron.*, vol. 10, no. 7, pp. 835–845, Jun. 2017, doi: 10.1049/iet-pel.2016.0578.

[44] V. Samavatian and A. Radan, "A high efficiency input/output magnetically coupled interleaved buck–boost converter with low internal oscillation for fuel-cell applications: Small signal modeling and dynamic analysis," *Int. J. Electr. Power Energy Syst.*, vol. 67, pp. 261–271, May 2015, doi: 10.1016/j.ijepes.2014.11.011.

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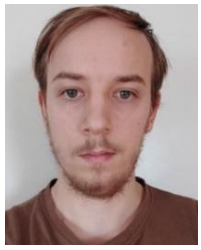

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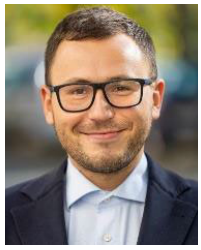

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