IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 24 July 2023, accepted 9 August 2023, date of publication 17 August 2023, date of current version 29 August 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3306050

RESEARCH ARTICLE

Exploring the Performance of 3-D Nanosheet FET in Inversion and Junctionless Modes: Device and Circuit-Level Analysis and Comparison

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This work was supported in part by the National Science and Technology Council (NSTC), Taiwan, under Grant NSTC 112-2221-E-A49-171, Grant MOST 111-2221-E-A49-181, Grant NSCT 112-2218-E-006-009-MBK, and Grant NSCT 111-2218-E-492-009-MBK; and in part by the "2022 Qualcomm Taiwan Research Program, National Yang Ming Chiao Tung University (NYCU)," under Grant NAT-487835 SOW.

ABSTRACT In this article, the performance of 3-D nanosheet FET (NS-FET) in inversion (INV) and junctionless (JL) modes is demonstrated and compared at both device and circuit levels. In JL mode, the ON current (I_{ON}) rises with an increase in temperature compared to the downfall trend in INV mode. In addition, compared to JL mode, the INV mode exhibits a better negative temperature coefficient of threshold voltage (dV_{th}/dT). Further, the mixed mode circuit simulations are carried out using the Cadence Virtuoso platform through the Verilog-A model. From the analysis, it is observed that an increase of 20% gain in INV mode compared to JL mode for a common source (CS) amplifier. The JL mode NS-FETs achieve higher CMOS inverter switching current (I_{SC}) and lower energy-delay products (EDP) as temperature rises. A three-stage ring oscillator (RO) is designed, and the oscillation frequencies (f_{OSC}) of 43.39 GHz and 38.8 GHz are obtained with INV and JL modes. Although JL NS-FET offers less intrinsic capacitances, the f_{OSC} is high for INV mode due to higher I_{ON}. Furthermore, reducing supply voltage (V_{DD}), the f_{OSC} falls by 67% with INV and 62.6% with JL modes. These results will give a better understanding of this emerging NS-FET at both device and circuit levels at advanced technology nodes.

INDEX TERMS CMOS inverter, CS amplifier, inversion, junctionless, nanosheet FET, Verilog-A, ring oscillator.

I. INTRODUCTION

The high performance and low power analog and digital systems are required in emerging applications like artificial intelligence and IoT, in which the operating efficiency of the system should be more. To obtain more efficiency and performance by continuing Moore's law, advanced and emerging FETs are required. In addition to that, the switching capability of the device is the prime recruitment to get more operating efficiency [1]. Scaling the transistor will reduce chip size, power dissipation, and increase switching speed, which tends for high-speed and high-density logic applications. However, aggressive scaling leads to disadvantageous and unavoidable short channel effects (SCEs).

The associate editor coordinating the review of this manuscript and approving it for publication was Inam Nutkani.

TABLE 1. Device design parameters.

Device Parameter	INV Mode	JL Mode
Gate length (L_G)	16 nm	16 nm
Source/drain length	12 nm	12 nm
Nanosheet width (NS_W)	10 nm	10 nm
Nanosheet thickness (NS_T)	5 nm	5 nm
EOT	0.78 nm	0.78 nm
S/D doping	10^{19} cm^{-3} (Donor-N_D)	10^{19} cm^{-3} (Donor-N_D)
Channel doping	10^{15} cm^{-3} (Acceptor-N_A)	10^{19} cm^{-3} (Donor-N_D)
Threshold voltage (V_{th})	0.38 V	0.38 V
Work function	4.5159 eV	4.579 eV
Height of the gate	60 nm	60 nm
Effective width (W_{eff})	60 nm	60 nm

The SCEs will degrade the device's performance and may lead to various adverse effects and malfunction of the device. To circumvent these SCEs, various device engineering techniques are proposed by researchers. To achieve good electrostatic integrity and to suppress SCEs, multigate device architectures like double gate, trigate, fin-shaped field effect transistor (FinFET) and emerging FETs like gate all around (GAA) structures are proposed [2], [3], [4]. Since 2011, semiconductor companies have adopted FinFETs into their 16/14-nm, 10-nm, and 7-nm CMOS technology nodes [5], [6], [7]. However, with continuous scaling, beyond 7-nm technology nodes, scaling of FinFET tends to have adverse SCEs [8], [9]. For sub-3-nm technological nodes and beyond, the GAA structures are promising candidates to enable scaling further [10]. It is shown that GAA NS-FETs offer superior electrostatic performance towards the channel due to their robustness to SCEs [11], [12], [13]. Moreover, it is proved that within the same footprint, a 30% higher effective width (W_{eff}) can be achieved by using NS-FETs compared to FinFETs. Also, due to the greater effective width of NS-FET in each footprint, it is more capable of driving capacitive loads [14], [15]. Using a higher number of stacked nanosheets is a preferable alternative to maximise the driving current, but increased device height worsens the parasitic capacitances [16]. Hence, in this paper, two stacked GAA NS-FET is designed, and the same is used for the simulations towards device and circuit perspective.

The junctionless (JL) transistors have been employed for sub-10-nm technology since the formation of ultra-sharp junctions is highly difficult with CMOS scaling [9], [10]. Moreover, using the JL mechanism thermal budget can be reduced, and JL FETs fabrication is less complex than inversion (INV) mode FETs, which offers less cost [17]. In addition, the JL transistors have advantages like immunity toward surface roughness effects between channel and oxide, low gate capacitances, and better scalability [18].

Although some literature is available on NS-FET, the performance variations with INV and JL modes still need significant analysis. Moreover, as the nanoscale devices are more sensitive to temperature [19], a comprehensive investigation of NS-FET performance among INV and JL modes at elevated temperatures needs to be explored. In addition, detailed circuit analysis of NS-FET with INV and JL modes has not been done and needs to be explored. Hence, in this paper, to provide a detailed circuit performance analysis of the emerging device, the circuits like complementary metal oxide semiconductor (CMOS) inverter, common source (CS) amplifier and ring oscillator (RO) are explored. The Cadence Virtuoso platform is used to design and simulate the above said circuits using the Verilog-A model.

TABLE 2. The DC characteristics comparison of NS-FET in INV and JL modes.

Parameter	INV Mode	JL Mode
I_{ON} (A)	2.55×10^{-5}	2.07×10^{-5}
I_{OFF} (A)	5.07×10^{-13}	5.83×10^{-13}
I_{ON}/I_{OFF}	5.03×10^{7}	3.54×10^{7}
SS (mV/dec)	61.48	63.7
DIBL (mV/V)	34.29	51.55

The contents of the paper are arranged as follows. Section II deals with various parameters used for device design along with the physical models used in the simulation. In addition to the scaling impact of L_G, the temperature dependency on DC figures of merit (FOMs) of NS-FET with INV and JL modes are presented in Section III. The demonstration of circuit performance towards alternating current (AC), direct current (DC) and mixed mode is done in Section IV, and the conclusion of the paper is reported in Section V.

II. DEVICE DESCRIPTION AND SIMULATION METHODOLOGY

The schematic of 3-D NS-FET with spacer is shown in Fig. 1(a). The cross-sectional view of NS-FET in the X-Y plane is depicted in Fig. 1(b). Fig. 1(c) shows the INV mode (N^+-P-N^+) n-type NS-FET with donor doping (N_D) in the source and drain and acceptor doping (N_A) in the channel. Fig. 1(d) shows the JL mode (N^+-N^+-N^+) n-type NS-FET with donor doping (N_D) in the source, channel and drain. The simulated device with L_G of 16 nm is considered according to the international road map for devices and circuits (IRDS) for 3-nm technology node [20] and shown in Table. 1. To obtain an effective oxide thickness (EOT) of 0.78 nm for a high-k gate stack, thickness values of 0.5 nm and 1.5 nm for SiO_2 and HfO_2 are used. To enhance the subthreshold characteristics, a spacer length of 5 nm with nitride (Si_3N_4) is used for the simulations [15]. The channel doping for INV mode for SOI FET is reported as 10^{15} cm^{-3} for 14- and 7-nm technology nodes [21], and according to Lee et al., the general doping order for JL FET is 10^{19} cm^{-3} [22].

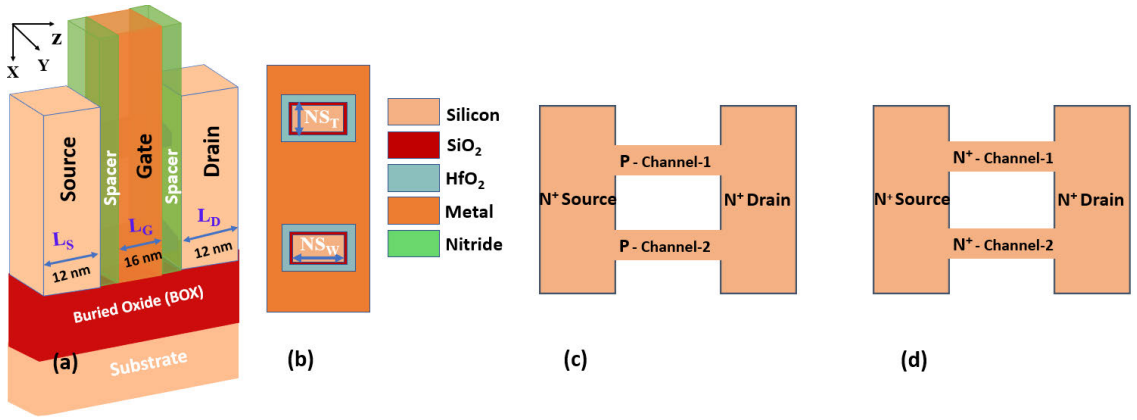

FIGURE 1. (a) Schematic of 3-D NS-FET (b) 2-D view of gate stack in X-Y plane (c) Doping profiles of INV NS-FET and (d) JL NS-FET in X-Z plane.

Thus, we have incorporated above said doping profiles for NS-FET. The proposed NS-FET is adopted with silicon-on-insulator (SOI) technology which improves electrostatics, near ideal subthreshold characteristics, minimizes parasitic capacitances, less power consumption and suppressed threshold voltage (V_{th}) variations [23]. The Genius 3D TCAD simulator by Cogenda [24], is used for the generation and simulation of the JL and INV mode NS-FET structures. Initially, the calibration of TCAD models is done, which are used for NS-FET simulation using Loubet et al. [15], based on the self- consistent drift-diffusion, continuity and Poisson equations. The density gradient method is used to account for quantum confinement phenomena. Schenk's bandgap narrowing model is used to address the band gap narrowing effects due to high doping concentrations. For the generation and recombination of electrons and holes, the Shockley-Read-Hall recombination model is incorporated. To account for the mobility reduction at silicon to oxide interface due to phonon and coulomb scattering mechanisms, the Lombardi mobility model is used. In order to account for tunneling in the lateral direction, the non-local band-to-band tunneling model is included. The Selberherr impact ionization model is used to account electron-hole pair generation rate. The Lucent model is considered to capture the high-field mobility effects. The linear and log transfer characteristics obtained from calibrated models are depicted in Fig. 2. The various device parameters considered for simulation are given in Table 1.

III. RESULTS AND DISCUSSION

In this section, the DC performance of NS-FET in INV and JL modes is studied in detail. Further, the DC performance metrics like ON current (I_{ON}), OFF current (I_{OFF}), switching ratio (I_{ON}/I_{OFF}), subthreshold swing (SS), threshold voltage (V_{th}) and drain-induced barrier lowering (DIBL) are assessed and compared with both INV and JL modes. The I_D-V_{GS} characteristics of both INV and JL modes are depicted in Fig. 3 at V_{DS} of 0.7 V and 0.04 V. The I_{ON} is extracted at $V_{GS} = V_{DS} = 0.7$ V and I_{OFF} at $V_{GS} = 0$ V and $V_{DS} = 0.7$ V. More I_{ON} is observed for the INV mode compared to the JL

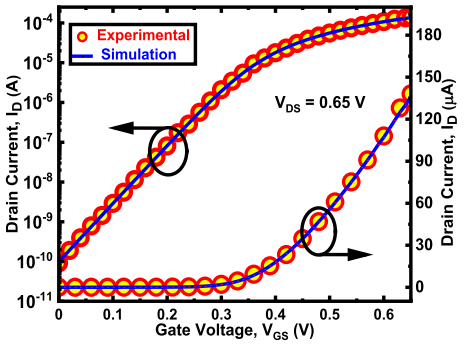

FIGURE 2. Calibration of TCAD simulation models with the experimental results of stacked GAA NS-FET [15].

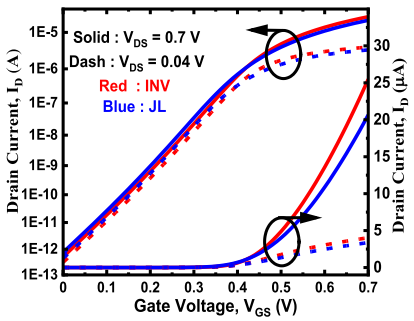

FIGURE 3. Transfer characteristics of n-type NSFET for INV and JL modes.

mode. This may be attributed to the degradation of mobility in JL mode due to strongly ionized impurity scatterings owing to the high doping profile in the channel [25]. Table 2 shows the various DC FOMs comparison of NS-FET in INV and JL modes. The SS gives the value of the required variation in gate voltage to get a change of one decade in I_D. The mathematical expression for SS is as follows (1) [26]:

$$SS = \left[\frac{\partial \log_{10} I_D}{\partial V_{GS}}\right]^{-1} \tag{1}$$

Lower values of SS are required to ensure good subthreshold performance. From Table 2, an increment of 3.6% in SS is observed for JL mode compared to INV mode NS-FET. The DIBL is another important subthreshold performance

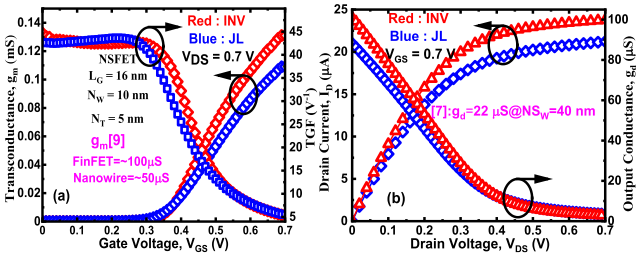

FIGURE 4. (a) Transconductance (g_m) and TGF (b) I_D-V_{DS} and output conductance (g_d) of NS-FET for INV and JL modes.

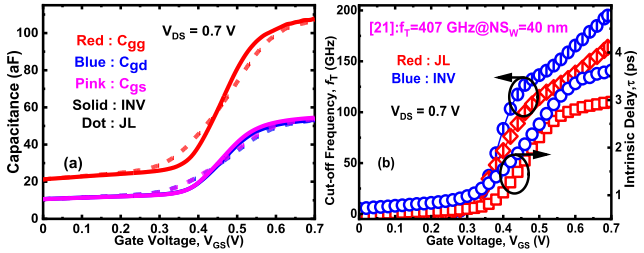

FIGURE 5. (a) Capacitances (b) Cut-off frequency (f_T) and intrinsic delay (τ) of NS-FET for INV and JL modes.

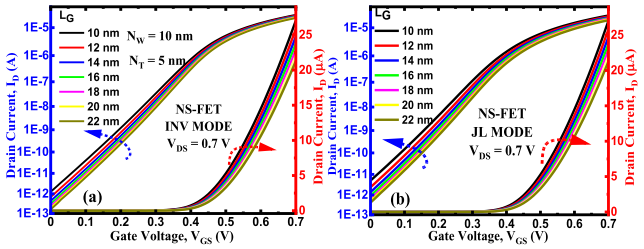

FIGURE 6. Transfer characteristics of NS-FET for (a) INV and (b) JL modes with L_G scaling from 22 nm to 10 nm.

metric, and minimum DIBL values are preferred for optimum device performance. The mathematical expression of DIBL is calculated by using the following formula [26]:

$$\text{DIBL (mV/V)} = \left| \frac{V_{\text{th1}} - V_{\text{th2}}}{V_{\text{DS1}} - V_{\text{DS2}}} \right|. \tag{2}$$

Here, V_{th1} and V_{th2} are the threshold voltages extracted at V_{DS} of 0.04 V and 0.7 V, respectively. By using the constant current method, V_{th} is extracted at $W_{\text{eff}}/L_{\text{G}} \times 10^{-7}$A [26]. Where W_{eff} is the number of stacks of nanosheet multiplied by the perimeter of the nanosheet. In the INV mode, the minority carriers (electrons) are drawn to the surfaces by the field, with a maximal concentration near the Si/oxide interfaces. The gate field in the JL device, on the other hand, is of the opposite sign and forces the majority carriers (electrons) away from the surfaces, resulting in a fully depleted body with a peak concentration in the device centre [27]. When the charge centroid is close to the centre, the equivalent electrical oxide thickness is higher, and gate control degrades. As a result, a large DIBL is observed for the JL mode compared to the INV mode device [27]. An increment of 50.3% in DIBL is noticed for JL modes compared to INV mode.

The transconductance ($g_m = \partial I_D/\partial V_{GS}$) is one of the crucial analog FOM, which gives the relation between the corresponding change obtained in I_{D} with the change of V_{GS} and is attributed by taking the derivative, as shown in Fig 4(a). The g_m also decides the amplification capability of the device [28]. Usually, the higher values of g_m are preferred to get good performance. It is noticed that for INV mode, higher g_m is obtained compared to JL mode because of the higher I_{ON} in INV mode. Also, the transconductance generation factor (TGF = g_m/I_D) is another important metric towards power essential for attaining more speed with V_{GS}, and higher TGF values are required for a device to operate at low voltages without degrading the efficiency of the devices [26]. From Fig. 4(a), the higher TGF values are noticed for INV mode compared to JL mode due to higher g_m. Fig. 4(b) depicts the output characteristics (I_D-V_{DS}) and g_d values as a function of drain voltage at $V_{\text{GS}} = 0.7$ V. The g_d is high for INV mode due to the higher I_{D}. However, in the saturation region, the g_d is slightly lower for INV mode compared to JL. Lower g_d ensures reduced channel length modulation, which is useful for driving constant current source applications. Fig. 5(a) depicts the capacitance versus gate voltage characteristics in INV and JL modes at $V_{\text{DS}} = 0.7$ V. The gate capacitance (C_{gg}) can be expressed as the sum of both C_{gs} and C_{gd}, where C_{gs} is the gate to source capacitance and C_{gd} is the gate to drain capacitance. From Fig.5(a), it is observed that C_{gd} is slightly lowered due to the depletion of electrons at the drain end at high V_{DS}. The presence of saturation current-blocking region on drain side instead of channel tends to offer less capacitance in JL mode compared to INV mode [29]. It is observed from Fig. 5(b) that for INV mode, higher cut-off frequency ($f_T \approx \frac{g_m}{2\Pi(C_{\text{gd}}+C_{\text{gs}})}$) is obtained due to higher g_m. Although the C_{gg} is less for JL mode NS-FET, due to higher I_{ON}, more f_T is observed in INV mode [29]. Further, the intrinsic gate delay ($\tau = \frac{C_{gg}V_{DD}}{I_{ON}}$) is slightly higher for JL than INV mode because of lower I_{ON} for JL mode, as shown in Fig 5(b). The τ decides the speed of the device, and from the results, INV NS-FET offers more speed than JL NS-FET.

A. SCALING EFFECT ON INV AND JL MODES

In this section, the performance comparison of NS-FET with both INV and JL modes is presented with scaling L_G. Fig. 6(a) and (b) depict the transfer characteristics of NS-FET in INV and JL modes for various L_G. As scaling is inevitable for future electronics, in this paper, the scaling feasibility of NS-FET with both INV and JL modes is analysed. The L_G is scaled from 22 nm to 10 nm to observe various performance metrics like I_{ON}, I_{OFF}, $I_{\text{ON}}/I_{\text{OFF}}$ and DIBL. Fig. 7(a) and 7(b) depict the I_{ON} and I_{OFF} values with respect to L_G scaling in both INV and JL modes. For all the L_G, the INV mode outperforms in terms of I_{ON} due to the reduced mobility degradation compared to the JL mode. With the downscaling of L_G from 22 nm to 10 nm, the I_{ON} is increased. As the L_G shrinks, the distance between the source and drain decreases which increases the current. However, the OFF current (I_{OFF}) also increases significantly due to the various SCEs and is shown in Fig.7(b). The I_{OFF} increases with L_G scaling due

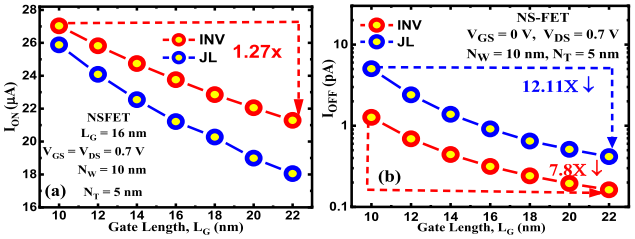

FIGURE 7. (a) I_{ON} and (b) I_{OFF} of INV and JL modes with L_G scaling.

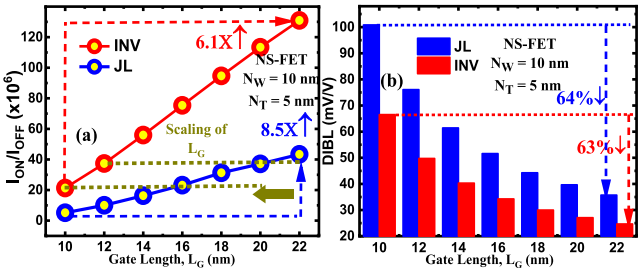

FIGURE 8. (a) I_{ON}/I_{OFF} and (b) DIBL of INV and JL modes with L_G scaling.

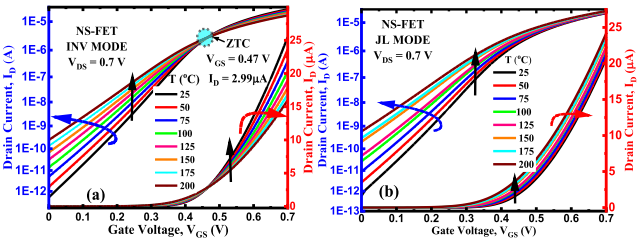

FIGURE 9. Transfer characteristics of NS-FET for (a) INV and (b) JL modes with temperature.

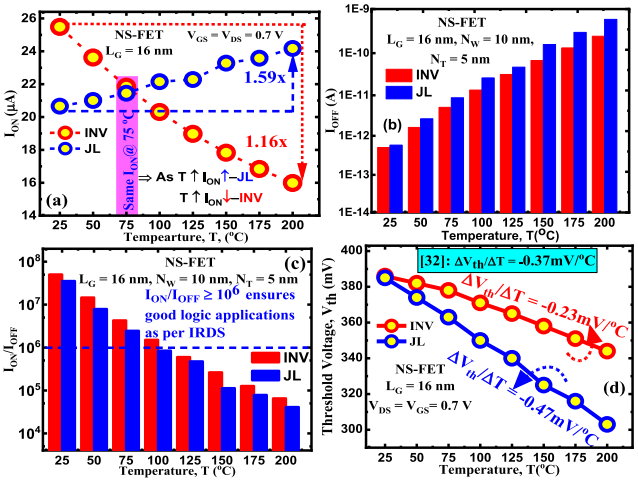

FIGURE 10. (a) I_{ON} (b) I_{OFF} (c) I_{ON}/I_{OFF} and (d) V_{th} of NS-FET for INV and JL modes as a function of temperature.

to the degradation of gate control over the channel region. A decrement of 12.11 × and 7.8 × is noticed in I_{OFF} for JL and INV modes, respectively, with L_G variation from 10 nm to 22 nm.

Fig. 8(a) shows the switching ratio (I_{ON}/I_{OFF}) with scaling, and is noticed that with an increment in L_G, the switching ratio improves due to a substantial reduction in I_{OFF}. An increment of 6.1 × and 8.5 × is noticed for INV and JL modes with L_G rise from 10 nm to 22 nm. Moreover, for all the variations, the I_{ON}/I_{OFF} is greater than 10^6, which supports the scaling feasibility of NS-FET [11]. Fig. 8(b) depicts the DIBL variations with respect to L_G for both INV and JL modes. Higher DIBL values are observed for JL mode for all the L_G values compared to INV mode. Also, a decrement of 64% and 63% noticed for JL and INV modes, respectively when L_G increased from 10 nm to 22 nm.

B. TEMPERATURE IMPACT ON INV AND JL MODES

As the nanoscale devices are more sensitive to temperature variations, in this section, the temperature impact on both INV and JL modes is analyzed at elevated temperatures. The temperature is varied from 25°C to 200°C, and various crucial metrics like I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and DIBL are analysed in this section.

Fig. 9(a) and (b) depict the I_D-V_{GS} characteristics of INV and JL mode NS-FET for various temperatures at V_{DS} = 0.7 V. Usually, the analog and digital applications are used at different temperatures. It is advised to bias these circuits so that the performance should be independent of temperature. This biasing point is called zero temperature coefficient (ZTC) or temperature compensation point (TCP) and is used in IC applications. In INV mode, decreasing the V_{th} with the rise in temperature causes the drain current to increase, whereas decreasing mobility with temperature due to increased phonon scattering tends to decrease it [30]. As a result, the ZTC exists in INV mode FET and is observed at V_{GS} = 0.47 V and I_D = 2.99 μA. In contrast to the INV mode, the drop in mobility with temperature in JL transistors is substantially lower than in the INV mode transistors. As a result, the current grows in a predictable pattern with no ZTC point [19].

Fig. 10(a) shows I_{ON} for INV and JL modes with temperature. At room temperature (25°C), more I_{ON} is observed for INV compared to JL mode. This may be accredited to the reduction in mobility due to higher doping concentrations [25]. Moreover, it is observed that the I_{ON} in the JL mode constantly increases as the temperature rises. Since the V_{th} of JL mode reduces more with temperature than that of INV mode NS-FET, resulting in a lower mobility reduction [19]. The I_{OFF} variation for JL and INV mode NS-FET is depicted in Fig. 10(b). The I_{OFF} increases with temperature due to an increase in intrinsic carrier concentration. The I_{OFF} is higher for JL FETs compared to INV FETs and exhibits low leakage at 25°C. Fig. 10(c) depicts the switching ratio (I_{ON}/I_{OFF}) for various modes of NS-FET. It is noticed that as temperature increases, the I_{ON}/I_{OFF} tends to fall due to the increment in I_{OFF}. The increment in I_{OFF} is mainly due to the rise in intrinsic carrier concentration (n_i), which causes to enlargement in both generation and diffusion currents. Fig. 10(d) depicts V_{th} variations for various temperatures for JL and INV modes. It is noticed that as temperature rises, a fall in V_{th} is observed for both modes. Both JL and INV modes exhibit negative values of variation in V_{th} with temperature, i.e., dV_{th}/dT. Fig. 10(d) depicts the dV_{th}/dT of

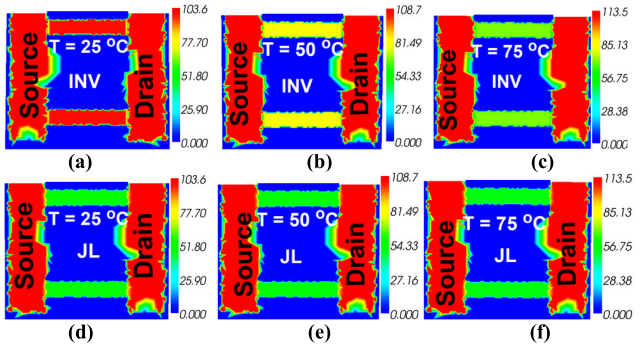

FIGURE 11. Contour plots of electron mobility (cm^2/V-s) in X-Z plane for INV mode at (a) 25 °C (b) 50 °C (c) 75 °C and JL mode at (d) 25 °C (e) 50 °C and (f) 75 °C in the ON state.

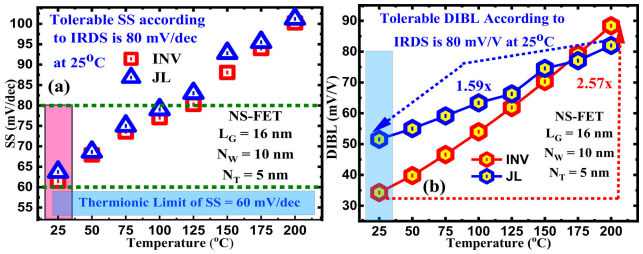

FIGURE 12. (a) SS (b) DIBL of NS-FET for INV and JL modes as a function of temperature.

-0.47mV/°C for JL and -0.23mV/°C for INV mode, which is quite close to the experimental value (dV_{th}/dT is -0.37mV/°C) reported by Trevisoli et al [31].

The electron mobility variations with respect to temperature for JL and INV modes are depicted in Fig. 11. The contour mechanisms show a fall in electron mobility in the INV mode FETs (Fig. 11(a)-(c)). In INV mode, the phonon scattering is dominant due to less channel doping, and it varies with $T^{-3/2}$ [19]. Whereas in JL mode, impurity scattering is dominant mechanism and varies with $T^{3/2}$ [19]. Both scattering mechanisms compensate each other in JL modes, which causes mobility to be almost independent of temperature [19] (Fig. 11(d)-(f)).

Fig. 12(a) shows the variation of SS as a function of temperature, which is varied from 25°C to 200°C. It is noticed that at 25°C, the INV and JL modes offer an acceptable SS as per IRDS rules [20]. Moreover, irrespective of operating mode, the SS tends to increase with the rise in temperature due to the increment in I_{OFF}. An increment of 63% and 59% in SS is observed for INV and JL modes when the temperature increased towards its upper bound. It can be concluded that with high temperatures, the subthreshold performance of the device tends to degrade. Fig. 12(b) depicts the DIBL variations for various temperatures with different modes. At 25°C, the DIBL values for two modes are below 80 mV/V and meet the IRDS criteria [20]. It is observed that with the increment in temperature for all the modes, an increment in DIBL is noticed due to the significant increment in leakage currents. Large DIBL is observed for JL mode compared to INV mode due to the degradation of gate control [22]. An increment of 2.6× and 1.59× is noticed for DIBL in INV and JL modes

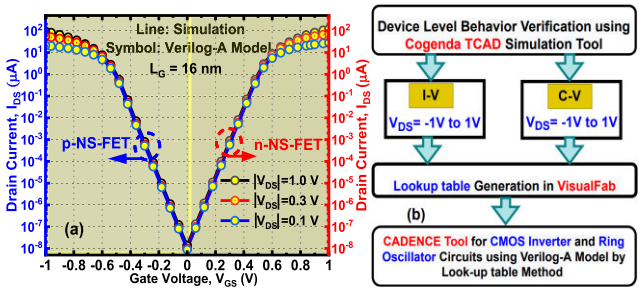

FIGURE 13. (a) Matching of TCAD with SPICE simulation and (b) Flow chart of Verilog- A model creation and SPICE simulation.

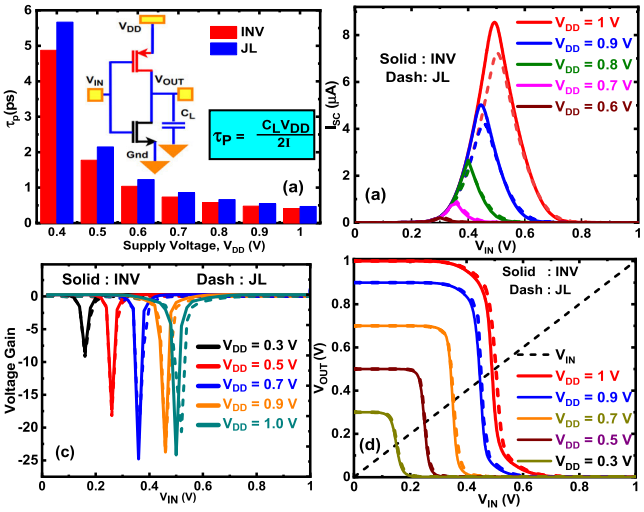

FIGURE 14. (a) Propagation delay (τ_P) (b) Switching current (I_S) (c) Voltage gain and (d) Transfer characteristics of NS-FET based CMOS inverter.

when temperature increases towards 200°C. It is noticed that the subthreshold performance degrades with the rise in temperature.

IV. CIRCUIT ANALYSIS

In this section, INV and JL modes performance is assessed and compared using the Verilog-A model [32]. Fig. 13(a) shows the calibration of SPICE simulation characteristics with TCAD results. The steps considered for circuit simulation are depicted in Fig. 13(b). The 3D Cogenda Visual TCAD is used to design the GAA NS-FET device [24]. The Visual Fab parallel simulation tool [24] is also used to extract DC and AC characteristics. The lookup tables are used for symbol creation in the Cadence Virtuoso tool [33], which later used in circuit design.

The schematic of the inverter circuit is shown in Fig. 14(a). Here, V_{DD}, V_{IN} and V_{OUT} are the supply voltages, input voltage and output voltages, respectively. To estimate the performance of the inverter, it is very much required to assess crucial FOM like average propagation delay (τ_P) [34], energy-delay product (EDP) and switching current. The τ_P decreases with an increase in V_{DD}. Compared to JL mode, INV mode exhibits lower τ_P with V_{DD} variation. Reducing load capacitance (C_L) or boosting average current (I) can minimise τ_P, which ensures high-speed switching. Fig. 14(b) depicts the switching current (I_s) of the inverter for both INV

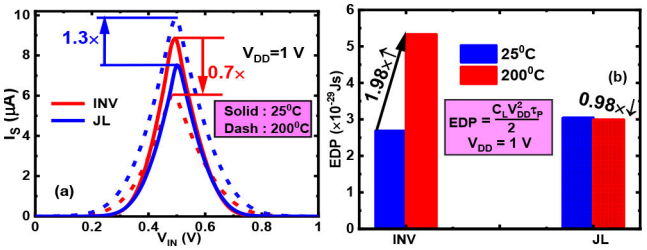

FIGURE 15. Impact of temperature on CMOS inverter (a) Switching current (I_S) (b) EDPat 25°C and 200°C for INV and JL modes.

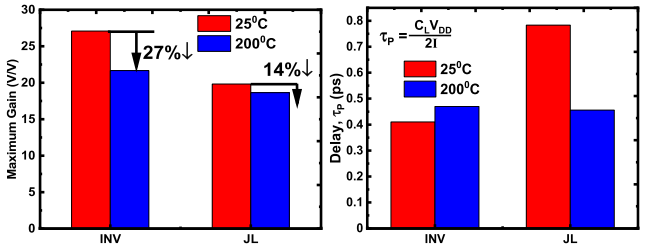

FIGURE 16. (a) CMOS inverter gain and (b) propagation delayat 25°C and 200°C for INV and JL modes.

and JL modes. The increment of 15.8% is noticed in I_s for INV mode because of the relative increment in I_{ON} compared to JL mode [29]. Fig. 14(c) depicts the output characteristics of the CMOS inverter. As the supply voltage decreases, the shift in the switching threshold moves towards the left. Fig 14(d) depicts the inverter gain in both INV and JL modes. A higher gain is observed in the INV mode inverter than in the JL mode because of the high I_{ON}. The gain of the INV mode inverter is marginally higher than the JL mode inverter. This may be attributed to the higher I_{ON} in INV mode.

Fig. 15(a) depicts the switching current (I_s) of the inverter for INV and JL modes at different temperatures. The I_s represents the maximum current drawn when both transistors are in saturation [34]. There is an increment of 1.3× in I_s for JL modes as the temperature rises from 25°C to 200°C at a fixed value of V_{DD}. However, 0.7× decrement is noticed for I_s of INV mode due to the degradation of I_{ON}. The EDP for various modes is depicted in Fig. 15(b). The EDP of INV mode raised by 1.98× due to the increment in delay with the rise in temperature towards 200°C. However, the EDP is lowered by 0.98× for JL modes respectively due to the degradation of delay with increment in temperature.

Fig. 16(a) depicts the inverter gain (dV_{OUT}/dV_{IN}) for INV and JL modes with respect to temperature. The gain falls with a rise in temperature in INV mode by 27%. However, the fall is marginal in the case of JL mode. For JL and INV modes, the gain is higher at 25°C due to steeper output characteristics. Moreover, the deterioration of gain is low for JL mode due to a significant increment in I_{ON} with respect to the temperature. Fig. 16(b) depicts the delay (τ_p) in INV and JL mode. The τ_p increase with the rise in temperature in INV mode. However, τ_p downfalls in JL mode FET with the increase in temperature. Although the capacitances of JL mode are smaller than INV mode, the higher I_{ON} leads to lower propagation delay at 25°C.

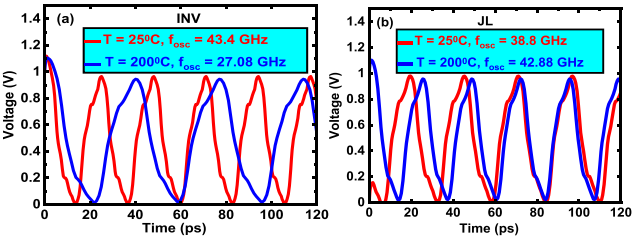

FIGURE 17. NS-FET based ring oscillator (RO) schematic diagram (a) INV mode and (b) JL mode.

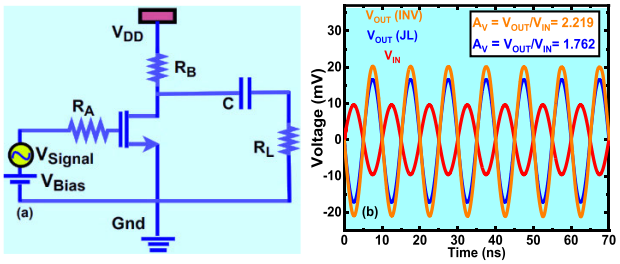

FIGURE 18. (a) NS-FET based CS amplifier schematic diagram and (b) transient response of CS amplifier with INV and JL modes.

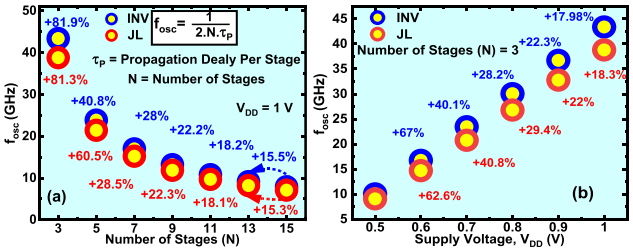

FIGURE 19. The RO and f_{osc} variations of INV and JL modes with (a) Number of stages (N) and (b) Supply voltage (V_{DD}).

The ring oscillator (RO) performance with 3-stages for INV and JL modes for various temperatures is shown in Fig. 17. The highest oscillation frequency, f_{osc} is obtained for INV mode RO at 25°C due to the highest I_{ON} (Fig. 17(a)). Whereas, at 200°C the JL RO outperforms with an f_{osc} of 42.88GHz (Fig. 17(b)). The decrement of 37% in f_{osc} is noticed for INV mode when temperature increased from 25°C to 200°C. Whereas, an increment of 10% in f_{osc} is noticed for JL modes respectively when temperature increased towards 200°C.

In the analog circuit applications, the common source (CS) amplifier plays a very crucial role as it amplifies the weak signal for better driving capability. Fig. 18(a) depicts the CS amplifier schematic diagram. For amplification purpose, the V_{bias} of 0.7 V is applied, and a peak-to-peak AC voltage of 20 mV is considered. Also, resistance values of 100Ω, 15kΩ and 1MΩ are taken for R_A, R_B, and R_L, respectively. To avoid DC voltage at output, a capacitor of 1μF is considered to analyze the transient response. Due to the higher drive current, more gain is obtained for the INV mode CS amplifier, which is depicted in Fig. 18(b). It is noticed that with INV mode, 20% more gain is obtained compared to the JL mode NS-FET CS amplifier.

Further, Fig. 19(a) depicts the f_{osc} with number of stages of RO at V_{DD} = 1V. Increase in number of stages the f_{osc}

decreases due to increase in τ_p between the stages. 19(b) depicts the f_{osc} variations with supply voltage provided to RO. As the supply voltage rises, the increment in f_{osc} is noticed due to the increment of I_{ON}. Also, the INV mode RO outperforms the JL RO in both variations due to its highest I_{ON} [29].

V. CONCLUSION

In this paper, both device and circuit level comparison have been assessed and compared by considering various DC, analog/RF, and circuit level FOMs of 3D vertically stacked GAA NS-FET in JL and INV modes. For mixed mode simulations, circuit applications like CMOS inverter, RO and CS amplifiers were considered. At the device level, INV mode outperforms JL mode in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS and DIBL. Furthermore, the scaling feasibility of NS-FET for sub-3-nm was assessed and it has been observed that even at an L_G of 10 nm, the switching ratios greater than $\sim 10^6$ are noticed. Also, the temperature effects on the device and circuit performance have been analyzed in detail for both modes. Both the JL and INV mode of NS-FETs exhibit marginal variation in f_{OSC} with reduced V_{DD}. Coming to the digital and analog circuit applications, compared to the JL mode, INV mode offers less propagation delay and high gain for the inverter. Also, it has been observed that for analog applications like CS amplifier and RO, the INV mode outperforms JL mode in terms of gain and $f_{OSC,}$ respectively. These analyses on the device and circuit-level performances will give brief insights into digital and analog applications of NS-FET for sub-3-nm technological nodes with INV and JL modes.

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