IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 31 July 2023, accepted 11 August 2023, date of publication 15 August 2023, date of current version 28 August 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3305593

RESEARCH ARTICLE

On-Chip Batteries as Distributed Energy Sources in Heterogeneous 2.5D/3D Integrated Circuits

PEYMAN DEHGHANZADEH[1], JUNJUN HUAN[1], (Member, IEEE), ROHAN REDDY KALAVAKONDA[1], SOUMYAJIT MANDAL[2], (Senior Member, IEEE), AND SWARUP BHUNIA[1], (Senior Member, IEEE)

[1]Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, USA
[2]Instrumentation Division, Brookhaven National Laboratory, Upton, NY 11973, USA

Corresponding author: Peyman Dehghanzadeh (p.dehghanzadeh@ufl.edu)

ABSTRACT Energy efficiency in digital systems faces challenges due to the constraints imposed by small-scale transistors. Moreover, the growing demand for portable consumer electronics necessitates the use of compact energy sources. To address these challenges, heterogeneous 3D IC technology has emerged as a promising solution for the former. Regarding the latter, we propose the concept of distributed batteries within a heterogeneous 3D IC. This approach involves utilizing multiple smaller batteries with different specifications among different modules of 3D ICs. This approach optimizes performance and overcomes limitations associated with both 3D ICs and conventional power delivery methods. Distributed batteries play a vital role in effectively managing the heat generated by energy sources and modules within a 3D IC. Furthermore, they contribute to achieving a uniform distribution of heat throughout the entire structure, which ultimately ensures the optimal performance of the batteries and modules. The simulation results indicate a 40 percent enhancement in achieving a more even distribution of generated heat. Additionally, the proposed distributed battery techniques improve power delivery, enhance reliability, and enable optimized voltage regulation while improving efficiency. In addition to the primary benefits, alternative configurations of the proposed approach can offer extra energy storage capacity and act as efficient electromagnetic shields, resulting in an impressive reduction of external electromagnetic noises by 60 dB.

INDEX TERMS Heterogeneous 3D IC, point of loads, solid-state batteries, power delivery network.

I. INTRODUCTION

The aspiration for enhanced energy efficiency in digital systems through silicon CMOS scaling encounters growing difficulties owing to the inherent limitations in the physical size, complexity, and manufacturability of small-scale transistors [1]. Additionally, the increased costs and lower yield associated with producing miniature transistors pose significant obstacles. To address this technical challenge, 3D integration has emerged as a promising solution, involving the vertical stacking of smaller, low-cost, high-yield dies [2]. This approach offers notable benefits such as improvements in input/output (I/O) bandwidth, energy efficiency, latency, and form factor [3], [4], [5]. Heterogeneous ICs, which combine discrete modules or chiplets (such as logic, memory, mixed-signal circuits, and RF circuits) into a single system in package (SiP), further enhance system functionality [6], [7]. The integration of ICs with sensors and passive components is also gaining importance in distributed wireless sensor networks.

Along with improvements in 3D ICs, the worldwide need for portable consumer electronics has increased the demand for miniature energy sources. Efforts have been ongoing to create miniature sensing and computing nodes for use in intelligent medical implants and the Internet of Things (IoT). Such small autonomous devices are typically wireless, which means they need to be energy autonomous, i.e, include their own energy sources [8], [9], [10]. Conventional large-scale energy sources can be utilized to energize groups of sensors and actuators, but this approach results in

The associate editor coordinating the review of this manuscript and approving it for publication was Renato Ferrero.

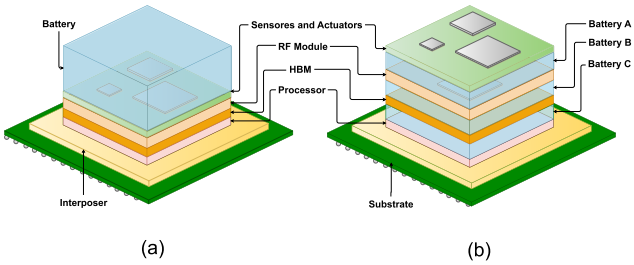


FIGURE 1. (a) Conventional on-chip battery structure (b) Proposed on-chip battery structure.

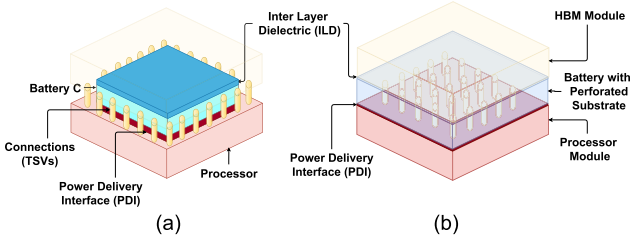


FIGURE 2. Layout of TSVs andÂ connections for connecting upper and lower modules. (a) Around the battery. (b) Inside the battery by using a perforated substrate [16].

problems with interconnection, noise, and voltage regulation. By designing the energy source to be commensurate in size with the sensors and actuators, the intricacies involved in the process of delivering power are mitigated. Thus, the efficiency and operating lifetime of autonomous devices can be improved by incorporating miniaturized energy storage elements such as micro-batteries. Since planar 2D cells have inherent energy density restrictions [11], the implementation of 3D micro-structures is critical for improving micro-battery technology [12]. The development of 3D solid-state batteries (SSBs) has accordingly been driven by the goal of enhanced energy density. Micro-batteries employing such 3D structures have the potential to provide significant energy and power densities after attachment to planar surfaces [13].

Obtaining access to a high-quality power source is a critical prerequisite for both 2D and 3D ICs. The integration of on-chip micro-batteries with heterogeneous 3D ICs is expected to be compelling because it would allow for extreme miniaturization of the point-of-load (POL) DC-DC converters used to generate such power sources [14]. The use of on-chip batteries is also likely to 1) improve the efficiency of such converters by eliminating the parasitic impedance of the package and board-level traces, and 2) simplify the development of on-chip power distribution networks for supplying multiple voltage domains. It is important, however, to recognize that alongside these benefits, there are significant challenges associated with this integration. To overcome these challenges, we proposed the concept of distributed batteries in the 3D IC structure, fully leveraging the potential benefits that on-chip batteries offer. This paper primarily aims to conduct a comprehensive examination of the benefits associated with integrating distributed micro-batteries within heterogeneous 3D ICs. Additionally, we will provide a concise overview of the potential challenges and limitations that may emerge during the implementation of these structures within 3D ICs.

The rest of the paper is organized as follows. The proposed architecture for utilizing distributed batteries in heterogeneous 3D ICs is discussed in Section II. In Section III, the advantages of the proposed concept are discussed. The concept has some extensions and limitations, which are discussed in Section IV. Finally, Section V concludes the article.

II. PROPOSED STRUCTURE

In order to generate high-quality power supplies with minimal energy loss for the various voltage domains within a chip, it is crucial to effectively manage the available power regulation and conversion resources. Fig. 1(a) shows a typical on-chip battery configuration, in which the unregulated DC voltage from the battery is converted and stabilized to a suitable voltage level and then distributed to individual modules by the power delivery system. However, this power distribution approach faces several challenges, including low efficiency, localized heat generation, noise, design complexity, and reduced lifetime [15]. To overcome these issues, we propose to use distributed batteries within a heterogeneous 3D IC. Fig. 1(b) illustrates a simplified version of this concept, which uses multiple smaller batteries with various voltage levels and specifications (instead of one larger battery) to power a heterogeneous 3D IC. These batteries can output various voltage levels and currents for different loads. Different battery technologies and chemistries can be utilized to optimize the performance of individual modules, resulting in heterogeneous batteries. Implementing this approach can mitigate or resolve all the problems and challenges mentioned earlier. However, placing batteries between modules also acts as a barrier to data transfer between them. It is crucial to identify a solution to overcome this issue, which should not add to the design complexity or nullify the benefits of 3D ICs. One potential solution involves moving all the through-silicon vias (TSVs) and other connections between upper and lower modules outside the battery area, as shown Fig. 2(a). While this technique makes it simple to incorporate the battery, it severely reduces the density of inter-module connections, thus negating the benefits of 3D integration to some extent.

A higher-performance alternative involves the use of a perforated substrate to establish connections between upper and lower modules in the presence of an SSB located in the middle. The use of multichannel plate substrates to fabricate 3-D thin-film micro-batteries was demonstrated for the first time in [16]. The battery substrate was modified by introducing a large number of ‘‘through holes’’ to enhance the area, resulting in an increase in both power density and energy density. The utilization of a perforated substrate, instead of a solid substrate, enables a substantial gain in geometrical area for film deposition. The additional area for each cylindrical

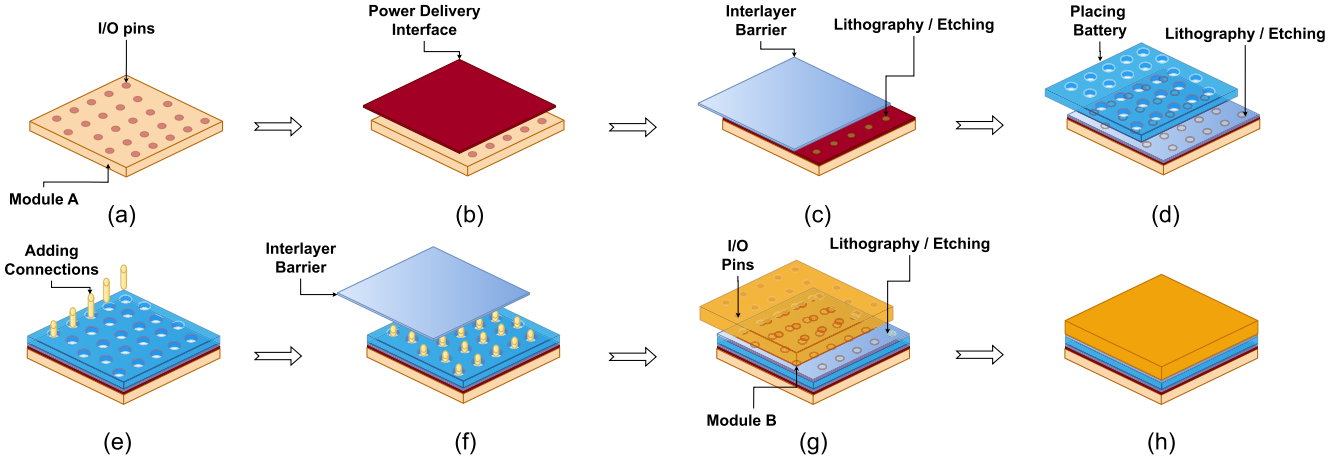


FIGURE 3. Typical process flow for putting a battery between two different modules. (a) Module A inside a 3D IC with its I/O pins. (b) Placing power delivery interface (PDI) on top of Module A. (c) Opening I/O pin locations on PDI by lithography/Etching technique and depositing Inter-layer Barrier (ILB) on top of PDI. (d) Opening I/O pin locations on the ILB and placing the battery with the perforated substrate. (e) Adding connections inside through holes of battery with perforated substrate. (f) Depositing another ILB. (g) Opening connection locations on ILB by lithography/Etching technique and placing Module B on the top. (h) Final structure with a battery between two Module A and B.

hole can be determined as [16]:

$$AG = \frac{\pi.d}{(d+s)^2}\left(t - \frac{d}{2}\right) + 2 \tag{1}$$

where AG is the area gain, s is the interchannel spacing, d is the micro-channel diameter, and t is the substrate thickness. As a practical example, for a perforated substrate with a $d = 50\mu$m, $s = 10\mu$m and $t = 500\mu$m, the active surface area gain is approximately 23. The TSVs can be routed through these through holes to connect the upper and lower modules. Fig. 2(b) depicts the positioning of TSVs and other inter-module connections inside a battery with such a perforated substrate.

It is crucial that the battery fabrication process work with standard semiconductor fabrication technology. The silicon substrate used by the SSB only serves as a structural support, so it is important to incorporate a barrier interlayer, like TiN, Pt, SiO_2, or Al_2O_3, between the battery substrate and other integrated electronic devices to prevent any injection of Li ions into other parts of the structure and other modules. Battery components can be deposited on 3D Si-based substrates using atomic layer deposition (ALD), chemical vapor deposition (CVD), and sputtering techniques [17], [18], [19]. The typical process flow for placing a battery between two distinct modules is illustrated in Figs. 3 (a) through (h). For the sake of simplicity and to highlight other concepts, the positioning of inter-module connections is disregarded for the rest of this study.

III. ANALYSIS OF THE PROPOSED TECHNOLOGY

A. HEAT MANAGEMENT

One of the primary concerns that lead to a decrease in system performance in heterogeneous ICs is the production of heat by various modules. Heat is generated not only by components such as power amplifiers and processors but also by on-chip batteries, exacerbating the problem. During charging and discharging cycles, a battery produces heat due to internal electrochemical reactions and charge transport processes. The rate at which heat is generated depends on factors such as internal resistance, charging/discharging rate, and cell temperature. Inefficient dissipation of the heat generated can cause the cell temperature to rise, leading to reduced battery performance and enhanced degradation of the electrodes and/or electrolyte. Therefore, efficient heat management is crucial to maintain optimal battery performance and prevent damage. Given the requirement for a battery to supply significant current to various sections and modules in a heterogeneous IC, it is anticipated that a substantial amount of heat will be produced in and around the battery. Due to the localized heat generated in this area, a specific volume of the 3D IC will experience elevated temperatures. The high heat density resulting from confinement within a small volume poses a challenge for conventional heat transfer techniques to dissipate it externally. Additionally, it is critical to consider the mechanical stress and dimensional changes that result from such localized heating.

Controlling battery temperature is essential for both safe operation and a long lifespan. The surface area to volume ratio of a battery decreases with size, thus making it difficult to maintain a uniform and controlled temperature across all the components of a large battery. Consider the situation where a single large battery energizes all the modules of a heterogeneous 3D IC. Such a battery has to supply the entire load current of the 3D stack, resulting in the generation of a significant amount of internal heat that cannot be efficiently transferred to the environment. The result is a localized hotspot, as shown in Fig. 4(a). By contrast, the proposed distributed batteries concept suggests using one battery per module, resulting in much lower current demand for each battery and less heat generated per unit area. Furthermore, the generated heat will be more evenly dispersed throughout the 3D IC structure, thus avoiding the generation of hotspots as indicated in Fig. 4(b).

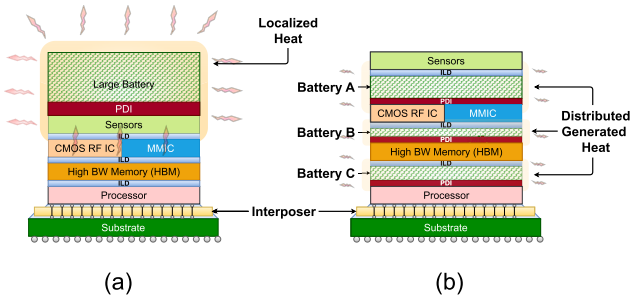


FIGURE 4. (a) Localized generation of heat as a result of using a single large battery. (b) Distribution of heat generation throughout the 3D IC structure using distributed batteries.

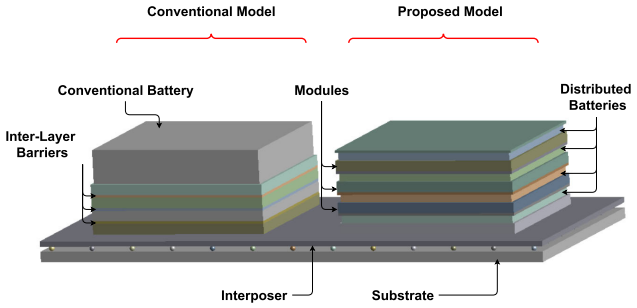


FIGURE 5. Geometry employed to directly compare the thermal performance of the conventional and proposed approaches. The conventional model is situated on the left side, while the proposed model is located on the right side.

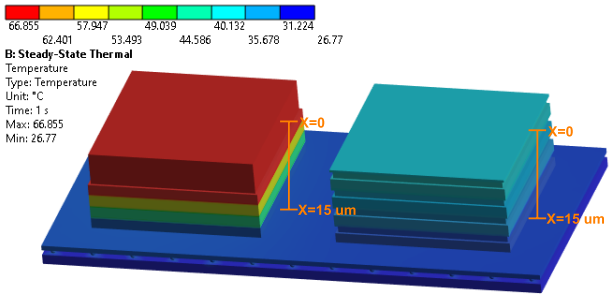


FIGURE 6. Simulation temperature distribution within 3D IC structures due to battery heat dissipation in two cases: (left) a single large battery, and (right) a fully-distributed battery (one per die).

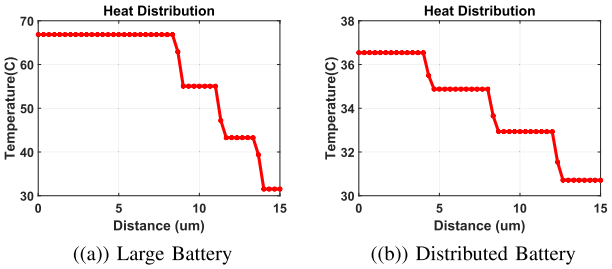


FIGURE 7. Simulated temperature distribution along the vertical axis (x) in Fig. 6 through one edge of a 3D IC in two cases: (a) a single large battery, and (b) a fully-distributed battery (one per die).

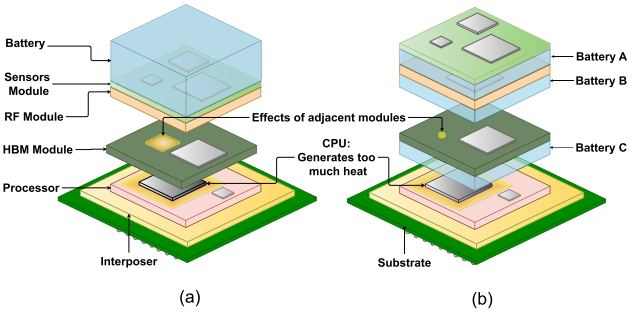


FIGURE 8. (a) Generation of hotspots and their effects on adjacent modules. (b) Distributed batteries serve as thermal buffers that hinder the formation of hotspots.

To facilitate a direct comparison of thermal performance between the conventional and proposed approaches, we designed a geometry that integrates both ideas on a single interposer, as shown in Fig. 5. This allows us to evaluate the benefits of the proposed approach and identify any issues that need to be addressed to optimize its performance.

Fig. 6 shows thermal simulation results of 3D IC structures using conventional (left) and distributed (right) batteries. For this simulation, the large battery supplies 100 mA to power the entire 3D stack, which matches its capacity (assumed to be 100 mAh). On the other hand, each battery in the proposed model supplies only one module, resulting in much lower output current; however, the sum of all these currents is equal to 100 mA. ANSYS software was utilized to simulate the resulting temperature distribution, which is clearly much more uniform for the distributed battery structure as expected. This difference is evident even more clearly in Fig. 7, which shows the simulated temperature along the vertical (x) axis through one edge of the 3D stack. Note that the temperature of the substrate was set to a fixed value of 27°C (modeling a perfect heat sink) in both cases and convection was neglected.

Certain components within 3D ICs, such as power amplifiers and processors, are particularly power-hungry and thus generate a significant amount of heat. These components can generate additional hotspots within the 3D structure that may impact nearby modules. One issue caused by such hotspots is physical strain resulting from thermal expansion. This problem is illustrated in Fig. 8(a). The use of distributed batteries can significantly reduce this problem since individual battery modules act as thermal buffers that hinder the formation of hotspots, as shown in Figure 8(b).

The qualitative advantages mentioned above were quantified using a thermal simulation of the same geometry as in Fig. 5. However, in this case, only a single die (within module #3) was assumed to dissipate energy, thus acting as a localized heat source. Fig. 9 shows that the use of a distributed battery greatly reduces both the hotspot and its impact on neighboring modules. Figs. 10(a)-(b) plot the temperature data along a path across the top surface of the module in more detail. The single battery case results in a hotspot with a maximum temperature rise of ∼15°, while

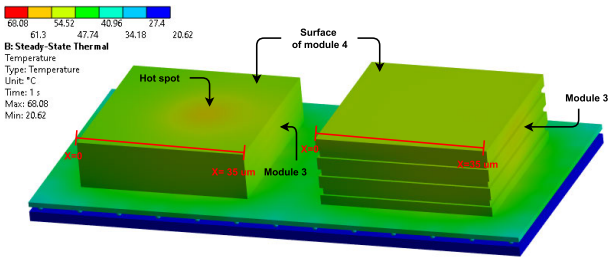
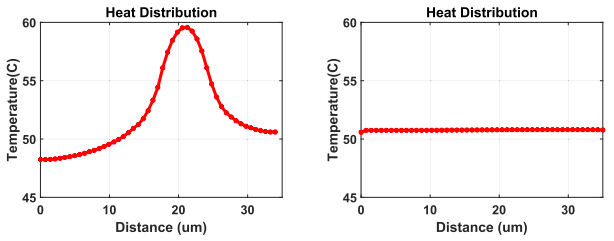
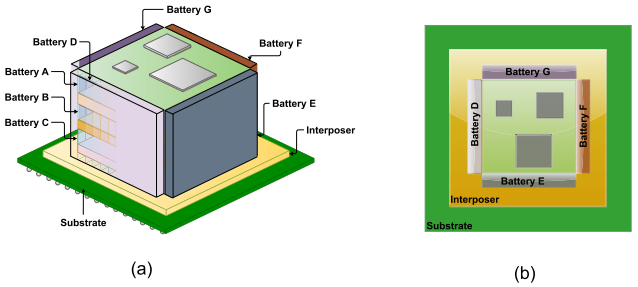


FIGURE 9. Simulation temperature distribution within 3D IC structures due to heat dissipation within a single die in two cases: (left) a single large battery, and (right) a fully-distributed battery (one per die). Top-mounted batteries are not displayed for clarity.



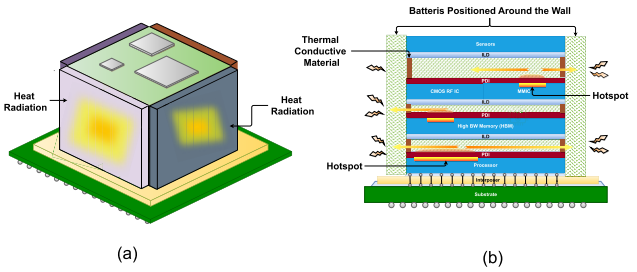
((a)) Large Battery ((b)) Distributed Battery

FIGURE 10. Temperature distribution generated by a localized heat source (a single die inside module #3): (a) a single large battery, and (b) a fully-distributed battery (one per die). In both cases, the temperature was measured along a path between two opposing edges on the surface of the top module.



(a) (b)

FIGURE 11. Batteries mounted on the walls of a 3D IC: (a) side view, and (b) top view.



(a) (b)

FIGURE 12. Batteries mounted on the walls function as an efficient heat sink: (a) side view, and (b) front view.

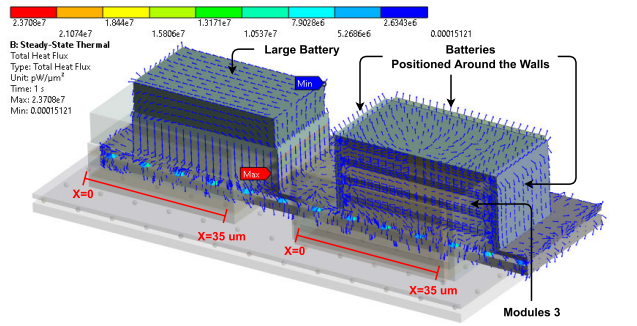
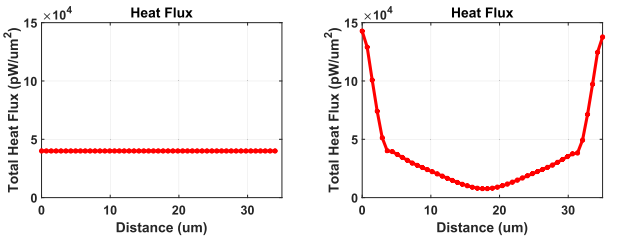


FIGURE 13. Simulation results for heat flux inside a 3D IC structure: (left) large battery, (right) combination of horizontal and vertical distributed batteries.



((a)) Large Battery ((b)) Distributed Battery

FIGURE 14. Heat flux along the path from two opposing edges on the surface of module #3: (a) large battery, and (b) distributed battery.

the distributed battery case results in an almost uniform temperature distribution with a rise of only ∼5°C.

B. ADDITIONAL ENERGY STORAGE

Since 3D ICs often require a high power density per area, their overall form factor can be minimized by positioning additional batteries around the walls of the module, as shown in Fig. 11. This concept also reduces thermal resistance by increasing the battery surface area in contact with the ambient. As shown in Fig. 12, horizontally-oriented batteries can absorb heat from the modules and efficiently transport it to the wall-mounted batteries, thereby cooling the entire structure.

Fig. 13 shows the simulated heat flux inside a 3D IC structure for both the conventional (left) and proposed (right) structures. For simplicity, all modules within both structures were assumed to generate the same amount of heat. For the conventional structure, all heat flux from the upper modules finds its way to the lower modules, leading to high thermal resistance. By contrast, the proposed structure (combination of horizontal and vertical batteries) can easily conduct heat to the sides of the 3D IC structure with the help of an appropriate inter-layer material, thus decreasing the thermal resistance.

Fig. 14 plots heat flux data from Fig. 13 along a path across the surface of a single module. While the conventional structure experiences the same amount of heat flux throughout the module, the proposed structure redirects most of the heat flux to the edges, resulting in improved thermal management, reliability, performance, and power consumption.

C. EM INTERFERENCE AND SHIELDING

Another notable advantage of utilizing vertically-mounted batteries is their inherent ability to act as a two-layer electromagnetic shield. This characteristic offers an additional benefit by effectively reducing radiated EMI. The $\vec{E}$-field

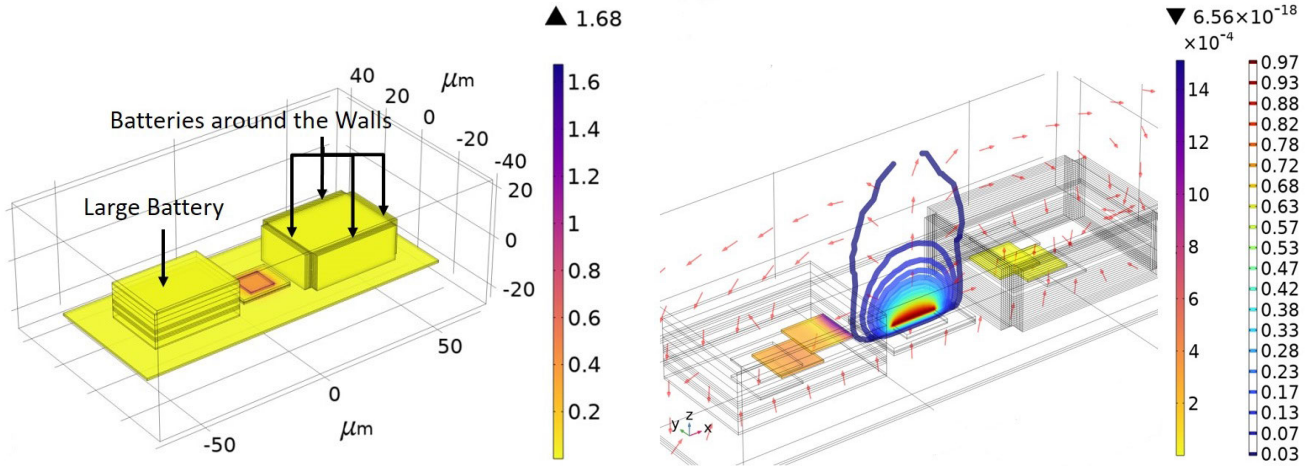


FIGURE 15. (a) $\vec{E}$-field on the surfaces of a 3D IC with (left) a large top-mounted battery, and (right) combination of horizontal and vertically distributed batteries. The voltage source is placed at the same distance from the two systems, and (b) $\vec{E}$ field on the surface of the same modules in both systems. The electric potential on the xz ($y = 0$) plane is also shown.

shielding provided by a typical battery geometry was evaluated through multiphysics simulations. For this purpose, we built a 3D model of the conventional and proposed systems on a substrate, as shown in Fig. 15. The system on the left has one large battery deposited at the top, while that on the right has four batteries distributed on different layers and four additional batteries mounted on the walls. The current collector materials of the batteries were assumed to be aluminum (cathode) and copper (anode).

Fig. 15(a) depicts the $\vec{E}$-field generated by a 1 V source is applied at a distance of 30 μm from both systems. The low field amplitudes on the surfaces of the 3D ICs qualitatively shows that they both act as good EM shields. Fig. 15(b) shows a more quantitative comparison of the shielding provided by the two systems. The system with distributed horizontal and vertical batteries provides $\sim$1000$\times$ (i.e., 60 dB) better shielding than the conventional structure.

Another advantage of the distributed batteries concept within 3D ICs is its ability to mitigate the potential impact of internal electromagnetic fields generated by batteries and charging processes, thereby enhancing the system's reliable operation. The proposed approach effectively addresses this issue by strategically distributing the batteries throughout the system, resulting in lower currents required from each battery compared to a single large battery. Consequently, the electromagnetic emissions produced by individual batteries are significantly reduced and spread across the system. This distribution of electromagnetic emissions prevents the high concentration of electromagnetic interference in specific areas, creating a more favorable environment for noise-sensitive or electromagnetic-sensitive modules to operate reliably. Furthermore, the reduced electromagnetic emissions from each distributed battery synergize with conventional shielding techniques. With lower levels of electromagnetic radiation, shielding can more efficiently minimize the impact on the surrounding EM, ensuring sustained system performance. Moreover, the proposed approach's distributed nature allows for greater flexibility in routing the charging paths for each battery. By strategically distributing these paths in locations less susceptible to electromagnetic interference, the impact of internal electromagnetic fields on sensitive circuitry is minimized. These considerations collectively contribute to improved electromagnetic compatibility and a reduction in the concentration of electromagnetic radiation within the system. As a result, the distributed batteries concept provides enhanced electromagnetic interference management, bolstering the overall reliability and efficiency of 3D IC systems.

D. POWER DELIVERY

In the conventional structure, the vertically stacked modules of the 3D IC are located at varying distances from a single battery. Modules located further away from the battery have longer power supply connections, which increases the impedance of the supply network. The unwanted series resistance and inductance generate voltage drops within the power delivery network (PDN). Consider the scenario in which a conventional on-chip battery, depicted in Fig. 16(a), supplies power to a power-hungry module such as a processor or memory. Such switching-intensive modules can generate significant $L(dI/dt)$ switching noise. Decoupling capacitors must be added near such noisy modules to decrease the impedance of the PDN, thus increasing the overall volume of the 3D IC.

The need for decoupling capacitors can be reduced by using shorter connections within the PDN, leading to proportionally smaller resistance and inductance. Distributed batteries are beneficial for this purpose, as shown in Fig. 16(b). The resulting PDN has greatly reduced connection lengths, and thus voltage drops. The smaller area of the power supply loops also results in significant decreases in radiated EMI. Finally, the distributed nature of the PDN increases isolation between the modules, which in turn limits the propagation of

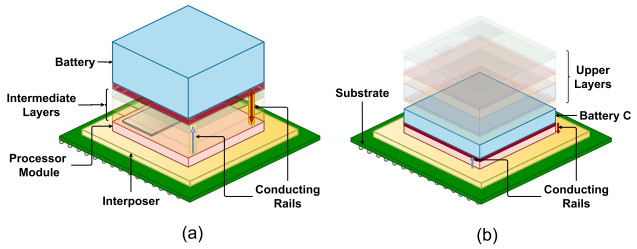


FIGURE 16. (a) Conventional designs require the use of lengthy connections to power the processor module. (b) Use of a distributed battery can shorten these connections and reduce unwanted series resistance and inductance in each rail.

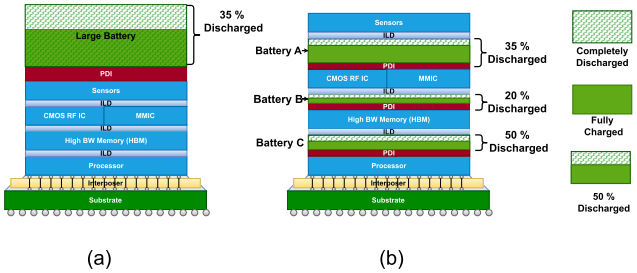


FIGURE 17. (a) Using a large battery increases its stress level, leading to premature failure. (b) The distributed battery concept aids in distributing the stress more uniformly between the batteries.

switching noise from noisy modules (such as processors) to sensitive ones (such as RF transceivers).

E. RELIABILITY

Reliability of the power supply is obviously critical for wireless and/or autonomous operation since no other energy sources are likely to be available. Using distributed batteries can improve reliability by providing redundancy to localized failures and/or unexpected increases in the power requirements of particular modules. In addition, the use of distributed batteries can prolong battery lifetime by limiting discharge rates and internal heat generation, as indicated in Fig. 17.

F. OPTIMIZED VOLTAGE REGULATION

Each module in a heterogeneous 3D IC typically requires its own supply voltage for optimal performance. These voltage levels may also need to be adjusted over time, e.g., due to the use of dynamic voltage scaling (DVS) to minimize the energy usage of digital processors. The utilization of these DC-DC converters leads to an increase in die area, the number of passive components, and system volume. DC-DC converters, both linear and switching types, depicted in Fig. 18, have extensive applications for converting and regulating DC voltages. Generally, larger switching mode power supplies are favored over smaller linear power supplies due to their high power efficiency, ideally reaching 100%. Compact switching power converters can be designed to operate at higher switching frequencies, but this leads to increased parasitic impedance, which reduces the overall power efficiency of the power delivery system. Therefore, these switching DC-DC regulators are not suitable for on-chip power conversion due to their large physical size and technology constraints, making on-chip integration more challenging. Therefore, when

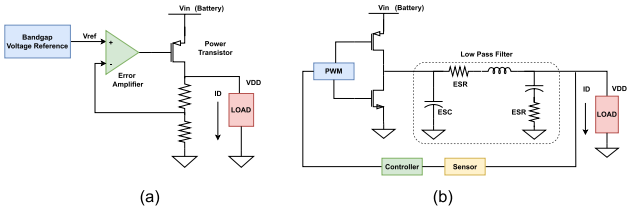


FIGURE 18. (a) Linear, and (b) switching DC-DC converters for converting and regulating DC voltages.

delivering high-quality power to the load circuitry within limited space, on-chip linear regulators should be considered. Linear regulators are preferred over switching power supplies, especially when dealing with small input-output voltage differences.

The size, complexity, and efficiency of a linear regulator are generally linked to two crucial parameters: the maximum load current and the dropout voltage. Assume, that a heterogeneous 3D IC with a single battery uses a low-dropout linear regulator (LDO) to supply current to several modules with similar supply voltage requirements. The die area of a linear regulator, A_{linear}, is mainly determined by the size of the output power transistor (assumed to be a MOSFET), which increases with peak load current, I_{DD}, as:

$$A_{Linear} \approx \alpha.W.L_{min} = \alpha \frac{I_{DD}.L_{min}^2}{\mu C_{ox}(V_{IN} - V_{th})^2} \qquad (2)$$

where V_{IN} is the unregulated battery voltage, V_{th} is the MOSFET threshold voltage, L_{min} is the minimum channel length, W is the channel width, α is the ratio of transistor area to WL_{min}, μ is the carrier mobility, and C_{ox} is the gate capacitance per unit area. An increase in I_{DD} results in a larger power transistor, leading to a more complex gate driver circuit. In the case of distributed batteries, since each linear regulator is responsible for providing current for only one module, the maximum current is lower compared to the conventional case where the linear regulator should provide current for several modules with the same voltage level. In this situation, multiple smaller linear regulators are needed to supply the necessary voltage and current for the entire system. On the other hand, the size and complexity of the error amplifier in the linear regulator are directly influenced by the load regulation requirements. If tight load regulation is needed, the error amplifier may need to be designed with higher gain and better precision. This can result in a larger and more complex circuit implementation, potentially involving more components and increased design complexity. Similarly, in the distributed battery structure, tight load regulation is less required compared to the conventional case.

The concept of distributed batteries is also beneficial for reducing power loss and improving the efficiency of linear regulators within 3D ICs. The power loss within an LDO is defined as Eqn. 3.

$$P_{Linear} \approx (V_{IN} - V_{DD}).I_{DD} + I_Q V_{IN} \qquad (3)$$

where V_{DD} is the regulated voltage level to the module and I_Q is the quiescent current. As the input-output voltage

difference increases in a linear DC-DC converter, the power dissipation within the linear voltage regulator also increases. By employing distributed batteries, each battery can be designed to generate a slightly higher voltage than the desired operating voltage (VDD) of the load circuitry. This approach helps reduce the input-output voltage difference in the linear DC-DC converter, thereby minimizing power dissipation and improving overall energy efficiency. Assuming $I_Q \ll I_{DD}$ in Eqn. 3, the efficiency of the LDO is approximately $\eta = V_{DD}/V_{IN}$, which is equal to the voltage transformation ratio. The distributed batteries concept, by reducing the input-output voltage difference, contributes to enhancing the efficiency of linear regulators.

The implementation of distributed batteries enables individual optimization of linear regulators to maximize their efficiency and simplify the design of each regulator. As a result, the overall volume, power consumption, and operating lifetime of the 3D IC can be enhanced.

IV. EXTENSIONS AND LIMITATIONS

A. APPLICABILITY

SiP and advanced packaging technologies such as 2.5D and 3D packaging have revolutionized the integration of multiple chips and components in the semiconductor industry. The use of combinations of 2.5D and 3D IC packages is becoming increasingly popular in a wide range of applications due to the many advantages they offer, such as improved performance, smaller form factor, and reduced power consumption. This is particularly useful in applications such as CPUs, mobile application processors, and display driver ICs, where high-performance computing is required in a compact form factor. The utilization of the distributed battery technique within SiP or advanced packaging technologies like 2.5D and 3D brings notable benefits. Firstly, by incorporating distributed batteries, power delivery becomes more localized and efficient, reducing the need for long power traces and minimizing power losses. This, in turn, enables the design of compact and densely integrated SiP solutions with improved power integrity. Secondly, the use of distributed batteries allows for flexible power management, as each module or sensor can be powered independently. This flexibility facilitates dynamic power allocation and optimization, enhancing the overall system performance and energy efficiency. Additionally, distributed batteries can be strategically placed near power-hungry components, mitigating voltage drop issues and reducing the impact of power supply noise. Furthermore, the distributed battery approach can enhance the reliability and fault tolerance of SiP systems. In case of battery failure, only the affected module is affected, while the rest of the system remains operational. This fault isolation capability reduces the impact of failures and simplifies maintenance and repair processes. As shown in Fig. 19, the proposed distributed battery technique is applicable to SiP, 2.5D, 3D IC packages and their combination. Furthermore, the benefits of our proposed distributed battery approach extend beyond SiP, 2.5D, and 3D IC packages. It is also applicable to monolithic ICs, where all components are integrated on a single chip. Even in this scenario, the distributed battery technique proves to be advantageous.

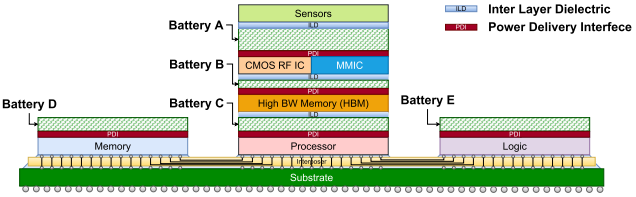


FIGURE 19. The proposed distributed battery technique enhances SiP and advanced packaging technologies like 2.5D and 3D.

B. OPERATING TEMPERATURE RANGE

Given the high energy density of 3D ICs, many applications require SSBs that can operate up to ∼70°C. Recent improvements in high-energy density SSB design are making such high operating temperatures feasible [20], [21]. For example, using a complex hydride as a solid electrolyte allows internal resistance to be reduced [22], thus enabling Li-ion SSBs that operate at temperatures up to 150°C with $< 10\%$ degradation in capacity. This feature makes these batteries a perfect fit for incorporation within 3D integrated circuits.

C. SELF-PROTECTION AND SMART THERMAL CONTROL

Safe usage of distributed batteries requires protecting against short-circuit faults, which can damage the 3D IC and its surroundings through excessive heat generation (i.e., thermal runaway). Physical safety measures such as fuses are valuable but only offer one-time protection with no guarantee of system recovery after the fault is cleared. The situation can be improved via active thermal control. For example, the distributed batteries can use ''smart'' thermoresponsive polymer electrolytes that prevent thermal runaway by automatically transitioning between low- and high-conductivity states [23], [24], [25], [26].

D. SYSTEMATIC APPROACH TO DETERMINING DISTRIBUTED BATTERY REQUIREMENTS

The determination of appropriate output voltage levels, capacities and the minimum number of distributed batteries in our 3D IC design takes into account a comprehensive set of factors, including the power requirements and profiles of the modules, system constraints, and performance goals. This process follows a systematic approach, commencing with a detailed analysis of the power profiles of each module. Peak and average power consumption, as well as specific power requirements during different operational states, are carefully considered to identify optimal voltage levels and capacity ranges that precisely align with the power needs of the modules. Consequently, the required number of batteries to fulfill these requirements is determined. Additionally, the battery-to-module relationship is established based on compatibility

factors such as chemistry, voltage, and current requirements. For effective power distribution, a well-thought-out strategy is developed, taking into account physical placement, interconnectivity, and thermal aspects to ensure seamless power delivery to each module from the distributed batteries. The battery distribution and configuration are refined using advanced simulation tools and optimization techniques, with the number of batteries being iteratively adjusted to achieve the most efficient distribution while satisfying all module power requirements. The process also includes a thorough consideration of factors like redundancy, system reliability, cost, and design constraints. Furthermore, the maximum number of batteries inserted inside 3D IC structure is carefully limited, taking cost and yield considerations into account. The selection of the appropriate electrochemistry entails a thorough evaluation of various battery types, encompassing factors such as energy density, power density, cycle life, safety features, and cost-effectiveness. The primary objective is to opt for battery chemistries that strike the most advantageous balance between performance, reliability, and cost-effectiveness for the intended application.

E. LIMITATIONS

One of the main issues with high-power modules such as processors, DRAM, or power converters is overheating, which can degrade the performance of nearby batteries. This is because these modules generate a significant amount of heat, which can be transferred to the batteries through conduction or radiation, leading to an increase in their operating temperature. This can pose a risk of elevated temperatures near the batteries, potentially compromising their performance and reliability. The degradation of battery performance can manifest as reduced capacity, increased internal resistance, and diminished overall power delivery. Batteries also reduce the interconnect density between adjacent modules, which may not be acceptable when very high inter-module bandwidths are required. In this case, one can move to a semi-distributed structure in which two adjacent modules can share one battery. Alternatively, vertical batteries mounted to the walls can be used to power some of the modules, as discussed in Section III. This approach involves using thin, high-capacity batteries that can be mounted vertically on the walls of the system. These batteries provide a high-power density and do not take up much space, making them an attractive option for powering modules that require a lot of power.

F. COMPLEXITY AND SCALABILITY

The fabrication of 3D ICs is complex and time-intensive, with layer count playing a significant role in the fabrication time. Additional layers introduce more process steps like deposition, lithography, etching, and metallization, contributing to overall fabrication time. Higher layer counts pose challenges in alignment and registration, requiring additional time for precise verification.

In addition to the impact of layer count, incorporating a distributed battery technology further adds to the complexity.

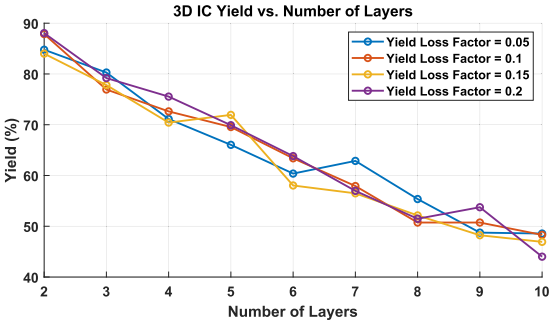


FIGURE 20. The plot illustrates the relationship between the number of layers and the corresponding yield, demonstrating a decrease in yield as the number of layers increases. Each layer's yield was determined as a random value ranging from 90% to 98%.

The integration of a distributed battery involves various considerations related to power management, thermal management, and safety mechanisms. Designers must ensure efficient power delivery to different components within the 3D IC while managing potential heat dissipation and adhering to safety standards. These considerations demand extensive testing, simulations, and optimization, which further extend the development timeline. Moreover, the integration of a distributed battery may require additional manufacturing processes, such as the deposition of energy storage materials and the implementation of battery management systems. These additional steps and requirements contribute to the overall fabrication time.

G. YIELD AND COST

In a distributed battery system, each individual battery can be considered as a distinct layer, each with its own yield considerations and testing challenges. As the number of layers in a 3D IC stack increases, the fabrication process becomes more complex, leading to an elevated likelihood of encountering defects. The yield in 3D ICs is directly linked to the successful production of each layer of the stack. Each layer can be viewed as an independent manufacturing step, and the overall yield of the 3D IC relies on the cumulative yield of all layers. The yield loss factor assumes a critical role in evaluating the efficiency and cost-effectiveness of the manufacturing process. A higher yield loss factor signifies a greater incidence of defects, resulting in a lower overall yield and increased costs for producing functional units.

Fig. 20 showcases the yield for different numbers of layers, considering various yield loss factors. It is evident that a higher number of layers corresponds to a reduced yield, which reflects the percentage of successfully manufactured and fully functional ICs. A lower yield implies the need to produce a larger quantity of ICs to achieve the desired number of functional chips, leading to escalated material and manufacturing expenses. Furthermore, lower yield levels translate into higher testing and validation costs, as more time and resources are required to identify and address defects. The plot in Fig. 21 further illustrates the relationship between

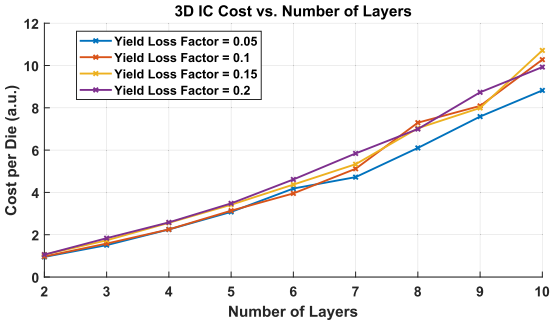


FIGURE 21. The graph showcases the correlation between the number of layers and the total cost in 3D IC fabrication, revealing a rise in cost as the number of layers increases. The yield for each layer was determined as a random value ranging from 90% to 98%.

the number of layers and the total cost involved in 3D IC fabrication for different yield loss factors.

It is important to evaluate the trade-offs when deciding to incorporate a distributed battery in a 3D IC design. While distributed battery technology can offer significant advantages, it comes at the cost of increased complexity and extended development timelines. Designers and manufacturers must strike a balance between these factors and prioritize their objectives to ensure the successful and timely commercialization of 3D ICs with distributed battery integration.

V. CONCLUSION

In conclusion, this paper explores the advantages of integrating distributed micro-batteries within heterogeneous 3D ICs for improved energy efficiency and performance. The proposed concept of distributed batteries addresses the challenges associated with conventional power distribution approaches and offers several benefits. The utilization of one battery per module significantly reduces heat generation and improves thermal performance. The simulation results demonstrate a more uniform temperature distribution of at least 40 percent compared to the conventional approach. The integration of distributed batteries also enhances power delivery by reducing voltage drops and electromagnetic interference. The smaller power supply loops and increased isolation between modules result in decreased radiated EMI and limit noise propagation. Furthermore, the use of distributed batteries improves reliability by providing redundancy and prolonging battery lifetime through controlled discharge rates and reduced internal heat generation. Additionally, the positioning of additional batteries around module walls improves thermal management, reliability, performance, and power consumption by reducing thermal resistance and redirecting heat flux. The vertically-mounted distributed batteries act as effective electromagnetic shields, providing significant shielding improvement compared to conventional structures. The proposed technique offers approximately 1000 times (60 dB) better shielding. Undoubtedly, it is crucial to recognize that the concept of distributed batteries in 3D ICs brings forth a host of benefits. However, these advantages are accompanied by increased intricacies, reduced yield, and elevated costs, all of which warrant careful evaluation when implementing the technology for specific applications.

REFERENCES

[1] X. Huang, C. Liu, and P. Zhou, "2D semiconductors for specific electronic applications: From device to system," *NPJ 2D Mater. Appl.*, vol. 6, no. 1, p. 51, Aug. 2022.

[2] M. Vinet et al., "Monolithic 3D integration: A powerful alternative to classical 2D scaling," in *Proc. SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2014, pp. 1–3.

[3] V. F. Pavlidis, I. Savidis, and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*. Oxford, U.K.: Newnes, 2017.

[4] K. Dhananjay, P. Shukla, V. F. Pavlidis, A. Coskun, and E. Salman, "Monolithic 3D integrated circuits: Recent trends and future prospects," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 3, pp. 837–843, Mar. 2021.

[5] G. Murali and S. K. Lim, "Heterogeneous 3D ICs: Current status and future directions for physical design technologies," in *Proc. Design, Autom. Test Eur. Conf. Exhib. (DATE)*, Feb. 2021, pp. 146–151.

[6] T. Li, J. Hou, J. Yan, R. Liu, H. Yang, and Z. Sun, "Chiplet heterogeneous integration technology—Status and challenges," *Electronics*, vol. 9, no. 4, p. 670, Apr. 2020.

[7] J. Kim, G. Murali, H. Park, E. Qin, H. Kwon, V. C. K. Chekuri, N. M. Rahman, N. Dasari, A. Singh, M. Lee, H. M. Torun, K. Roy, M. Swaminathan, S. Mukhopadhyay, T. Krishna, and S. K. Lim, "Architecture, chip, and package codesign flow for interposer-based 2.5-D chiplet integration enabling heterogeneous IP reuse," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 11, pp. 2424–2437, Nov. 2020.

[8] S. K. Gawali and M. K. Deshmukh, "Energy autonomy in IoT technologies," *Energy Proc.*, vol. 156, pp. 222–226, Jan. 2019.

[9] F. Goodarzy, E. S. Skafidas, and S. Gambini, "Feasibility of energy-autonomous wireless microsensors for biomedical applications: Powering and communication," *IEEE Rev. Biomed. Eng.*, vol. 8, pp. 17–29, 2015.

[10] Y. Duroc and G. A. Vera, "Towards autonomous wireless sensors: RFID and energy harvesting solutions," in *Internet of Things*, 2014, pp. 233–255. [Online]. Available: https://link.springer.com/chapter/10.1007/978-3-319-04223-7_10#citeas

[11] S. Zheng, X. Shi, P. Das, Z. Wu, and X. Bao, "The road towards planar microbatteries and micro-supercapacitors: From 2D to 3D device geometries," *Adv. Mater.*, vol. 31, no. 50, Dec. 2019, Art. no. 1900583.

[12] W. Lai, C. K. Erdonmez, T. F. Marinis, C. K. Bjune, N. J. Dudney, F. Xu, R. Wartena, and Y.-M. Chiang, "Ultrahigh-energy-density microbatteries enabled by new electrode architecture and micropackaging design," *Adv. Mater.*, vol. 22, no. 20, pp. E139–E144, May 2010.

[13] Y. Li, J. Qu, F. Li, Z. Qu, H. Tang, L. Liu, M. Zhu, and O. G. Schmidt, "Advanced architecture designs towards high-performance 3D microbatteries," *Nano Mater. Sci.*, vol. 2020, pp. 140–153, Oct. 2020. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2589965120300568

[14] F. C. Lee and Q. Li, "High-frequency integrated point-of-load converters: Overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127–4136, Sep. 2013.

[15] Y. Li, M. Zhu, V. K. Bandari, D. D. Karnaushenko, D. Karnaushenko, F. Zhu, and O. G. Schmidt, "On-chip batteries for dust-sized computers," *Adv. Energy Mater.*, vol. 12, no. 13, Apr. 2022, Art. no. 2103641, doi: 10.1002/aenm.202103641.

[16] M. Nathan, D. Golodnitsky, V. Yufit, E. Strauss, T. Ripenbein, I. Shechtman, S. Menkin, and E. Peled, "Three-dimensional thin-film Li-ion microbatteries for autonomous MEMS," *J. Microelectromech. Syst.*, vol. 14, no. 5, pp. 879–885, Oct. 2005.

[17] J. Zhang, Y. Li, K. Cao, and R. Chen, "Advances in atomic layer deposition," *Nanomanufacturing Metrol.*, vol. 5, no. 3, pp. 191–208, 2022.

[18] M. El Hammoumi, V. Chaudhary, P. Neugebauer, and A. E. Fatimy, "Chemical vapor deposition: A potential tool for wafer scale growth of two-dimensional layered materials," *J. Phys. D, Appl. Phys.*, vol. 55, no. 47, Nov. 2022, Art. no. 473001.

[19] R. M. R. Pinto, V. Gund, C. Calaza, K. K. Nagaraja, and K. B. Vinayakumar, "Piezoelectric aluminum nitride thin-films: A review of wet and dry etching techniques," *Microelectron. Eng.*, vol. 257, Mar. 2022, Art. no. 111753.

[20] J. Liu, Z. Bao, Y. Cui, E. J. Dufek, J. B. Goodenough, P. Khalifah, Q. Li, B. Y. Liaw, P. Liu, A. Manthiram, Y. S. Meng, V. R. Subramanian, M. F. Toney, V. V. Viswanathan, M. S. Whittingham, J. Xiao, W. Xu, J. Yang, X.-Q. Yang, and J.-G. Zhang, "Pathways for practical high-energy long-cycling lithium metal batteries," *Nature Energy*, vol. 4, no. 3, pp. 180–186, Feb. 2019.
[21] X. Han, Y. Gong, K. Fu, X. He, G. T. Hitz, J. Dai, A. Pearse, B. Liu, H. Wang, G. Rubloff, Y. Mo, V. Thangadurai, E. D. Wachsman, and L. Hu, "Negating interfacial impedance in garnet-based solid-state Li metal batteries," *Nature Mater.*, vol. 16, no. 5, pp. 572–579, May 2017.
[22] H. Kawasoko, S. Shiraki, T. Suzuki, R. Shimizu, and T. Hitosugi, "Extremely low resistance of Li_3PO_4 electrolyte/$Li(Ni_{0.5}Mn_{1.5})O_4$ electrode interfaces," *ACS Appl. Mater. Interface*, vol. 10, no. 32, pp. 27498–27502, Aug. 2018, doi: 10.1021/acsami.8b08506.
[23] F. Mo, H. Li, Z. Pei, G. Liang, L. Ma, Q. Yang, D. Wang, Y. Huang, and C. Zhi, "A smart safe rechargeable zinc ion battery based on sol-gel transition electrolytes," *Sci. Bull.*, vol. 63, no. 16, pp. 1077–1086, Aug. 2018.
[24] J. Zhou, T. Qian, J. Liu, M. Wang, L. Zhang, and C. Yan, "High-safety all-solid-state lithium-metal battery with high-ionic-conductivity thermoresponsive solid polymer electrolyte," *Nano Lett.*, vol. 19, no. 5, pp. 3066–3073, May 2019.
[25] Z. Chen, P.-C. Hsu, J. Lopez, Y. Li, J. W. F. To, N. Liu, C. Wang, S. C. Andrews, J. Liu, Y. Cui, and Z. Bao, "Fast and reversible thermoresponsive polymer switching materials for safer batteries," *Nature Energy*, vol. 1, no. 1, pp. 1–2, Jan. 2016.
[26] T. Yu, P. Xue, S. Ma, Y. Gu, Y. Wang, and X. Xu, "Thermal self-protection behavior of energy storage devices using a thermally responsive smart polymer electrolyte," *ChemistrySelect*, vol. 7, no. 7, Feb. 2022, Art. no. e202104499.

PEYMAN DEHGHANZADEH is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of Florida, Gainesville, FL, USA. His current research interests include communication systems, RFIC design, analog and digital IC design, and hardware security.

JUNJUN HUAN (Member, IEEE) received the B.S. degree in electronic information engineering and the M.S. degree in electrical engineering from the University of Dayton, Dayton, OH, USA. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of Florida, Gainesville, FL, USA. His current research interests include electronics for ultrasound imaging and image-guided treatment, wearable medical sensors, and hardware security.

ROHAN REDDY KALAVAKONDA is currently pursuing the Ph.D. degree with the Department of Computer Engineering, University of Florida, USA. His research interests include designing multimodal sensor systems, prototyping, and validation of forward-backward hardware security solutions for the IoT devices.

SOUMYAJIT MANDAL (Senior Member, IEEE) received the B.Tech. degree from the Indian Institute of Technology (IIT) Kharagpur, India, in 2002, and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2009 and 2004, respectively. He was a Research Scientist with SchlumbergerDoll Research, Cambridge (2010–2014); an Assistant Professor with the Department of Electrical Engineering and Computer Science, Case Western Reserve University, Cleveland, OH, USA (2014–2019); and an Associate Professor with the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA (2019–2021). He is currently a Senior Engineer with the Instrumentation Division, Brookhaven National Laboratory, Upton, NY, USA. He has over 175 publications in peer-reviewed journals and conferences and holds 26 patents. His research interests include analog and biological computation, magnetic resonance sensors, low-power analog and RF circuits, and precision instrumentation for various biomedical and sensor interface applications. He was a recipient of the President of India Gold Medal, in 2002, the MIT Micro-Systems Technology Laboratories (MTL) Doctoral Dissertation Award, in 2009, the T. Keith Glennan Fellowship, in 2016, and the IIT Kharagpur Young Alumni Achiever Award, in 2018.

SWARUP BHUNIA (Senior Member, IEEE) received the B.E. degree (Hons.) from Jadavpur University, Kolkata, India, the M.Tech. degree from the Indian Institute of Technology (IIT) Kharagpur, and the Ph.D. degree from Purdue University, West Lafayette, IN, USA. He is currently a Professor and a Semmoto Endowed Chair with the University of Florida, Gainesville, FL, USA. Earlier, he was appointed as the T. and A. Schroeder Associate Professor of electrical engineering and computer science with Case Western Reserve University, Cleveland, OH, USA. He has over ten years of research and development experience with over 200 publications in peer-reviewed journals and premier conferences. His research interests include hardware security and trust, adaptive nanocomputing, and novel test methodologies. He received the IBM Faculty Award, in 2013, the National Science Foundation CAREER Award, in 2011, the Semiconductor Research Corporation Inventor Recognition Award, in 2009, and the SRC Technical Excellence Award as a Team Member, in 2005, and several best paper awards/nominations. He has been serving as an Associate Editor for IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS, and *ACM Journal on Emerging Technologies in Computing Systems*. He served as the Guest Editor for IEEE DESIGN & TEST OF COMPUTERS, in 2010 and 2013, and IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, in 2014. He has served on the organizing and program committees for many IEEE/ACM conferences.