IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 23 July 2023, accepted 11 August 2023, date of publication 15 August 2023, date of current version 25 August 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3305571

RESEARCH ARTICLE

A 16.5-μW 73.7-dB-SNDR Second-Order Fully Passive Noise-Shaping SAR ADC With a Hybrid Switching Procedure

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This work was supported by the Science and Technology Program from State Grid Corporation of China through the Development of Flexible Liquid Metal Based Micro-Sensor With Anti-Electromagnetic Interference Ability for Power Engineering Applications under Grant 5700-202155453A-0-0-00.

ABSTRACT Noise-shaping (NS) successive approximation register (SAR) analog-to-digital converters (ADCs) using passive integrators have drawn increasing attention owing to their simplicity and power efficiency. However, a capacitor array with a passive integrator result in a huge number of unit capacitors and power consumption. This paper presents a second-order fully passive NS-SAR ADC with a segmented capacitor array and a hybrid switching procedure. We use a most-significant-bit(MSB) sampling-segmented capacitor array to reduce the number of unit capacitors, and a common mode voltage(VCM)-based hybrid switching procedure to reduce the average switching power. Compared to fully passive NS-SAR ADCs with conventional capacitor array and switching procedure, the total number of unit capacitors is reduced by about 84%, and the average switching power is also reduced by about 97.8%. The prototype was fabricated using 180nm complementary metal oxide semiconductor(CMOS) technology, it only uses 478 unit capacitors, resulting in an area of 0.086 mm^2. It consumes 16.5 μW, achieves 73.7 dB peak signal-to-noise-and-distortion ratio(SNDR), and a Schreier figure of merit(FoMs) of 165.5 dB.

INDEX TERMS Analog-to-digital converter (ADC), successive approximation register (SAR), segmented capacitor array, noise-shaping (NS), hybrid ADC, energy efficient, switching procedure.

I. INTRODUCTION

The analog-digital converter(ADC) serves as a bridge connecting the digital and analog worlds. The Successive approximation register (SAR) ADC is often used in sensor interface circuits because of its low power consumption. However, creating a high-precision SAR ADC (> 10 bit) would require a significant number of unit capacitors. This would result in a substantial area and pose challenges in terms of capacitor layout. Furthermore, comparator noise is a crucial issue that limits the precision of SAR ADC. To reduce comparator noise, a significant amount of power consumption is required. Delta-sigma (Δ-Σ) ADCs can achieve high precision through oversampling and noise shaping(NS) techniques, but the use of high-performance amplifiers increases design complexity and power consumption, making it unsuitable for low-power systems.

The NS-SAR ADC is a hybrid structure combining Δ-Σ ADC and SAR ADC. As illustrated in Fig. 1, a SAR ADC comprises switches, a capacitor array, a comparator, and a

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

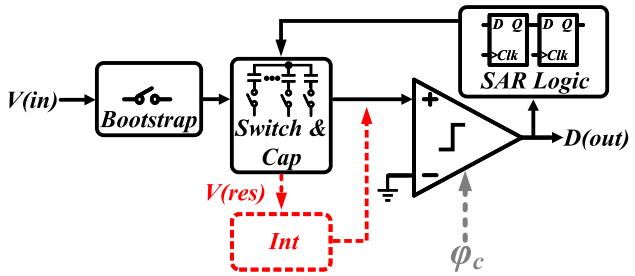

FIGURE 1. Architecture of NS-SAR ADC.

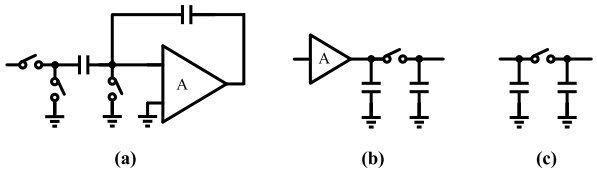

FIGURE 2. Architecture of integrators: (a) closed-loop OTA-based integrator; (b) open-loop amplifier-based integrator; and (c) passive integrator.

SAR logic circuit. The addition of an integrator in the loop results in a NS-SAR ADC.

To achieve higher accuracy and lower power consumption, scholars have proposed different structures of integrators used in NS-SAR ADC. The closed-loop OTA-based NS-SAR ADC achieves a sharp noise transfer function(NTF), which ensures high resolution [1], [2], [3]. The gain of the closed-loop is determined by the ratio of the capacitors, providing excellent process, voltage, and temperature(PVT) stability, as illustrated in Fig. 2(a). However, the significant static power consumption incurred by OTA renders this structure unsuitable for low-power systems. To reduce power consumption, [4], [5] proposed a type of NS-SAR ADC based on open-loop amplifiers, as shown in Fig. 2(b). Open-loop amplifier not only exhibits strong noise suppression capabilities but also delivers high energy efficiency. However, the gain of open-loop amplifiers is highly affected by PVT, necessitating the additional design of calibration circuits to ensure circuit stability, thereby increasing circuit design complexity. The incorporation of switches and capacitors is all that is required to form a fully passive NS-SAR ADC [6], [7], [8], [9], as shown in Fig. 2(c). Such NS-SAR ADC structures are characterized by their simplicity, extremely stable PVT performance, and absence of static power consumption, which allows for high energy efficiency, making them highly suitable for low-power systems.

In a fully passive NS-SAR ADC, the capacitor that makes up the passive integrator is closely related to the capacitor array. As an essential component of the SAR ADC, the capacitor array, which can also be referred to as a digital-to-analog converter(DAC), has a significant impact on the overall performance. Even the most recent studies require a 9-10 bit DAC to achieve > 12 bit ENOB, employing such a large DAC would occupy a significant amount of space and consume a great deal of energy. Moreover, it would also raise concerns regarding driving capability.

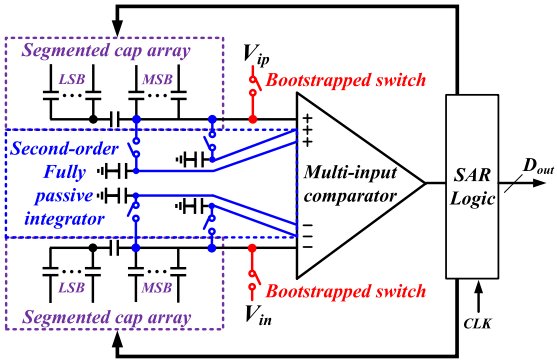

FIGURE 3. Architecture of proposed NS-SAR ADC.

For an N bit conventional binary capacitor array-based NS-SAR ADC, at least 2^N unit capacitors are required to make up the DAC. The passive integrator is also composed of unit capacitors, with the number typically being a multiple of 2^N. The NS-SAR ADC proposed in [7] uses a total of 4.6 $\times 2^N$ unit capacitors and only achieves first-order NS. [8] uses a total of 7 $\times 2^N$ unit capacitors to achieve second-order NS. In [9], a two-step residual voltage acquisition method is used, which can slightly reduce the total amount of capacitors required($\approx 6.6\times 2^N$), but it leads to attenuation of the residual voltage.

A segmented capacitor array is highly suitable for fully passive NS-SAR ADC as it reduces the number of unit capacitors required for both the capacitor array and the passive integrator. Moreover, implementing a common mode voltage(VCM)-based switching procedure can effectively minimize switch power consumption. However, conventional segmented capacitor arrays typically set the bridging capacitors to fractional multiples of the unit capacitor [10], [11], [12], which poses challenges for achieving matching. In order to improve matching, a split and segmented CDAC with little VCM shift is proposed in [13]. However, VCM shift leads to variations in the input noise and offset of the comparator. In [14], a split and segmented capacitor array is proposed, but it requires splitting the most significant bit(MSB) capacitor to achieve VCM-based switching procedure, thereby increasing circuit complexity. Another segmented capacitor array is presented in [15], but the use of the bottom sampling technique results in increased input capacitance.

This paper presents a second-order fully passive NS-SAR ADC that utilizes a 5+4 bit MSB sampling-segmented capacitor array. We use the MSB segment capacitors for top-plate sampling to reduce number of unit capacitors, and employ a VCM-based hybrid switching procedure to save power consumption. Therefore, the proposed structure requires 84% fewer unit capacitors than [7] and 89% fewer unit capacitors than [8], respectively. The average switching energy is also reduced by 97.8% compared to the conventional NS-SAR ADC. Fabricated in 180nm CMOS technology, the prototype consumes 16.5 μW from a 1.5-V supply while operating at 500 kS/s, and occupies an area of

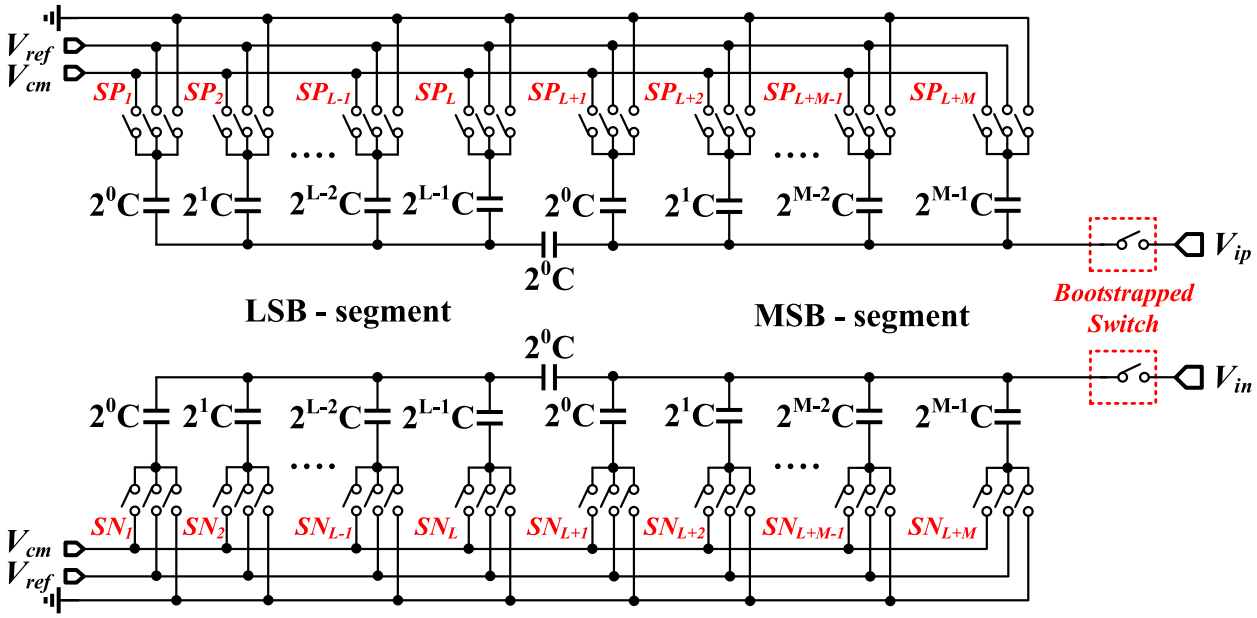

FIGURE 4. Architecture of MSB sampling-segmented capacitor array.

0.0864mm^2. It achieves 73.7 dB of SNDR over the bandwidth of 25 kHz at the OSR of 10, leading to a Schreier figure of merit(FoMs) of 165.5 dB.

The rest of this paper is organized as follows. Section II presents the architecture of the proposed second-order fully passive NS-SAR ADC, including segmented capacitor array, second-order fully passive integrator, multi-input comparator, and SAR logic control circuit. Section III shows the measurement results. Conclusions are given in Section IV.

II. ARCHITECTURE

Fig. 3 illustrates the proposed second-order fully passive NS-SAR ADC, both capacitor array and passive integrator are composed of unit capacitors. The operating process of the NS-SAR ADC can be divided into four steps: sampling, conversion, obtaining the residual voltage, and processing the residual voltage. Firstly, the bootstrapped switches sample the signal to the top plate of the MSB capacitors, and then the comparator begins to work. The comparison result will control the segmented capacitor array through the SAR logic. After the last bit comparison result is fed back to the capacitor array, the capacitor array stores the residual voltage of this cycle. Subsequently, the passive integrator processes the residual voltage through charge redistribution. In the next cycle, use a multi-input comparator to add the residual voltage to the input signal to achieve integration.

A. SEGMENTED CAPACITOR ARRAY

Fig. 4 illustrates the proposed segmented capacitor array. The top-plate sampling technique is capable of reducing both input capacitance and switch power consumption. During sampling, the input is sampled to the top plate of the MSB capacitor through a bootstrapped switch, which improves the linearity and sampling speed. At this point, the bottom plates of all capacitors are connected to VCM. After sampling, the bootstrapped switch is disconnected, and the comparator performs the first comparison directly. Based on the output of the comparator, MSB switches SP_{L+M} and SN_{L+M} will switch to V_{ref} or GND, and then the comparator will perform the next comparison. The ADC repeats the conversion process until the last bit comparison result is obtained and then feeds back the result to the capacitor array to obtain the complete residual voltage.

For the sake of clarity, we shall analyze each conversion of the proposed ADC using 3 bit as an example(The feedback step of the last bit was omitted). Fig. 5 illustrates the proposed hybrid switching procedure, where M=1 and L=2. Moreover, the power consumption for each bit conversion is also indicated on the diagram. Since the comparator performs its first comparison directly after the end of sampling, the first conversion does not consume any energy. Based on the result of the first comparison, the voltage of the bottom plate of the first capacitor in the MSB stage is switched, with an average energy consumption.

$$P = \frac{3}{14} C V_{ref}^2. \tag{1}$$

After the second comparison, the voltage of the bottom plate of the first capacitor in the Least Significant Bit(LSB) switches, resulting in the average switching energy of

$$P = \frac{3}{7} C V_{ref}^2. \tag{2}$$

Since the example has a low number of bits, and the switching energy is also dependent on the size of the

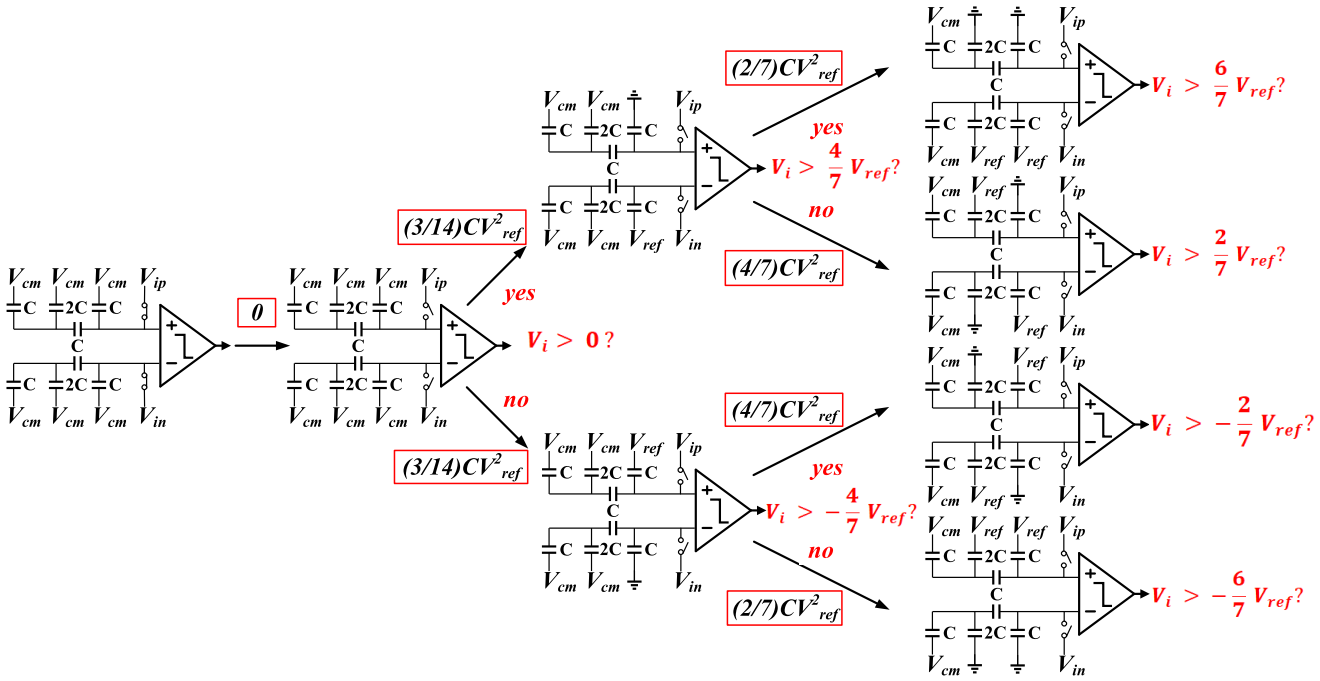

FIGURE 5. Proposed segmented capacitor array-VCM-based hybrid switching procedure.

capacitor, the power optimization brought about by the proposed architecture can not be well demonstrated.

For a segmented-capacitor array ADC with M+L=N bit, in order to simplify the equations for analysis, we specify

$$V_{cm} = \frac{1}{2}V_{ref}, \tag{3}$$

and each digital output code is equiprobable, the average switching power can be derived as

$$P = \left[\sum_{i=1}^{M} 2^{M-1-i}\left(1 - \frac{2^{N-i}}{2^N - 1}\right)\right] CV^2_{ref} + \left[\sum_{i=1}^{L} 2^{L-1-i}\left(1 - \frac{2^{N-i}}{2^N - 1}\right)\right] CV^2_{ref}. \tag{4}$$

When M = 5, L = 4, i.e. the ADC is 9 bit, the power consumption of the proposed capacitor array is only 15 CV^2_{ref}. This represents a reduction of 97.8% compared to the conventional switching procedure [16], 88.2% compared to the monotonic switching procedure [17], and 82.3% compared to the VCM-based switching procedure [18]. Fig. 6 shows a comparison of switching energy for the four methods versus the output code.

This is because the switching procedure retains the characteristics of the VCM-based switching procedure. During each switch toggle, one side of the capacitor array only switches between VCM and GND. In addition, the segmented structure greatly reduces the number of unit capacitors. For the MSB sampling-segmented capacitor array ADC with M+L=N bit,

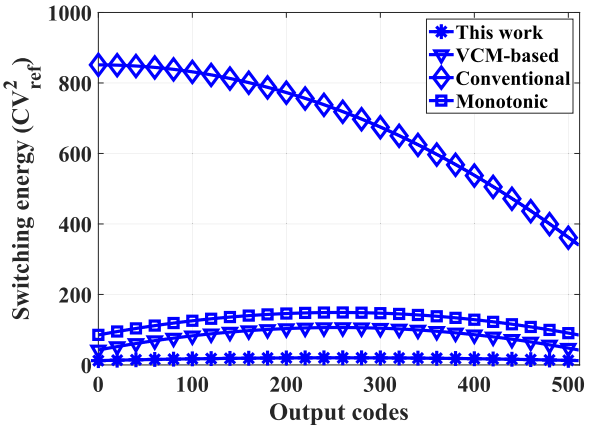

FIGURE 6. Switching energy versus output code.

the number of unit capacitors is

$$C = 2^M + 2^L - 1 = 2^M + 2^{N-M} - 1. \tag{5}$$

Taking the derivative concerning M yields

$$\frac{d}{dM}(2^M + 2^{N-M} - 1) = 2^{-M}(4^M - 2^N)log(2) \tag{6}$$

From (6), it can be concluded that the number of unit capacitors in the segmented capacitor array is minimized when $N = 2M = 2L$. The average power consumption and the number of unit capacitors for different switching procedures are shown in Table 1.

Although segmented capacitor arrays can effectively reduce the number of unit capacitors and power consumption,

TABLE 1. Comparison of switching procedures.

Switching procdure	Conventional [16]	Monotonic [17]	VCM-based [18]	This work
Switching power (CV_{ref}^2)	680.67	127.5	84.83	15
Normalized switching power	1	0.19	0.12	0.03
No. of capacitors	1024	512	512	94

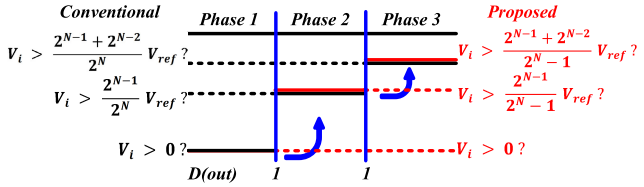

FIGURE 7. Comparison of two architectures at different phases.

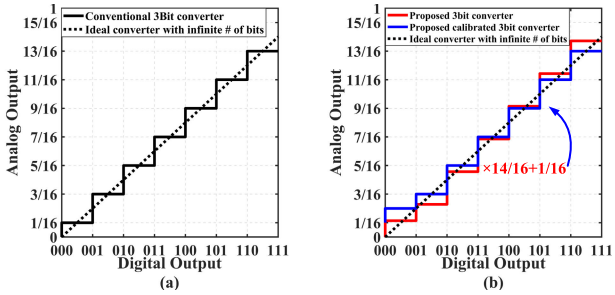

FIGURE 8. Comparison of transfer characteristic of two architectures: (a) conventional; and (b) proposed.

they also have the problem of matching difficulty because the bridging capacitor is often not an integer multiple of the unit capacitor. To ensure the matching of the bridging capacitor, we set its size to be the same as that of the unit capacitor. This results in a non-binary number of capacitors involved in the sampling process, making it different from conventional binary capacitor arrays. As shown in Fig. 7, in phase 1, similar to the conventional structure, the initial comparison of the proposed ADC is the same.

$$V_i > 0? \tag{7}$$

However, in phase 2, for the conventional structure, the comparison is

$$V_i > \frac{2^{N-1}}{2^N} V_{ref}? \tag{8}$$

for the proposed ADC, the comparison is

$$V_i > \frac{2^{N-1}}{2^N - 1} V_{ref}? \tag{9}$$

We have compared the conversion characteristics of these two structures, taking 3 bit as an example in both cases. Fig. 8(a) illustrates the conversion characteristic curve of the conventional ADC [19]. Similarly, according to Fig. 5, the

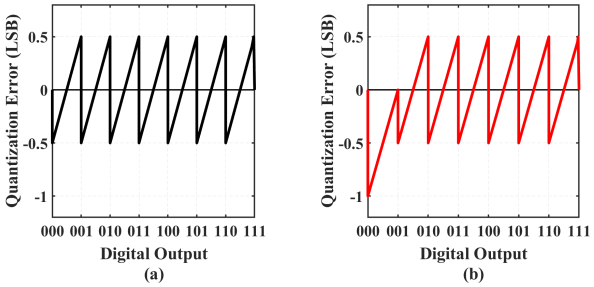

FIGURE 9. Comparison of quantization error of two architectures: (a) conventional; and (b) proposed.

conversion characteristic curve of the designed segmented array can be obtained, as shown by the red curve in Fig. 8(b). The slope of the red curve is multiplied by 14/16, and it is shifted upward by 1/16, corresponding to gain error cancellation and offset error cancellation, resulting in the blue curve, which differs from the conventional ADC conversion curve only when the digital output is "001". The black dashed line represents the conversion characteristic of an ideal ADC with infinite conversion accuracy.

Fig. 9 shows the quantization error for both architectures obtained by subtracting the analog output of the finite bit ADC from that of the ideal infinite bit ADC. According to the root mean square(RMS) formula for quantization noise.

$$Q(t)_{rms} = \sqrt{\frac{1}{T}\int_0^T Q(t)^2\, dt} \tag{10}$$

we calculate the RMS value of quantization noise for the conventional 3 bit ADC as

$$Q(t)_{rms} = \frac{\sqrt{\frac{1}{T}\int_0^T LSB^2(\frac{t}{T} - 0.5)^2\, dt} \times 7}{7} = \frac{LSB}{\sqrt{12}} \tag{11}$$

It should be noted that the quantization error curve in a conventional architecture remains the same within each period, whereas in the designed architecture, two quantization error curves need to be considered,

$$\begin{aligned} Q(t)_{rms} &= \frac{\sqrt{\frac{1}{T}\int_0^T LSB^2(\frac{t}{T} - 1)^2\, dt} \times 1}{7} \\ &\quad + \frac{\sqrt{\frac{1}{T}\int_0^T LSB^2(\frac{t}{T} - 0.5)^2\, dt} \times 6}{7} \\ &= \frac{8}{7} \times \frac{LSB}{\sqrt{12}} \end{aligned} \tag{12}$$

The proposed ADC has a signal-to-noise ratio (SNR) of approximately 1.16 dB lower than that of the conventional ADC for the same input signal. We modeled and simulated both architectures using MATLAB, and the Fast Fourier Transform(FFT) results are presented in Fig. 10. The SNR difference between the two architectures can be observed to be 1.09 dB.

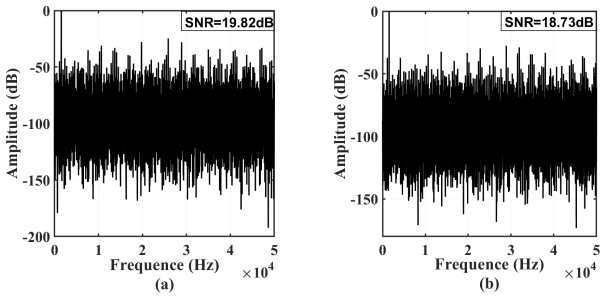

FIGURE 10. FFT result of two architectures: (a) conventional 3 bit ADC; and (b) proposed 3 bit SAR ADC.

TABLE 2. Comparison of SNR of two architectures.

SNR	Conventional(dB)	Proposed(dB)	difference(dB)
3 bit	19.82	18.73	1.09
4 bit	25.85	25.34	0.51
5 bit	31.84	31.60	0.24
N bit	$N \times 6.02 + 1.76$	$(N\times6.02+1.76)+$ $20\times\log(\frac{2^N-1}{2^N})$	$20\times\log(\frac{2^N-1}{2^N})$

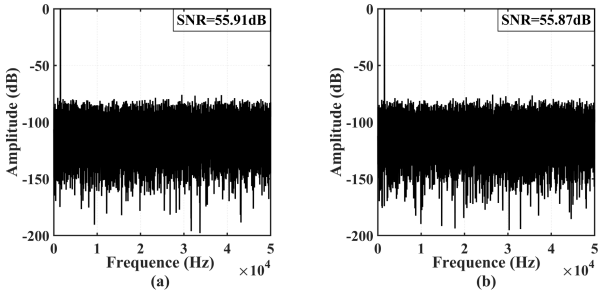

FIGURE 11. FFT result of two architectures: (a) conventional 9 bit ADC; and (b) proposed 9 bit SAR ADC.

SNR of the M+L=N bit proposed architecture will be lower than that of the N bit conventional architecture by

$$20 \times \log \frac{2^N - 1}{2^N} \ dB \tag{13}$$

As shown in (13), the effect of the proposed MSB sampling-segmented capacitor array diminishes with increasing resolution. The simulation results are presented in Table 2.

Fig. 11 presents the FFT results for 9 bit case, indicating a negligible difference in SNR between the two architectures. Considering the power and area optimization benefits of the proposed architecture, this minor negative impact can be disregarded.

B. SECOND-ORDER FULLY PASSIVE NS INTEGRATOR

Fig. 12(a) represents the second-order fully passive NS integrator. For clarity, the analysis is presented in the single-ended case. Fig. 12(b) illustrates the timing diagram. After the dynamic comparator controlled by φ_c completes its comparison in period N, at φ_1, C_1 is connected to the top plate of the MSB capacitors. The residual charge on the capacitor array from period N and the charge on C_1 from period N-1 are redistributed, completing the first integration. Subsequently, at φ_2, C_2 is connected to the top plate of the MSB capacitors. At this point, the residual charge on the capacitor array is redistributed with the charge on the C_2 from period N-1, completing the second integration. The proportion of charge redistribution is determined by the ratio of the capacitors involved. In the N+1 cycle, the integrated voltage on C_1 and C_2 from the previous cycle is combined with the input signal using a multi-input comparator.

Fig.12(c) depicts the signal flow diagram of the system, with the noise of each component also indicated in the diagram. $n_{\varphi s}$, $n_{\varphi(1,1)}$, $n_{\varphi(1,2)}$, and $n_{\varphi 2}$ represent the kT/C noise introduced by the switch capacitor, Q denotes the quantization noise of the system, V_{os} is the input offset voltage of the comparator, n_3 represents the input noise of the comparator, and n_4 refers to the noise generated by the DAC. The noise introduced during sampling is denoted as

$$\begin{aligned} {n_{\varphi s}}^2 &= \frac{kT}{C_{MSB} + C_E}, \\ C_E &= \frac{C_B \times C_{LSB}}{C_B + C_{LSB}} \end{aligned} \tag{14}$$

The noise introduced by φ_1 during the first integration is

$$\begin{aligned} {n_{\varphi(1,1)}}^2 &= \frac{kTC_1}{(C_{MSB} + C_E)(C_1 + C_{MSB} + C_E)} \\ &= \frac{3kT}{4(C_{MSB} + C_E)} \end{aligned} \tag{15}$$

$$\begin{aligned} {n_{\varphi(1,2)}}^2 &= \frac{kT(C_{MSB} + C_E)}{C_1(C_1 + C_{MSB} + C_E)} \\ &= \frac{kT}{12(C_{MSB} + C_E)} \end{aligned} \tag{16}$$

The noise introduced by φ_2 during the second integration is

$$\begin{aligned} {n_{\varphi 2}}^2 &= \frac{kT(C_{MSB} + C_E)}{C_2(C_2 + C_{MSB} + C_E)} \\ &= \frac{kT}{12(C_{MSB} + C_E)} \end{aligned} \tag{17}$$

From the signal flow diagram, the noise transfer function can be obtained as

$$NTF(z) = (1 - \frac{3}{4}z^{-1})^2 \tag{18}$$

It should be noted that the NTF is determined by the ratios between the capacitors and the ratios between the three inputs of the comparator.

And the total noise in the system of NS system can be obtained as

$$n_{tot} = n_{\varphi s} + 3n_{\varphi(1,2)} + 3n_{\varphi(1,1)}(1 - \frac{3}{4}z^{-1})$$

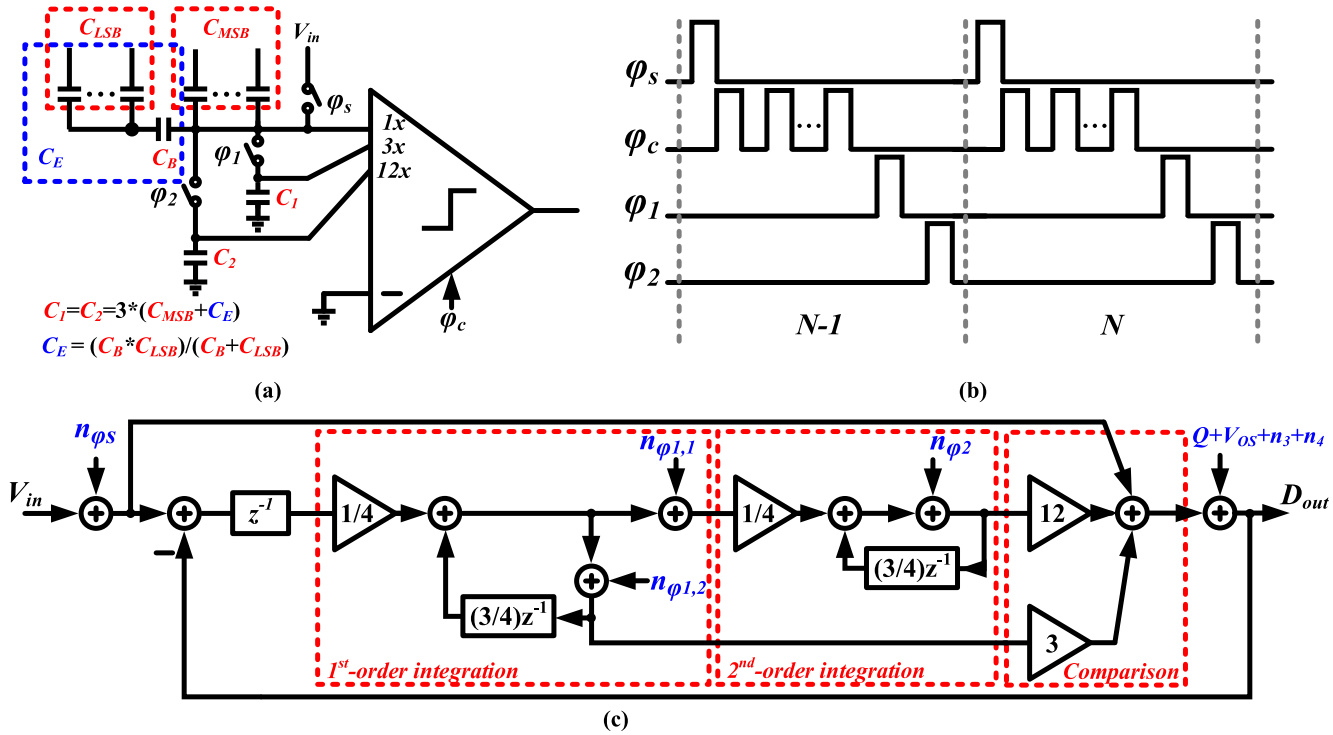

FIGURE 12. Proposed integrator (a) Simplified schematic (b) timing diagram (c) signal flow diagram with noise.

$$+ 12n_{\varphi 2}(1 - \frac{3}{4}z^{-1}) + (Q + V_{OS} + n_3 + n_4)(1 - \frac{3}{4}z^{-1})^2 \quad (19)$$

The above equation shows that $n_{\varphi s}$ and $n_{\varphi(1,2)}$ are not shaped, $n_{\varphi(1,1)}$ and $n_{\varphi 2}$ are subjected to first-order shaping through the loop. The quantization noise, input noise and offset voltage of the comparator, and the DAC noise are subjected to second-order shaping. This approach significantly reduces the complexity and power consumption of the comparator.

The MSB sampling-segmented capacitor array can simultaneously reduce the number of unit capacitors in the DAC and the passive integrator, thereby reducing chip area and power consumption. Taking 9 bit as an example, compared to the fully passive NS-SAR ADC proposed in [7] and [8], the number of unit capacitors can be reduced by 84% and 89%, respectively. We compared the number of unit capacitors used in three structures, and the results are shown in Fig. 13. As the resolution increases, the MSB sampling-segmented capacitor array can bring higher benefits, but higher resolution requires complex calibration circuits.

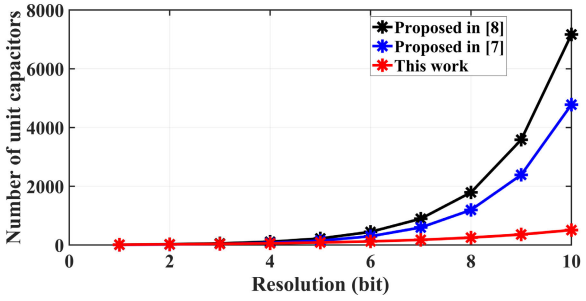

FIGURE 13. Comparison of the number of unit capacitor.

C. MULTI-INPUT COMPARATOR

To implement the addition of the input signal and the integration voltage, the system requires an adder. Expanding the comparator to accommodate multiple inputs and utilizing the tail current source to sum the currents can enable the realization of an analog adder. Using the strong arm latch [20] as the core of a multi-input comparator results in no static power dissipation, and it can be easily expanded to accommodate multiple inputs. Controlling the voltage gain by designing the size ratio of the input transistors in the multi-input comparator can achieve the NTF described in section B. The multi-input comparator is shown in Fig. 14, with a size ratio of 1:3:12 for the input transistor pairs.

The multi-input comparator introduces more input noise due to the increased number of input transistors. For the multi-input comparator designed in this project, the widths of the three input transistor pairs are W, $3W$, and $12W$, respectively. Compared to a classic one-path comparator with the same total input pair width of 16W (to keep the same comparator power consumption), the noise of the three-path

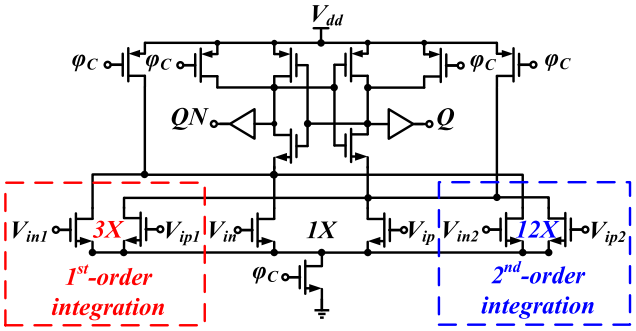

FIGURE 14. Multi-input comparator.

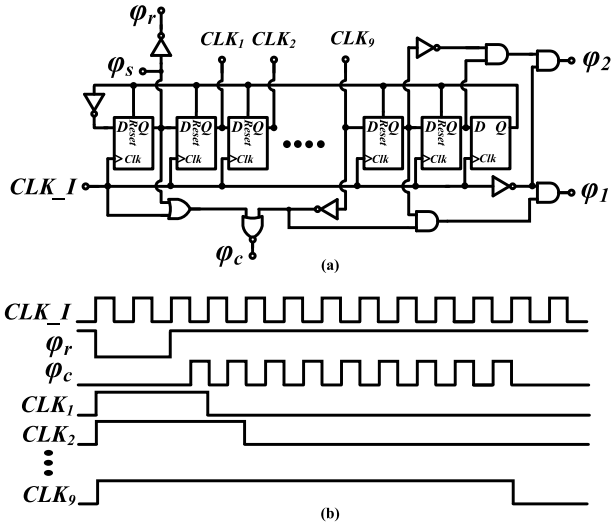

FIGURE 15. SAR logic (a) schematic (b) timing diagram.

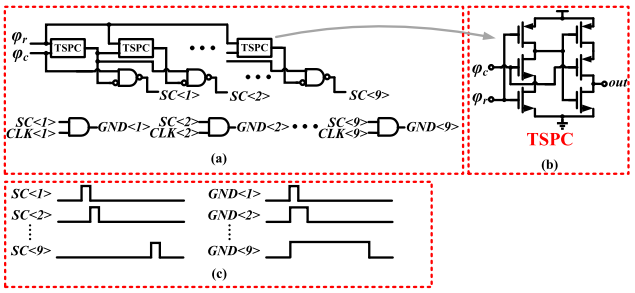

FIGURE 16. SAR and VCM-based control logic: (a) schematic of sequential select signal and VCM-based control signal generator, (b)TSPC, and (c) timing diagram of sequential select signal and VCM-based control signal.

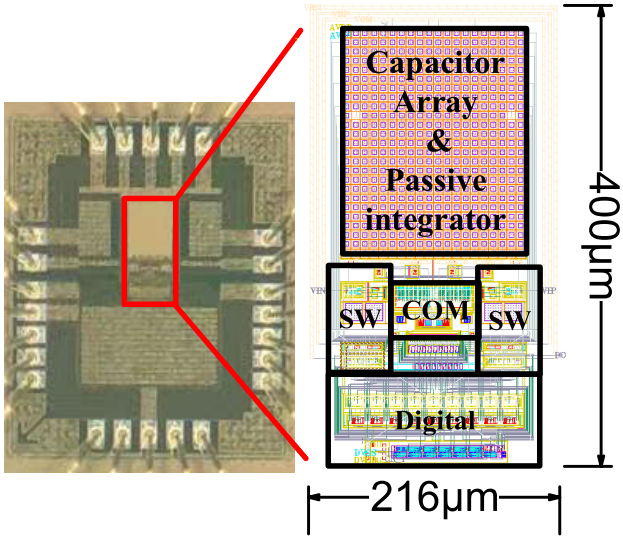

FIGURE 17. Die micrograph and the zoomed layout view.

comparator, when input referred to the 1X path, is 16 times larger than that of the one-path comparator [9]. As a result, even though the three-path comparator input referred noise is attenuated by 16 times due to NS, its net in-band noise is equal to that of the one-path comparator. However, it reduces the quantization error and increases SQNR. Compared to a classic SAR ADC with a one-path comparator, the proposed NS SAR ADC is actually beneficial.

D. SAR LOGIC

To achieve a low-power VCM-based switching procedure, we designed an internal clock signal using a frequency divider based on D-flip-flop. Fig. 15 shows the clock generation circuit and its timing diagram. For a proposed 9 bit NS-SAR ADC, 14 clock pulses are required to complete a conversion cycle. Therefore, if the sampling rate is 1MS/s, an external clock of 14MHz is required.

We used a chain of the true single-phase clock(TSPC) to form a shift register that generates the sequential select signal for latching the output of the comparator, as shown in Fig. 16(a). The circuit of the TSPC is shown in Fig. 16(b). The control signal of the VCM-based switching procedure is generated by using $CLK_1 - CLK_9$ and the sequential select signal. During the sampling process, all capacitor bottom plates are connected to V_{cm}. After sampling, they are sequentially disconnected from V_{cm} and connected to V_{ref} or GND. The sequential select signal and the VCM-based control signal are shown in Fig. 16(c).

III. MEASUREMENT RESULTS

The prototype was fabricated using 180nm CMOS process. The full micrograph is shown in Fig. 17. To provide a clearer display, the zoomed-in view of the core is a layout image. Thanks to the MSB sampling-segmented capacitor array, the number of unit capacitors in the circuit is greatly reduced. The area of the ADC core is 216 μm $\times$ 400 μm. The ADC consumes 16.5 μW from a 1.5-V supply at 500-kHz sampling frequency, which consists of power consumption from the supply voltage, reference voltage, and common mode voltage.

Fig. 18 shows the measured spectrum at an input signal frequency of 8.02 kHz and a sampling frequency of 500 kS/s.

TABLE 3. Comparison to state-of-art works.

specifications	ISSCC 12 [1]	ESSCIRC 16 [7]	MWSCAS 18 [22]	CICC 19 [23]	TCASI 21 [21]	TVLSI 14 [15]	*ISCAS 18 [11]	This work
Architecture	NS	NS	NS	NS	NS	segmented	segmented	NS-segmented
Process(nm)	65	130	180	65	130	90	180	180
Supply(V)	1.2	1.2	1.8	2.1	1.6	1.2	1.8	1.5
Sampling rate (MS/s)	90	2	0.128	80	0.128	100	10	0.5
Bandwidth(kHz)	11e3	125	2	2e3	2	50e3	5e3	25
SNDR(dB)	62	74	78.8	73.8	82.6	56.6	65.2	73.7
ENOB(bit)	10	12	12.8	11.97	13.4	9.1	10.5	11.95
Area(mm^2)	0.0323	0.13	0.2	0.081	0.2	0.18	0.12	0.0864
Power(μW)	806	61	74.2	2.1e3 w/buffer	40.8	3e3	620	16.5
**FoMs(dB)	163	167	153	164	160	158.8	164.3	165.5

*Simulation results

**FoMs= SNDR + $10\log_{10}$(BW/Power)

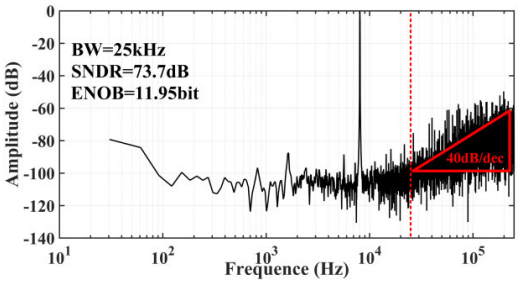

FIGURE 18. Measured ADC output spectrum.

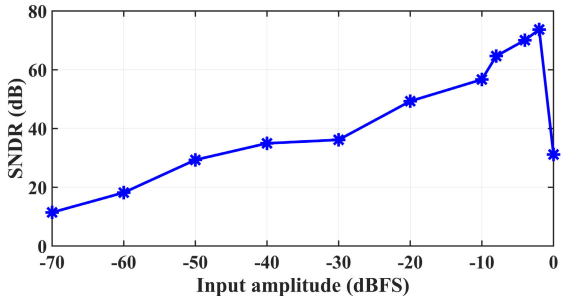

FIGURE 19. Measured SNDR versus input amplitude.

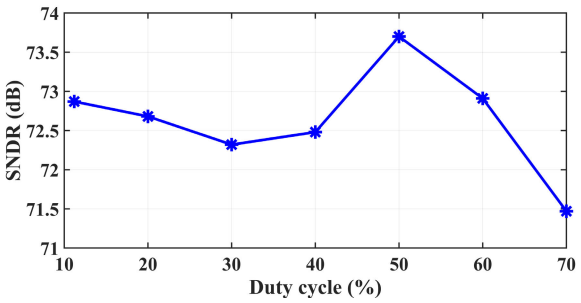

FIGURE 20. Measured SNDR versus the duty cycle of the input clock.

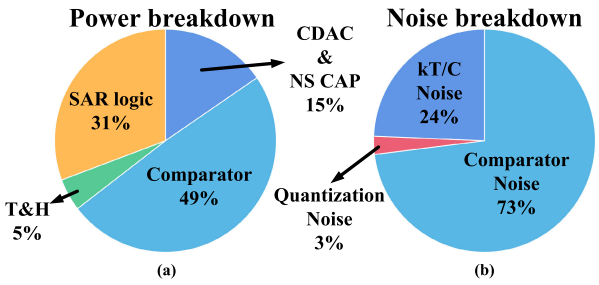

FIGURE 21. (a) Power breakdown (b) Noise breakdown.

The spectrum uses a 2^{14}-point FFT with a Hanning window. The proposed NS-SAR ADC has an SNDR of 73.7 dB at an OSR of 10. Fig. 19 shows the measured SNDR versus different input amplitude. The peak SNDR is 73.7 dB, and the dynamic range(DR) is at least 70 dB.

Fig. 20 shows the measured SNDR versus the duty cycle of the input clock, which affects the SAR logic circuit. It shows that the performance is not very sensitive to the duty cycle of the input clock.

Based on simulations, the ADC power and noise breakdown are shown in Fig. 21. The capacitor array and passive integrator power only occupy 15% of the total power due to the MSB sampling-segmented capacitor array and the hybrid switching procedure, and the comparator power occupies 49% as a result of the noise-limited width of multi-input pairs. Although shaped, the comparator noise is still the main source of system noise, accounting for 73%.

Table 3 shows the comparison of the performance of this prototype ADC with prior NS-SAR ADCs. It achieves 165.5 dB FoMs, which indicates that the energy efficiency of the proposed structure is relatively high. Compared to [7], although the FOMs value is slightly lower, the area is 34% smaller than it.

IV. CONCLUSION

This paper proposes a low-power, small-area, and robust second-order fully passive NS-SAR ADC. It uses a segmented capacitor array to reduce the number of unit capacitors used in DAC and passive integrator, which solves the problem of excessive use of unit capacitors in fully passive NS-SAR ADC. Meanwhile, a segmented-VCM-based hybrid switching procedure significantly reduces power consumption. It achieves 73.7dB-SNRD and consumes 16.5μW, which is suitable for low-power circuits, such as sensor front-end circuits.

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