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RESEARCH ARTICLE

# Optimized Modulation Scheme for Four-Leg Quasi Z-Source Inverter: Reducing Power Loss and Improving Output Quality

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**ABSTRACT** This study introduces a new three-dimensional space vector modulation technique for a four-leg quasi Z-source inverter (4L-qZSI) integrating a qZSN and a two-level four-leg inverter. The proposed method encompasses three variants, namely 3DZSVM2, 3DZSVM4, and 3DZSVM8, designed to enhance steady-state operations and harmonic distortions for 4L-qZSI. One of the main contributions of this research is the establishment of a new modulation technique for the 4L-qZSI. The proposed method amalgamates the benefits of SVMs in both abc and $\alpha\beta\gamma$ coordinates. The design processes of the 3DZSVM algorithm are carried out in the newly proposed $\rho\sigma\tau$ coordinates, while the space vector diagram (SVD) of the 4L-qZSI is utilized in the $\alpha\beta\gamma$ location. The proposed algorithm is applied in a single sector, optimizing time interval calculations and pulse creation without requiring trigonometric functions. Extensive simulation studies were conducted to validate the performance of the introduced modulation scheme for the 4L-qZSI. The simulation results show excellent steady-state performance and benefit over the conventional space vector modulation with zero sequences (CZPWM), including a power loss reduction of 50% and a 50% decrease in the THD of the output voltage. In addition, applying this technique results in enhanced output current quality, reduced power loss by 40%, and decreased inductive current ripple by 50% under unbalanced load conditions. Furthermore, the proposed 3DZSVM control strategy for 4L-qZSI is experimentally verified using the TMS320F28379D kit based on the Hardware-in-the-Loop (HIL) simulator. This demonstrates the practicality and effective performance of the suggested control strategy under unbalanced load conditions.

**INDEX TERMS** Four-wire system, quasi Z-source inverter, harmonic spectrum, space vector modulation, unbalanced load, power quality.

## I. INTRODUCTION

With the increased penetration of distributed solar and wind power, the output voltage quality in isolated power-supply systems is getting more concerned, where it must comply with several technical and performance standards [1], [2]. According to IEEE Standard 1547-2014, the current harmonic component, measured by the total harmonic distortion index (THD), must not exceed 5%. The distribution power supplies are generally three-phase and supply three-phase

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linear or nonlinear loads, with many single-phase loads. Therefore, the absorbed inter-phase currents are of different amplitudes, which causes the voltage to be unbalanced. This unbalanced voltage generates inverse and zero current components. However, the European standard EN 50160 recommends keeping the voltage unbalance factor (VUF) under 2% [3].

Nevertheless, unbalanced loading conditions occur in distributed energy generation systems in which the power is generated according to load demand. An unbalanced load absorbs unbalanced currents, resulting in more than the neutral line current in the three-phase systems. Moreover, it causes a high harmonic distortion in the system voltage and current [4], [5]. Consequently, some converters are used to cope with the neutral-line current, where the three commonly-used four-wire VSI configurations are three-phase three-leg VSI (3L-VSI) with capacitor midpoint, three-phase H-bridges VSI, and three-phase four-leg VSI (4L-VSI).

The initial configuration employs a 3L-VSI in conjunction with split dc-link capacitors [6], where the neutral line, also known as the fourth wire, is linked via the midpoint of these two capacitors. While this structure has its benefits, such as simplicity and minimal switch usage, it faces the drawback of low dc-link voltage utilization. This is caused by an uncontrolled $2\omega$ voltage ripple on the dc-link, necessitating larger capacitors to prevent current ripples [7]. The three-phase H-bridge setup includes three full-bridge inverters connected to the three-phase four-wire system through single-phase isolation transformers. Contrary to the 3L-VSI using split capacitors, this setup utilizes a lower dc bus voltage since the maximum voltage is seen across each H-bridge in the single-phase voltage instead of the three-phase voltage. However, the primary downsides of this three-phase H-bridge configuration are the augmented number of switch devices and the necessity of using transformers [8]. For inverters functioning in three-phase-four-wire systems, the third topology, the 4L-VSI, is considered the most advantageous option [9], [10]. It employs another fourth leg to manage the zero component current/voltage through the neutral wire. This setup boasts a multitude of benefits, including i) enhanced dc-link voltage utilization in comparison to the 3L-VSI configuration (15% higher), ii) diminished voltage ripple in the dc-link, iii) less necessity for a large dc-link capacitor, and iv) compactness in terms of size and volume [11], [12].

An extra leg in the 4L-VSI expands the switching states from 8 ($2^3$) to 16 ($2^4$). This enhancement leads to greater control flexibility and improves the quality of output voltage and current compared to the 3L-VSI.

Therefore, due to these advantages, 4L-VSIs are commonly utilized in different stand-alone and grid-connected scenarios, mainly distributed generation [5]. The 4L-VSI is typically linked with an inductive filter in grid-tied systems, facilitating controlled current injection into the grid. Additionally, the 4L-VSI has seen wide-ranging applications in various grid-connected scenarios, such as shunt active power filters [13] and distributed static compensators (DSTATCOM) [14]. For stand-alone applications like an uninterruptible power supply [15] and electric motor drives [16], the 4L-VSI, equipped with an LC filter, maintains regulated operation.

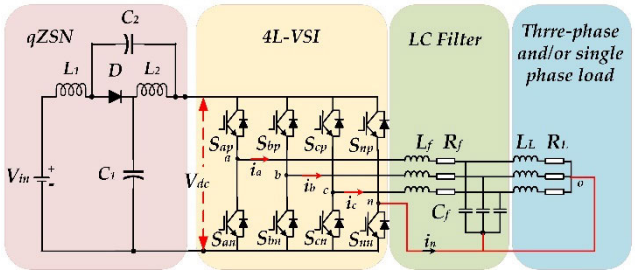


**FIGURE 1.** 4L-qZSI with an output *LC* filter.

Renewable energy sources (RESs) typically require two-stage power conversion to be integrated into the distributed power system. Therefore, a dc/dc converter is commonly used between the RES and the 4L-VSI to boost the input dc voltage [5]. However, such a dual-stage conversion increases the complexity of the control block, system cost, and size and decreases the system's efficiency [17]. Nevertheless, the single-stage inverter topology has several advantages over the dual-stage one, including fewer active switching devices, better efficiency, and higher reliability [18]. The quasi-Z-source inverter (qZSI) is one of the successful single-stage topology candidates for photovoltaic (PV) systems that have gained a lot of attention [19], [20]. Equipped with a straightforward impedance (*L, C*) network, qZSI can provide both buck/boost and dc/ac conversion operations in a single stage [21]. Although the three-phase, three-leg qZSI has found utility in numerous independent applications [22], it has several constraints. One of its primary drawbacks, which is also a driving reason for its design, is its capacity to cater only to balanced three-phase loads. On the other hand, the 4L-qZSI provides several benefits, including a fault-tolerant feature, increased reliability owing to the absence of a required dead time, and a diminished trip current resulting from the short circuit in each leg [23], [24]. Figure 1 illustrates a typical example of how the 4L-qZSI is applied in a stand-alone power system.

The literature review shows a few control schemes that have been investigated for the 4L-qZSI. These control strategies utilize nonlinear controllers, such as finite control set-model predictive control (FCS-MPC) [24], [25], [26].

The FCS-MPC has the following merits: simple concept, handling nonlinearity and constraints, controlling multiple variables in the same control law, and faster response during transients [27], [28], [29]. However, the effectiveness of FCS-MPC relies heavily on the system model's precision. Given the lack of a modulation stage, FCS-MPC functions at variable switching frequencies with a broad spectrum. However, this impacts the load harmonic spectrum, marking the biggest drawback of these methods [30], [31].

Numerous Pulse Width Modulation (PWM) strategies for the 4L-VSI have been put forth in the literature. For instance, Carrier-based PWM (CPWM) [31] requires the creation of an unbalanced voltage by introducing an offset voltage ($V_{fn}$) into the three-phase voltage reference, which is then used as the voltage reference for the fourth leg [32].

As a result, numerous improvements in discontinuous Pulse Width Modulation (DPWM) techniques have been suggested to reduce power loss in power devices by reducing the commutation frequency [33]. For example, a selective harmonics elimination (SHE) control approach for a three-phase 4L-VSI has been documented in [34]. This strategy helps to eradicate certain lower-order harmonics in a switching waveform, thereby enhancing the total harmonic distortion of the output wave.

On the other hand, space vector modulation (SVM) has proven to be an efficient PWM because it provides significant flexibility for optimizing the switching waveforms and is well-adapted for implementation [35], [36]. Three-dimensional space vector modulation (3DSVM) [37] strategies are commonly used for 4L-VSI. When comparing them to carrier-based PWM, the 3DSVM provides many improvements, such as high dc-link exploitation and low output distortion [38]. On the other hand, it has some inherent limitations due to the necessity of complex modeling and longer computational time [32].

To minimize the complexity and computation time, a streamlined 3DSVM for the four-leg multilevel inverter was previously proposed, which employs a single prism in the voltage space vector to determine all the switching sequences for the 3DSVM approach. However, as far as the authors know, no research has been conducted on the 3DZSVM for the 4L-qZSI up to this point. Consequently, this paper proposes an optimized 3DZSVM for the 4L-qZSI.

The optimized 3DSVM for the four-leg multilevel inverter was suggested to decrease complexity and computation time [39], [40]. This was accomplished by utilizing just one prism, representing a defined region or sector within the diagram where the proposed 3DZSVM strategy is applied, in the voltage space vector to compute all the switching sequences for the 3DSVM strategy. However, to the authors' knowledge, there has been no application of the 3DZSVM for the 4L-qZSI so far. Hence, this paper aims to introduce a new 3DZSVM for the 4L-qZSI.

The proposed 3DZSVM technique can simultaneously provide control objectives, i) output voltage reference tracking, ii) boosting the dc voltage at the desired value, and iii) compensating the zero-sequence output current. Furthermore, the proposed 3DZSVM algorithm is implemented only in one sector of the space vector diagram based on the idea proposed in [41] for the multilevel four-leg diode clamped converter (4L-DCC).

According to the chosen number of inserted shoot-through (*ST*),the proposed 3DZSVM is divided into three categories: 3DZSVM with eight *ST* (3DZSVM8), 3DZSVM with four *ST* (3DZSVM4), and 3DZSVM with two *ST* (3DZSVM2). These categories have been intensely discussed and investigated to reduce the inductor current ripple in the 4L-qZSI. To recap, the main contribution of this paper lies in proposing a new 3DZSVM algorithm for the three-phase 4L-qZSI, including a comprehensive investigation of its categories 3DZSVMx (x = 2, 4, and 8).

The remaining structure of this paper is as follows: Section II elaborates on the topology and operational principles of the 4L-qZSI. The basic premise of the 3DZSVM strategy is discussed in Section III. Section IV presents the proposed 3DZSVM for 4L-qZSI. Section V verifies and validates the efficacy of the proposed 3DZSVM through simulation results obtained from MATLAB/PLECS models, utilizing a 0.6-kVA 4L-qZSI, and evaluates the power losses compared to the CZPWM strategy. In Section VI, the advantages of the proposed 3DZSVM method are validated through the application of the Hardware-in-the-Loop (HIL) simulation. Lastly, the conclusions drawn from this paper are presented in Section VII.

## II. FOUR LEG-QUASI Z-SOURCE INVERTER

### A. CONVENTIONAL TOPOLOGY DESCRIPTION

Figure 1 depicts the 4L-qZSI topology with an *LC* output filter. There are two stages for investigating this topology: i) the qZS network and ii) the 4L-VSI with *LC* output filter and ac load. The qZS network (qZSN) comprises *LC* impedance components in the first stage of this topology, which can increase the dc voltage in response to the shoot-through zero states (*ST*) of the inverter switching cycle. The 4L-VSI will be used in the second stage of this topology, where the load neutral point is wired to the mid-point of the fourth leg to enable the flow of the zero sequence current/voltage, as seen in Figure 1. On the one hand, compared to the 3L-VSI, the integration of an additional leg (that is, the neutral leg) complicates the switching scheme. Nevertheless, adding a phase leg to the inverter increases its efficiency and performance. On the other hand, the 4L-VSI can be operated under balanced or unbalanced three-phase loads, as well as the capability to feed both three-phase and single-phase loads [12].

### B. PRINCIPLE OF 4L-qZSI

The qZSN, depicted in Figure 1, comprises two inductors ($L_1$ and $L_2$), two capacitors ($C_1$ and $C_2$), and a single reverse diode. These components are interconnected between the direct current (dc) input source ($V_{in}$), and the inverter is utilized [26], [42]. The qZSI can either decrease (buck) or increase (boost) the dc source voltage, eliminating the need for an extra dc-dc converter. This is accomplished by activating one to four legs concurrently, a process known as the ST state, something that traditional VSIs cannot perform. With the *LC* filter at the ac end, the qZSI has the flexibility to operate in two modes: as a standalone system supplying single or three-phase ac loads, or in a grid-tied mode. The qZSI's equivalent circuit, displayed in Figure 2, can be separated into two operational stages. The first of these is the ST state,

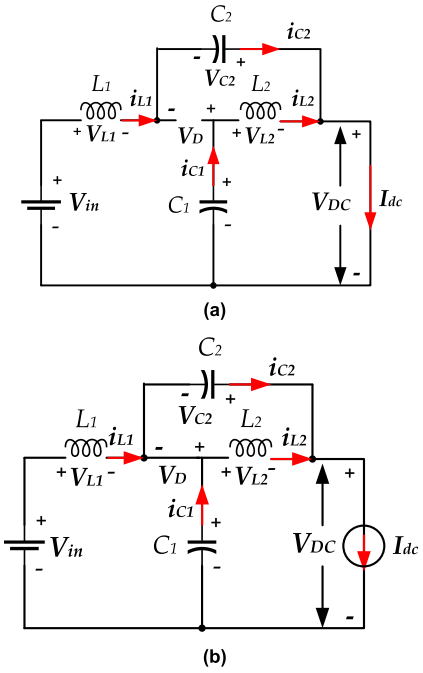


**FIGURE 2.** The 4L-qZSI's operational modes: (a) the ST state and (b) the active states.

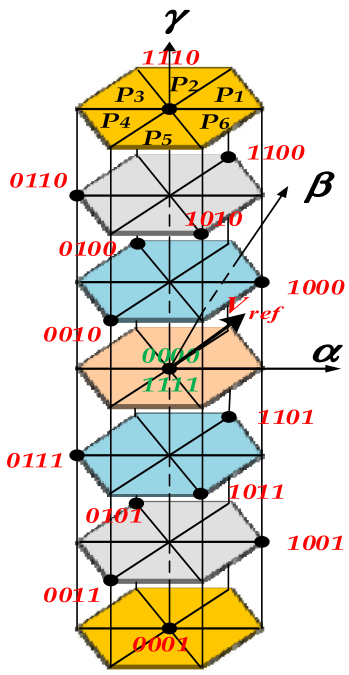


**FIGURE 3.** Switching vectors of 3DSVM.

during which both the upper and lower switches of the same phase-leg are turned *ON* at the same time.

In the given scenario, the dc input power, in conjunction with capacitors $C_1$ and $C_2$, concurrently transfers energy to inductors $L_1$ and $L_2$. First, the diode D is inhibited from conducting due to the negative voltage, as illustrated in Figure 2(a). The next mode is the active state (*ACT*), depicted in Figure 2(b), during which diode *D* is activated. In this state, the dc input power, assisted by the inductors, imparts energy to the ac loads while simultaneously charging the capacitors.

From the reference [43], during a steady state, the average voltages across capacitors $V_{C1}$ and $V_{C2}$ can be calculated, respectively.

$$V_{C1} = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_{in}, \quad V_{C2} = \frac{D_{ST}}{1 - 2D_{ST}} V_{in} \tag{1}$$

The maximum voltage across the dc-link is defined as

$$V_{DC} = V_{C1} + V_{C2} = \frac{1}{1 - 2D_{ST}} V_{in} = B.V_{in} \tag{2}$$

where $B$ is defined as the boost factor.

The $D_{ST}$, which represents the *ST* duty ratio, is calculated by dividing $T_{ST}$, the total *ST* duration by $T_S$, and the switching period.

## III. CONVENTIONAL 3DSVM FOR THE 4L-VSI

Generally, SVM strategies produce an average voltage vector identical to the reference voltage vector. Richard Zhang created the theory of 3DSVM, and it was first presented in [37]. Under an unbalanced load, the 3DSVM strategy has been considered one of the best switching schemes for a three-phase 4L-VSI [44]. The main objective of the 3DSVM algorithm is to produce the reference voltage vector by using the time average of four adjacent switching vectors in $\alpha\beta\gamma$ space. The switching voltage vector is defined during every switching period and state in the 4L-VSI. Figure 3 shows the three-dimensional representation of the switching vectors of the 4L-VSI in $\alpha\beta\gamma$ space. The matrix transformation between the *abc* and $\alpha\beta\gamma$ coordinates is given by Clarke transformation as:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3}$$

The switching vectors with 14 positions in three-dimensional space are viewed as a graphic domain of six prisms, as shown in Figure 3. Two zero switching vectors (1111, 0000) are placed in the middle layer of the $\alpha\beta\gamma$ space. According to the various voltage levels of $V_\gamma$, the other 14 active switching vectors are placed at seven different layers. Meanwhile, $V_\gamma$ presents the zero-sequence component and depends on the neutral current value [37]. Two categories of switching strategies were evaluated and analyzed in [37]. It was determined that the Class II center-aligned strategy achieves an optimal balance between switching loss and harmonic output value, thus making it a popular choice for real-time applications.

Usually, the components of $V_{ref} = [V_\alpha, V_\beta, V_\gamma]^T$ can be balanced or unbalanced and sinusoidal or non-sinusoidal. When the components of $V_{ref}$ are sinusoidal and balanced, the trajectory of $V_{ref}$ is a circle in $\alpha\beta$ plane ($V_\gamma = 0$) and is similar to the conventional SVM circle. Moreover, in the unbalanced

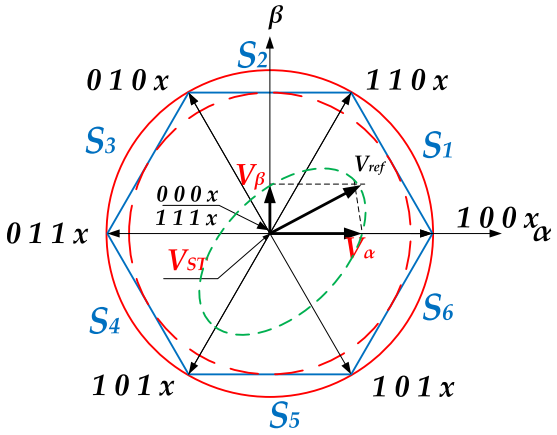


**FIGURE 4.** Vertical projection on $\alpha\beta$ plan ($x$ can be 0 or 1) in case of an unbalanced load.

load, the trajectory of the $V_{ref}$ is an ellipse inclined, as illustrated in Figure 4.

## IV. PROPOSED OPTIMIZED 3DZSVM for 4L-qZSI

Generally, the SVM algorithms for either the 3L-VSI or 4L-VSI have three main steps to build the reference voltage vector as follows, i) reference vector location, ii) switching times calculation, and iii) switching sequence definition. The first and second steps of the SVM algorithm are the same as for the ZSVM for the qZSI. The difference between the two algorithms (SVM and ZSVM) lies in the third step, i.e., how to define the switching sequence. Therefore, this section focuses on the third step and how to insert the *ST* state in the switching sequence [45].

To simplify and expedite the computation process of the proposed 3DZSVM for the 4L-qZSI, the optimized 3DSVM algorithm, as referenced in [41], is utilized.

The core idea of the 3DSVM for the multilevel four-leg diode clamped converter is to simplify the 3DSVM method by employing just one sector of the space vector diagram. This means that the phases mentioned above of the 3DSVM are only done in one sector, significantly reducing computational time. The three steps of the proposed 3DZSVM for the 4L-qZSI are briefly described in the subsections below.

### A. REFERENCE VOLTAGE VECTOR LOCATION

Before identifying the reference voltage vector must be reconstructed to rotate only in the first sector $S_1$ of the space vector diagram (SVD) [41]. The reconstructed reference voltage vector (RRVV) is denoted by $U^*(U_a^*, U_b^*, U_c^*)$, whereas the original reference voltage vector (ORVV) is $v^*(v_a^*, v_b^*, v_c^*)$. The components of the RRVV are deduced based on the sector number that contains the ORVV and its components $(v_a^*, v_b^*, v_c^*)$, as given in Table 1.

For the m-level of the 4L-DCC, all tetrahedrons situated in S1 of the SVD can be categorized into six types. These form two adjoining prisms ($PR^1$ and $PR^2$), as depicted in Figure 5. These neighboring prisms create a 3D parallelepiped with

**TABLE 1.** Choosing the components of the RRVV.

| | S1 | S2 | S3 | S4 | S5 | S6 |
|---|---|---|---|---|---|---|
| $U_a^*$ | $v_a^*$ | $v_b^*$ | $v_b^*$ | $v_c^*$ | $v_c^*$ | $v_a^*$ |
| $U_b^*$ | $v_b^*$ | $v_a^*$ | $v_c^*$ | $v_b^*$ | $v_a^*$ | $v_c^*$ |
| $U_c^*$ | $v_c^*$ | $v_c^*$ | $v_a^*$ | $v_a^*$ | $v_b^*$ | $v_b^*$ |

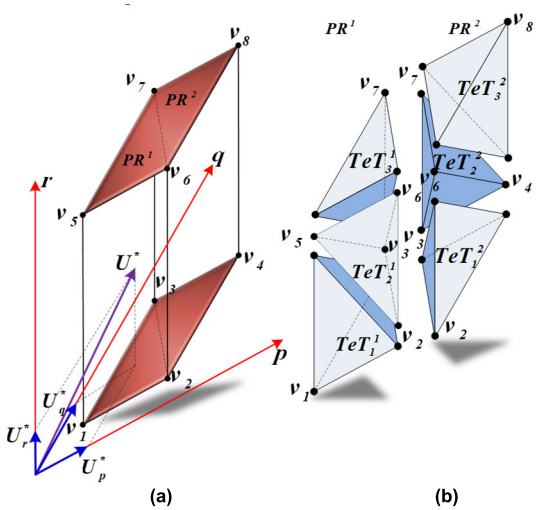


**FIGURE 5.** (a) Three-dimensional parallelepiped, (b) the six categories of tetrahedrons [41].

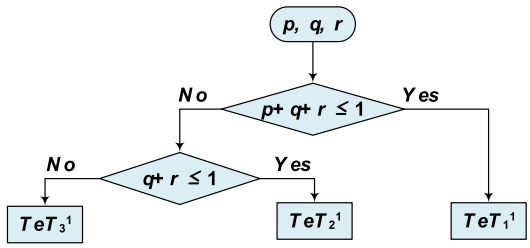


**FIGURE 6.** Tetrahedron type identification process (Particular case for 4L-VSI).

eight switching vectors (SWVs) $v_1, v_2, \ldots, v_8$. Here, $TeT_i^j$ represents the $i^{th}$ tetrahedron situated within the $j^{th}$ prism, $PR^j$).

In the case of two-level 4L-VSI ($m = 2$), the $PR^2$ in Figure 5(a) does not exist, and therefore, only three types of tetrahedrons remain to be identified ($T_eT_1^1$, $T_eT_{2,}^1$ and $T_eT_3^1$ (see Figure 5(b)). Therefore, new axes called $\rho$-$\sigma$-$\tau$ (see Figure 5(a)) are used to identify the type of tetrahedron, select the appropriate SWVs, and calculate the corresponding switching times for $m$-level 4L-DCC by putting $m = 2$ for two-level 4L-VSI, it yields:

$$\begin{bmatrix} U_\rho^* \\ U_\sigma^* \\ U_\tau^* \end{bmatrix} = \frac{m-1}{V_{DC}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} U_a^* \\ U_b^* \\ U_c^* \end{bmatrix} \quad (4)$$

The fractional parts of the components of the RRVV $U^*$ in (4) are denoted by $p$, $q$, and $r$. Based on these values, the tetrahedron type for two-level 4L-VSI is easily identified, as illustrated in Figure 6.

**TABLE 2.** Duration periods of the neighboring switching vectors.

| | Tetrahedron types | | |
|---|---|---|---|
| | $TeT'_1$ | $TeT'_2$ | $TeT'_3$ |
| **Adjacent vectors** | $v_1$ $v_2$ $v_3$ $v_5$ | $v_6$ $v_2$ $v_3$ $v_5$ | $v_6$ $v_7$ $v_3$ $v_5$ |
| Time intervals | $t_1=T_s(1-p-q-r)$ | $t_6=T_s(p+q+r-1)$ | $t_6=T_sp$ |
| | $t_2=T_sp$ | $t_2=T_s(1-q-r)$ | $t_2=T_s(q+r-1)$ |
| | $t_3=T_sq$ | $t_3=T_sr$ | $t_3=T_s(1-r)$ |
| | $t_5=T_sr$ | $t_5=T_s(1-q-q)$ | $t_5=T_s(1-p-q)$ |

**TABLE 3.** Interchanging of switching states in all sectors.

| *Sector 1* | *Sector 2* | *Sector 3* | *Sector 4* | *Sector 5* | *Sector 6* |
|---|---|---|---|---|---|
| *a, b, c, n* | *b, a, c, n* | *b, c, a, n* | *c, b, a, n* | *c, a, b, n* | *a, c, b, n* |

### B. COMPUTATION OF SWITCHING DURATIONS

During each switching period, $T_s$, the adjacent SWVs of the RRVV are selected to be applied at precalculated times. Then, the duration intervals for the different types of tetrahedrons are computed using straightforward formulas, as presented in Table 2.

### C. SWITCHING SEQUENCE DEFINITION

In the switching process of a 4L-qZSI, when facilitated by the 3DZSVM, there are 14 active voltage vectors, a duo of standard zero vectors, and an extra *ST* vector. For each tetrahedron, the reference voltage vector for the 4L-qZSI is defined as

$$V_{ref} = V_1\frac{T_1}{T_S} + V_2\frac{T_2}{T_S} + V_3\frac{T_3}{T_S} + V_0\frac{T_0}{T_S} + V_{ST}\frac{T_{ST}}{T_S} \quad (5)$$

duration ($T_{ST}$) should be added to the switching time ($T_1$, $T_2$, $T_3$, and $T_0$) of the traditional 3DSVM by switching between the *ST* and active states. In this way, the capacitors and inductors are charged and discharged.

A technique is employed to minimize extra switching operations and the accompanying energy losses to enhance the dc-link voltage of the 4L-qZSI and achieve the intended ac output voltage. The *ST* intervals are incorporated prior to or after each active time's initiation or conclusion ($T_1$, $T_2$, $T_3$). The total desired duration of the *ST* intervals is evenly distributed across various segments within a switching period. This distribution is implemented by activating every two switches in a single phase leg at a time. Consequently, the *ST* state can be introduced by adjusting the modulation where $V_{ST}$ is the *ST* voltage vector. Figure 4 illustrates the respective voltage space vectors of the 4L-qZSI within the $\alpha\beta$ coordinate framework.

For the implementation of the 3DZSVM of 4L-qZSI, the conventional 3DSVM technique should be modified. A new reference while maintaining a constant output voltage reference vector $V_{ref}$.

Alternatively, the single-leg *ST* state can be employed by introducing *ST* states in one leg during the zero-state in the proposed 3DZSVM of the 4L-qZSI. The number and placement of *ST* periods in a switching period are modified in a switching period to generate different schemes. 3DZSVM schemes are possible by introducing 8, 4, and 2 for *ST* periods within a switching period, namely 3DZSVM8, 3DZSVM4, and 3DZSVM2, respectively. Figure 7a-c shows their various switching patterns.

Figure 7(a) illustrates the switching sequence for the 3DZSVM8 throughout the switching period. The operating periods of the eight switches are modified such that the total time interval of *ST* states is divided into eight equal portions for every control period. In addition, each *ST* duration is incorporated into the transition time between zero and active states. Consequently, each of the four legs naturally meets the ($T_{sh}$/8) *ST* time interval eight times within a single switching period without requiring additional switching activities.

As depicted in Figure 7(b), the *ST* time interval for the 3DZSVM4 is likewise partitioned into four sections within a single control cycle. Similarly, the 3DZSVM2 splits the total *ST* time interval into two portions in one control period, involving modifications in the switching times of four switches (see Figure 7(c)). Consequently, the reference voltage is generated using four nearby switching vectors. Again, the primary goal is to reduce harmonic content in the output voltage/current via a strategically arranged switching transition. Table 3 provides a summary of the implemented exchanges between phases *a, b, c,* and *n* across all sectors, further illustrating the specific arrangements and interactions involved in the modulation techniques [41].

Lastly, Figure 8 provides a detailed flowchart of the proposed optimized 3DZSVM method for the 4L-qZSI. The flowchart demonstrates the step-by-step procedure of the modulation technique, including the calculation of time intervals, determination of switching sequences, and control of the inverter operation. This comprehensive visualization helps to illustrate the intricacies and sequence of operations involved in implementing the 3DZSVM method, providing a clear understanding of its application in the 4L-qZSI system.

## V. SIMULATION RESULTS

The simulation utilizes the parameters specified in Table 4. Three scenarios were assessed to showcase the performance of 3DZSVM for 4L-qZSI in both steady-state and transient conditions.

- Case *(C1)*: Balanced peak reference voltages ($V_{oa} = V_{ob} = V_{oc} = 88$ V) and balanced loads ($R_a = R_b = R_c = 20\,\Omega$, $L_a = L_b = L_c = 10$ mH)).
- Case *(C2)*: Balanced peak reference voltages ($V_{oa} = V_{ob} = V_{oc} = 88$ V) and unbalanced loads ($R_a = 30\,\Omega$, $R_b = 10\,\Omega$, $R_c = 60\,\Omega$, $L_a = 0$ mH, $L_b = 5$ mH, $L_c = 10$ mH).
- Case *(C3)*: Unbalanced peak reference voltages ($V_{oa} = 88$ V, $V_{ob} = 44$ V, $V_{oc} = 22$ V) and balanced loads ($R_a = R_b = R_c = 20\,\Omega$, $L_a = L_b = L_c = 10$ mH)).

The input voltage is established at $V_{in} = 130$ V for all scenarios, with the *ST* duty ratio fixed at 0.2. Consequently, the theoretical peak voltage of the $V_{DC}$ is expected to reach 216V.

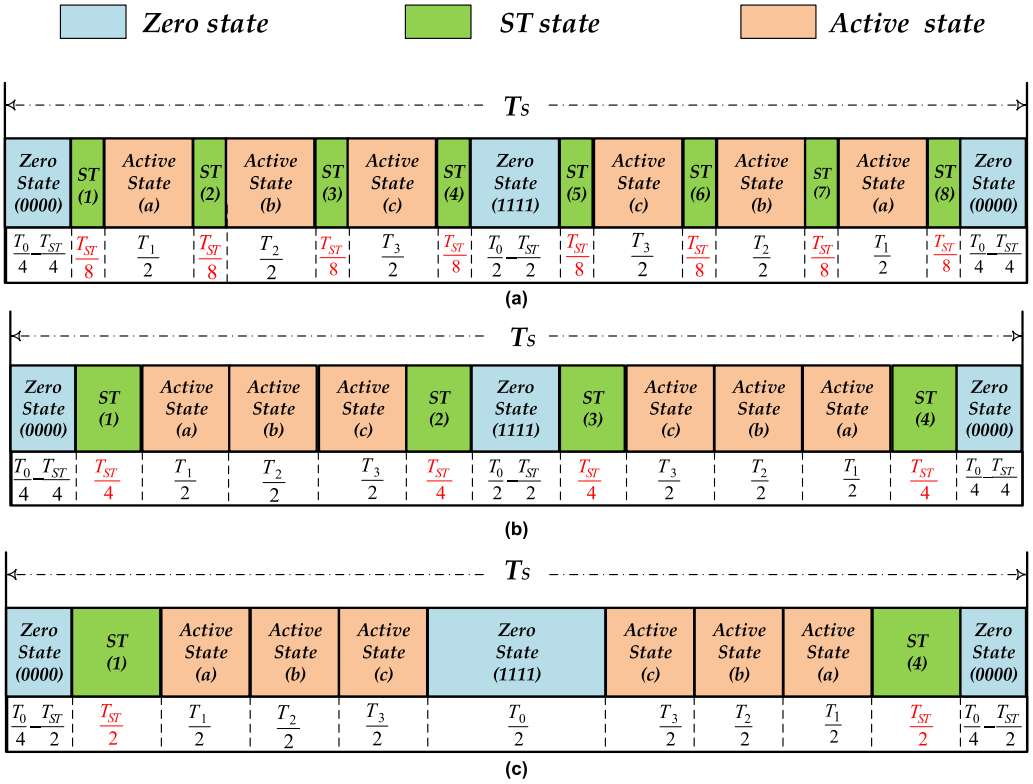


**FIGURE 7.** Switching pattern for 4L-qZSI for different modulation schemes (a) 3DZSVM8, (b) 3DZSVM4, and (c) 3DZSVM2.

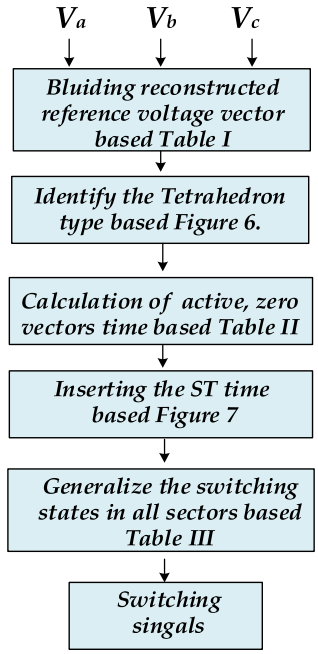


**FIGURE 8.** Flowchart of the proposed 3DZSVM for the 4L-qZSI.

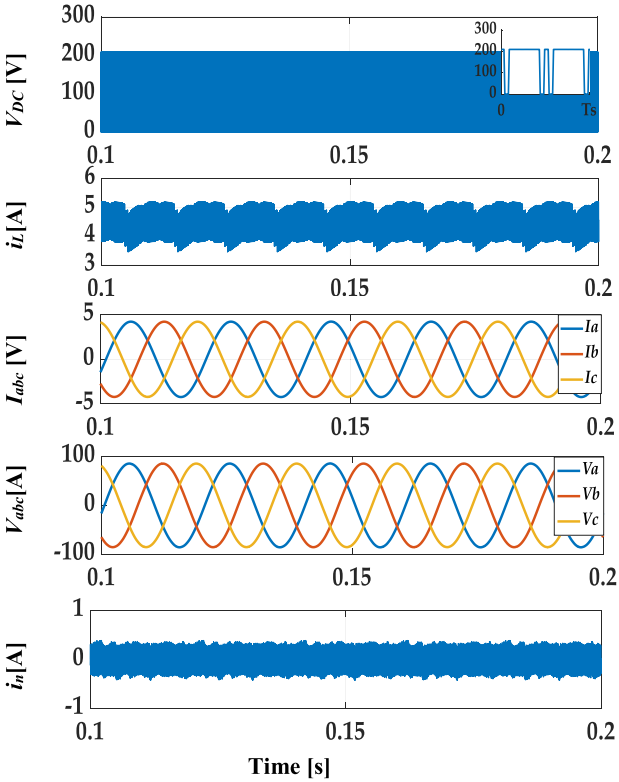


**FIGURE 9.** Simulation results of case C1.

Finally, a simulation of an *RL* load is performed, with the load connected to the inverter through an *LC* filter, as illustrated in Figure 1.

Figures 9-11 display the simulation outcomes for the 4L-qZSI using the proposed 3DZSVM4 technique, which

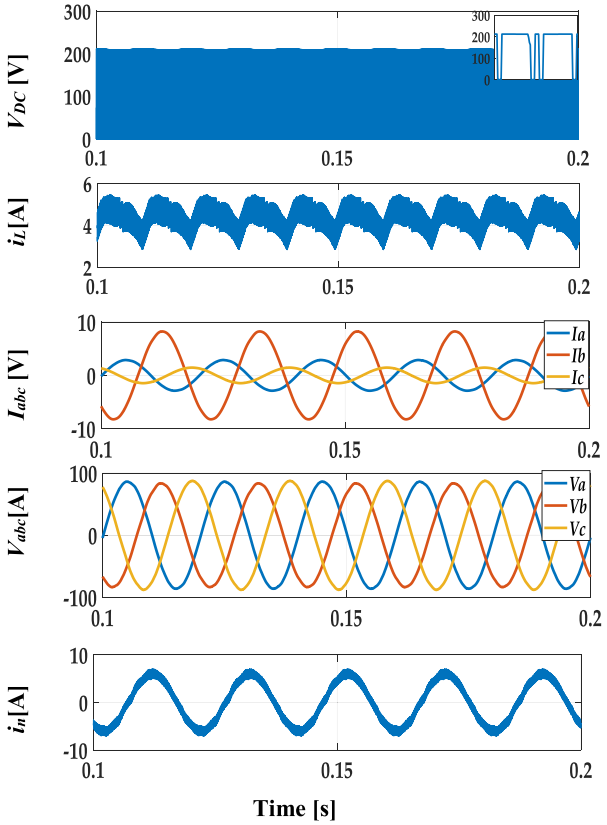


**FIGURE 10.** Simulation results of case C2.

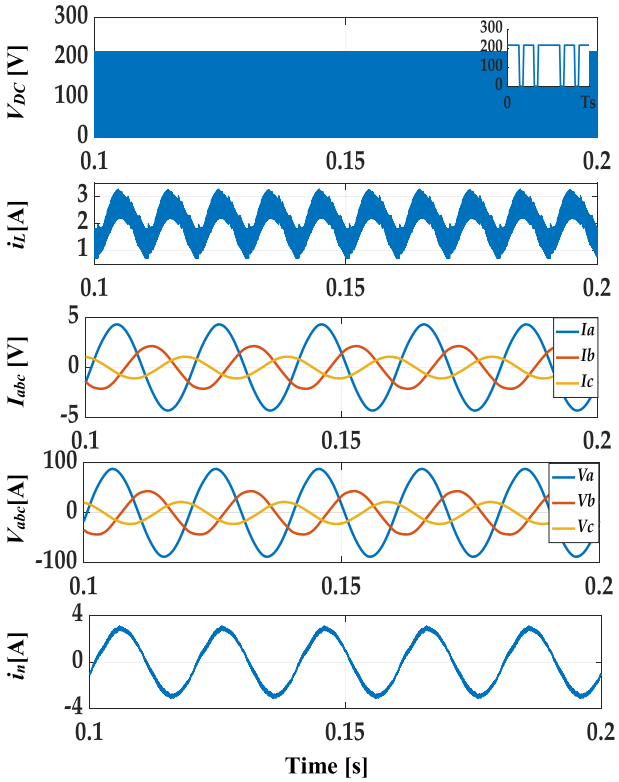


**FIGURE 11.** Simulation results of the steady-state analysis with unbalanced reference voltages and balanced loads.

**TABLE 4.** General parameters of the 4L-qZSI system.

| Circuit parameters | Value |
|---|---|
| qZS network $C_{1,2}$, $L_{1,2}$ | 2,5 mF, 1mH |
| Internal resistance $r_c$, $R_L$ | 0.38 Ω, 0.1 Ω |
| Filter inductance $L_f$, $r_f$ | 3 mH, 0.1 Ω |
| Filter capacitor $C_f$ | 50 µF |
| Switching frequency $f_s$ | 10 kHz |
| Input dc voltage $V_{in}$ | 130 V |
| Line frequency $f$ | 50 Hz |

includes the dc-link voltage, the inductor current, the output current, the output voltage, and the neutral current.

The proposed modulation approach is validated through simulations conducted on a 4L-qZSI using Matlab/Simulink.

Every simulation outcome demonstrates that the output voltage ($V_a$, $V_b$, $V_c$) aligns considerably with their references ($V_a^*$, $V_b^*$, $V_c^*$). The peak $V_{DC}$ voltage is also elevated to 216 V from an initial $V_{in}$ (fixed to 130 V), accompanied by a modulation index $M$ of 0.7. The $V_{DC}$ remains constant under all the tests mentioned above.

In case *C1*, a balanced three-phase load is supplied by the 4L-qZSI. The reference peak voltage is set to 88 V, and as can be seen in Figure 9, the peak ac voltage is at its reference, i.e., at 88 V. In the case of balanced references and load, the neutral current, the sum of the three-phase load currents, is zero.

Also, the $V_{DC}$ has a pulsating shape, where its peak equals 215 V during the active vectors and zero during the shoot-through vectors. As a result, the average inductor $L_1$ current equals approximately 4.5 A, with a peak-peak ripple ($\Delta i_{L1}$) value of 1 A. On the other hand, the neutral current flows through the fourth leg of the inverter in case *C2*, which corresponds to unbalanced loads (see Figure 10). The output voltage tracks the output reference while the output current reaches the unbalance loads.

In contrast, under case *C2*, the neutral current navigates through the inverter's fourth leg for unbalanced loads (refer to Figure 10). The output voltage adheres to the output reference, while the output current mirrors the unbalanced loads.

In case C3, we intentionally created an unbalanced reference voltage by decreasing the amplitude of $V_{ref}$ for phases (*b*) and (*c*) to 50% and 25%, respectively, as shown in Figure 11. The results obtained from Figure 11 demonstrate that the system successfully aligns the unbalanced output voltages with their respective reference values. This indicates that the system can regulate its output voltages accurately, even when faced with varying degrees of reference voltage across different phases. It highlights the system's ability to maintain output consistency and accuracy efficiently, even under unbalanced voltage references. It is worth noting that in all three cases, the peak value of $V_{DC}$ remains the same at 215V, as they have the same $V_{in}$ and *ST* value of 0.2.

### A. INDUCTOR CURRENT RIPPLE ANALYSIS

Figure 12 presents the inductor current of the 4L-qZSI over two fundamental cycles (equivalent to 40 ms) using the

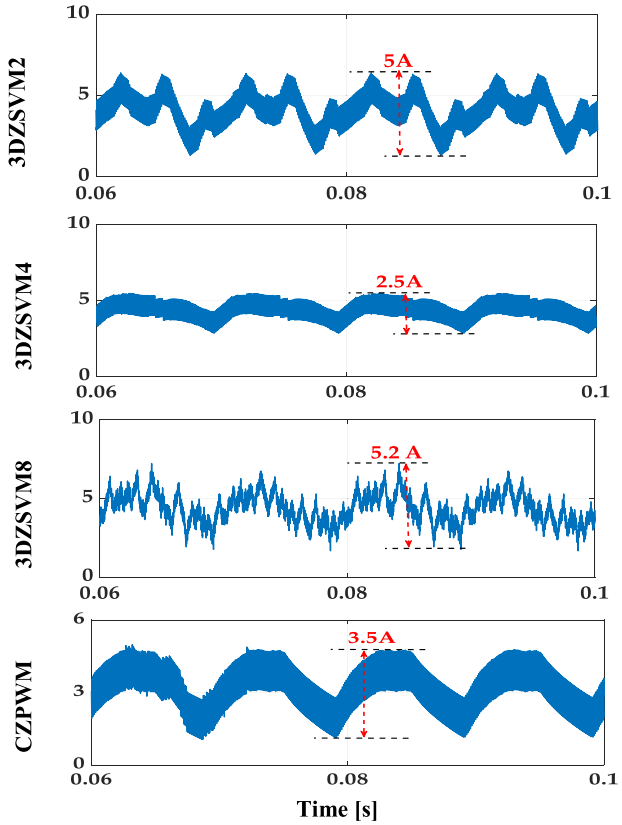


**FIGURE 12.** The simulation outcomes illustrate the $i_{L1}$ behavior of the 4L-qZSI strategy throughout a single cycle in scenario C2.

3DZSVM2, 3DZSVM4, and 3DZSVM8 strategies, in comparison with the traditional CZPWM technique [23], when applied under conditions of unbalanced loads (case *C2*). The instantaneous inductor current ripples for the 4L-qZSI utilizing all strategies display a periodic fluctuation within one fundamental cycle. For example, for one cycle, the maximum instantaneous current ripples $\Delta i_{L1}$ with the 3DZSVM2, 3DZSVM4, 3DZSVM8, and CZPWM methods are 5 A, 2.5 A, 5.2 A, and 3.5 A, respectively. Notably, the maximum instantaneous current ripple $\Delta i_{L1}$ in the 3DZSVM4 strategy sees a reduction of 49% in comparison to the 3DZSVM2 and 3DZSVM8 strategies.

These findings highlight the efficiency of the 3DZSVM4 strategy in mitigating ripple inductor current. Furthermore, it suggests that the 3DZSVM4 strategy is the most effective in controlling the magnitude of current ripples, leading to a smoother and more predictable system performance, especially under unbalanced loads. This is of particular importance in applications where stability and reliability of the output are crucial.

### B. POWER LOSS EVALUATION

Furthermore, to assess the influence of the proposed 3DZSVM techniques on the efficiency of the inverter, the switching and conduction losses of the IGBTs and antiparallel diode were measured using the PLECS toolbox. The IGBT and antiparallel diode *D* models are FS50R06W1E3

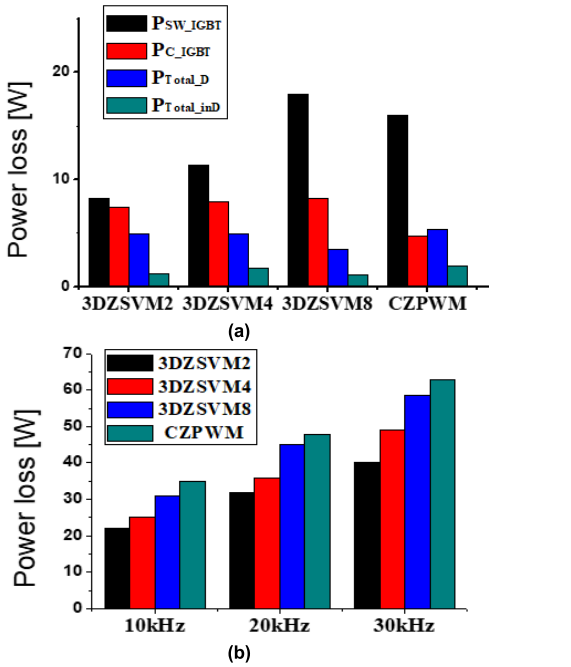


**FIGURE 13.** (a) Measured switching and conduction power losses distribution in the 0.6 kVA 4L-qZSI different IGBTs and input D under case C2 by PLECS for CZPWM and proposed 3DZSVM strategies, (b) Total power loss of the 4L-qZSI in different switching frequencies.

and VS30EPH06PbF, respectively. The analysis was based on our study's findings and the reference papers by [46] and [47]. Figure 13(a) depicts the breakdown of these losses specifically for scenario *C2*. The conventional CZPWM [23] technique and the proposed 3DZSVM strategies were evaluated to compare their impact on loss distribution. The total power loss ($P_{Total}$) in each modulation technique, as described by

$$P_{Total} = P_{SW-IGBT} + P_{C-IGBT} + P_{Total-D} + P_{Total-inD} \quad (6)$$

where the $P_{SW-IGBT}$, $P_{C-IGBT}$, $P_{Total-D}$, and $P_{Total-inD}$ are the switching power loss and the conduction power loss in the IGBT, the total loss in the antiparallel diode *D*, and the total loss in the input diode, respectively.

The examination of various switching frequencies provides detailed insights into the total power losses of the 4L-qZSI when utilizing the proposed 3DZSVM modulation strategies, as depicted in Figure 13(b).

The results indicate that the proposed modulation strategies increased switching loss when using more *ST* divisions. Figure 13(a) clearly illustrates how the power loss increases with more *ST* divisions. The 3DZSVM2 approach exhibits a smaller total power loss than the other 3DZSVM methods. This can be attributed to reduced commutations while maintaining the same average switching frequency. Conversely, the CZPWM technique demonstrates the highest power loss across all switching frequencies, suggesting its less efficient performance in terms of power utilization. These findings shed light on the comparative performance of the different modulation strategies, enabling a more comprehensive understanding of their impact on power losses in the 4L-qZSI system.

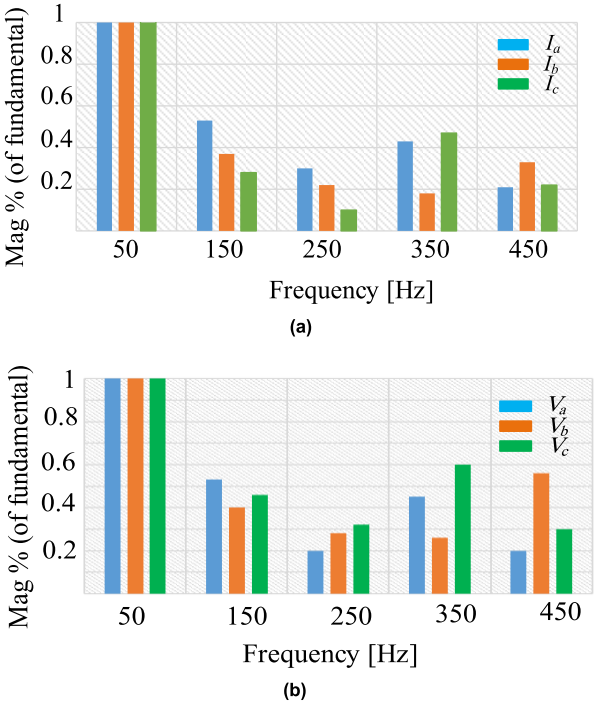


**FIGURE 14.** THD spectrum at different switching frequencies for (a) output currents and (b) output load voltage.

**TABLE 5.** THD of the load voltage with the proposed 3DZSVM methods under case *C2*.

| *Case* | *3DZSVM2* | | | *3DZSVM4* | | | *3DZSVM8* | | |
|---|---|---|---|---|---|---|---|---|---|
| | *a* | *b* | *c* | *a* | *b* | *c* | *a* | *b* | *c* |
| *C1* | *0.79* | *0.72* | *0.7* | *0.63* | *0.68* | *0.69* | *1.5* | *1.4* | *1.3* |
| *C2* | *0.81* | *1.9* | *1.4* | *0.75* | *0.85* | *0.7* | *0.9* | *1.7* | *1.6* |
| *C3* | *1.33* | *3.1* | *3.1* | *1.34* | *3.26* | *3.1* | *4.7* | *7* | *4.5* |

### C. OUTPUT CURRENT AND VOLTAGE QUALITY

Figure 14 shows the THD spectrum for both the three-phase output currents and voltages in case *C2*. The THD values for the three-phase output currents are 0.75%, 0.21%, and 0.75% for phases *a*, *b*, and *c,* respectively. In addition, the THD value of the voltage is documented in Table 5, indicating compliance with the IEEE 519 standard. These results highlight the system's effectiveness in minimizing harmonic distortion and ensuring the output currents and voltages meet the required standards for quality and performance.

## VI. HIL VALIDATION RESULTS

The proposed system was tested and confirmed using a Hardware-in-the-Loop (HIL) emulator constructed with the C2000TM- microcontroller- LaunchPadXL TMS320F28379D kit. The HIL emulator operates by simulating a specific system component, in this case, the power component, within the computer as a MATLAB model [48], [49].

The MATLAB software simulates and hosts the planned system power units, such as power converters and filters. In contrast, the microcontroller kit implements the control algorithms, specifically the proposed 3DZSVM. Communication between the PC and the kit is facilitated through

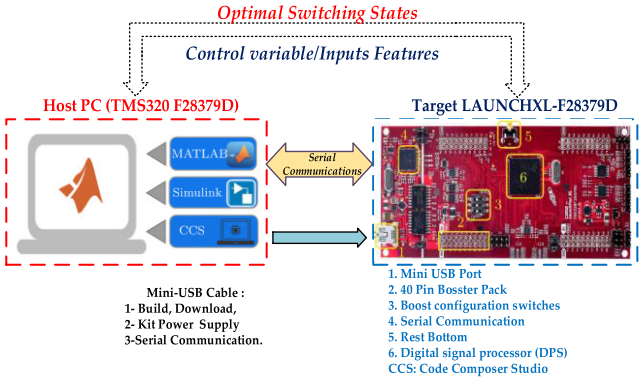


**FIGURE 15.** Schematic of the HIL simulator for the proposed system.

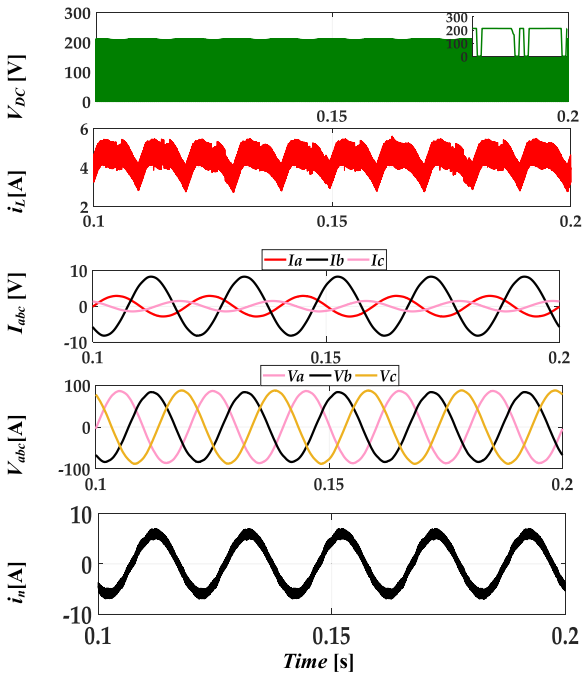


**FIGURE 16.** Validation results under case *C2* c.

virtual serial COM ports [50], [30], allowing MATLAB to provide measured signals from the power circuit to the kit. These signals include the DC bus voltage, inductive current, capacitor voltage, load voltages, and load currents. The kit then processes the control algorithms to generate the 4L-qZSI switching signals. Figure. 15 provides a schematic representation of the HIL implementation of the proposed 3DZSVM.

Figure 16b-e provides a detailed representation of the HIL validation results for the proposed 3DZSVM4 with 4L-qZSI under a specific set of conditions, referred to as case *C2*. In this particular case, the 4L-qZSI is operating under an unbalanced load. The figures illustrate the system's response and performance characteristics when subjected to these unbalanced load conditions, offering a comprehensive view of its operational capabilities and robustness under such circumstances.

In the case *C2*, 4L-qZSI is responsible for supplying an unbalanced three-phase load. The reference peak voltage is established at 88 V, and as demonstrated in Figure 9, the

peak ac voltage aligns with its reference, maintaining at 88 V. The output voltage successfully follows the output reference, while the output current is directed towards the unbalanced loads. The $V_{DC}$ exhibits a pulsating pattern, reaching a peak of 215 V during the active vectors and dropping to zero during the shoot-through vectors. Consequently, the average current for inductor $L_1$ is approximately 4.5 A, with a peak-peak ripple ($\Delta i_{L1}$) value of 2 A. The neutral current is channeled through the inverter's fourth leg for unbalanced loads, as depicted in Figure 10.

Finally, the experimental validation of the proposed 3DZSVM control strategy for the 4L-qZSI, using the TMS320F28379D kit, has been successfully carried out. The HIL simulator was instrumental in this process, demonstrating our proposed control strategy's practical applicability and robust performance under unbalanced load conditions. The negligible discrepancies between the simulation and HIL results further underscore the success of the proposed 3DZSVM for 4L-qZSI in terms of practical implementation.

## VII. CONCLUSION

A new three-dimensional space vector modulation technique for a 4L-qZSI, which combines a qZSN and a two-level four-leg inverter, has been developed in this study. The proposed method includes three variants aiming to achieve superior steady-state operations and harmonic performance for 4L-qZSI, called 3DZSVM2, 3DZSVM4, and 3DZSVM8. The main achievement of this investigation is to propose a new modulation technique applied to the 4L-qZSI with enhanced output current quality, reduced power loss, and reduced inductive current ripple under unbalancing load. The proposed method combines the benefits of SVMs that are applied in both abc and $\alpha\beta\gamma$ coordinates. The proposed approach utilizes the SVD of 4L-qZSI in the coordinates, whereas the 3DZSVM algorithm's designing processes are carried out in the newly proposed $\rho\sigma\tau$ coordinates. While performing the localization process of the RRVV, calculating the duration time intervals of neighboring switching vectors, and designing switching sequences in the $\rho\sigma\tau$ coordinates, it utilizes the SVD of the 4L-qZSI in the $\alpha\beta\gamma$ location. In practice, there is only one sector where the proposed algorithm is used. Moreover, without using trigonometric functions, the time interval calculation can be done while integrating the *ST* state and the creation of pulses.

To validate the performance of the introduced modulation scheme for the 4L-qZSI, extensive simulation studies were conducted. The results of these studies not only demonstrate the exceptional steady-state performance of the proposed technique and reveal its advantages over CZPWM. The proposed scheme exhibits lower power loss and reduced inductive current ripple, enhancing its effectiveness.

Since all the calculations are based on the first sector, which reduces the computational capacity, the proposed 3DZSVM control strategy for 4L-qZSI has been experimentally validated using the TMS320F28379D kit. The validation was conducted within the framework of a HIL simulator. The results from this experimental validation underscore the practical applicability and robust performance of our proposed control strategy, particularly under conditions of unbalanced load.

The proposed 3DZSVM for 4L-qZSI is suitable for the fuel-cell or PV applications in stand-alone mode, with the ability to provide a high control for unbalanced systems, and can also be applied to other improved Z-source networks. Moreover, the proposed 3DZSVM can be applied for grid-connected power to improve the utility grid's power quality.

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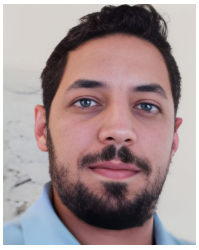

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