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RESEARCH ARTICLE

Design Trends and Perspectives of Digital Low Dropout Voltage Regulators for Low Voltage Mobile Applications: A Review

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ABSTRACT Low-dropout (LDO) voltage regulator has fascinated industry professionals and academia for the past few decades, and this trend is expected to continue in the coming years. The high demand for a stable linear regulator architecture that performs well in systems-on-chip (SoC) power management integrated circuits (PMICs) is a key factor driving innovation with different complementary metal-oxide-semiconductor (CMOS) technologies. Yet, there are several performance parameter trade-offs to be considered, such as transient response, output ripple, area, power efficiency, supply voltage range, and current efficiency in the current LDO design architecture. All these parameter trade-offs become more severe during the back-end CMOS processes with additional limitations, for example, channel length modulation, stress sensitivity, and power leakage, among others. Therefore, this paper presents an overview and comparison of various digital LDO (DLDO) topologies, functionalities, and performance specifications, which can serve as a virtual study or reference for others.

INDEX TERMS Digital low-dropout (DLDO) regulators, synchronous, analog-assisted, hybrid, asynchronous, event-driven, self-clocked, power management integrated circuit (PMIC), system-on-chip (SoC), CMOS process.

I. INTRODUCTION

The emergence of body communications [1], [2], high-speed wireless [3], [4], and wireline [5], [6], [7], [8], [9] communications have spurred innovation in system-on-chip (SoC) power management integrated circuits (PMICs). Typical electronic devices may consist of multiple modules, each with varying voltage, power, and current requirements [10]. For example, a low-energy Bluetooth transceiver module might operate with a 1-V supply voltage and consume power 10 mW [11], while a low noise amplifier (LNA) might operate with a >1.2-V supply voltage [12], [13], [14], [15]. Hence, a dedicated power converter is necessitated for each module to operate at the optimum voltage level. The area limitation has become one of the major challenges in PMICs, as each module, involving the respective power converter, occupies a dedicated core area. Thus, it is vital to reduce silicon area for cost savings while keeping the requirements of the power supply [10].

The PMICs with various outputs have been widely used to power multiple modules in a single portable device [10]. Power converters can be categorized into two major types:

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linear and *switching*. A linear power converter has low efficiency but can produce a smooth and stable output voltage [16], while a switching-type power converter has higher efficiency and can step-up or step-down the voltage. However, switching-type converters are mostly complicated in circuit design and contribute to ripples and noise at the output node due to the switching operation. A typical hybrid type of the SoC PMIC module, as shown in Figure 1, consists of a switching power converter (e.g., DC-DC converter) and parallel linear power converters, such as low-dropout (LDO) regulators cascaded to the output of the switching converter [17]. Such an approach enables a single switching power converter to connect to multiple linear power converters, thus reducing the duplication of dedicated power converters and overall components count, while combining the advantages of both linear and switching power converters [18]. In this review, the linear power converters or linear voltage regulators will be studied and investigated. Also, among the different types of LDOs, only the state-of-the-art digital LDOs (DLDOs) and their respective topologies are comprehensively reviewed and discussed.

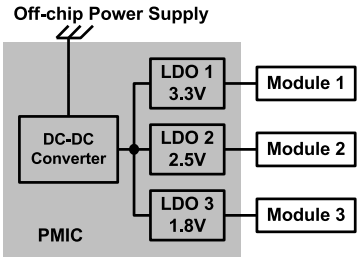

FIGURE 1. Block diagram of the typical SoC PMIC with the single DC-DC converter.

Apart from that, off-chip power supply occupies a large area, which prompts the development of battery-less SoC, as shown in Figures 2 and 3, incorporating energy harvesting (EH) solutions to replace the usage of the batteries. EH is achieved with different ambient energy sources, such as solar [19], thermal [20], piezoelectric [21], electromagnetic, or radio frequency (RF) waves [22], [23], [24], [25]. Section II reviews the common design parameters and types of LDOs, along with the justification for the usage of the DLDO. This is followed by Section III, which introduces the operation of the conventional DLDO, in particular, the synchronous DLDO (S-DLDO) structures [26]. The design trade-offs among important LDO performance parameters are discussed in Section IV, with the comparison of state-of-the-art DLDOs given in Section V, followed by the conclusions and perspectives of the DLDOs in Section VI.

II. LDOs

There are a few types of linear voltage regulators which can be divided into series, shunt, and LDO. LDO is the most widely-used voltage regulator in CMOS technology due to its superior functionality performance [16]. Figure 4 outlines the basic architecture of the classic LDO [27].

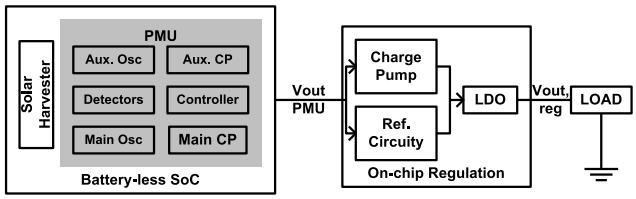

FIGURE 2. Battery-less SoC PMU integrated with on-chip regulation [19].

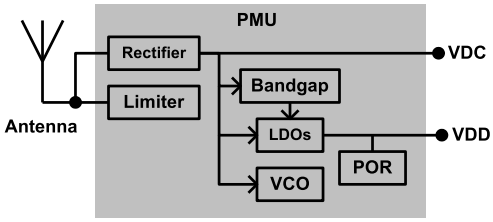

FIGURE 3. Block diagram of the RFEH SoC PMU [25].

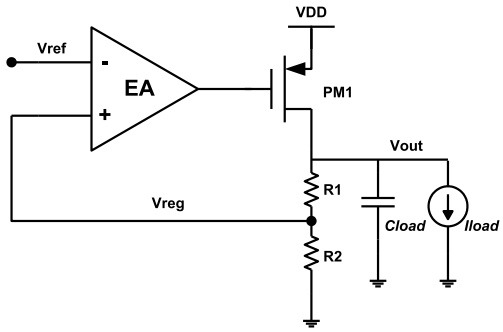

FIGURE 4. The basic architecture of the classic LDO [27].

A. DESIGN PARAMETERS OF COMMON LDO

In the state-of-art LDO topologies, there are several common design parameters which are the dropout voltage, quiescent current, line, load regulation, output noise, power supply rejection ratio (PSRR), efficiency, and transient response including the ripple [28].

The dropout voltage is the most important parameter in designing the LDO, as it impacts the overall performance of the LDO. It is defined as the output voltage deviation from the input. An efficient and stable LDO has a small dropout voltage. In an LDO, the power device typically operates in the saturation region. However, there is a key distinction between analog LDO and digital LDO regarding the dropout voltage characteristics and the operation of the respective power devices. In an analog LDO, the dropout voltage does not depend on the drain-source resistance (R_{DS}) of the power device when the power device is operating in saturation, but instead is determined by other factors such as the reference voltage, error amplifier, and pass transistor characteristics, it remains independent of R_{DS}. However, when the analog

LDO operates with a heavy load, the power device may enter a triode region where the dropout voltage will be affected by the R_{DS} that changes across the loading effect [27]. On the other hand, DLDOs typically employ power devices operating in the linear region. In this region, the power device acts as a variable resistance, with R_{DS} directly affecting the dropout voltage. Higher R_{DS} leads to an increased voltage drop across the device, resulting in a higher dropout voltage in DLDOs. Hence, the mathematical expression of the dropout voltage, $V_{DROPOUT}$, is given by:

$$V_{DROPOUT} = I_{LOAD} \times R_{DS} \tag{1}$$

where the I_{LOAD} is the load current and R_{DS} is the drain-source resistance at the PMOS switch at the output.

The quiescent current, I_Q, describes the minimum operating current for the LDO and is defined as the difference between the input and output current, as described:

$$I_Q = I_{IN} - I_{OUT} \tag{2}$$

where the I_{IN} is the total input current used in the DLDO while the I_{OUT} is the output current delivered to the load.

Apart from the inherent noise at the circuit output, the input supply will be the main source of noise in the circuit. Thus, the output noise generated by the LDO becomes crucial to the overall circuit performance, especially for noise-sensitive circuits, such as phase-locked loops [29], [30], [31] and oscillators [32], [33]. Therefore, designing a low-output-noise LDO with a high-power supply rejection ratio is the most important.

The line regulation is defined as the deviation of the LDO output voltage, V_{OUT}, concerning the input voltage, V_{IN}:

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \tag{3}$$

Load regulation is the measurement of the LDO's output voltage sustainability upon a certain range of current load:

$$\text{Load Regulation} = \frac{\partial V_{OUT}}{\partial I_{LOAD}} \tag{4}$$

To characterize the overall performance of the LDO, the figure-of-merits (FoMs) are devised to determine the relative utility of the LDOs, and are expressed as follows [34], [35]:

$$\text{FoM}_1[\text{s}] = \frac{c_{LOAD} \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}} \tag{5}$$

$$\text{FoM}_2[\text{F}] = \frac{\Delta V_{OUT}}{V_{OUT}} \times \frac{I_Q}{I_{MAX}} \times C_{LOAD} \tag{6}$$

$$\text{FoM}_3[\text{s}] = \frac{I_Q}{I_{MAX}} \times T_{RES} \tag{7}$$

where ΔV_{OUT} is the undershoot by overshoot voltage, I_{MAX} represents the maximum load current, C_{LOAD} is the designed load capacitance placed at the LDO's output, and T_{RES} is the LDO response time given as:

$$T_{RES} = \frac{c_{LOAD} \times \Delta V_{OUT}}{I_{MAX}} \tag{8}$$

Besides the response time, the settling time, T_{Settle} is another parameter where it indicates the time taken for the output voltage to settle after a load transient. A superior LDO performance is indicated by a small value of FoM [35]. In addition to the generalized FoMs, power, and current efficiency also offer good performance benchmarks for the LDO [27]:

$$\text{Power Efficiency} \cong \frac{V_{REG}}{V_{DD}} = 1 - \frac{V_{DROPOUT}}{V_{DD}} \tag{9}$$

$$\text{Current Efficiency} = \frac{I_{LOAD}}{I_{LOAD} + I_Q} \tag{10}$$

where V_{REG} is the feedback voltage of the LDO and V_{DD} is the supply voltage. In addition, the LDO's power and area consumption also serves as the key design criteria, especially for SoC PMICs [36].

B. LDO TOPOLOGY

During the past few decades, LDOs have undergone a series of design architecture improvements as reviewed in [37]. Figure 5 depicts the conventional analog LDO (ALDO) [27], DLDO, and hybrid LDO which includes analog-assisted-digital as well as digital-assisted-analog techniques.

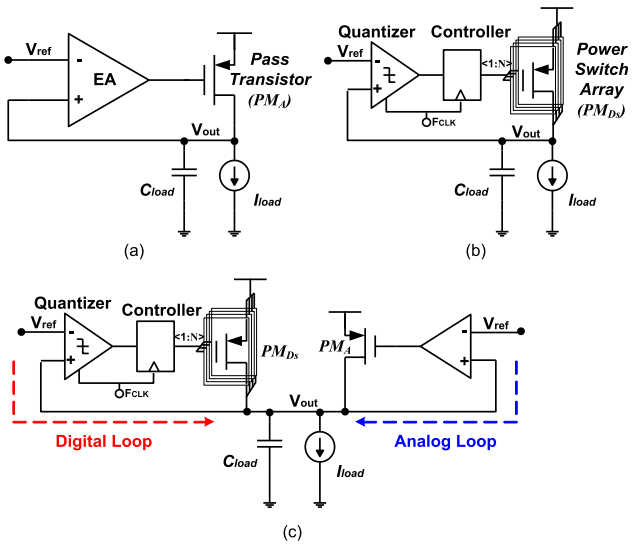

FIGURE 5. Overview of (a) ALDO, (b) DLDO, and (c) hybrid LDO [38].

Figure 5(a) shows the conventional ALDO design. This ALDO provides a superior transient response and achieves a high PSRR with the aid of a large external capacitor [39]. The external capacitor consumes a large circuit area and indirectly increases the production cost. To implement LDO in the SoC solution, output capacitor-less LDO (OCL-LDO) designs are developed [17]. Through this integration, the capacitance present at the output node is determined by the on-chip capacitor, which is typically less than 100pF [40]. Due to the small output capacitance, maintaining the circuit stability of the OCL-LDO becomes the key design challenge [41], [42]. This can be observed in the controller design of an ALDO, where without the large output capacitor to form a dominant

pole in the feedback system, the poles might be located very near to one another, which will degrade the phase margin, thus reducing the stability of the OCL-LDO [38]. Moreover, the pole at the output node is shifted with the respective variation in load current and output resistance of the power switch transistor, which further complicates the circuit design [43].

To mitigate the stability issue without the use of a large output capacitor load in the zero-pole feedback system, the ALDO needs to drive the logic circuits near-threshold or subthreshold voltage (NTV). This worsens with the increase in the quiescent current to support the larger load current with a bigger power switch [44]. The emerging portable device market creates high demands for low-power supplies such as sub-1V PMUs. This encourages innovation on DLDOs which can provide high open loop DC gain in the core circuit with low input voltage supply [38], [45].

Figure 5(b) shows a DLDO in a synchronous circuit that consists of a sampling clock, FCLK at the comparator, and feedback to the quantizer which also acts as a clock controller [46]. However, the DLDO switching nature causes output ripple which affects LDO PSRR [47]. To address the design limitation such as small signal performance in DLDO, the combination of ALDO and DLDO resulting in a hybrid LDO compromises the weakness and provides a state-of-the-art performance, between the ALDOs and DLDOs [48]. A typical analog-assisted-digital LDO as in [48] integrates an ALDO to suppress the output ripples with a feedback loop regulation and achieves a fast transient response with a dynamic voltage scaling in DLDO. In this proposed architecture, the main core of DLDO is implemented with a digital-assisted-analog technique ALDO to the comparator in the feedback loop. The analog-assisted-digital technique is commonly used in hybrid PMIC to achieve a low dropout LDO performance [18].

In short, the ALDO offers superior PSRR performance with low output ripples, while a DLDO exhibits excellent large signal transient response with a small regulator size and greater reliability. The hybrid LDO combines the benefits of the ALDO and DLDO, allowing researchers to achieve further innovation in SoC design. However, as CMOS technology continues to scale down into deep submicron features and the design trend moves into the sub-1V range, the ADLO becomes a bottleneck for low power supply due to insufficient voltage headroom which degrades the loop gain, thus impacting the performance [5]. Hence, the hybrid LDO, which requires a large and complex circuitry, may not be the best choice for submicron IC design. Alternatively, the DLDO has become the main attraction for researchers due to its ability to operate with very low supply voltage, better process scalability, and portability [35], [44].

III. CONVENTIONAL SYNCHRONOUS DLDO (S-DLDO)

The main basic building blocks of the conventional synchronous DLDO (S-DLDO), as proposed in [26], include the sensing circuit, which is generally a comparator, a digital controller based on bi-directional shift registers (BiSHRs), and an array of unary-weighted power switches or power transistors, as shown in Figure 6.

TABLE 1. Structural comparison among different types of LDO.

Aspect \ LDO Type	Analog	Digital	Hybrid
Supply voltage	High	Low	High
Design complexity	Low	Moderate	High
Sampling clock	No	Yes	Yes
Output ripple	Low	High	Moderate
PSRR	Good	Poor	Moderate
Power dissipation	High	Low	Moderate
Process scalability	Poor	Good	Moderate

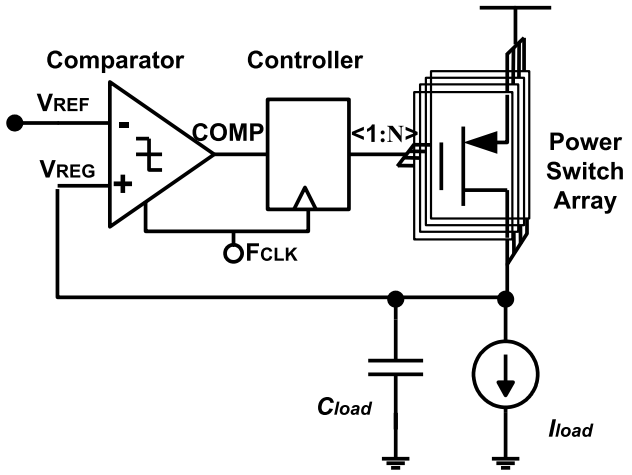

FIGURE 6. Overview of the S-DLDO.

The conventional S-DLDO, as proposed in [26], typically consists of several basic building blocks. The front stage is a quantizer that includes a comparator and its controller. This stage converts a continuous analog voltage input signal into a discrete digital signal by dividing the input voltage into a finite number of levels or steps, with each step representing a specific digital code. The controller is generally in digital form and requires an external sampling clock, F_{CLK}, for operation. The comparator senses the difference between V_{REF} and V_{REG} and quantizes the voltage error, which is then fed into the BiSHRs. To maintain the targeted output voltage, the DLDO adjusts the current flow through the power switch array and regulates V_{OUT} when the load current changes. The BiSHRs produce an N-bit digital code corresponding to the voltage difference, and this code is used to control the power switch array by performing digital shifting at the sampling clock edges, as shown in Figure 7.

IV. DLDOs' DESIGN CONSTRAINTS

The proposed S-DLDO [26] achieved good performance with a simple design among voltage regulators; however, it encountered several limitations, such as the incorrect

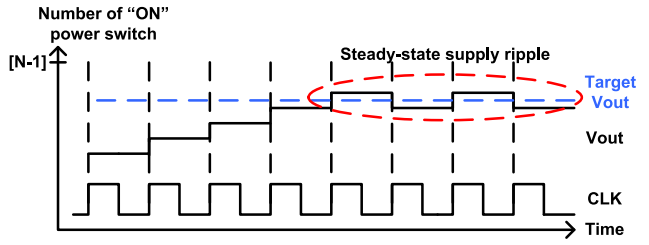

FIGURE 7. DLDO output voltage response concerning the number of turned-on power switches at different states [49].

DLDO power-on state value due to clock skew, failure in the DLDO output locking, and the operating frequency that affects the quiescent current of the DLDO [50]. The basic building block of the DLDO and the design constraints will be discussed in detail in the following sections.

A. BUILDING BLOCKS IN DLDO

The basic operation of the S-DLDO with its basic blocks has been discussed in the previous section. In this section, the functionalities of the blocks will be discussed in detail.

1) QUANTIZER

The first stage of the DLDO involves quantizing the voltage error between V_{REF} and V_{REG}, which is usually accomplished by employing amplifier-based voltage comparators with high open-loop gain.

In the DLDOs proposed so far, a latch-based comparator has been used at this first stage, which is typically built using a strongArm latch, as shown in Figure 8(a)) [26], [45], [49], [50], [51], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60]. The strongArm latch offers high voltage gain and precision but comes at the cost of high transient current consumption at the inputs, which reduces system power efficiency. To avoid continuous current consumption, a sampling clock, F_{CLK}, is used in the comparator, but this clocking system causes kickback noise, and the speed of the comparator is limited by the sampling frequency. Although the kickback noise can be reduced by accepting a higher input offset at the differential pair, this can result in a large dynamic offset at the output, as well as larger area consumption, with speed improvements coming at the penalty of power consumption. Moreover, the speed is still limited by the metastability which is inherent in the latch design [61], [62], [63], [64].

Apart from the clock-based comparator, a few types of enhanced comparator architectures have been used in DLDOs. For instance, asynchronous comparators do not rely on a clock signal to determine the output but just use the internal trigger signals to resolve the output with minimum latency, resulting in a faster response time compared to clock-based comparators. Asynchronous comparators have been proposed in [65], [66], and [67] as a promising alternative to conventional comparator types in DLDOs due to their ability to improve regulator performance by reducing response time and increasing efficiency, as well as eliminating the need for a

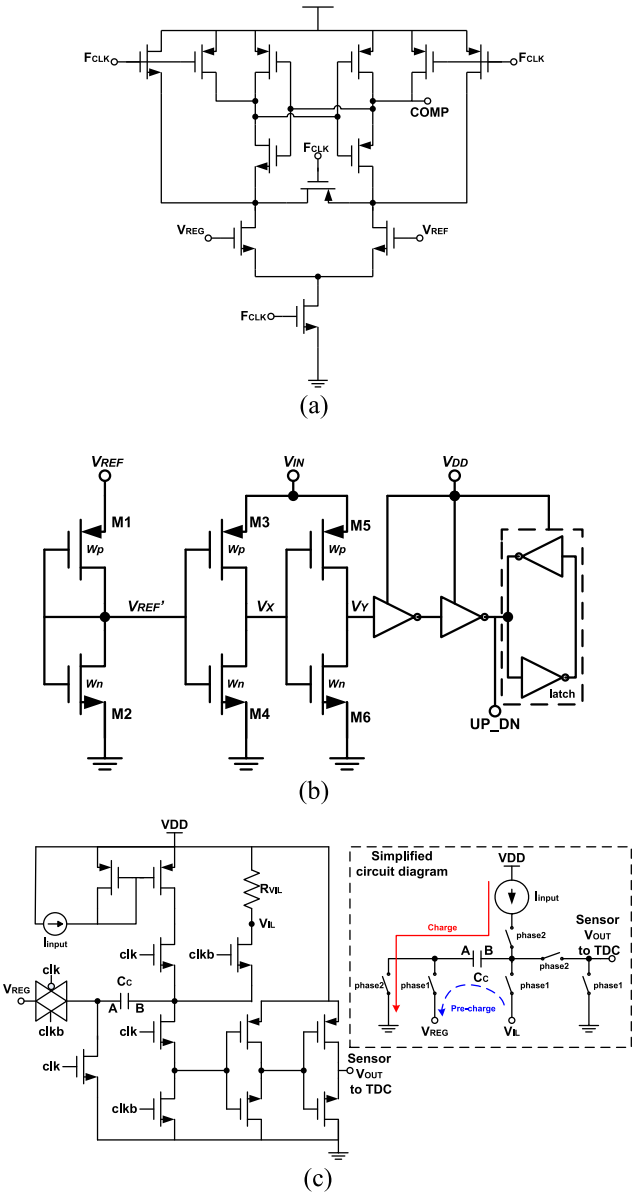

FIGURE 8. Schematics of (a) latch-based comparator, (b) logic-threshold triggered comparator, and (c) voltage sensor.

clock signal. By reducing power consumption and improving stability, asynchronous comparators offer an attractive option in DLDO design. Additionally, a logic-threshold triggered comparator (LTTC), as shown in Figure 8 (b), has been proposed in [68] as another good alternative with a simple, high-performance architecture compared to conventional comparators. In some proposed DLDOs, a voltage sensor is used instead of a comparator [35], [69]. In [69], the circuit utilizes a TDC-based signal converter to transform an analog voltage to digital. It consists of a voltage sensor and a time-to-digital converter. The simplified voltage sensor schematic is built with a capacitor bank with several switch controls for pre-charging and charging phases against a clocking system to convert the analog signals into time signals, as shown in

Figure 8 (c) [69]. The voltage sensor pre-charges the capacitor plates to V_{OUT} and V_{IL} during phase 1, generating a voltage difference between node A and node B. Node A is then grounded, causing node B to have a voltage of (V_{IL} - V_{OUT}). In phase 2, a constant current source, I_{input} charges node B, supplied by a PMOS in the saturation region. The linearity of the voltage sensor remains relatively unaffected by changes in node B's voltage, ensuring stable and accurate conversion of the analog signal to digital. Although the voltage sensor design is simple, it is sensitive to parasitic capacitance, which can worsen the performance at the back-end process.

Other than that, analog-to-digital converters (ADCs) such as flash ADCs [70], [71], delay line ADCs, and asynchronous ADCs [72], [73] have been utilized at the front stage of the proposed DLDOs to convert the output voltage into the digital domain and regulate it with the multibit digital controller [74], [75], [76], [77], [78], [79]. The ADC-based quantizer has a faster response time in analog voltage sensing within the power budget, but due to the limited resolution, the accuracy is compromised. To address this issue in accuracy, the multi-step switching technique is becoming popular, which briefly switches a larger number of power MOS units for a faster transient response or implements the input or output calibration to improve the ADC performances [80], [81], [82]. However, this comes with a tradeoff in quiescent power consumption for achieving higher speed. To enable fast transient response while consuming low power, asynchronous, event-driven, or self-clocking digital control are implemented [65], [66], [79], [83], [84]. However, the DLDO with multi-step switching requires improvement in load regulation at coarse-grained mode where the controller takes a longer time to settle to the targeted voltage, especially after a hard switching from fine-grained mode [76].

Overall, ADCs as time-domain quantizers generally provide higher accuracy with lower power consumption than voltage-domain quantizers as proposed in [44], [78], [85], and [86]. The voltage-controlled oscillator (VCO) or voltage-to-time converter (VTC), which plays an important part in the voltage-domain quantization in DLDOs, offers higher resolution with the penalty of slower speed and larger area consumption due to the required long delay chains. It is also important to carefully consider the advantages and characteristics of both comparators and ADCs when designing a system.

In general, using a comparator for 1-bit quantization and BiSHRs-based control can lead to a simpler design with lower I_Q, but to reach a steady state, many clock cycles are required due to the fixed step update in each cycle [87]. To improve transient response, increasing the clock frequency is indeed possible, but it also increases power consumption. However, DLDOs with comparator-based bang-bang control may suffer from limit cycle oscillations (LCO) problems. Limit cycle oscillations in an LDO are unwanted, repetitive oscillations that occur when the control loop is improperly designed or compensated. These oscillations have a fixed frequency and amplitude and can cause voltage ripple or noise at the output of the LDO. However, the LCO can be mitigated by adding a dead zone around V_{REG}. Consequently, ADCs have a dead zone that is equal to the LSB voltage by default, leading to a considerable decrease in limit cycle oscillations [88].

Moreover, using ADCs with higher resolution can further reduce LCO and improve V_{REG} accuracy at a steady state [89], [90]. The steady-state voltage ripple and LCO will be discussed in detail in the following subsection. Therefore, multi-bit voltage quantizers or ADCs are becoming more attractive for DLDOs. Ultimately, the choice between the comparator and the ADC should be based on the specific requirements and constraints of the system, such as performance, power consumption, and cost. It is vital to carefully evaluate and compare the advantages and disadvantages of each option to make an informed decision.

2) POWER SWITCH ARRAY

The power transistors in a power switch array are typically sized based on the maximum current and voltage requirements of the load to be driven. The sizing of the transistors in the power switch array directly affects the transient response and steady-state ripple of the DLDO, as shown in Figure 9. This is necessary to provide a stable output voltage with a low dropout voltage [44].

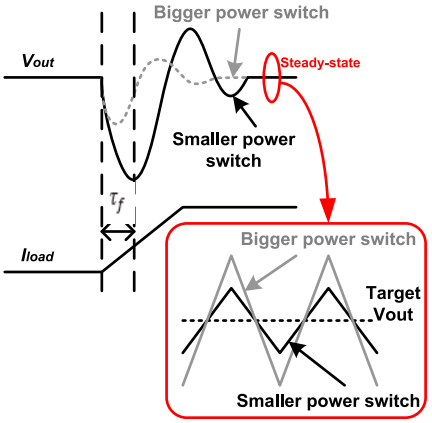

FIGURE 9. Impact of the power switch sizing on the transient response.

Unary-weighted sizing involves using transistors of equal size in the switch array [91], [92]. This approach is simple and easy to implement, but it can result in high ripple voltage and poor transient response due to the uneven current distribution among the transistors. This is because while the concept of unary-weighted sizing aims for equal current distribution, the actual current flow among the switches can deviate due to process variations and transistor mismatch. These deviations can introduce non-uniformities in the current distribution, leading to uneven operation and performance issues. These deviations in the current distribution can result in a couple of problems such as contributing to a higher ripple voltage in the output. The ripple voltage arises from the non-uniform charging and discharging of capacitors within the DLDO circuit, causing fluctuations or ripples in the output voltage.

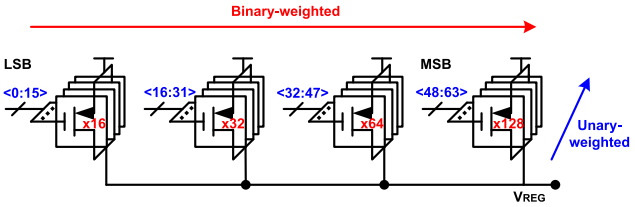

FIGURE 10. Overview of the power switch array [94].

The uneven current distribution among the transistors can exacerbate these ripple voltage variations. Apart from that, the non-uniform current distribution can impact the transient response of the DLDO. Ideally, a balanced and even current distribution ensures that each transistor contributes proportionally to the load current demands and facilitates a rapid response to load variations. However, when current is unevenly distributed, some transistors may carry more current than others, resulting in a slower response time and potentially poorer transient performance. Furthermore, the unary weighted power switch array requires a larger number of control bits for gain configuration, which in turn increases the area consumption and response time of the system [93].

Binary-weighted sizing involves using transistors that are proportional to powers of two in size, as implemented in [44], [65], [91], and [93]. For example, the largest transistor in the array would be twice as large as the second largest transistor, which would be twice as large as the third largest transistor, and so on. By using a binary-weighted approach, the DLDO can quickly determine the desired on/off combinations of the power transistors, starting from the most significant bit (MSB) to the least significant bit (LSB). This can lead to faster transient response time when the load current changes significantly. This approach can provide better current distribution and lower ripple voltage than a unary weighted power switch array, but it may cause longer settling time and larger voltage ripple, especially when non-LSB bits are toggling during the steady state. These issues arise as the binary-weighted approach provides a fast transient response at the expense of accuracy in the steady state. Therefore, a trade-off exists between transient response and steady-state performance, and the choice of power transistor sizing technique depends on the specific application requirements.

The work in [94] proposed the UBS (unary and binary sizing) scheme as shown in Figure 10, which combines the advantage of both binary and unary weighted sizing techniques. It uses multiple-unary weighted sizing with "1× ∼ 3×" transistors in both fine and coarse switch arrays. The notation "1× ∼ 3×" refers to the relative transistor sizes in the circuit, with each unary weighted switch array having a scaling factor of 1×, 2×, and 3× relative to the base transistor size, indicating a multiple-unary weighted approach. However, in Figure 10, the fine switch array has four binary-weighted groups, each containing eight unary-weighted PMOS transistors, but the coarse switch array also has four binary-weighted groups with transistors grouped in multiples of 16. The UBS scheme that has been proposed addresses the problems associated with the binary and unary schemes, such as large errors and slow speed, respectively. It enables a fast response time with minimal steady-state ripples and mitigates voltage peaking.

Alternatively, an exponentially weighted sizing scheme is implemented in [48] and [95] involving the use of transistors that are proportional to the exponential functions of a weighted factor, as shown in Figure 11. This approach can provide better current distribution and lower ripple voltage than the binary-weighted sizing, but it may require more complex control circuits and incurs higher cost due to the need for more precise sizing of the transistors by the q factor in the equation shown in Figure 11:

$$(W/L)_n = const \times q^n$$
$$q^n \geq 1 \tag{11}$$

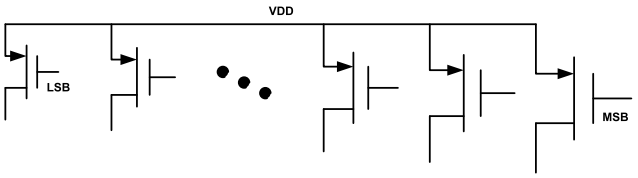

FIGURE 11. Exponentially-weighted power switch array [48].

In general, the choice of transistor sizing scheme will depend on the specific requirements of the DLDO design, including the desired output voltage, load current, and voltage regulation accuracy.

B. POWER-SPEED TRADE-OFF

Most S-DLDOs face a trade-off between power consumption and voltage-scaling speed, which stems from their synchronous operation in BiSHRs. As shown in Figure 4, the shift operations occur only at the rising edges of F_{CLK}, meaning that the voltage-scaling speed of the DLDO is primarily governed by F_{CLK}. Voltage scaling refers to the time taken by the DLDO output V_{REG} to track a certain voltage step of V_{REF}, expressed in FoM_3 in equation (7). Consequently, DLDOs can achieve faster voltage scaling by increasing F_{CLK}, but this also leads to a proportional increase in power consumption, as described in [96]. Figure 12 demonstrates the general trend of the power-speed trade-off and the detailed is given in [65]. The power-speed trade-off significantly impacts the load transient performance of the DLDO, which will be discussed in the subsequent subsection.

C. POOR TRANSIENT RESPONSE AND PSRR

The S-DLDOs used to regulate the output voltage of power supplies can experience significant voltage overshoot or undershoot during load current transients, which is caused by delays in the comparator and BiSHRs, as shown in the load transient response analysis as shown in Figure 13 [94].

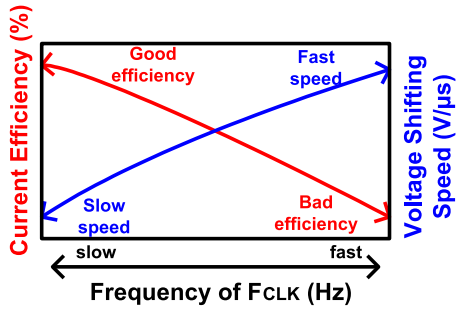

FIGURE 12. Illustration of the power-speed trade-off of the S-DLDO.

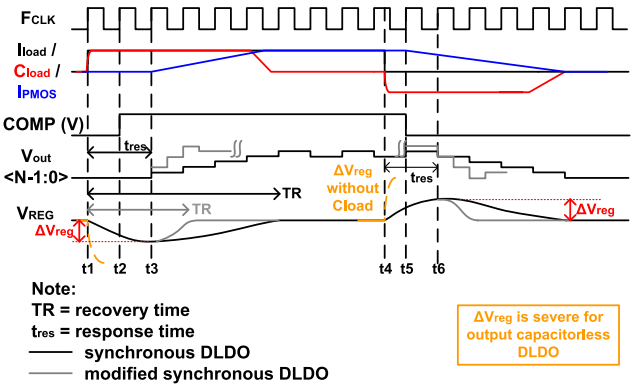

FIGURE 13. Load transient response analysis of the typical and modified S-DLDO [94].

In the case of a load current step-up, the S-DLDO cannot regulate instantaneously by switching the power switch array according to the load due to these delays. Therefore, the dynamic current from the output capacitor C_{load} starts discharging to the I_{load} to compensate for the voltage undershoot. The comparator output, COMP, toggles at the next rising edge of F_{CLK} and this is fed to the BiSHRs. After one additional clock period, the BiSHRs start shifting at the rising edge of F_{CLK}. The S-DLDO loop takes two or more cycles to generate the required current to stabilize the output voltage. The delay in response is represented by t_{res}, which is the loop response time of the S-DLDO when I_{load} changes. As mentioned before, a large C_{load} can help reduce the undershoot or overshoot voltage, as indicated by the large variation of V_{REG}, but at the cost of large area consumption and long settling time at the output [74]. Due to the power-speed trade-off in S-DLDOs, they can either respond quickly to load transients or operate at a low switching frequency, but not both. Hence, adjusting the switching frequency, F_{CLK}, can optimize the DLDO's performance, balancing the trade-off between the response time and efficiency [52], [85], [96], [97].

PSRR refers to the ability of a voltage regulator to reject variations or fluctuations in the power supply, often referred to as ''power supply noise'' at different frequencies. PSRR is frequency-dependent and measures how effectively the LDO can attenuate or reject noise present on the power supply line. It provides information about the LDO's performance in filtering out AC noise components and maintaining a stable output voltage in the presence of such disturbances. Although both line regulation and PSRR are important characteristics of LDOs that address the performance through the deviation of output voltage concerning the input, line regulation focuses on the response to DC variations in the input voltage, while PSRR characterizes the regulator's ability to reject AC noise on the power supply line at various frequencies. During steady-state, line regulation and PSRR can be considered equivalent [28]. However, as soon as AC noise or frequency-dependent disturbances come into play, the differences between line regulation and PSRR become apparent. The PSRR is often expressed in decibels (dB) and is calculated as the ratio of the change in the power supply voltage to the resulting change in the output voltage. Mathematically, the PSRR equation can be represented as:

$$\text{PSRR [dB]} = 20log_{10}(\frac{V_{OUT}}{V_{IN}}) \tag{12}$$

where PSRR is the power supply rejection ratio in decibels. V_{OUT} is the output voltage of the regulator and V_{IN} is the power supply voltage.

However, as compared to the ALDO counterparts, conventional DLDO is inferior in PSRR performance. Due to the dynamic sampling process in DLDOs, the control bit N changes in the loop regulation, assuming it is synchronized with the optimum control word N_{opt} at the rising edge of the sampling clock. This can result in significant glitches during the steady state while the input supply is rippling, as shown in Figure 14 [97]. In an ideal case, the controller can find N_{opt} at each synchronization time (t_0, t_1, t_2, t_3) and regulate V_{OUT} back to V_{REF} at every sampling interval. However, the output still ripples as the regulation occurs at every clock edge, not in the interval between t_0 and t_1. Therefore, the PSR at the sampling interval or certain DC point can be defined using a resistive divider equation:

$$\text{PSRR} = \frac{1}{\frac{R_{load}}{r_{ds}} + 1} \tag{13}$$

where R_{load} is the load resistance and r_{ds} is the power transistor drain to source resistance. This implies that the DLDO is susceptible to input noise during the periods of sampling. During the non-ideal case where $N \neq N_{opt}$, an error, V_e forms, and the regulation increase respective to the error, thus resulting in a large output ripple. The faster the clock, the smaller the glitches at the V_{OUT}. Respective to equation (3), a smaller line regulation indicates a good PSRR of the DLDO, meaning that the difference between the input and output voltages should be close to each other, or a smaller ΔV_{OUT} is preferred. A burst mode technique is introduced in [98] to reduce the ΔV_{OUT} by using nonlinear control. This high-efficiency technique also reduces the output voltage ripple.

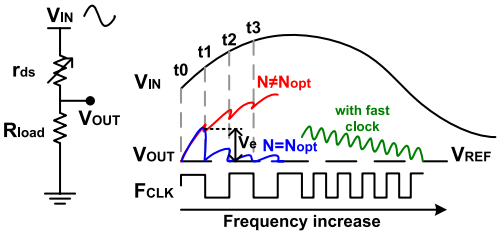

FIGURE 14. DLDO output waveforms with input ripples [97].

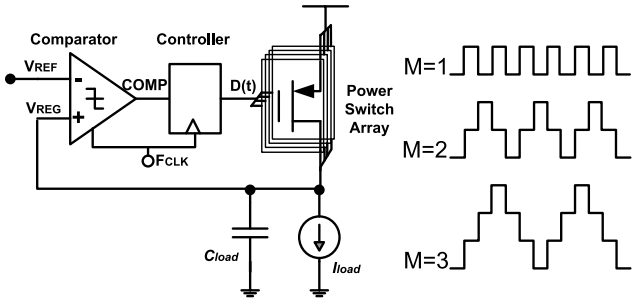

FIGURE 15. DLDO sampling outputs with different LCO modes [88].

D. STEADY-STATE OUTPUT VOLTAGE RIPPLES AND LIMIT CYCLE OSCILLATION (LCO)

From the previous subsection, it is obvious that another inherent drawback of an S-DLDO is output voltage ripple, V_{ripple}, especially during transient steady-state. The output voltage ripple, V_{ripple}, can be estimated using the equation [99]:

$$\Delta V_{ripple} \approx \frac{V_{IN} \times R_{load}}{r_{ds} \times N} \tag{14}$$

Several approaches have been implemented to suppress V_{ripple}, such as the implementation of a current source power-FET using a System on Chip (SoC) approach as proposed in [100]. The power-FET array is digitally switchable through PMOS headers with complementary-to-absolute-temperature voltage (VCTAT) NMOS current sources, which reduces V_{ripple} and variation across PVT. Moreover, a freeze mode can effectively eliminate V_{ripple} by fixing the number of power transistors when the regulator output voltage, V_{REG}, is close to the reference voltage, V_{REF} [65]. However, this method may be susceptible to an offset between V_{REG} and V_{REF} if there is a current error between I_{PMOS} and I_{load}. The design architecture, such as VTC-based DLDO [44], as well as a high-resolution ADC-based DLDO [89], [90], also contributes to the steady-state V_{ripple} improvement.

DLDOs may experience steady-state LCO, particularly at light load conditions, due to quantization errors in the loop. The occurrence of LCO can be investigated by referring to Figure 15 consists of an ADC (comparator), a digital controller, and a DAC (usually the power switch array). This can occur when the resolution of the DAC and ADC is imbalanced, resulting in the DAC being unable to regulate the DLDO output according to the reference from the ADC. As a result, the controller output and DLDO output oscillate around the target V_{OUT}, with the average of the oscillating controller output being the same as the target value. To reduce LCO, a dead zone can be added around the output voltage using comparator-based bang-bang control, with the cost of DC regulation accuracy [87]. The ADC also provides an inherent dead zone equivalent to LSB, which helps mitigate LCO to some extent. However, at the larger integral gain and light load conditions, LCO can still occur. Adding zeros at z_{PI} and z_{PD} can also help reduce LCO, as proposed in [88], where adding a feed-forward zero forces the DLDO system into mode 1 or mode 2 LCO. Figure 15 shows waveforms of the controller output, $D(t)$ for LCO modes 1, 2, and 3, with the corresponding V_{ripple} having a frequency of two times the LCO mode, $Freq$=2M, where $Freq$ is the DLDO sampling frequency and M is the mode of LCO. It's important to note that while LCO can cause voltage ripple, it does not typically cause loop instability. Various design techniques have been proposed to eradicate LCO in the DLDO, such as using a higher resolution DAC than the ADC or introducing a dithering and dynamic frequency scaling mechanism to eliminate LCO and improve DLDO performance using a first-order sigma-delta modulator [101].

V. STATE-OF-THE-ART DLDOs

In the past decade, several DLDO architectures have been suggested to overcome the design trade-offs and limitations mentioned earlier. A detailed comparison of the state-of-the-art DLDOs will be presented in this section and the most recent DLDOs are benchmarked with the respective applications.

A. ARCHITECTURAL ADVANCEMENTS IN S-DLDO

During the early stages, DLDO designs were mostly based on the S-DLDO topology, but with different digital controllers or circuits that had similar functionality to the basic building blocks in a conventional S-DLDO. A power-efficient DLDO can be constructed using a comparator and BiSHRs with very low quiescent current [26], [65], [102], [103], but at the cost of slow loop transient response. Therefore, increasing the clock frequency to speed up the transient response is necessary to improve the performance of a conventional S-DLDO. Various techniques have been introduced, such as coarse-fine dual-loop controllers [104], [105], [106], adaptive sampling [49], [52], [53], [60], [76], [78], [85], phase integration (PI) [35], [74], [77] controllers, and conditional clock boosting controllers [44], [98], [105]. To further improve the transient performance of a DLDO, an auxiliary path or transient enhancement circuitry [44], [98], [104], [106], [107] can be implemented as supportive circuitry in the loop system to improve the regulator's response to sudden changes in load current. When there is a sudden increase in load current, the output voltage of the LDO can drop due to the regulator's internal resistance. The transient enhancement circuit helps to reduce this drop by quickly adjusting the output voltage to compensate for the change in load current.

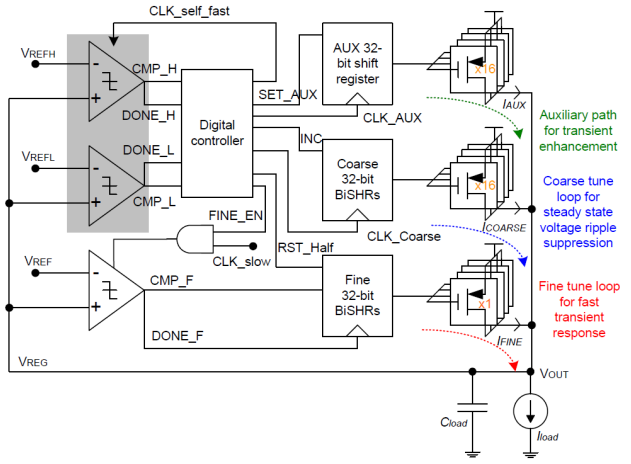

FIGURE 16. Coarse-fine DLDO incorporating the auxiliary path [104].

The proposed DLDO architecture design in [104], shown in Figure 16, includes a coarse-fine PMOS array consisting of two sets of PMOS transistors with different sizes. The coarse-tuning PMOS array consists of larger transistors that are turned on during steady-state conditions to reduce quiescent current, while the fine PMOS array consists of smaller transistors that are turned on during transient conditions to provide a fast transient response. An auxiliary power stage provides an additional current path during transient conditions to improve the transient response of the DLDO. The auxiliary PMOS array and shift register (SR) are controlled by the same clock signal as the conventional DLDO but with a phase shift. During transient conditions, the auxiliary SR turns on half of the PMOS transistors in the auxiliary PMOS array, which provides an additional current path and reduces the voltage drop across the main PMOS array.

The proposed DLDO is fabricated using a 65-nm CMOS process and shows improved performance in terms of settling time, undershoot, and overshoot compared to other DLDOs. It has a maximum output current of 100 mA, quiescent current of 75 μA, and peak current of 3.3 mA. When the load current was changed from 10mA to 100 mA, the proposed DLDO's undershoot and overshoot decreased from 139 mV to 47 mV and 30 mV to 23 mV, respectively, with a settling time decreasing from 2.1 μs to 130 ns. The measured ripple voltage is 4 mV at a steady state at a load current of 10 mA. Overall, the proposed coarse-fine DLDO with an auxiliary power stage and a complete comparison signal improved the transient response, reduced settling time, and minimized the undershoot and overshoot voltages during load current changes. It also achieved a low quiescent current and high maximum output current, making it a promising solution for applications requiring high performance and efficiency.

Furthermore, in addition to the digital controller, the ADC also plays a crucial role in the quantizer of a DLDO. Several studies and research have been conducted in this area to further enhance the performance of DLDOs, utilizing various types of ADCs such as flash ADC, delay line ADC, and asynchronous ADC at the front stage [74], [75], [76], [77],

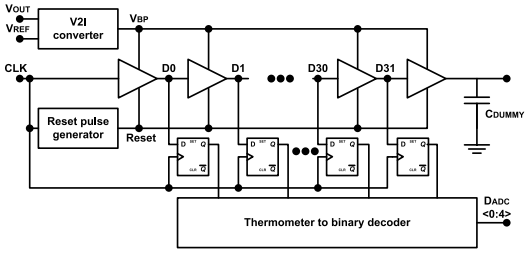

FIGURE 17. Overview of the delay-line ADC in [74].

[78], [79]. For instance, a delay-line ADC (DL-ADC) integrated with a PI controller was proposed in [74], as shown in Figure 17, which achieved a peak current efficiency of 99.2% and a settling time of 250 ns. The DL-ADC used in the DLDO design had a resolution of 5 bits and employed a 32-cell current-starved delay line with a voltage-to-current converter to control the delay of each cell. As the DLDO output voltage decreases, the delay of each cell increases, resulting in a decrease in the digital equivalent code of the DLDO output voltage. Although the V-I block in the voltage-to-time converter (V-I) has a nonlinear transfer characteristic, it exhibits promising monotonicity. By sensing the DLDO output voltage, the V-I converter converts it into current to regulate the propagation time of the current-starved delay cell. In the DL-ADC design, a thermometer-to-binary decoder based on a multiplexer is utilized to generate the digital output. However, the resolution of the DL-ADC directly affects the DLDO output voltage regulation accuracy at steady-state. As the resolution increases, the delay-line chain becomes longer, and the area consumption increases. Nevertheless, the transient-enhanced proportional-integral (PI) controller has helped this proposed DLDO achieve high efficiency and fast settling time. Incorporating an ADC into a DLDO regulator can provide improved accuracy, enhanced monitoring, and real-time adjustments to ensure stable operation under varying load conditions, which is ideal for applications that require stable and accurate voltage regulation, including microprocessors, digital signal processors, microcontrollers, and other digital integrated circuits. The DLDO design can also be used in portable electronic devices such as smartphones, tablets, and laptops, where low power consumption is critical [108], [109]. However, it may increase the complexity and power consumption of the circuit, impacting overall efficiency and requiring additional design considerations. The cost of an ADC should also be considered as it can be a significant portion of the overall cost of the LDO circuit. In some cases, a time-to-digital converter (TDC) [69] can be used instead of an ADC to transform the output voltage into digital codes. However, the correlation between the buffer-gate's power supply and propagation delay in TDC is not linear, resulting in a deterioration of the TDC's resolution.

Other than using ADC as the time-domain quantizer, voltage-to-time circuits have also been implemented in the quantizer part of DLDOs [44], [78], [85], [86]. For example, in [85], voltage-to-time conversion is performed by a VCO

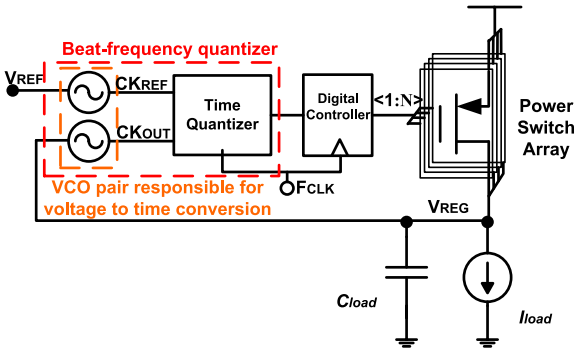

FIGURE 18. DLDO with the proposed beat-frequency quantizer [85].

pair-fed to a reference clock and a loop feedback quantization error to form a beat-frequency quantizer (BFQ), as shown in Figure 18. The proposed DLDO operates in two modes: sampling mode and regulation mode. In the sampling mode, the regulator measures the output voltage error and the load current to determine the optimal output voltage level. In the regulation mode, the regulator actively adjusts the output voltage level to maintain the desired voltage level. The BFQ is used to accurately measure the output voltage error by comparing the output voltage to a reference voltage by using beat-frequency technique. The adaptive sampling technique is used to reduce the sampling frequency and power consumption when the output voltage is stable and increase the sampling frequency when the output voltage is changing. The proposed LDO regulator was implemented in a 65 nm CMOS process and achieved a power supply rejection ratio of -38 dB at a 1 MHz cut-off frequency and a load regulation of 0.638 mV/mA. The regulator also demonstrated a fast transient response with a settling time of 1.24 μs at a 50 mA load current.

In summary, the S-DLDO still suffers from slow load transient response despite implementing various techniques mentioned above. As discussed in Section II-A, according to Equations (7) and (8), the LDO response time is directly proportional to the load capacitance required to provide a stable output with minimum current consumption. This limits the S-DLDO's ability to downscale the supply voltage and eliminate the output load capacitor. Moreover, to ensure stable operation across process, voltage, and temperature (PVT) variations, design margins must be widened, which exacerbates the issue of slow transient response.

B. ANALOG-ASSISTED DLDOs

An analog-assisted DLDO has a different approach to achieving voltage regulation compared to conventional digital LDOs. The analog-assisted DLDO uses a combination of analog and digital circuits, whereas the DLDO uses only a digital control loop. Generally, the AA-DLDO leverages the speed and accuracy of the digital control loop while maintaining the stability and noise immunity of analog circuits. analog-assisted DLDOs typically have a faster response time than DLDOs, responding quickly to changes in input voltage due to the use of digital control loops. Digital circuits are generally more immune to noise than analog circuits. Analog-assisted DLDOs use analog circuits to provide stability while still using digital circuits to provide speed, accuracy, and noise immunity [38]. However, DLDOs can be more power-efficient than analog-assisted DLDOs, as they use digital circuits exclusively, which can operate at lower power levels than analog circuits. analog-assisted DLDOs provide more design flexibility than DLDOs since both analog and digital circuits can be used to optimize the regulator's performance. In contrast, DLDOs are limited to using digital circuits only. Hence, the choice between the two depends on the specific application requirements and design constraints [38].

To further improve the S-DLDO's performance, several analog-assisted techniques have been proposed in [75], [110], [111], [112], [113], [114], and [115]. Figure 19 presents a passive analog-assisted SR S-DLDO through the high-pass filter created by R_C and C_c components. The output voltage is connected to the ground node of the gate drive of the inverter in an AC-coupled manner that allows the power switches to turn on immediately with the negative gate drive voltage. One benefit of this passive analog-assisted loop is that it has no negative impact on the available voltage headroom or power consumption. However, the working principle of this analog-assisted loop is that in cases where the load current is low and only one least significant bit (LSB) power transistor is active, the coupling has a minimal effect and provides only a small amount of fast and instantaneous compensation current to the LSB when the drop in output voltage occurs.

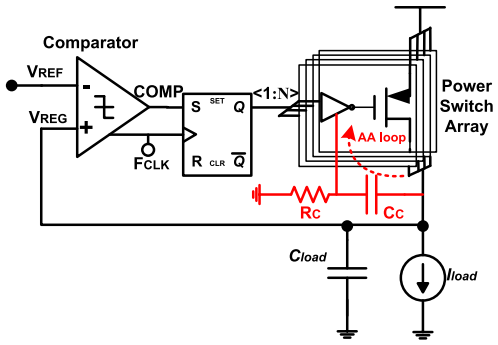

FIGURE 19. The S-DLDO with one analog-assisted loop.

In [115], an AC-coupled high-impedance (ACHZ) loop is introduced into the charge-pump-based DLDO. The proposed ACHZ loop theoretically functions like the AA S-DLDO in Figure 20. In the suggested DLDO architecture, a lone PMOS power transistor is utilized, powered by two charge pumps that are driven by a pair of time-interleaved dynamic-inverter-based continuous-time comparators, which set the upper and lower regulation boundaries. To enhance the regulation accuracy of the LDO, a low-current charge pump is

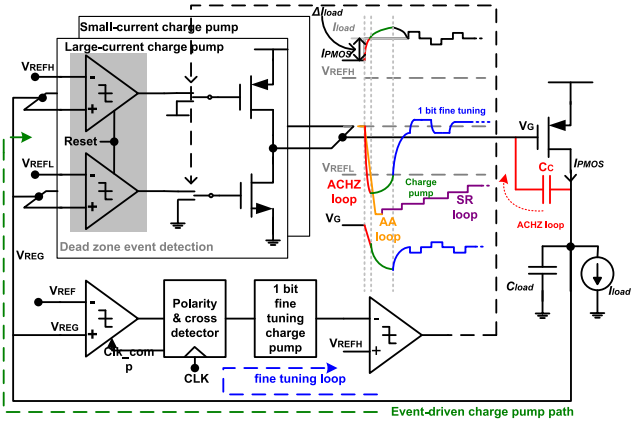

FIGURE 20. Overview of charge-pump-based DLDO with ACHZ analog-assisted loop [115] and the output waveforms comparison.

also used. Capacitor C_c is placed across the power transistor to form the direct AC-coupled high-impedance (ACHZ) feedback loop to enhance the stability and dynamic response time of the system. Due to the single-power transistor used, the analog-assisted ACHZ loop has a significant impact on the overall DLDO operation.

To further enhance the regulation accuracy, an auxiliary clocked comparator is employed to compare the output voltage with V_{REF} and detect whether the output voltage is higher or lower than the desired reference voltage. This auxiliary comparator is accompanied by a 1-bit fine-tuning charge pump to further refine the regulation. During a steady state, where V_{REG} is within the dead zone between the boundaries, the main charge pumps are disabled, and the gate voltage, V_G, is high. Any residual charge stored on C_c and parasitic capacitance C_G determines the power transistor's gate voltage and thus the current supplied by the LDO. The ACHZ loop helps to significantly shorten the response time by providing near-instantaneous compensation current through the power transistors.

The charge pumps come into effect when V_{REG} falls below V_{REFL}, and the lower continuous-time comparator is triggered to discharge V_G and further increase the current through the power transistor to assist V_{OUT} settle back within the dead zone. The paper reports impressive performance results for the proposed LDO, achieving a sub-4-fs FoM_1 and a low voltage drop of only 36mV at a load transient current of 100 mA which is significantly lower than other state-of-the-art LDOs. The output voltage noise is also low, at 5.6 μV_{rms}. The LDO also achieves a fast load transient response, with a settling time of 65 ns for a FoM_1 of 1.8 fs. Additionally, for the entire load range of 1 μA to 105 mA, the steady-state ripple amplitude is less than 15 mV.

Overall, the proposed LDO design offers a promising solution to the power management challenges faced by modern electronic systems, especially those that require high efficiency and low voltage drop, such as battery-operated devices.

C. HYBRID LDOs

The hybrid topology differs from dual-loop DLDOs, which use two digital loops. Dual-loop DLDOs are a type of DLDO architecture that includes both a regulation loop and a noise-cancellation loop to improve PSRR performance. In contrast, the hybrid topology includes both an analog LDO and a digital LDO as shown in Figure 5 (c) working in parallel to improve overall performance.

Generally, the hybrid LDO employs a closed-loop control that can switch adaptively between digital and analog modes depending on the difference between V_{REF} and V_{REG}. The hybrid topology was implemented in [48], [97], [116], [117], [118], [119], [120], and [121]. By combining the benefits of both analog and digital LDOs, hybrid topology can achieve better PSRR performance and reduced sensitivity to supply noise, making it suitable for driving noise-sensitive loads such as RF and analog circuits. When the quantization error exceeds a certain threshold during load transient states in hybrid LDO, the digital control loop is activated, while the analog controller takes over when the quantization error is small. This enables the hybrid LDO to achieve high PSRR and ripple-free output voltage. Hybrid LDO can provide good load transient performance while maintaining a ripple-free output voltage with high PSRR. However, like ALDO, hybrid LDO has a significant voltage dropout which compromises the power efficiency and limits the regulation range.

D. ASYNCHRONOUS DLDOs (AS-DLDOs)

The S-DLDO offers the benefit of a straightforward design, with the clock serving as the primary controller of the circuit's operation. However, this approach is not without its challenges. One issue is the potential for clock skew, which can result in incorrect internal control state values and prevent the digital LDO's output voltage from stabilizing. In the context of digital circuits, clock skew refers to the variation in arrival times of the clock signal across different parts of the circuit. Clock skew can occur due to various factors such as differences in trace lengths, temperature variations, or process variations [94]. Clock skew can lead to variations in the timing of critical signals involved in the voltage regulation process. If the control signals do not arrive at the intended components of the circuit synchronously, it can result in incorrect internal control state values and hinder the proper stabilization of the output voltage. Another issue is the difficulty of setting the operating frequency correctly, which generally involves a power-speed trade-off. To overcome these limitations in S-DLDOs, an asynchronous shift register has been introduced and implemented in conventional DLDOs. This new technique is known as the asynchronous DLDO (AS-DLDO) group. Figure 21 shows the simplified circuit diagrams of an AS-DLDO.

The development of AS-DLDOs has undergone several improvements in the design architecture since its early stages [65], as proposed in [50], [55], [66], [67], [76], [117], and [122]. Hybrid architectures have been proposed in [50]

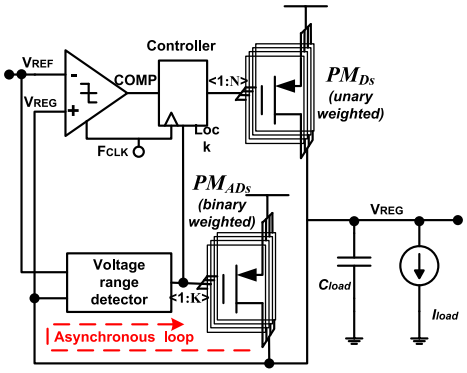

FIGURE 21. Simplified circuit diagram of AS-DLDO.

and [55], which combine asynchronous and synchronous loops as coarse-fine loops, aiming to achieve a quick response to load transients and reduce the size of the output capacitor, C_{load} or even achieve an output-capacitor less LDO. Although C_{load} was significantly reduced in these DLDOs, these architectures are susceptible to voltage ringing during loop transitions as the asynchronous and synchronous loops work independently, and each loop is regulated by its own voltage quantization stages, causing rough transitions.

AS-DLDOs regularly adopt a controller that works at the natural delay of circuit components, eliminating the necessity for F_{CLK} and downscaling C_{load}. However, the delay of circuit components is greatly influenced by PVT variations and becomes more vulnerable in low-voltage environments, increasing delay. Consequently, the performance of asynchronous DLDOs may not be sustained in low-power and low-voltage applications.

The AS-DLDOs proposed in [65], [84], [94], [122], and [123] eliminate the need for output capacitors, and clock-less or self-clocking systems have been implemented in [22], [51], [94], [107], [123], and [124] to enable these DLDOs to outperform synchronous DLDOs in terms of I_Q, current efficiency, response time, and dynamic range of load current. For example, an output capacitor-less asynchronous DLDO was proposed in [122], as shown in Figure 22. The proposed asynchronous loop is designed to suppress voltage undershoot by connecting a clock-less voltage-range tracker (VRT) to a binary-weighted PMOS switch array. The VRT tracks voltage across predefined ranges and provides output codes in proportion to the level of deviation. When there is an undershoot, the VRT injects current to compensate for the deviation before the coarse loop responds. The proposed asynchronous loop can significantly reduce voltage undershoot compared to typical DLDOs and is equivalent to an 80 nF capacitor. The proposed OCL-DLDO occupies an active area of 0.0418 mm^2 and has a V_{REG} range of 0.55 V to 1.15 V for an input power supply of 0.6 V to 1.2 V. The regulator achieves a minimum dropout voltage of 50 mV with a response time of 0.9 μs at a maximum I_{LOAD} of 24.5 mA, and the measured startup response shows the operation of the

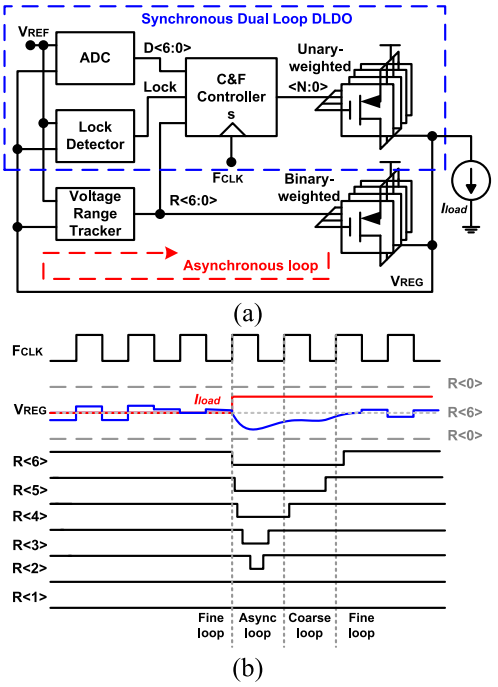

FIGURE 22. (a) AS-DLDO and (b) the operational waveforms of the during load transient [122].

coarse and fine loops and the transition between the two. The proposed DLDO has a peak current efficiency of 99.91 % and a figure of merit (FoM$_1$) of 2.87 fs.

The self-clocked DLDO [94] includes an asynchronous kick-start mechanism that eliminates the need for output capacitance during load transients. The self-clocked technique was achieved with a level-triggered comparator (LTTC), voltage-range detector (VRD), and BiSHRs, resulting in a shortened total feedback response time. However, the self-clocked structure is vulnerable to PVT variations and consumes significant quiescent current due to its fast self-shifting clock, making it unsuitable for low-power applications.

Besides the techniques introduced above, event-driven AS-DLDOs [83], [84], [124], [125] also help achieve significant downscaling of the output capacitance, and the event-driven control, which operates conditionally, eliminates the need for a clocking system. Moreover, the introduction of event-driven DLDOs has overcome the limitation of the AS-DLDOs' circuit operation, which is sensitive to PVT variations. This is because the event-driven control substantially minimizes the latency of the control loop more effectively by immediately detecting and responding to any variations in V_{REG} without requiring a sampling clock. The minimum loop latency allows event-driven DLDO designs to achieve good transient response with minimal output capacitor load or even in an output-capacitor-less architecture [94]. Generally, an event-driven circuit is formed with a transient detection circuit to detect the ΔV_{OUT} from the feedback loop and produce a series of conditional pulse signals to drive the

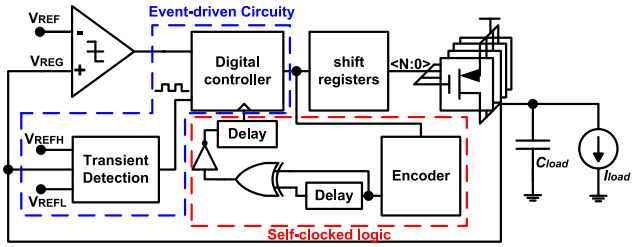

FIGURE 23. Overview of the event-driven and self-clocked AS-DLDO.

digital controller parallel with the synchronous loop. The self-clocked DLDO also uses a transient detection circuit but produces only a reset pulse, which is fed into the digital controller. The output of the digital controller is then looped back through a self-clocked logic [107], which contains the encoder, frequency doubler, and a series of delay chains to generate a clock for the digital controller. Figure 23 shows the simplified block diagram for event-driven and self-clocked DLDOs.

E. COMPARISON ON STATE-OF-THE-ART DLDOs

In summary, the S-DLDO typically consists of a comparator and BiSHRs with very low quiescent current, at the expense of slow loop transient response. Various techniques, such as coarse-fine dual loop controllers, adaptive sampling, phase integration controllers, and conditional clock boosting controllers, have been developed to enhance performance and speed up the transient response. To improve the regulator's response to sudden changes in load current, an auxiliary path or transient enhancement circuitry is typically employed.
S-DLDOs are easy to design and robust against PVT variations but require a large C_{load} and suffer from power-speed tradeoffs, large steady-state ripples, and poor PSRR.

Analog-assisted DLDOs, on the other hand, offer faster response time and noise immunity, while maintaining stability and accuracy, and reducing the need for C_{load} by using a smaller compensation capacitor. However, this capacitor still consumes silicon area. The S-DLDO approach uses a clock as the primary controller, but it can face challenges such as clock skew, difficulty in setting the operating frequency, and vulnerability in low-power and low-voltage applications. Asynchronous DLDOs (AS-DLDOs) have been introduced to eliminate the need for a clock and use an asynchronous shift register. Asynchronous, self-clocked, and event-driven DLDOs can overcome the clock-dependent limitations of S-DLDOs in terms of current efficiency, response time, and dynamic range of load current. In some cases, they can achieve good transient response with minimal or no output capacitor. Hybrid architectures that combine asynchronous and synchronous loops have been proposed to achieve quick responses to load transients and reduce the size of the C_{load}. However, these architectures are susceptible to voltage ringing during loop transitions. Hybrid architectures are best suited for driving analog load circuits due to high PSRR without ripples at output voltage, but their voltage regulation range is limited due to a large dropout voltage, making them unsuitable for driving digital load circuits when operating in hybrid mode. However, in Section IV, it is emphasized that despite the variations in performance offered by different DLDO topologies, the design process should begin with careful consideration at the transistor level due to various design constraints in the building blocks. Figure 24 shows the design constraints on DLDO variants.

There are various types of DLDOs with distinct characteristics and benefits, each suitable for specific applications. The state-of-the-art DLDOs, such as synchronous DLDOs, analog-assisted DLDOs, hybrid LDOs, AS-DLDOs, self-clocked DLDOs, and event-driven DLDOs, were compared based on the performance metrics and potential applications. S-DLDOs are typically used for digital load circuits that have low voltage and low current consumption such as the SoC PMIC of low-power applications in IoT, sensors, and portable, wearables devices. Analog-assisted and hybrid LDOs offer a balanced trade-off between power consumption and performance which is appropriate for applications such as audio amplifiers, motor control, and LED drivers that has multi-core processor platforms where fast switching or load currents occur irregularly. These LDOs have a larger output load capacitor and faster transient response time than pure DLDOs that are resistant to higher output load current changes without any stability issues. Furthermore, these DLDOs are less prone to LCO due to better stability. AS-DLDOs are optimal for high-speed applications such as data centers and high-performance computing that require a fast transient response. The greatest contribution of self-clocked or event-driven DLDOs which results in the output-capacitors (OCL) design are the best choice for submicron applications like microprocessors and the self-clocked DLDOs are suitable for the energy harvesting system due to the requirement on the voltage regulation for the harvested energy at the front end to supply a stable voltage output.

Table 2 shows the measured performance parameters for most of the recent state-of-the-art DLDOs. The table summarizes the comparison of the architecture advancement on S-DLDOs from the works in [35], [44], [49], [52], [53], [68], [74], [77], [78], [85], [86], [92], [98], [101], [104], and [106], AA-DLDOs with the study from [75] and [115], the study of [121] which represents the hybrid LDO while the comparison of AS-DLDOs with self-clocked and event-driven architectures are done from the study of [22], [50], [51], [55], [107], [122], and [123]. From the table, it is obvious that most of the DLDOs are suitable for low-voltage applications with the possibility of scaling down to 0.45 V. Moreover, the comparison shows that the asynchronous self-clocked DLDOs successfully downscale the on-chip C_{load} to 0.1 nF or even eliminate the C_{load} as an OCL design in [122] and [123].

The self-clocking burst logic in [51] helped the DLDO to achieve a dropout voltage as low as 50 mV and an outstanding FoM_1 of 0.075 ps, with a very low quiescent current of 0.65 μA. The event-driven charge-pump-based DLDO with

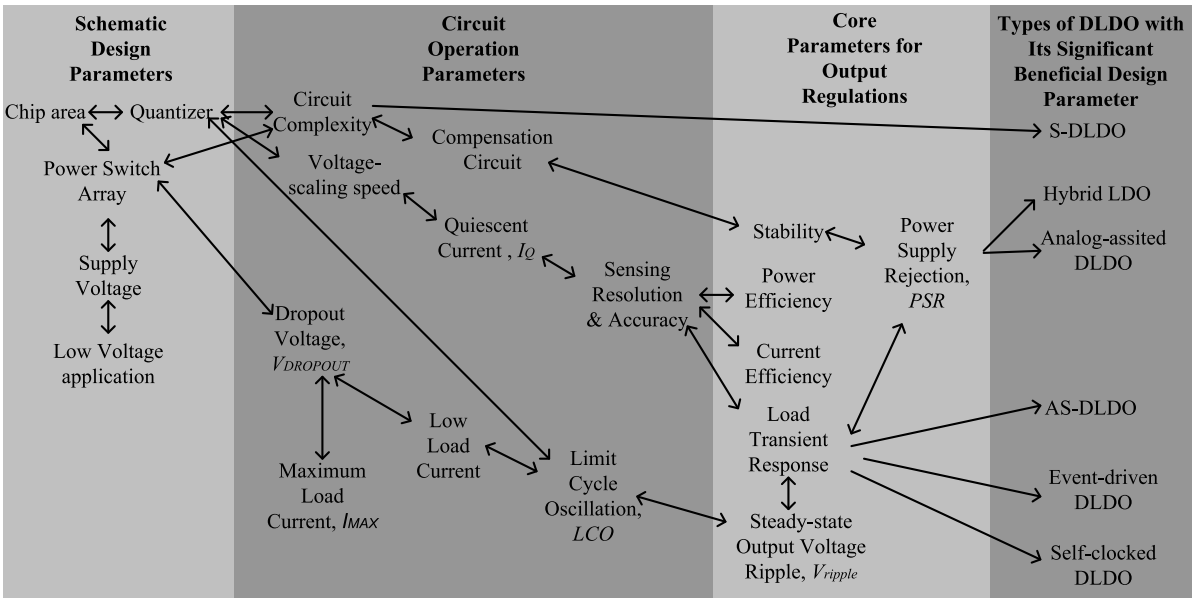

FIGURE 24. Design constraints on DLDO variants.

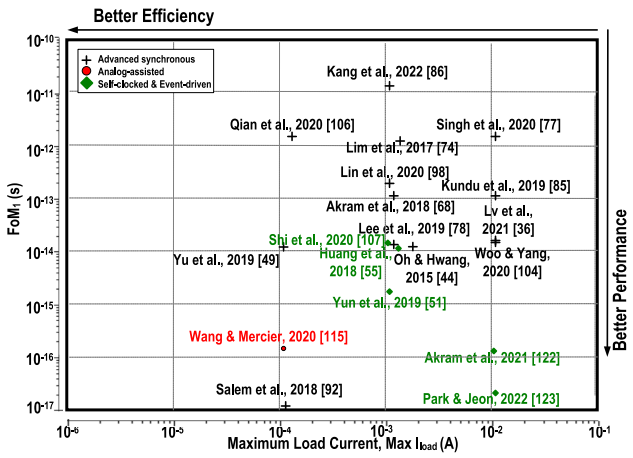

FIGURE 25. FoM_1 versus load current.

high impedance AC-coupled analog-assisted loop in [115] has achieved the lowest FoM_1 of 3.8 fs among all the proposed designs while supporting a large load current up high to 105 mA with a fast transient response. The hybrid DLDO in [121] outperforms other DLDOs with the load regulation of 0.09 mV/mA and a fast-settling time that is less than 1 ns due to the continuous time operations of analog blocks offering a good PSRR in the hybrid LDO.

Figure 25 plots the relationship of the maximum supporting I_{load} across the FoM_1. This relationship of these parameters is elaborated with equation (5) discussed in Section II. By targeting a lower FoM_1, the DLDO offers a better performance since it tends to support a higher load current while consuming a lower quiescent current. FoM_1 from equation (5) is used instead of FoM_3 from the equation (7) to avoid source error that can lead to artificially improved FoMs.

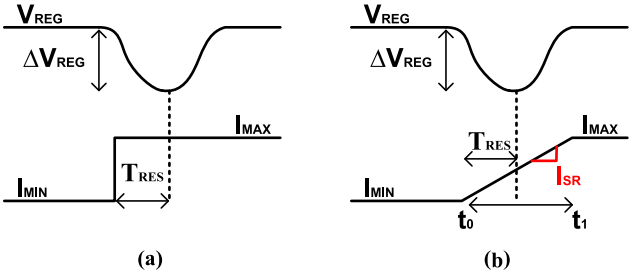

FIGURE 26. Effect of load current slew rate on FoMs [74].

This is because it should be noted that Equation (7) is only valid when the response time is significantly longer than the step edge time used in the measurement. When the step edge time is comparable to or longer than the response time, the equation becomes incorrect. The FoM_1 is based on the assumption that the load current changes instantaneously as depicted in Figure 26 (a) where the T_{RES} is expressed by equation (8).

Figure 26 demonstrates the critical significance of the response time of the DLDO when comes to performance benchmarking. Typically, the load current slew rate, I_{SR} during a load change is finite, as illustrated in Figure 26 (b). The response time of the DLDO is dependent on the load current slew rate and can be expressed as a function of I_{SR} [74].

$$T_{RES} = \sqrt{\frac{2C_{LOAD} \times \Delta V_{OUT}}{I_{SR}}} \tag{15}$$

where I_{SR} in this case can be defined as:

$$I_{SR} = \frac{\Delta I_{LOAD,MAX}}{t_1 - t_0} = \frac{I_{MAX} - I_{MIN}}{t_1 - t_0} \tag{16}$$

TABLE 2. Comparison of the past five years DLDOs' performance.

Ref.	CMOS [nm]	V_{IN} [V]	V_{REG} [V]	Max I_{load} [mA]	I_Q [µA]	Total C_{load} [nF]	I_{SR} [mA/ns]	ΔV_{OUT} [mV] @ $\Delta I_{load,max}$ [mA], V_{OUT} [V]	Peak I Eff. [%]	FoM_1 ** [ps]	Cal. FoM *** [ps]	FoM ****
[44]	110	0.6-1.2	0.5-0.9	80	32	1	80 / 25000*	53 @ 80, 0.5	N.A.	0.26	72.8011	0.03
[35]	180	1-1.2	0.95	100	34.68	0.5	40 / 1	36 @ 40, 0.95	99.64	0.65	0.8225	0.05
[68]	65	0.7-1.2	0.6-1.1	25	6	1	23.5 / 2080*	200 @ 23.5, 0.6	99.97	2.17	48.0409	0.47
[74]	130	0.84-1.24	0.6-1	50	400	0.5	40 / 10	250 @ 40, 0.6	99.2	20	79.0569	2.15
[85]	65	0.6-1.2	0.4-1.1	100	1070	0.04	50 / 1240*	108 @ 50, 0.8	99.5	1.38	313.2539	0.30
[77]	130	0.5-1.22	0.35-1.17	145	N.A.	1.5	40 / 0.1	280 @ 40, 0.92*	97.8	63.9	N.A.	6.88
[53]	130	0.5-1.2	0.45-1.14	4.6	N.A.	0.9	N.A.	90 @ 1.4, 0.45	98.3	N.A.	N.A.	N.A.
[92]	65	0.5-1	0.3-0.45	< 2	14	0.4	1.06 / 1	40 @ 1.06, 0.45	99.8	199	72.5678	43µ
[78]	65	0.5-1	0.45-0.95	25	127	0.1	20 / 400	47 @ 20, 0.45	N.A.	0.29	87.0668	0.06
[86]	65	0.9-1.2	0.5-1.1	19	131	0.2	3 / 90	80 @ 3, 1	99.3	342	1352.9622	73.66
[52]	130	0.45-1.2	0.35-1.15	1.5	8.9	1	1.48 / 50*	100 @ 1.48, 0.45	99.9	N.A.	494.3078	N.A.
[49]	55	0.5	0.45	1	2.3	0.0001	0.79* / 40	40 @ 0.79*, 0.45	99.99	0.17	1.8529	0.04
[106]	65	0.6-1.0	0.55-0.95	4.5	10.2	1	4.4 / 10	118 @ 4.4, 0.55	99.7	62.2	53.6880	13.39
[98]	40	0.6-1.1	0.5-1	20	19.6	4.7	19 / 400	40 @ 19, 0.5	99.8	9.21	91.7803	3.22
[101]	28	0.5-1	0.45-0.95	10	3.7	0.1	9.5* / 1*	52* @ 9.5*, 0.95	99.97	N.A.	0.4075	N.A.
[104]	65	0.6-1.2	0.5 - 1.0	100	75	1	90 / 20	47 @ 90, 1	99.93	0.43	3.8087	0.09
[75]	130	0.83-1	0.6 - 0.8	25	N.A.	0.8	25 / 0.1	160 @ 25. 0.8	99.4	N.A.	N.A.	N.A.
[115]	65	0.5-1	0.45-0.95	105	4.9	0.042	100 / 10	88 @ 100, 0.5	99.995	0.0007-0.0038	0.0421	150µ - 818µ
[121]	55	0.8-1.5	0.76-1.46	5	3.18	0.022	4.5 / 1	85 @ 4.5, 1.456	99.996	N.A.	0.6442	N.A.
[51]	14	0.5-0.85	0.45-0.8	11	0.69	0.1	10 / 4	122 @ 10, 0.45*	N.A.	0.075	0.2156	0.075
[55]	28	0.5-1	0.45-0.95	33.2	10.5	0.1	30.7 / 20	101.7 @ 30.7, 0.45	99.97	0.11	1.2450	0.055
[50]	90	0.35	0.3	2.4	5	N.A.	N.A.	N.A.	99.8	N.A.	N.A.	N.A.
[122]	65	0.6-1.2	0.55-1.15	25	21.35	0.00084[1]	24.5 / 20	96 @ 24.5, 1.15	99.91	0.0029	0.3164	225µ
[107]	40	0.7	0.65	< 16	19.4	0.0505	15.5 / 2	93 @ 15.5, 0.65	99.87	0.379	1.3779	0.13
[22]	55	0.55-0.8	0.5-0.75	< 0.1	0.36	0.075	N.A.	14* @ 0.003*, 0.5	N.A.	N.A.	N.A.	N.A.
[123]	65	0.5-1.2	0.15-1.15	270	12.7	0.0074	20 / 1	75 @ 20, 0.45	99.99	0.0009	0.1496	193µ

[1] Estimated power switch array parasitic capacitance is used in this case.
* Estimated value from the graph.
** Provided by the reference publication.
*** Calculated based on the information on bolded columns with equation:

$$\text{Cal. FoM} = \sqrt{\frac{2C_{LOAD} \times \Delta V_{OUT}}{I_{SR}}} \times \frac{I_Q}{\Delta I_{LOAD,MAX}}$$

**** Normalized process FoM, the smaller the FoM the better.

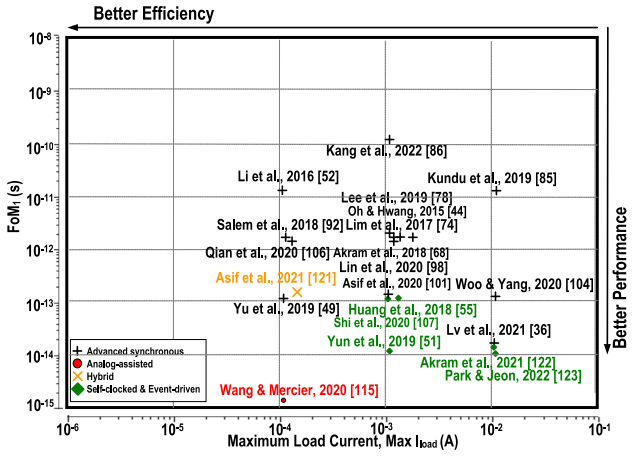

FIGURE 27. Calculated FoM versus load current.

Therefore, the modified FoM_3 can be written as:

$$\text{FoM}_4 = \sqrt{\frac{2C_{LOAD} \times \Delta V_{OUT}}{I_{SR}}} \times \frac{I_Q}{\Delta I_{LOAD,M\ AX}} \tag{17}$$

Hence, to further ensure the FoMs are fairly and properly compared, the calculated FoM based on equation (17) is included in Table 2 while Figure 27 shows the relationship of the maximum supporting I_{load} across the calculated FoM. It can be concluded that the proposed design in [123] offers the best performance without the external C_{load} but with the price of current efficiency. The analog-assisted DLDO in [115] has successfully maintained good performance with very low quiescent current.

Due to the difference in process, the normalized FoM is calculated with the technology scale for fairness [51]. The normalized FoM equation is derived as below:

$$\text{FoM} = \text{FoM}_1/K \tag{18}$$

where K is the CMOS technology process scaling factor [51], denoted as:

$$K = \frac{\text{process}}{\text{smallest process used in comparison}} \tag{19}$$

The smallest process used in Table 1 is 14 nm.

VI. CONCLUSION

This article reported the hierarchical theory in power regulators, focusing on the design trend and perspectives of DLDOs in different CMOS processes for sub-1V applications which provide deep novel insight from the transistor level to readers as compared to the recently published review [126]. Various S-DLDOs with different architectural advancements, such as coarse-fine dual-loop controllers [104], [105], [106], adaptive sampling [49], [52], [53], [60], [76], [78], [85], or phase integration (PI) [35], [74], [77] controllers, and conditional clock-boosting controllers [44], [98], [105], have been discussed in previous Sections. However, most of these architectures require a transient enhancement unit to boost the output transient performance. Various design techniques have been introduced to improve the trade-off between transient response and power consumption. Asynchronous circuits have been suggested in several studies to enhance transient response without increasing power consumption. Yet, the delay of these circuits is sensitive to process, voltage, and temperature variations, which can affect design robustness. Other studies have proposed event-driven DLDOs with a proportional-integral controller, analog-assisted loops, hybrid synchronous-asynchronous architectures, self-clocked techniques, and hybrid LDOs to improve transient response and regulation precision. The effectiveness of these techniques varies depending on factors, such as turned-on MOS devices, settling time, and power supply ripple rejection. Hence, the trend towards AS-DLDOs, either with the event-driven or self-clocked system in the loop regulation, is optimistic, especially the downscaling in the voltage supply and the trending for OCL-LDOs that are lower in cost with smaller active area.

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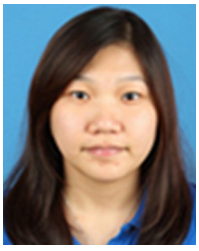

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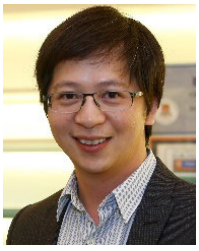

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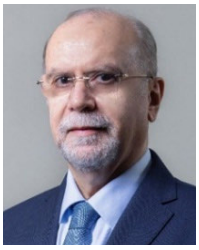

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He has been with DECE/IST, University of Lisbon, since October 1980, where he has been on leave, since October 1992, and DECE, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor, since August 2013. In FST, he was the Dean (1994–1997), and has been the UM's Vice-Rector, since September 1997. From September 2008 to August 2018, he was the Vice-Rector (Research) and from September 2018 to August 2023, he was the Vice-Rector (Global Affairs). Within the scope of his teaching and research activities he has taught 21 bachelor's and master's courses and, in UM, has supervised (or co-supervised) 47 theses, Ph.D. (26), and master's (21). He has authored or coauthored: nine books and 12 book chapters; 49 patents, USA (39), Taiwan (three), and China (seven); 675 papers, in scientific journals (289), and in conference proceedings (386); and other 70 academic works, in a total of 815 publications. In 2003, he was with the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated, in January 2011, to the State Key Laboratory (SKLAB) of China (the first in Engineering in Macao), being its Founding Director. He was the Founding Chair of UMTEC (UM Company), from January 2009 to March 2019, supporting the incubation and creation of Digifluidic, in 2018, the first UM Spin-Off, whose CEO is a SKLAB Ph.D. graduate. He was also the Co-Founder of Chipidea Microelectronics, Macau (later Synopsys-Macao and now Akrostar, where the CEO is one of his Ph.D. graduates), in 2001 and 2002.

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