APPLIED RESEARCH

A Study of the Latest Updates of the DAQ Firmware for the DSSC Camera at the European XFEL

ANDREA COSTA [1], (Member, IEEE), **NICOLA LUSARDI** [1], (Member, IEEE),
FABIO GARZETTI [1], (Member, IEEE), **ENRICO RONCONI** [1], (Member, IEEE),
STEFANO MAFFESSANTI [2], **CYRIL DANILEVSKI** [3], **DAVID LOMIDZE** [3],
MONICA TURCATO [3], (Member, IEEE), **MATTEO PORRO** [3,4], (Member, IEEE),
AND ANGELO GERACI [1], (Senior Member, IEEE)

[1] Politecnico di Milano, 20133 Milan, Italy
[2] Deutsches Elektronen-Synchrotron DESY, 22607 Hamburg, Germany
[3] European XFEL, 22869 Schenefeld, Germany
[4] Department of Molecular Sciences and Nanosystems, Ca' Foscari University of Venice, 30172 Venezia, Italy

Corresponding author: Andrea Costa (andrea1.costa@polimi.it)

ABSTRACT The European X-ray Free Electron Laser (EuXFEL) is a light source of the 4th generation which provides spatially coherent ultrashort X-ray pulses at high rate. The facility enabled unprecedented advancement in fundamental research, but also needed new detectors to fit the EuXFEL requirements, such as single photon resolution, large dynamic range, and high repetition rate: three 2D megapixel detectors have been developed to cope with the demanding environment. The DEPleted Field Effect Transistors (DEPFET) Sensor with Signal Compression (DSSC) detector is one of them. The parallel readout from each pixel is performed employing a dedicated Application Specific Integrated Circuit (ASIC). The generated data flow is read through a 2-stage Field Programmable Gate Array (FPGA)-based Data AcQuisition (DAQ) chain: the Input Output Board (IOB) controls the primary readout from 16 ASICs and serializes data on high-speed links that are sent to the Patch Panel Transceiver (PPT). It is also responsible for the clock distribution and timing control of the front-end and switched power channels. The PPT reorders and forwards the received data toward the EuXFEL back-end, and allows remote control over the whole DAQ. A first DSSC camera, based on miniaturized silicon drift detectors (mini-SDD) has been available for users' experiments since 2019, and a second DEPFET-based camera is under construction. The IOB firmware has been thoroughly reviewed and modified to cope with the new DEPFET sensors' physics and to improve the performance of both the mini-SDD and DEPFET versions. We present an overview of the DSSC, focusing on the DAQ, highlighting the main properties of the environment where the detector operates. We assess the firmware improvements introduced, with a particular focus on the IOB, and present the results obtained in comparison to the original firmware.

INDEX TERMS Field-programmable gate array (FPGA), XFEL, free electron laser, DSSC, DEPFET, MiniSDD, DAQ, throughput.

I. INTRODUCTION

The European X-ray Free Electron Laser (EuXFEL) is a state-of-the-art facility located in Schenefeld, Germany [1], [2],

The associate editor coordinating the review of this manuscript and approving it for publication was Ludovico Minati .

designed to produce ultra-short, high-intensity X-ray laser pulses with unprecedented brilliance and coherence. The EuXFEL is a 3.4 km-long facility that uses a superconducting linear accelerator (LINAC) to generate high-energy electron beams that are then converted into X-ray pulses through a process called self-amplified spontaneous emission (SASE).
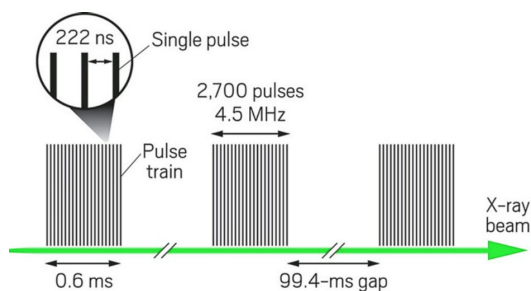
FIGURE 1. X-ray pulses bunch structure at the European XFEL.

FIGURE 2. X-ray hologram of a [Co(6)/Pt(8)]x10 multilayer sample at the Co L3 edge recorded in transmission with the DSSC detector. The object hole is 2.5um with multiple reference holes. The data consists of 2.4M X-ray pulses accumulated over 20min.

One of the most remarkable features of the EuXFEL is its capability of producing femtosecond pulses with peak powers in the gigawatt range. The X-ray pulses can be tuned to cover a wide range of wavelengths from 0.05 to 5 nm, enabling scientists to probe the inner structure of materials and molecules at a level of detail that was previously unattainable. The EuXFEL machine generates coherent X-ray pulses satisfying extremely challenging timing, as shown in Figure 1. The so-called "train" is a structure composed of up to 2700 bunches, which are separated from one another by a $222 ns$ time interval (a frequency of 4.5 MHz). The duration of a train is, consequently, around 0.6 ms. The train is repeated every $100 ms$: considering the train duration, what is left is an inter-train gap of around 99.4 ms. The single pulse generated by the Free Electron Laser (FEL) process is an ultra-short flash lasting less than $100 fs$.

DEPleted Field Effect Transistor (DEPFET) Sensor with Signal Compression (DSSC) [3] is a planar megapixel detector designed for the European XFEL. A first 1-megapixel camera, based on passive mini-Silicon Drift Detector sensors (Mini-SDD), is in operation since 2019 on two of the instruments of SASE 3 beamline: the spectroscopy and coherent scattering (SCS) [4] and the small quantum systems (SQS) [5] soft X-ray instruments of the facility. It is designed specifically for low energy regimes and wavelengths belonging to the long X-ray spectra (0.5-6 keV), thus greatly enhancing the capabilities of both SCS and SQS. The DSSC camera is able to cope with the machine bunch structure and is able, thanks to an in-pixel digitization and memory that can store digitally up to 800 single-pulse images per train among 2700 generated, at the peak 4.5 MHz frame rate generated by the Free-Electron Laser, which is the most among the megapixel detectors at the EuXFEL: in fact, Large Pixel Detector (LPD) [6] can store up to 512 frames per bunch, while Adaptive Gain Integrating Pixel Detector (AGIPD) [7] stops at 352. It is, however, objective of the consortium to push the memory capabilities of the ASIC towards the full bunch dimensions.

In order to show what kind of output images DSSC is able to deliver, we show the result from an acquisition taken fom SCS in Figure 2.

As the experiments at EuXFEL, upon synchronizing with the challenging electron bunch timing of the facility, produce a huge amount of data, with rates up to hundreds of Gb/s 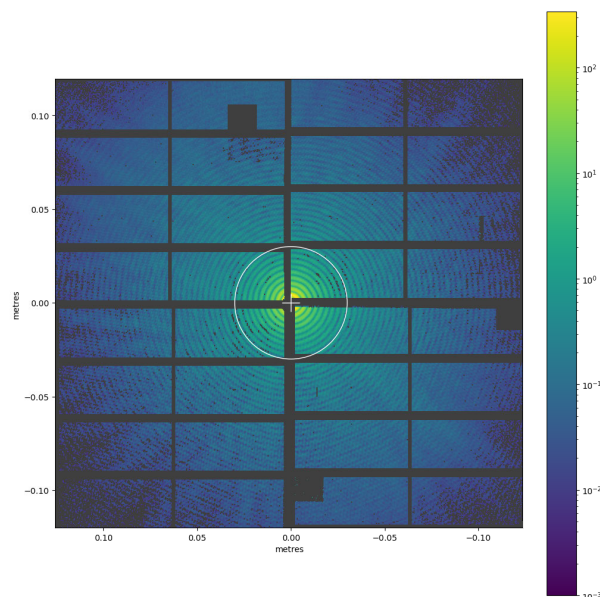to be handled, the development of the Data AcQuisition (DAQ) electronics had been driven by the need to combine different requirements, such as:

- large bandwidth, for handling the data generated from the detector
- standardized networking and protocols for communication and remote control mechanisms
- online data processing, to mitigate the requirements for storage, data transfer, and post-processing
- scalability, to foresee future larger detector compounds and allow integration of current modules
- flexibility, to possibly upgrade to new technologies, when available and if needed

Many different implementation options had to be considered for the realization of a DAQ that would fulfill these requirements [8]: starting from standard PC technology, which was immediately cast aside for the long latencies that would not cope with EuXFEL requirements, the addition to standard PC of peripheral board extensions was evaluated: 10 Gigabit Ethernet cards, for example, have been available for long [9], and offloading data processing to graphics processing units (GPUs) is a standard procedure nowadays [10]. This second solution would, however, have been too expensive in terms of build, power, maintenance, and poorly reliable for a first stage DAQ that would sit beside the detector. It was, instead, used to build the back-end PC layer that deals with the output of the detector DAQ.

The focus was, thus, redirected to the world of custom Printed Circuit Boards (PCBs), that are generally developed either around Application Specific Integrated Circuits (ASICs) or Field Programmable Gate Arrays (FPGAs). The choice was straightforward, as FPGAs offer unparalleled advantages in terms of flexibility and time-to-market with respect to ASICs, which are extremely valuable assets for
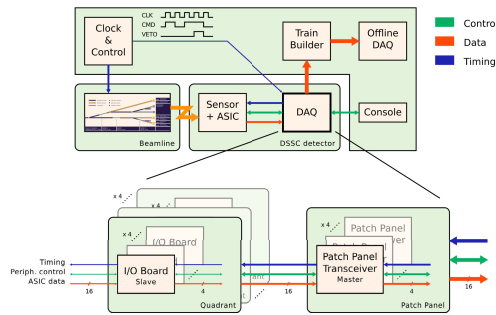
FIGURE 3. Scheme of DAQ (DSSC taken as example) placed inside the EuXFEL systems.

development, maintenance and allow future modifications of algorithms and processing structures, or even the addition of new functionalities.

For these reasons and the highly custom needs coming from a detector like DSSC, FPGAs were the best choice for implementing the core of the processing for the front-end DAQ, which we will refer to as just DAQ (as the back-end DAQ is not object of this paper). As a matter of fact, also the other two Megapixel detectors at EuXFEL, which are LPD and AGIPD, use DAQs based on FPGA stages [11], [12].

In this paper we present the corrections, improvements, and updates over the Input Output Board (IOB) and Patch Panel Transceiver (PPT) firmwares, and it is organized as follows: in Section II is presented a detailed overview of the EuXFEL environment and the DSSC DAQ that is currently in use at EuXFEL; Sections III and IV cover the IOB and PPT respectively, with a focus on internal firmware structure, the solutions to the issues and the improvements provided via firmware updates. In particular, in Paragraphs III-A and III-B the problems introduced by the skews between signals are addressed and solved. The same skew problem was also affecting the ASICs readout channels, and is treated in Paragraph III-C. Improvements over the clear process of the DEPFETs are discussed and applied in Paragraph III-D. Finally, due to the utilization of deprecated versions of the Linux kernel running on the PPT, causing really slow boot up phases, and compilers for the PPT FPGA, the update of these components is covered in Paragraph IV.

II. SYSTEM OVERVIEW

DSSC operates at the measuring stations of the instruments placed at the end of the EuXFEL beamlines, in particular on the aforementioned SCS and SQS instruments of SASE 3 beamline. The conceptual scheme of the interconnection of the generic DAQ (i.e., DSSC, LPD, and AGIPD) placed inside the EuXFEL environment is shown in Figure 3, with a focus on the DAQ itself, composed of two FPGA stages.

The system deals with many different kinds of information: referring again to Figure 3, in green are shown the signals related to the control domain: they originate from a console (i.e. a PC workstation), where the user is able to interface remotely to the detector via either a standalone software or Karabo distributed control system [13], that
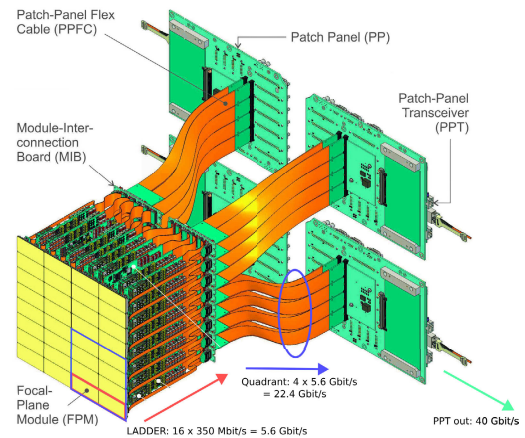

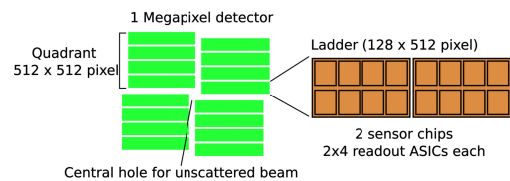**FIGURE 4.** Full 1Mpixel DSSC camera and front-end DAQ.

FIGURE 5. Sub-division of the focal plane into Quadrants and Ladders.

uses the DSSC library to communicate with the PPT. The DSSC consortium also developed an expert-mode standalone software, based on the same C++ libraries, that is used to fully exploit the detector configuration capabilities and can be used independently of the EuXFEL infrastructure. This gives the possibility to act on detector registers, tune parameters, power up the ASICs, trigger acquisitions and so on by communicating to the PPT which, in turn, acts as a master for the IOB. The PPT is provided a slow control server for this purpose, running on an embedded Linux system [14] that executes over an implementation of a soft-core processor called MicroBlaze [15], directly on the PPT's FPGA resources. Highlighted in blue are, instead, the timing signals, that are directly fed to the DAQ via the PPT, which then forwards them to both the IOB and the ASICs. The red signals represent, finally, the datapath: they are generated by the detector's pixels, integrated and temporarily stored on the ASICs, then sent over to the two front-end DAQ stages before getting offloaded to the backend DAQ (Train Builder and Offline DAQ in Figure 3).

As represented in Figure 4 and 5 the 1-megapixel detector is subdivided into four sub-units called Quadrants. The Quadrant is a fully functional, stand-alone unit that makes up for one-fourth of the full 1-megapixel. It is equipped with a complete front-end Data Acquisition system (DAQ) [16], which is composed of 4 + 1 Field Programmable Gate Array (FPGA)-based electronic boards: four IOBs and one PPT [17]. Referring to the Quadrant, each of the four IOBs handles the readout and control over one Ladder unit (Figure 4 and 6), a sub-matrix of $128 \cdot 512 = 65,536$ hexagonally-shaped pixels, which is the smallest independently operable unit of the system. [18].
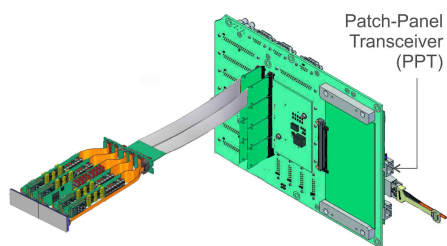
FIGURE 6. Representation of one Ladder and the related electronics.

On the readout ASIC, every pixel's accumulated signal is first shaped by a trapezoidal filter [18], then digitized by a 9-bit Analog to Digital Converter (ADC), which works in 8-bit mode when running at the maximum rate. In this scenario, considering the full-rate acquisition at 4.5 MHz, each Ladder would produce a peak rate of 2.36 Tb/s (i.e.; $65.536\,pixel \cdot 8\,b/pixel \cdot 4.5\,MHz = 2.36$ Tb/s); so, a Quadrant would generate a peak rate of 9.44 Tb/s (i.e., $262.144\,kpixel \cdot 8\,b/pixel \cdot 4.5\,MHz = 9.44$ Tb/s), and the full 1 Mpixel camera generates a global peak data rate around 38 Tb/s (i.e., $1\,Mpixel \cdot 8\,b/pixel \cdot 4.5\,MHz = 37.8$ Tb/s) during the bunch crossing.

The bunch structure of the EuXFEL machine, as described previously, has a duty cycle of 0.6%. Consequently, the Ladders, Quadrants and full 1Mpixel camera generate a real maximum rate of 14 Gb/s, 56.6 Gb/s, and 226.5 Gb/s respectively.

Due to space constraints on the ASIC, however, only 800 out the 2700 acquired images can be stored for each train. Therefore, the Ladders, the Quadrants and the full 1 Mpixel camera rates have to be further corrected for a 800/2700 factor, generating a real maximum rate of 4.15 Gb/s, 16.6 Gb/s, and 66.4 Gb/s respectively of pure data. The actual bandwidth increases along the DAQ chain, when considering headers and data manipulations (i.e., paddings and encapsulation layers), reaching a total output rate of 135.2 Gbit/s.

The detector, ASICs, IOBs, and auxiliary front-end electronics used to power-up IOBs, ASIC and detectors (Regulator Boards, Main Board, Module Interconnection Board) are placed in vacuum to preserve the beam quality, by avoiding as much as possible photons being scattered by gas particles, and operated at -20 Â°C for best noise performance. Flex cables bridge properly the in-vacuum electronics to the rest of the DAQ composed by the PPT and some auxiliary back-end electronics (i.e., the Patch Panel and the System Interlock Board), placed outside the DSSC vessel.

A first DSSC camera has been available for users' experiments since 2019; some minor issues arose during operations, affecting the camera performance and worsening the users' experience (i.e., the simplicity to put the camera into operation).

In the following paragraphs the main elements of the EuXFEL system and detector front-end DAQ are briefly described, to give a general idea of the system and its complexities for a better understanding of the following chapters.

A. BEAMLINES

The EuXFEL produces X-ray laser light from accelerated electrons by means of permanent magnet structures called undulators, which ''bend'' the electrons' trajectory making them emit X-ray light. There are 3 undulators along the beamlines [19], with different magnetic field strengths based on the X-ray wavelength to obtain, and DSSC is operated, as already mentioned, downstream SASE 3, one of the EuXFEL beamlines, covering the lower X-ray energy range, at the following instruments.

1) SCS

The Spectroscopy and Coherent Scattering instrument [20] allows time-resolved experiments for studying structure of molecules and complex materials in space and time [21].

2) SQS

The Small Quantum Systems [22], on the other hand, targets the investigation of fundamental processes generated by light-matter interaction such as atoms, molecules, ions or large biomolecules, provided generally in gaseous form.

B. CLOCK AND CONTROL

The EuXFEL machine generates coherent X-ray pulses satisfying extremely challenging timing, as shown in Figure 1.

A Micro Telecommunications Computing Architecture (MTCA) crate takes the 4.5 MHz bunch clock and trigger data from the EuXFEL timing receiver, using them to implement the Clock and Control (C&C) master and fanout slave functionalities [23]: it generates the $\sim 99\,MHz$ front-end electronics (FEE) clock, and the veto telegrams and fast commands that are needed to synchronize the detector with the global EuXFEL timing via an RJ45 connector on four total lines. The fast commands can either be signaling the start of a train 15 ms before the first X-ray pulse, to correctly initiate the detector electronics, the train end or a reset. As the detector produces pixel data for every incoming bunch, in principle a train would generate up to 1 Mpixel 2700 images, which is more than the technology allowed to store in the ASIC SRAM memory (800 for DSSC). For this reason, detectors are provided a low latency method to remove undesired data to free space for possibly storing better samples. This mechanism is called Veto. The ''Veto'' command identifies a bunch as not successful, providing the bunch ID to discard. A bunch identified as ''Golden'', on the other hand, is marked as protected, since it was most likely the source of a very good measurement. Lastly, ''NoVeto'' refers to bunches that are neither Veto nor Golden, and is the default for every bunch.

C. DSSC DAQ

Before focusing on the individual components of the DAQ a more detailed description of the signals involved in DSSC must be given. The DAQ functionalities can be classified in three different areas:
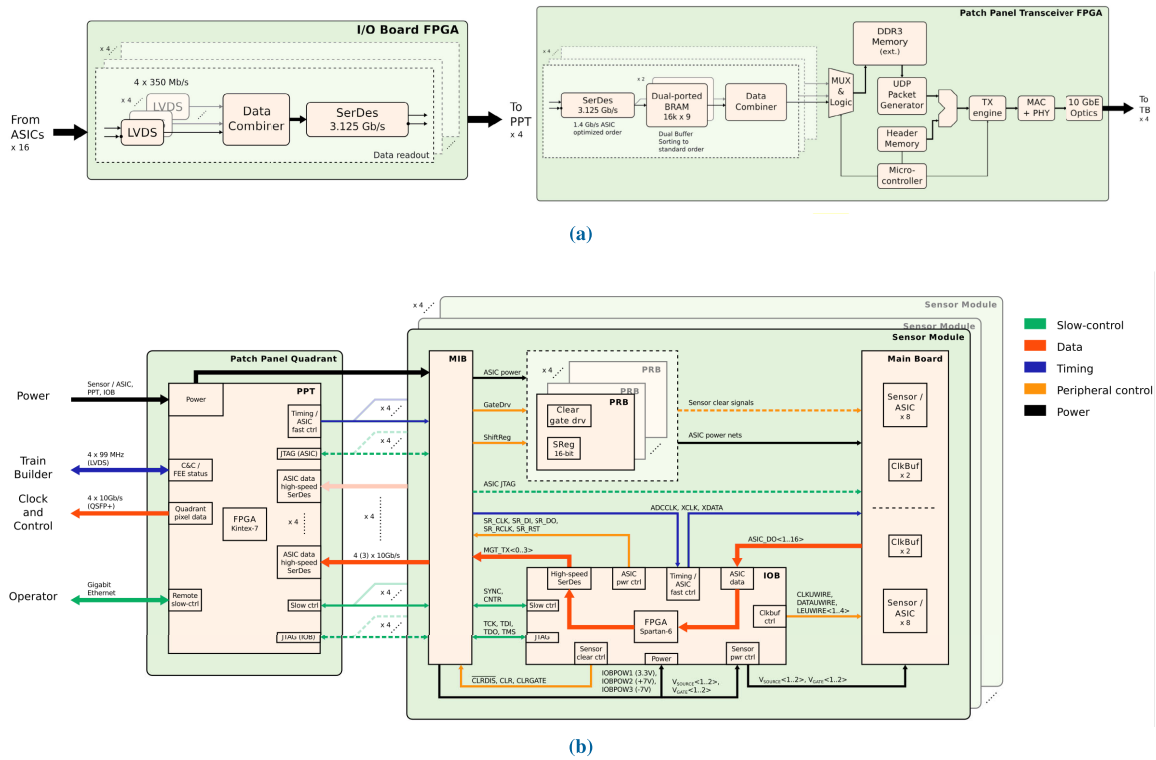
FIGURE 7. Detailed representation of FPGA stages of the DAQ and implemented functions.

1) **Data Path:**
every ASIC generates the data from $64 \cdot 64$ pixels, which is transferred to the IOB via 16 Low Voltage Differential Signaling (LVDS) lines at 350 MHz during the intra-train gap. This data stream is conveyed into 3 separate Aurora lines using Gigabit Transceivers, and sent over to the PPT. The PPT provides each of the four connected IOBs with a channel to transfer data toward four 10 Gigabit Ethernet (10GE) outputs, one for each Ladder of the DSSC camera. The four 10GE outputs are conveyed to a QSFP+ module before being sent out to the back-end DAQ packed into UDP Ethernet jumbo frames up to 9000 bytes in size [24]. The nominal throughput for a Quadrant is, thus, 40 Gbit/s (160 GBit/s for the full camera), larger than the input data rate which uses fewer bits per pixel.

2) **Timing:**
the PPT directly receives clock and control commands from the EuXFEL facility, generating upon them control telegrams that are detector-specific to control DSSC operation, as mentioned in Subsection II-B, generating upon them the signaling/timing for the operation of DSSC.

3) **Control:**
the control function of the PPT covers the download of configuration files to the IOBs FPGA and ASICs, and the modification of their functional parameters at run-time, startup, and shutdown sequences. The interfaces to these functions are offered by a variety of registers exposed by means of a soft-core processor

(MicroBlaze) implemented with the PPT's FPGA resources.

A more detailed representation of the DSSC FPGA stages of the DAQ is shown in Figure 7: in the top image is represented the actual data flow that is implemented by the DAQ, firstly on the IOB then onto the PPT. The bottom image, instead, shows a more comprehensive view of the vast variety of signals handled by the DAQ, from data to control, peripheral, control and timing.

1) SENSOR AND READOUT ASICs

The readout ASICs for the DSSC detector are built as 4k-pixel chips with $64 \cdot 64$ channels bump-bonded to DEPFET or MiniSDD sensors, for a total of 32 sensors and 256 readout ASICs for the 1-megapixel camera [18]. The ASICs are designed for low-noise readout of the DEPFET current with a 4.5 MHz operation frequency, or the charge collected on the mini-SDD anode. In case of DEPFETs [25], the signal from the sensor is fed into a cascode stage to keep the DEPFET at a constant potential and reduce speed and gain effects, and the biasing current subtracted by means of a current digital to analog converter (DAC) and additional analog branch for the fine tuning calibrated at the beginning of each train. In case of a mini-SDD sensor the collected charge is readout by a charge-sensitive preamplifier (CSA). A successive filter stage implements a trapezoidal filter function. A sample and hold capacitor store the filter's output voltage and a Wilkinson type ADC converts the voltage to a 8-bit + carry bit digital value that is stored in a 800-word static random access
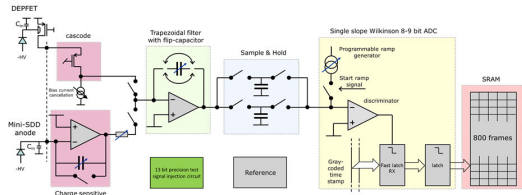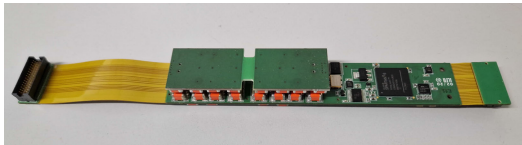
FIGURE 8. ASIC with MSDD or DEPFET topologies.
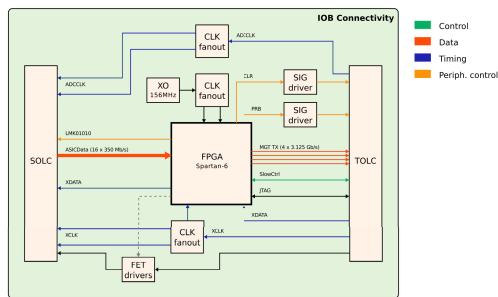

FIGURE 9. IOB rev1.1 PCB.

FIGURE 10. IOB FPGA stage scheme and its connection paths: data in red, timing in blue, controls in green and orange; orange is used to differentiate the controls of the input/output peripherals.

memory (SRAM) located in the pixel. An 8-bit Gray code counter located at the base of each ASIC column provides the timestamp for the ADC. The ASIC also has several auxiliary blocks such as control registers, monitoring lines, and injection circuits for calibration. A global logic controls the data taking sequence and the serial readout of the SRAM cells. A simplified pixel schematic is shown in Figure 8.

2) INPUT OUTPUT BOARD

The IOB, a real image of which can be seen in Figure 9, is the first FPGA stage; it sits close to the ASICs, it is placed in vacuum, and contains relatively uncomplicated logic. Its connectivity is represented in Figure 10 highlighting with different colors (i.e., red, blue, and green/orange) the different paths (i.e, data, timing, and controls).

A 60-pin terminal strip TOLC connector with a flex cable connects the IOB towards the PPT via the back-end electronics, while another 60-pin Socket strip SOLC connects the IOB towards the ASICs via the front-end electronics.

The IOB performs a low-level, close control over the front-end electronics (blue lines in Figure 10) and receives the rather slow (350 MHz) 16 LVDS pairs coming from the ASICs (ASICData red lines in Figure 10 with rate of 5.6 Gb/s), reorganizing and concentrating them into 3 fast Gbps lanes (3.125 Gb/s per line) that means a total of 9.375 Gb/s towards the following stage (a fourth fast Gbps lane is available and unused). The control functions are
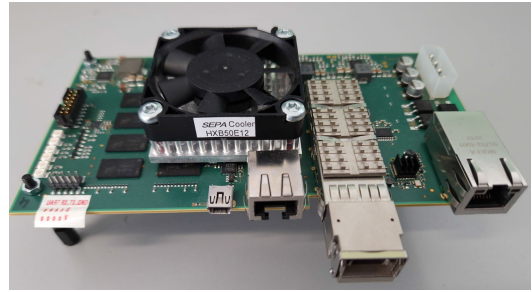

FIGURE 11. PPT rev2.1 PCB.

derived from the PPT, which performs the so-called "Slow Control" over the TOLC connector (green line in Figure 10) to read and write control registers on the IOB, that, in turn, used them to control its peripherals, such as the clear and clear gate signal drivers, the clock buffers, the power stages (orange lines in Figure 10), and send command telegrams to the ASICs via the SOLC and TOLC connectors.

Being the IOB near the focal-plane module, spatial constraints have been stringent, determining the final dimensions of the PCB and, subsequently, the maximum dimension of the FPGA that could be carried on the board. The trade-off, when choosing between different FPGA devices, is mainly driven by the quantity/cost/dimension of the components and the type of resources available. For the IOB case, in particular, one mandatory requirement was the presence resources like gigabit transceivers, which are essential for enabling high throughput communication. By the time the IOB was engineered, these constraints led to the selection of a Xilinx Spartan-6 LXT FPGA, which specifically features GTP transceivers [26]. It is, now, a rather old device, which firmware can be compiled only using a no longer supported software from Xilinx: ISE Design Suite, lastly released in 2013.

3) PATCH PANEL TRANSCEIVER

The second FPGA stage, which makes up the upper front-end DAQ layer, is called Patch Panel Transceiver (PPT), and it is a Xilinx Kintex-7 FPGA-based PCB, visible in Figure 11. PPT handles one full quadrant of DSSC, and it is placed outside the detector vessel, at ambient temperature and pressure. It is a much larger device with respect to the one hosted on the IOB, as the tasks it must deliver are more, and more complex. Its main functions are to act as a master to IOBs and to provide a user interface for the slow control, data, and timing, and forward the data to the EuXFEL back-end DAQ (Train Builder and Server PC layers). The FPGA of the PPT is used, among other things, to implement a soft-core processor, the MicroBlaze, with Linux capabilities. In fact, a Linux system equipped with both standard features as well as custom software to offer remote control over the DAQ, is run on the soft-core processor. The kernel version used until this work was an old 4.14 from 2017, and the PPT firmware was compiled with a 2019.2 version of Xilinx Vivado Design Suite, with some Xilinx IP Cores that have been updated by the manufacturer thereafter.
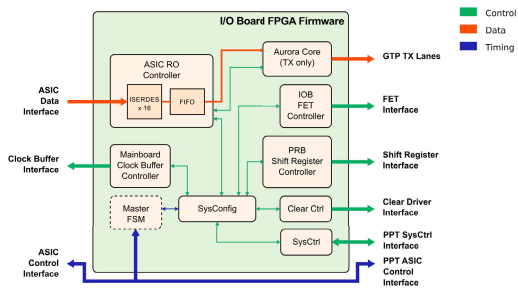
(a) Original firmware.
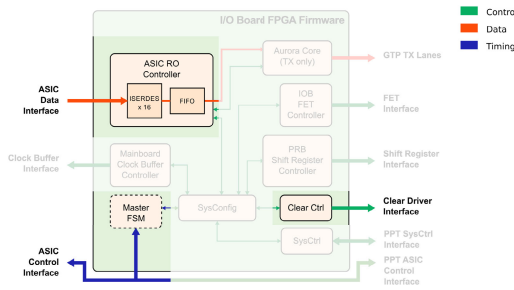
(b) Highlight of the updated sub-modules.

FIGURE 12. Schematization of the HDL sub-modules making up the IOB firmware.

III. IOB FIRMWARE, BUGS, AND IMPROVEMENTS

The IOB's Spartan-6 FPGA is equipped with dedicated hardware, described partly with VHSIC Hardware Description Language (VHDL, with VHSIC standing for Very High Speed Integrated Circuits) and partly with Verilog. The firmware configuration file is kept on a flash memory hosted on the PPT, which oversees the download of the configuration onto the Spartan-6 via a JTAG interface. To understand how the IOB functions are implemented, a brief description of the I/O Board can be helpful.

A schematic representation of the IOB firmware can be visualized in Figure 12a.

For the sake of simplicity, the only parts to be thoroughly discussed will be the ones that showed issues, misbehavior, or needed new features, which are the ones highlighted in Figure 12b: the ASIC control interface, in terms of transmission of XDATA and of the reset signals, is treated in subsections III-A and III-B, where some issues occur during operations; the ASIC readout channels are covered by subsection III-C, showing misbehaviors of similar nature with the ones of XDATA and ASIC Reset signals, and finally the Clear driver interface is discussed in subsection III-D, where improvements over the current firmware version are discussed and implemented.

A. XCLK AND XDATA

As previously mentioned, the XCLK corresponds to the EuXFEL FEE clock and is buffered from the EuXFEL C&C signal. It is a clock signal that is synchronous to the electron bunches, which is needed by the IOB main Finite State Machine (FSM) to generate local timing, and it acts
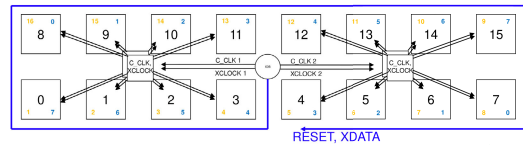

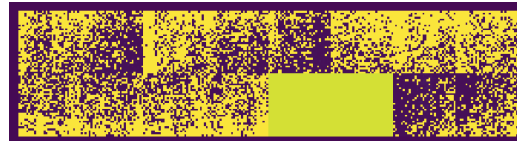**FIGURE 13.** XDATA and ASIC Reset distribution on MB.

FIGURE 14. Error caused by skew on XDATA reception by ASICs.

also as the reference for the control telegrams destined to the ASICs, whose FSM runs at XCLK frequency, too.

The XDATA signal is provided by the PPT to the IOB, which then forwards it to the ASICs, while the XCLK reference signal is instead directly delivered by the PPT to both IOB and ASICs. On the ASICs, the FSMs are triggered by the reception of telegram commands (i.e., XDATA), which, of course, need to be received synchronously to the XCLK signal.

In this context, setup and hold constraints for the reception of the XDATA control telegrams are mandatory to be respected for the correct data transmission, causing otherwise incorrect telegram reception from the ASICs. The XDATA and XCLK signals, however, must exit the IOB FPGA, go across the PCB, the flex cable, the SOLC, and reach the front-end electronics, and the ASICs through clock buffers with a programmable delay up to $2250\,ps + 400\,ps$ in $150\,ps$ steps, not enough to cover a full clock period. Moreover, there is a non-negligible delay in the distribution of the XDATA on the boards: the signal is not delivered in parallel, but rather chained circularly throughout the 16 ASICs, accumulating a delay of around 3 ns between the first and the last ASIC of the board, as shown in Figure 13.

The received data showing the corruption would look like in Figure 14, where two ASICs show a uniform yellow color, since they did not send their data, as the reception of the XDATA telegram violated the setup and hold constraints. A total of $2 \cdot 64 \cdot 64$ pixels if, thus, affected.

During operation, the inconvenience showed up from the software graphical user interface (GUI), where the visualized data showed by some of the ASICs would not be coherent with the expected one. Some investigation lead to relate the issue to the non-synchronized FSMs, which was confirmed when looking at the mentioned distribution system of XDATA to the ASICs. The solution would require a firmware correction on the IOB that would make it possible to correct for the signal skew and correctly align the signals with the reference clock, similarly to how the E-Link interfaces used in the GBTX ASIC developed at CERN are realigned in phase [27]; the XDATA to ASICs signal is generated, in fact, on the IOB FPGA. Due to the line length and the different delays, it is necessary to implement a firmware delay control to move the phase and avoid setup or hold timing violations.
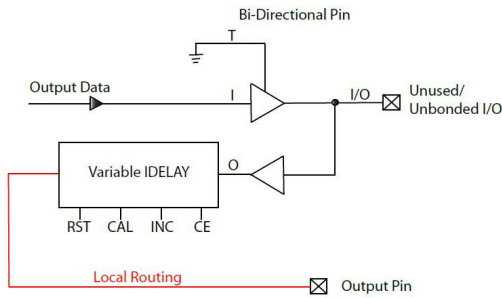
FIGURE 15. Workaround for using the variable delay for an output pin.

TABLE 1. IODELAY2 switching characteristics, delay of taps.

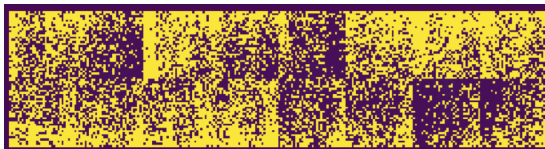| Symbol	Description	Delay [ps]
T_{TAP1}	Maximum Tap 1 Delay	8
T_{TAP2}	Maximum Tap 2 Delay	40
T_{TAP3}	Maximum Tap 3 Delay	95
T_{TAP4}	Maximum Tap 4 Delay	108
T_{TAP5}	Maximum Tap 5 Delay	171
T_{TAP6}	Maximum Tap 6 Delay	207
T_{TAP7}	Maximum Tap 7 Delay	212
T_{TAP8}	Maximum Tap 8 Delay	322

FIGURE 16. Correct data reception upon XDATA skew realignment.

By looking into the resources that are available on the Spartan-6 FPGA family, the one that would allow to generate a tunable delay and add it to an arbitrary signal was the IODELAY2, with the drawback of allowing to be used in "variable delay" mode only when applied to an input signal. A first try for solving this problem was already implemented, but was not working. In fact, a workaround [28], in the end was needed for the usage of the IODELAY2 resource as required for the described problem: as depicted in Figure 15, by "sacrificing" an unused I/O pin available on the IOB, and setting it as "tri-state", we could take advantage of the variable input delay, rerouting then the delayed net to an output pin towards the ASICs. This landed the possibility to add an 8-bit register to the ones of the IOB, and a small FSM that, upon reception of a new XDATA delay value, sets the Xilinx primitive to the correct delay.

A formula given by the manufacturer [29] allows determining the delay based on the digital number used on the 8-bit register setting the value, given the delay of each of 8 taps of the primitive, granting a total delay up to around 10ns, as reported in Table 1, which is more than sufficient to find a working point that works for every ASIC.

The correction worked as expected, allowing proper realignment between XCLK and XDATA signals, as seen in Figure 16, not missing telegram commands anymore; the modification is now part of the in-use firmware at DSSC.

B. XCLK AND ASIC Reset_n

The ASICs feature an external reset signal which is active low and serves to clear the clock dividers on chip, to synchronize with the external world (IOB/PPT). There are phase requirements that need to be met between the ASIC-internal 100MHz and the XCLOCK. This can be done by de-asserting the ASIC reset line, called ASIC_resetn, that allow the ASIC internal dividers to start counting after reset. The ASIC_resetn is chained along the ASICs with similar propagation delay to XDATA.

Given the proven effectiveness of the solution that solved the XDATA problem, and being the issue very similar, the implemented solution was similar to the one proposed for the XDATA signal: an IODELAY2 primitive used with a workaround to make its delay value variable at runtime. A partial modification was, however, needed to correctly set the desired delay value: the IODELAY2 primitive, in fact, needs data to be streamed across it upon setting a different delay value to reach it; differently form the XDATA signal, nevertheless, the ASIC reset signal is asserted only every once in a while. The modification to the XDATA solution, thus, consisted in isolating the IODELAY2 primitive after being given a new delay, and feeding its input with a fast-toggling signal, restoring then its input and output connections at the end of the process. The solution was once again successfully tested and kept for the final implementation on the IOB firmware.

C. ASIC READOUT CHANNELS

As mentioned, the readout channels from the ASICs are received by the IOB as 16 LVDS pairs (32 wires), directly on IOBs I/O banks. The clock signal to which the LVDS pairs are referred is called REFCLK_350, a 350 MHz signal fast enough to allow the readout of the ADC data of each of $64 \cdot 64$ pixels per ASIC, for all the 800 images temporarily stored in the ASIC SRAM. This signal is received by the IOB FPGA and used to generate other internal signals for data processing.

The skew problem given by the far origin of the signals and their reference is the same as the one that afflicted XCLK/XDATA signals, but on the receive direction, from an IOB standpoint. The solution, however, is practically the same, and it was already partially present in the IOB firmware implementation: in fact, 16 IODELAY2 primitives were used on each of the signals, but with only one delay value for the management of the variable delay. This allowed the tuning of the delay value, keeping it equal for each of the 16 inputs. It should be noted how, in this case, there is no waste of I/O pins, as the variable delay option is available for input signals.

This solution would work in the hypothesis that the 16 LVDS pairs are always perfectly matched, even with different productions of the same PCBs, which, unfortunately, was not verified. Moreover, the fast clock distribution or the ASIC internal delay could cause setup and hold timing violation, which is to be carefully avoided. In fact, a problem that was recurrently afflicting the acquisition setups would be that among the 16 ASICs, at least one would not "send" its data
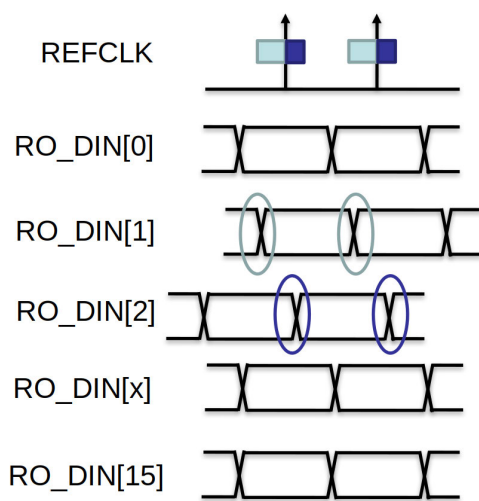
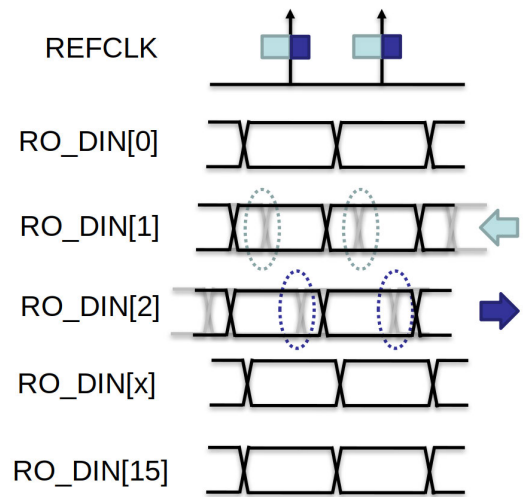**FIGURE 17.** Readout channels 1 and 2 violating setup and hold constraints.

FIGURE 18. ASIC readout channel with skew causing wrong data readings from ASIC 5.

FIGURE 19. Readout channels 1 and 2 respecting setup and hold constraints.

FIGURE 20. ASIC readout channel with skew compensated with proper delay setting.

FIGURE 21. DEPFET representation with clear and clear gate signals.

correctly, the reason being the violation of setup and hold constraints; other delay values that would fix the one not working would cause some other to break.

In the past, this problem was corrected manually by toggling the LMK fast clock output, so that the ASIC could realign itself. Since the reset of the ASIC is synchronized to the XCLOCK, the problem can still occur depending on the phase of the 350 MHz with respect to the 100 MHz. The problem can be visualized in Figure 17, with an outcome in the visualized ASIC data shown in Figure 18, with off ASICs flickering in an improper manner.

It was, thus, necessary to give the users the possibility to individually tune the delay values for every readout channel, by adding a register for every ASIC channel, to obtain the correct behavior shown in Figure 19.

The added registers were exposed to the PPT and the control software and have been successfully tested to verify the correct behavior of individual readout channels, allowing to reach a condition where data from all the 16 ASICs was correctly received on the IOB, enabling always correct operation, as can be seen in Figure 20.

D. CLEAR AND CLEAR GATE
Covering the operation principles of the DEPFET is not the aim of this work, but a quick note on some of its key signals and their driving is important for better understanding the importance of the firmware intervention described below.

The center of the DEPFET, also known as the internal gate, which can be seen in Figure 21, acts as a potential minimum for the electrons that are generated either thermally or due
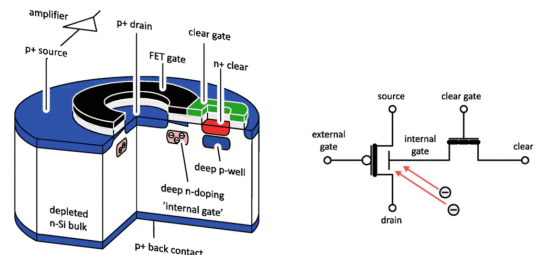
to absorption of ionizing radiation, modifying the transistor current at fixed source and external gate voltages until the charge is removed. The charge removal is a task taken care of by the clear transistor, by applying a positive voltage to both the clear and clear gate contacts. During the bunch crossing it is of great importance to be able to perfectly synchronize the clear phase and the charge integration time: 2700 electron bunches with 222 ns in between one another demand precise timing. Moreover, the clear and clear gate signals must be timed even among them: the clear gate signal has to rise "CLR_gate_on_ofs" clock cycles after the clear, in order to avoid charge injection instead of performing charge removal, and has to go low "CLR_off_ofs" clock cycles before the clear signal goes low: the longer the clear gate stays high, the better the charge removal is perfomed, with a limit set by the bunch crossing period. The values for the two delays are written to two different registers on the IOB. The flat top duration of the Clear signal is in the order of 60 ns. A waveform example of the clear and clear gate signals, with the mentioned offset delays between the rising and falling
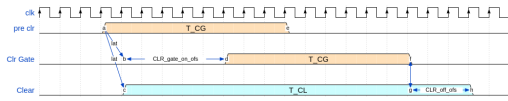
FIGURE 22. Representation in time of the functional signals for DEPFET charge removal.

edges can be seen in Figure 22 for best comprehension. The "pre clr" signal features the duration of the clear gate signal and is an internal signal that serves for triggering of the actual clear and clear gate signals.

The firmware module that drove these signals used to implement an FPGA resource called OSERDES2, an output deserializer that, upon receiving a trigger by an internal signal, would convert an input 2-bit word into an output "delay" to the edge of the clear or clear gate rising or falling edges, leading to a tunable delay over a range of 7.5 ns in steps of 2.5 ns, which corresponds to one-fourth of the 100 MHz clock period of that region.

Some observations by users were done, pointing out how during ordinary detector operation the delay would always be set at the maximum available, i.e. 7.5 ns, for both CLR_gate_on_ofs and CLR_off_ofs, to deliver the best performance in terms of final image quality: in fact, the maximum allowed delay is chosen as the one that best avoids the effect of charge injection into the internal gate, instead of the charge removal. The limitations in the implementation of the Clear and Clear Gate delays did not allow exploring what happens when trying to enlarge the reciprocal rising or falling edges, as the OSERDES2 primitive has limitations that were already reached. Moreover, it has to be considered that the clear phase duration is a tradeoff between the clear performance and the time available: if the detector is run at faster rates, there is less time available, and the charge injection is higher, being overall less efficient; at lower rates, however, the clear phase can take good advantage of the more relaxed timing and extend its duration for better performance.

As a first test, since the lower end of the available range was unused, a 10ns offset was added (by adding a pipeline stage) to the delay generated by the OSERDES2 primitive via the two registers, moving the range to 10-17.5 ns. The solution would work, but the flexibility was still limited by the only 2 bits available for individual delays.

The work made on the delay module lead to abandoning the OSERDES2 primitive due to its full-scale range limitations and to the adoption of a fast 4-bit counter logic, that by running at 400 MHz, close to the Spartan-6 FPGA fabric limit, would allow to extend the available range of delays from the previous 0-7.5 ns up to 0-37.5 ns, allowing to explore the clear phase extensively. The choice for the number of bits for the fast counter was forced by the primitive CARRY4 of the Spartan-6 family, which suggested that the fast carry logic could probably cope with the rated frequencies (up to 400 MHz), which did. A further couple of 4-bit registers have been introduced, one per each of the rising or falling edges of the clear and clear gate signals, for maximum flexibility in setting the desired delay.
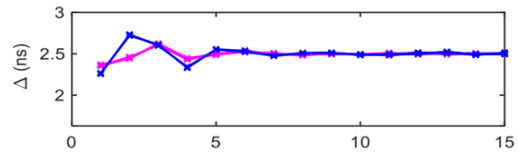

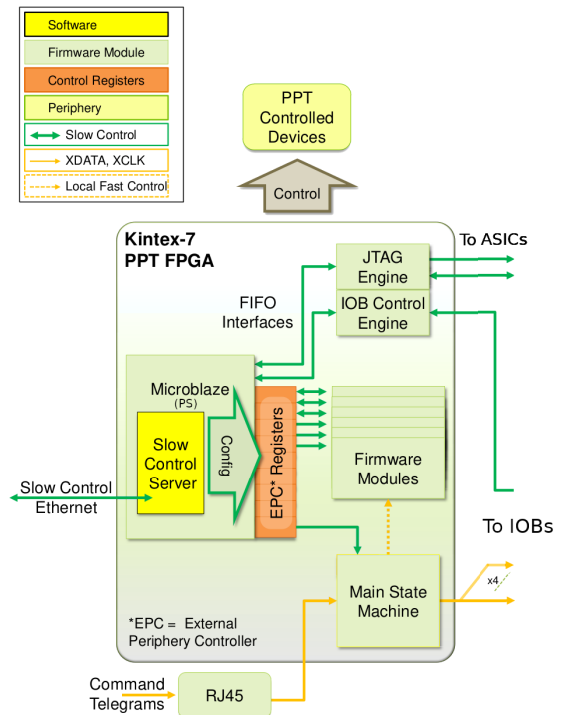**FIGURE 23.** Linearity of the 2.5ns steps for rising and falling edges.

FIGURE 24. Block scheme showing the PPT firmware concept, where the Microblaze implements the Processing System (PS) and all the rest is part of the Programmable Logic (PL).

The modification has been tested to verify the expected behavior; in Figure 23 is a plot of the measured step across the full-scale range of the available delays.

IV. PPT FIRMWARE, UPDATES

Even if the PPT features a device which is a "pure" FPGA (Kintex 7 Series family [30]), the way its firmware is conceived can be conceptually separated into a Programmable Logic (PL) part paired up with a Processing System (PS) component (MicroBlaze), as can be seen in Figure 24. The PS runs a Linux operating system, which is connected to a 256 MB Double Data Rate 3 (DDR3) memory, handles Transmission Control Protocol-Internet Protocol (TCP-IP) stack for the Gigabit Ethernet interface via RJ45, the registers for real-time control of different detector parts, a serial interface to a MicroUSB for debugging and monitoring, a so-called "Slow Control Server" providing a control interface to the System, General Purpose Input/Outputs (GPIOs) for management of the 4 IOBs JTAG configuration signals, and a couple of Serial Peripheral Interface (SPI) controllers to access the flash memories storing bitstreams for FPGAs from software. The PL counterpart, instead, mainly handles the datapath received from the IOBs, reconstructing pixel words,

buffering and sorting the images and generating the Ethernet packets to send out the data.

Concerning the Linux Operating System running on the Microblaze hosted on the PPT, the Kernel was updated in order to avoid obsolescence problems. Furthermore, the firmware was made compatible with the newest releases of the Xilinx IP-Cores (IPs) used in the PPT firmware; this was done by updating the Design Suite from Vivado 2019.2 to the more recent 2020.2. During this operation, to increase the portability of the project, we have completely reorganized the building environment of the Linux Image. We have chosen to migrate from the custom, hard-to-maintain, pre-existing set of bash scripts to Buildroot [31], an easy-to-use and efficient tool for the generation and maintenance of embedded Linux systems. Buildroot comprehends, among others, tools like Busybox [32], which were already used in the previous working environment.

Every custom driver which was present in the old images has been integrated into the Buildroot system as custom patches, which are easily integrated thanks to a cleaner and simpler interface for the included tools. We also added a DHCP client in the Linux image, as it will make it more practical to handle the IPs of the PPT as they move around different segments among the EuXFEL facilitiy.

V. CONCLUSION

An overview of the DSSC detector, with a more detailed description of its DAQ and the functions it carries out, has been presented, with quick reference to its integration in the EuXFEL environment.

Several problems afflicting the detector performance and user friendliness, due to hardware or firmware design limitations have been listed, and different solution have been proposed, implemented and the functionality verified in the final environment.

Different solutions to these issues have been evaluated and tried, which were then presented, implemented, and successfully tested, being ultimately included in the firmware of the IOB.

In particular, the wrong alignment between the XCLK, XDATA, and ASIC_resetn signals from the IOB to the ASICs was causing the ASICs to incorrectly receive command telegrams from the IOB. The implemented solution involved the utilization of an FPGA resource linked to an I/O pin for the implementation of a completely tunable delay, allowing for skew compensation among the interested signals. The same approach was used for finding a solution to the misalignment of with respect to the XCLK and the data generated by the detector and sent to the IOB via each of the 16 ASICs of a Ladder, which arrival time can be now individually tuned, whilst only a shared value for all the ASICs could be used in the previous firmware versions.

Moreover, the improvement of the DEPFET clear phase has been addressed: the old OSERDES2 primitive used to generate the delay between the edges of the Clear and Clear Gate signals, which had limited FSR and was mostly used at its maximum values, has now been replaced by a fast counter logic that allows to extend the range of these delays by a factor 5, enabling much larger bounds wherein to find an optimum for best imaging performance of the detector.

Regarding the PPT firmware and software did not show specific critical issues, but were updated to a newer version of the Vivado software suite, which required attentive work, and the build process for the embedded Linux image running on the MicroBlaze soft-core hosted on the PPT has been completely revised and reordered, granting accessibility and upgradability in an easy way; a DHCP server functionality has been added to the software package of the image, for easy reachability when the detector is moved across the facility, and the kernel version has been updated to the latest available version. This will ease further firmware and software updates.

REFERENCES

[1] W. Decking et al., "A MHz-repetition-rate hard X-ray free-electron laser driven by a superconducting linear accelerator," *Nature Photon.*, vol. 14, no. 6, pp. 391–397, Jun. 2020. [Online]. Available: https://www.nature.com/articles/s41566-020-0607-z

[2] B. W. J. McNeil and N. R. Thompson, "X-ray free-electron lasers," *Nature Photon.*, vol. 4, no. 12, pp. 814–821, Dec. 2010. [Online]. Available: https://www.nature.com/articles/nphoton.2010.239

[3] M. Porro et al., "Development of the DEPFET sensor with signal compression: A large format X-ray imager with mega-frame readout capability for the European XFEL," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 3339–3351, Dec. 2012.

[4] A. Scherz and O. Krupin, "Scientific instrument spectroscopy and coherent scattering (SCS)," Tech. Rep., 2013.

[5] M. Meyer et al., "The small quantum system (SQS) instrument at European XFEL: Results of commissioning and first experiments," *J. Phys., Conf. Ser.*, vol. 1412, no. 11, Jan. 2020, Art. no. 112005, doi: 10.1088/1742-6596/1412/11/112005.

[6] M. Hart, C. Angelsen, S. Burge, J. Coughlan, R. Halsall, A. Koch, M. Kuster, T. Nicholls, M. Prydderch, P. Seller, S. Thomas, A. Blue, A. Joy, V. O'shea, and M. Wing, "Development of the LPD, a high dynamic range pixel detector for the European XFEL," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. Rec. (NSS/MIC)*, Oct. 2012, pp. 534–537.

[7] A. Allahgholi et al., "Megapixels @ megahertz—The AGIPD high-speed cameras for the European XFEL," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 942, Oct. 2019, Art. no. 162324.

[8] M. Abdallah and O. Elkeelany, "A survey on data acquisition systems DAQ," in *Proc. Int. Conf. Comput., Eng. Inf.*, Apr. 2009, pp. 240–243.

[9] P. Willmann, H.-Y. Kim, S. Rixner, and V. S. Pai, "An efficient programmable 10 gigabit Ethernet network interface card," in *Proc. 11th Int. Symp. High-Performance Comput. Archit.*, Feb. 2005, pp. 96–107.

[10] A. Bhattacharya and P. De, "A survey of adaptation techniques in computation offloading," *J. Netw. Comput. Appl.*, vol. 78, pp. 97–115, Jan. 2017. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1084804516302570

[11] J. Coughlan, S. Cook, C. Day, R. Halsall, and S. Taghavi, "The data acquisition card for the large pixel detector at the European-XFEL," *J. Instrum.*, vol. 6, no. 12, p. C12057, Dec. 2011, doi: 10.1088/1748-0221/6/12/C12057.

[12] A. Allahgholi et al., "AGIPD, a high dynamic range fast detector for the European XFEL," *J. Instrum.*, vol. 10, no. 1, p. C01023, Jan. 2015, doi: 10.1088/1748-0221/10/01/C01023.

[13] S. Hauf et al., "The Karabo distributed control system," *J. Synchrotron Radiat.*, vol. 26, no. 5, pp. 1448–1461, Sep. 2019. [Online]. Available: http://scripts.iucr.org/cgi-bin/paper?S1600577519006696

[14] (Sep. 2022). *Embedded Linux: What it is, When and How to Use it—Lemberg Solutions*. [Online]. Available: https://lembergsolutions.com/blog/embedded-linux-what-it-when-and-how-use-it

[15] J. Seely, S. Erusalagandi, and J. Bethurem, "The MicroBlaze soft processor: Flexibility and performance for cost-sensitive embedded designs," Tech. Rep., 2017.

[16] T. Gerlach, A. Kugel, A. Wurz, K. Hansen, H. Klär, D. Müntefering, and P. Fischer, "The DAQ readout chain of the DSSC detector at the European XFEL," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, Oct. 2011, pp. 156–162.

[17] A. Kugel, M. Kirchgessner, M. Porro, J. Soldat, and T. Gerlach, "The PPT-module: High-performance readout for the DSSC detector at XFEL," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2013, pp. 1–6.

[18] F. Erdinger, L. Bombelli, D. Comotti, S. Facchinetti, P. Fischer, K. Hansen, P. Kalavakuru, M. Kirchgessner, M. Manghisoni, M. Porro, E. Quartieri, C. Reckleben, J. Soldat, and J. Szymanski, "The DSSC pixel readout ASIC with amplitude digitization and local storage for DEPFET sensor matrices at the European XFEL," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. Rec. (NSS/MIC)*, Oct. 2012, pp. 591–596.

[19] *Beamlines*. [Online]. Available: https://www.xfel.eu/facility/beamlines/indexeng.html

[20] *Scientific Instrument SCS*. [Online]. Available: https://www.xfel.eu/facility/instruments/scs/indexeng.html

[21] N. Z. Hagström et al., "Megahertz-rate ultrafast X-ray scattering and holographic imaging at the European XFEL," *J. Synchrotron Radiat.*, vol. 29, no. 6, pp. 1454–1464, Nov. 2022.

[22] M. Meyer et al., "The small quantum system (SQS) instrument at European XFEL: Results of commissioning and first experiments," *J. Phys., Conf. Ser.*, vol. 1412, no. 11, Jan. 2020, Art. no. 112005.

[23] E. Motuk, M. Postranecky, M. Warren, and M. Wing, "Design and development of electronics for the EuXFEL clock and control system," *J. Instrum.*, vol. 7, no. 1, p. C01062, Jan. 2012. [Online]. Available: https://iopscience.iop.org/article/10.1088/1748-0221/7/01/C01062

[24] M. Kirchgessner, J. Soldat, A. Kugel, M. Donato, M. Porro, and P. Fischer, "The high performance readout chain for the DSSC 1Megapixel detector, designed for high throughput during pulsed operation mode," *J. Instrum.*, vol. 10, no. 1, p. C01011, Jan. 2015. [Online]. Available: https://iopscience.iop.org/article/10.1088/1748-0221/10/01/C01011

[25] P. Lechner, L. Andricek, S. Aschauer, A. Bähr, G. De Vita, K. Hermenau, T. Hildebrand, G. Lutz, P. Majewski, M. Porro, R. H. Richter, C. Sandow, G. Schaller, H. Soltau, and L. Strüder, "DEPFET active pixel sensor with non-linear amplification," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, Oct. 2011, pp. 563–568.

[26] *ug386.pdf Viewer Documentation Portal*. [Online]. Available: https://docs.xilinx.com/v/u/en-US/ug3866

[27] P. Moreira et al. (2021). *GBTX Manual; V0.18 Draft*. [Online]. Available: https://cds.cern.ch/record/2809057

[28] *34276—Spartan-6 FPGA—Can the IODELAY2 be Used to Delay an Output in Variable Mode?* [Online]. Available: https://support.xilinx.com/s/article/34276?language=enUS

[29] *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics (DS162)*. [Online]. Available: https://docs.xilinx.com/v/u/en-U.S./ds162

[30] *7 Series FPGAs Data Sheet: Overview (DS180)*, 2020.

[31] *Buildroot—Making Embedded Linux Easy*. [Online]. Available: https://buildroot.org/

[32] *BusyBox*. [Online]. Available: https://busybox.net/

ANDREA COSTA (Member, IEEE) was born in Piacenza, in 1995. He received the B.Sc. degree in biomedical engineering and the M.Sc. degree in electronics engineering from Politecnico di Milano, in 2017 and 2020, respectively. He is currently pursuing the Ph.D. degree in information technology with the Digital Electronics Laboratory, Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano. His research interests include innovative hardware architectures for data processing in the field of FPGA time-domain devices and FPGA DAQ for high data rate environments.

NICOLA LUSARDI (Member, IEEE) was born in Piacenza, in 1990. He received the Ph.D. degree, in 2018.

He developed the thesis work with the Digital Electronics Laboratory, DEIB, Politecnico di Milano, on a topic regarding high-resolution time-to-digital converters (TDCs) in field programmable gate arrays (FPGA). He is currently a temporary Researcher with the Digital Electronics Laboratory, DEIB, a Professor of electronics with Politecnico di Milano, and an Associate Member of the Italian National Nuclear Physics Institute (INFN). Since 2014, he has been collaborating with CERN in the LHCb experiment; CAEN S.p.A., Viareggio, Italy; CAENels S.r.l., Basovizza, Italy; Elettra Sincrotrone Trieste S.C.p.A., Basovizza, Italy; Single Quantum B.V., Delft, The Netherlands; the Technology University of Delft; École Polytechnique Fédérale de Lausanne; Rete Ferroviaria Italiana; and European XFEL. He is also the Co-Founder of TEDIEL S.r.l., an Italian start-up and spin-off of Politecnico di Milano. His research line and knowledge as a digital designer have been acknowledged by public and private research centers.
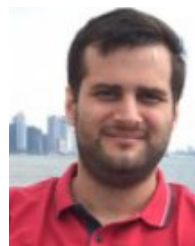
FABIO GARZETTI (Member, IEEE) received the bachelor's, master's, and Ph.D. degrees in electronics engineering from Politecnico di Milano. He developed the thesis work with the Digital Electronics Laboratory, DEIB, Politecnico di Milano, on a topic regarding innovative solutions for calibration and triggering of asynchronous signals for time-to-digital converters (TDCs) in field programmable gate arrays (FPGA), work for which he received the 2022 Dimitris N. Chorafas Foundation Award. He held a temporary research fellowship position with the Digital Electronics Laboratory, DEIB, Politecnico di Milano, within the framework of the "Design of modules for readout and processing of sampled data based on FPGA architectures" research programme, supported by CAEN ELS, and is currently a temporary Researcher.

ENRICO RONCONI (Member, IEEE) received the bachelor's and master's degrees in electronic engineering from Politecnico di Milano, in 2017 and 2020, respectively. He is currently with the Digital Electronics Laboratory, Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano, where he developed together with the time-to-digital and digital-to-time converters (TDC and DTC). His research interests include advanced programmable logic (PL) and software architectures for data processing and transfer in field programmable gate arrays (FPGA) implemented scientific equipment.

STEFANO MAFFESSANTI received the M.Sc. degree in electronics engineering from Politecnico di Milano, in 2014. He is currently a Research Scientist with Deutsches Elektronen-Synchrotron DESY, Hamburg, Germany. His research interests include the development of detector systems for high energy physics and photon science applications.

CYRIL DANILEVSKI was born in 1991. He received the bachelor's and master's degrees in computer science from the University of Aberdeen, with a focus on embedded systems. He is currently with European XFEL, where he specializes in control systems and detector integration.

DAVID LOMIDZE was the DP05 Project Manager with SQS. During the tenure with the Technological Institute of Georgia, he was a member of the scientific council and contributed to the establishment of master's degree course with the High Energy Physics School as well as the development of the hadron therapy megaproject. In addition, he was a Research Associate with the Institute of Experimental Physics, University of Hamburg, Germany, where he was involved in the development of analog hadron calorimeter (AHCAL) for the international linear detector (ILD), CALICE collaboration, and studies of neutron irradiation effects on SiPMs. Prior to this, he was with Johannes Gutenberg Universität Mainz, Germany, where he developed the Muon Veto Detector (MUV) for the NA62 experiment at CERN. He was also a Scientific Researcher with the University of Wisconsin–Madison, Madison, WI, USA, and contributed to the RPC system offline data quality monitoring development. He is currently a Detector Scientist with European XFEL, where he is responsible expert for the DSSC detector operation with SCS and SQS instruments. He is a highly experienced physicist with more than 17 years of research and development experience in experimental particle physics. He spend significant amount of the career with the Istituto Nazionale di Fisica Nucleare, Naples, Italy. In Naples, he held several scientific researcher positions, he contributed to the development and commissioning of RPC detectors for the CMS experiment with LHC, CERN. This included the development of test setups for high and low voltage power supplies of the RPC detectors, as well as the development of detector commissioning tools and the online data quality monitoring (DQM) tool for the RPC detector subsystem.

development of a large format X-ray imager with mega-frame readout capability for photon science experiments. The specifications of this system go beyond any existing instrument and required the development of new concepts and technologies. The first fully functional DSSC 1-Megapixel camera was completed and successfully installed and commissioned European XFEL, in 2019. DSSC is at the moment, the fastest existing 2D imaging detector for soft X-rays and opens up worldwide unique possibilities for photon science. Among the other projects, he has been responsible of the development of the ASTEROID ASIC which has been used for the Mercury Imaging X-ray Spectrometer (MIXS) instrument of BepiColombo, a joint cornerstone mission of the European Space Agency and the Japan Aerospace Exploration Agency for Mercury Exploration launched, in October 2018. His ASIC development activity also includes the design of the readout for pnCCDs for optical astronomy and for experiments with the new generation of X-ray Free Electron Lasers. He is the author and coauthor of more than 120 publications on peer-reviewed journals and conference proceedings. His research interests include the development of low-noise silicon detectors and the associated readout ASICs.

Dr. Porro received the IEEE Radiation Instrumentation Early Career Award, in 2010, and the IEEE Emilio Gatti Radiation Instrumentation Technical Achievement Award, in 2021. Since 2022, he has been an Associate Professor of electronics with the Department of Molecular Sciences and Nanosystems, University Ca'Foscari in Venice, Italy. He is at the moment the Chair of the Linac Coherent Light Source (LCLS) Detector Advisory Committee (LDAC), National Accelerator Laboratory (SLAC), operated by Stanford University, Stanford, CA, USA.

MONICA TURCATO (Member, IEEE) received the master's and Ph.D. degrees in physics from the University of Padua. Before joining the photon science community, she dedicated a significant part of the career to high energy physics. She was involved in the ZEUS experiment of the HERA accelerator with the University of Hamburg, where she covered different roles, from expert in data taking to scientific data analysis coordinator. In 2011, she joined European XFEL as a Detector Scientist, and became the in-house responsible and contact person for the DSSC Consortium, developing one of the MHz detectors deployed at the facility. In the DSSC project, she lead the integration of the first detector at the SCS instrument, in 2019. She is currently the Head of the Detector Group, European XFEL, which is mandated with detector installation, commissioning, testing, calibration, and operation; the group also coordinates and participates to detector development projects aimed to providing specific detectors for the European XFEL.

ANGELO GERACI (Senior Member, IEEE) received the M.Sc. degree (cum laude) in electrical engineering and the Ph.D. degree (cum laude) in electronics and communication engineering from the Politecnico di Milano, in 1993 and 1996, respectively. He is currently a Lecturer of the ''Sistemi Elettronici Digitali'' and ''Digital Electronic Systems Design'' courses with the School of Industrial and Information Engineering, Politecnico di Milano, and holds courses for the Ph.D. programme on information technology. He is also a member of a Management Board and Deputy Coordinator with the Ph.D. School of Information Engineering, Politecnico di Milano. Since 1995, he has been a Scientific Collaborator with the Italian National Nuclear Physics Institute (INFN). Since 2004, he has also been an Associate Professor with the Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano. His research interests include digital electronics based on microcontrollers, DSP and FPGA devices, specifically in the areas of radiation detection, medical imaging, energy storage for automotive electric systems, and HPC applications. He is an auditor of projects on behalf of the Italian MIUR. He is the author and coauthor of more than 320 publications on refereed international congress proceedings and journals, such as IEEE TRANSACTIONS Prize Paper Award by the IEEE Power Electronic Society, in 2004. He has been an Advocate and the Manager of several sponsored joint research projects between Politecnico di Milano and private/public companies. In 2003, he was elevated to the level of a Senior Member of the IEEE Nuclear and Plasma Society. As a referee for several international journals, including IEEE TRANSACTIONS ON NUCLEAR SCIENCE and *Review of Scientific Instruments*.

MATTEO PORRO (Member, IEEE) received the master's degree in electronics engineering and the Ph.D. degree in radiation science and technology from Politecnico di Milano, Italy.

From 2005 to 2015, he was a Research Scientist with the Max Planck Institute for Extraterrestrial Physics and the Semiconductor Laboratory Munich, Germany. He was also a Coordinator of the ASIC Design Team. In 2015, he moved to European XFEL, Schenefeld, Germany, with the role of Coordinator and the P.I. of the DSSC project. The project aims at the

• • •