IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 19 June 2023, accepted 15 July 2023, date of publication 7 August 2023, date of current version 24 August 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3302350

APPLIED RESEARCH

Input-Parallel Output-Series High Step-Up DC/DC Converter With Coupled Inductor and Switched Capacitor

SANG-WHA SEO[1], JOON-HYOUNG RYU[2], HAN HO CHOI[3], AND JAE-BUM LEE[4]

[1]Future Automobile Innovation Education Center, Dankook University, Yongin-si 16890, South Korea
[2]Propulsion System Research Team, Korea Railroad Research Institute, Uiwang-si, Gyeonggi-do 16105, South Korea
[3]Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, South Korea
[4]Department of Railroad Electrical and Electronics Engineering, Korea National University of Transportation, Uiwang-si, Gyeonggi-do 16106, South Korea

Corresponding author: Jae-Bum Lee (leejb@ut.ac.kr)

This work was supported in part by the Technology Innovation Program (Development of Power Module and Integrated Circuit Technology for High Power Density of Electric Components for Hydrogen Electric Commercial Vehicles) funded by the Ministry of Trade, Industry and Energy (MOTIE, South Korea), under Grant 20018971 and Grant 1415185855; in part by the Korea National University of Transportation Industry-Academy Cooperation Foundation, in 2023; and in part by the Human Resources Development Project of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) for the support grant funded by the Korean Government Ministry of Trade, Industry and Energy under the project titled: "Middle Market Enterprise Specialized Human Resources Development for Residential and Commercial Fuel Cell" under Grant 20224000000580.

ABSTRACT In this study, the authors propose a non-isolated high step-up interleaved DC/DC converter that can be applied to sustainable energy system. The proposed converter achieves high voltage gain by employing a coupled inductor and switched capacitor method based on an interleaved boost converter. The two coupled inductors connected in parallel with the input side have a distinct structure. Specifically, a single coupled inductor has a primary side and a secondary side connected in series, and it is further connected in parallel with an output side switched capacitor circuit. The switched capacitor circuit increases the voltage gain by being charged in parallel and discharged in series through the coupled inductor. The leakage inductor energy of the coupled inductor can be regenerated to the output side through the passive clamp circuit's performance. Moreover, it is possible to select devices with low voltage stress and on-state resistance of the switches, which results in reduced loss and size while alleviating the reverse recovery problem of diodes. The steady-state analysis and operation principle of the proposed converter are thoroughly explained and verified through a prototype circuit with 20V input voltage, 400V output voltage, and 320W level output power.

INDEX TERMS DC/DC converter, high step-up, interleaved converter, coupled inductor, switched capacitor.

I. INTRODUCTION

Sustainable energy sources, such as solar panels, fuel cells, and wind power, have low output voltage ranges. Therefore, a high step–up DC/DC converter delivers a high voltage DC load through a high voltage output, an AC load through a DC/AC inverter, and the DC bus of the microgrid, as depicted in Fig. 1. In developed countries, fuel cell systems are developing rapidly, primarily owing to their advantages of high performance and sustainability. Generally, the output voltage of the FC stack varies from 24V to 40V depending on the output power, which requires a high DC bus voltage (380V∼400V) on the input side of the DC/AC inverter to obtain utility AC power [1], [2], [3], [4], [42], [43], [47], [48]. Among numerous renewable energy sources, photovoltaic (PV) systems have achieved the greatest growth, primarily because the output voltage of a PV module is typically low (20V∼50V). A front–end high step–up DC/DC converter is required to step up and regulate the voltage level of the PV voltage onto the DC bus (400V or 800V) [5], [6], [7], [8]. In wind power generation, one–way DC/DC converters are used to connect wind farms to HVDC terminals, and

The associate editor coordinating the review of this manuscript and approving it for publication was Chi-Seng Lam.

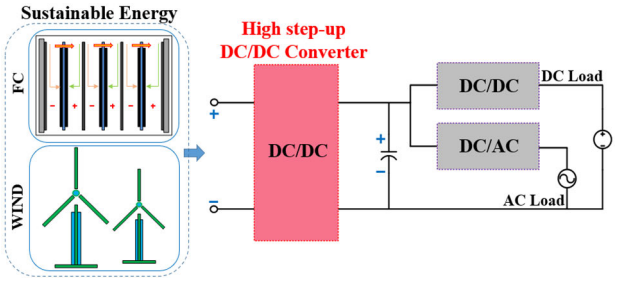


FIGURE 1. Block diagram of sustainable energy power conversion system.

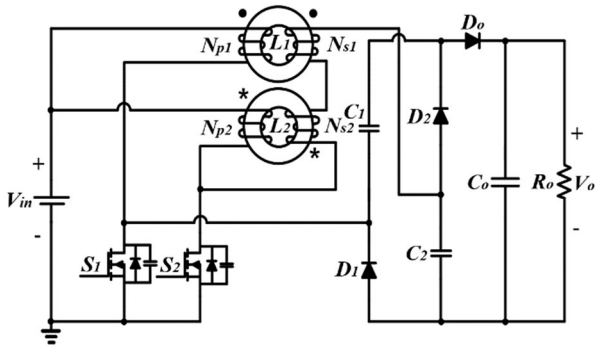


FIGURE 2. Topology of the proposed converter.

numerous power converter topologies are being developed. A modular multi–level converter is one of the most widely used structures in HVDC. Besides, unidirectional DC/DC converters are being developed to reduce the voltage stress of the switching device [9], [10], [11], [12].

A conventional boost converter has a simple structure and low component count; therefore, it is a topology that is applicable to numerous applications, and it can provide high voltage gain by increasing the duty cycle. However, in practice, the duty cycle is limited by the effect of the equivalent series resistance (ESR) of switches, diodes, inductors, and capacitors. Consequently, operating at very high duty cycles can result in severe reverse recovery problems for the output diode, low efficiency, and electromagnetic interference (EMI) problems [13], [14].

Moreover, there is a limit that the duty cycle must be increased to increase the voltage gain, and it is unsuitable for power density improvement and high voltage applications owing to the high voltage stress of semiconductor components [15], [16]. Numerous studies on single switch-based topologies with high step–up voltage gain have been conducted to overcome the limitations of conventional boost converters [17], [18], [19], [20], [21], [22], [23], [24], [25]. Coupled inductors, switched inductors, switched capacitors, and voltage–lift circuits are high step–up technologies that can increase the voltage gain using a low duty cycle. However, high voltage stress across components, ripple current, higher voltage gain, etc., can be very difficult to realize as common design goals. Therefore, an ideal topology for a high–voltage gain–conversion system should have few components, high efficiency, low cost, high voltage gain, small size, high power density, easy integration, and high reliability.

Interleaved technology offers numerous advantages, such as reduced ripple current and component size. Moreover, interleaved technology can effectively increase the switching frequency, and has been applied to high power applications. However, the interleaved boost converter still has disadvantages such as high voltage stress of the semiconductor device, reverse recovery loss of the output diode, and low voltage gain. The advantages of the interleaved boost converter and the application of high step–up technology have the following advantages [26], [27], [28]: 1. Low duty cycle 2. Low–voltage stress in semiconductor devices. 3. Utilization of active (switching and conduction losses) and passive (magnetic core) devices. Moreover, interleaved boost converters can be integrated with flyback boost converters and voltage multiplier cells (VMC) to achieve a high voltage gain [29], [30], [31], [32], [33], [34]. The VMC comprises a coupled inductor, switched capacitor, and a voltage lift circuit, which recycles the leakage energy to help achieve zero-voltage/current switching (ZVS/ZCS) of the switch and zero-current switching of the diode. However, flyback type interleaved high step–up converters increase control complexity because voltage balancing must be considered. In addition, the coupled inductor interleaved method, including the active clamp circuit, reduces power density and increases cost by adding switches and gate drivers [35], [36], [37].

Interleaved high step–up converters in which coupled inductors and VMC are combined can increase voltage gain through two switches, a parallel structure of an input-side coupled inductor, and an output side series structure [38], [39], [40]. The high step–up DC/DC converters can gain additional voltage gain through the turns ratio of the coupled inductor. The passive clamp performance of the VMC can recycle the leakage energy of the coupled inductor and mitigate the voltage spikes on the switch. Moreover, the leakage inductor energy can achieve ZCS of the switches, thereby alleviating the reverse recovery problem of the diodes. However, in these converters, if the turns ratio of the coupled inductor is increased to increase the voltage gain, the voltage stress of the output diode increases, and the voltage gain increases, and the power density is rather high. The proposed converter does not have a trade–off phenomenon in semiconductor devices even when the turns ratio of the coupled inductor is increased to increase the voltage gain, and has very low power density improvement characteristics. Therefore, it will be an effective choice for selecting semiconductor devices of the high step–up converter for sustainable energy applications and efficiently implementing the driving system.

In this study, the authors propose an interleaved DC/DC converter with a high voltage gain and power density, as depicted in Fig. 2. It comprises two coupled inductors (L_1, L_2), two switches (S_1, S_2), three diodes (D_1, D_2, D_o),

and three capacitors (C_1, C_2, C_o). The turns ratio ($N = N_{s1}/N_{p1} = N_{s2}/N_{p2}$) of the coupled inductors is identical, and the coupling standard according to the winding direction is indicated by " · " and " ∗ ", respectively. The primary windings of the coupled inductor are connected in parallel, and the secondary windings are connected in series. The proposed converter uses a coupled inductor and switched capacitor technology. Input–side coupled inductors were combined with switched capacitors to alternately charge in parallel and discharge in series to achieve a high step–up voltage gain. Additionally, the voltage gain can be increased by the turns ratio (N) of the coupled inductor, and the voltage stress of the switch can be lowered. Accordingly, the conduction loss can be reduced by adopting a low voltage range (V_{DS}) and low ON–state resistance (R_{DS_ON}) for the MOSFETs. The passive clamping performance of the switched capacitor reuses the leakage inductor energy of the coupled inductor to increase voltage gain. It also has the advantage of achieving zero voltage Turn–ON/Turn–OFF of switches and diodes by limiting the slope of the current rise. The proposed converter introduces a simple structure using a non-isolated coupled inductor method for alternative energy applications requiring a high step–up voltage gain.

The remainder of this paper is organized as follows. In Section II, the operating mode of the proposed converter is described. Section III presents a steady-state analysis. In Section IV, the improvement characteristics are confirmed through a comparison with experimental results. Finally, Section V presents the conclusions.

II. OPERATING PRINCIPLE

The equivalent circuit of the proposed converter is shown in Fig. 3. Among the two coupled inductors, the primary side has magnetizing inductors (L_{m1}, L_{m2}) and leakage inductors (L_{k1}, L_{k2}), and the secondary side has a leakage inductor (L_s), which is modeled as an ideal transformer. The voltage-multiplier circuit comprises two switched capacitor circuits (D_1, D_2, C_1, C_2) connected in parallel. Through the switched capacitor circuit and alternating Turn–OFF of the switches (S_1, S_2), the energy of the coupled inductor is charged in parallel and discharged in series on the secondary side.

The advantages of the proposed topology are as follows; 1) The proposed converter has a low input current ripple and low conduction loss through input side interleaved technology, making it suitable for high–power applications; 2) The proposed topology can achieve the high step–up voltage gain (M) required in the alternative energy system and higher power density because of having fewer components than those of converters; 3) The leakage energy of the coupled inductor can be recycled to the output terminal, which helps to ZCS Turn–ON in the switch and ZCS Turn–OFF in the diode; 4) The voltage stress of the switches and diodes is substantially lower than the output voltage; 5) Low cost and high efficiency are achieved through the low R_{DS_ON} and low rated voltage of the power semiconductor devices.

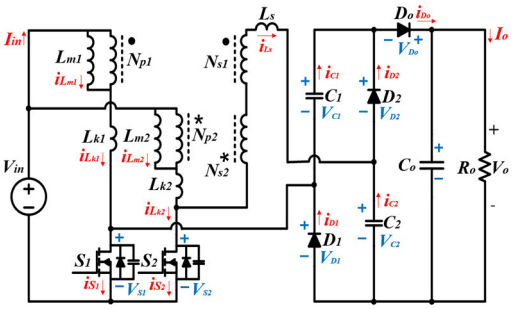


FIGURE 3. Equivalent circuit of the proposed converter.

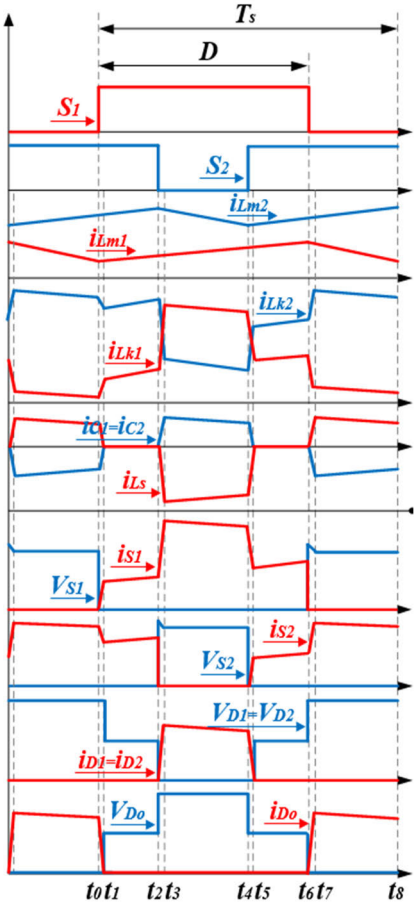


FIGURE 4. Key waveforms of the proposed converter.

The assumptions detailed below were made to simplify the analysis of the proposed topology.

1. The current of each major component is operated and analyzed based on the indicated direction.

2. The magnetizing inductor of coupled inductors operates in continuous conduction mode (CCM) and the duty cycle (D) is higher than 0.5.

3. Except for the leakage inductor of the coupled inductor and parasitic capacitor of the switch, all components are considered as ideal devices without parasitic parameters.

4. Since the capacitance of the capacitors (C_1, C_2, C_o) is sufficiently large, the voltage ripple is negligible.

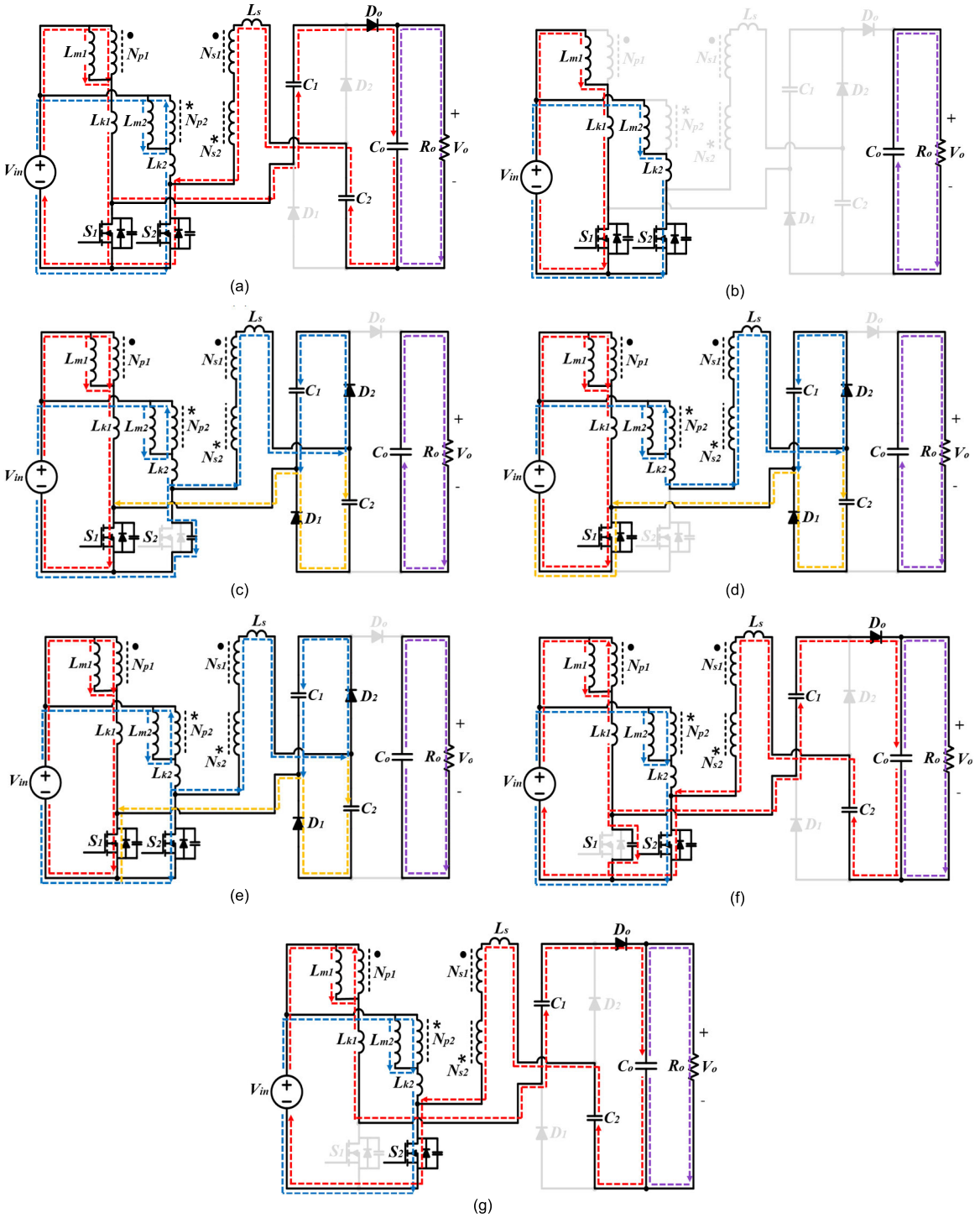


FIGURE 5. Current flow path in the operating mode of the proposed converter. (a) *Mode I* [t_0–t_1]; (b) *Mode II* [t_1–t_2]; *Mode VI* [t_5–t_6]; (c) *Mode III* [t_2–t_3]; (d) *Mode IV* [t_3–t_4]; (e) *Mode V* [t_4–t_5]; (f) *Mode VII* [t_6–t_7]; (g) *Mode VIII* [t_7–t_8].

1) *Mode I* $[t_0 - t_1]$

In the case of t_0, the *mode* starts when S_1 is Turned–ON, and this current flow is illustrated in Fig. 5(a). In this *mode*, current i_{Ls} gradually decreases because of the series-connected winding characteristics of the secondary side (N_{s1}, N_{s2}) of the coupled inductors (L_1, L_2), which causes S_1 to partially ZCS Turn–ON. In addition, since D_o is ZCS Turned–ON, and the current can be expressed as follows:

$$i_{Do}(t) = i_{Ls}(t) = I_{Do}(t_o) - \frac{V_o - V_{C1} - V_{C2}}{N^2(L_{k1} + L_{k2})}(t - t_0). \quad (1)$$

2) *Mode II* $[t_1 - t_2]$; *Mode VI* $[t_5 - t_6]$

In the case of $t = t_1$, S_1 and S_2 are ON, and this *mode* is started; this current flow is outlined as shown in Fig. 5(b).

All diodes (D_1, D_2, D_o) were reverse–biased, and L_{m1}, L_{m2}, L_{k1}, and L_{k2} were charged by the input source. In addition, C_o supplies power to R_o and the equation for this *mode* can be written as follows:

$$i_{Lmx}(t) = i_{Lkx}(t) = I_{Lmx}(t_1) + \frac{V_{in}}{L_{kx} + L_{mx}}(t - t_1) \quad (2)$$

$$V_{C1} = V_{C2} = V_{D1} = V_{D2} = V_{Do} \quad (3)$$

3) *Mode III* [$t_2 - t_3$]

In the case of t_2, this *mode* starts when S_2 is Turned–OFF, and the current flow is outlined in Fig. 5(c). The stored energy of L_{m2} charges C_1 and C_2 by forward–biasing D_1 and D_2 through the secondary side (N_{s1}, N_{s2}) of the coupled inductors (L_1, L_2). The voltage difference between the primary side (N_{p1} and N_{p2}) and secondary side (N_{s1}, N_{s2}) of the coupled inductors (L_1, L_2) is charged in the parasitic capacitor of S_2, and when it becomes $(2N/3{+}3N)V_o$, the *mode* is terminated.

4) *Mode IV* [$t_3 - t_4$]

In the case of t_3, *Mode IV*is started, and the current flow is outlined in Fig. 5(d). Energy is supplied to C_1 or C_2 through two paths ($V_{in} \rightarrow L_{m2} \rightarrow L_{k2} \rightarrow N_{s2} \rightarrow N_{s1} \rightarrow L_s \rightarrow D_2$ or D_1) for the flow of current, and the equation for this *mode* can be written as follows:

$$i_{Lk1}(t) = i_{Lm1}(t) + N\,(i_{D1} + i_{D2})\,(t) \quad (4)$$

$$i_{Lk2}(t) = -i_{Ls}(t) = N\,(i_{D1} + i_{D2})\,(t) \quad (5)$$

$$i_{S1}(t) = i_{Lm1}(t) + i_{Lm2}(t) = i_{Lk1}(t) - i_{Ls}(t) \quad (6)$$

5) *Mode V* [$t_4 - t_5$]

In the case of t_4, *Mode V* starts when S_2 is Turned–ON, and this current flow is outlined in Fig. 5(e). In this *mode*, the leakage inductor current gradually increases or decreases because of the series–connected winding characteristics of the secondary side (N_{s1}, N_{s2}) of the coupled inductors (L_1, L_2), which causes S_2 to partially ZCS Turned–ON. In addition, D_1 and D_2 are ZCS Turned–OFF, and there is no reverse recovery problem. The current in this *mode* can be written as follows:

$$i_{D1}(t) = i_{D2}(t) = I_{D1}(t_4) - \frac{V_{C1}}{N^2(L_{k1} + L_{k2})}(t - t_4) \quad (7)$$

$$i_{S2}(t) = \frac{2V_{C1}}{N^2(L_{k1} + L_{k2})}(t - t_4) \quad (8)$$

$$i_{Ls}(t) = I_{Ls}(t_4) + \frac{2V_{C1}}{N^2(L_{k1} + L_{k2})}(t - t_4). \quad (9)$$

6) *Mode VII* [$t_6 - t_7$]

In the case of t_6, *Mode VII* starts when S_1 is Turned–OFF, and the current flow is outlined, as shown in Fig. 5(f). The energy stored in L_{m1}, C_1, and C_2 charges C_o by forward biasing D_o through the secondary side (N_{s1}, N_{s2}) of the coupled inductors (L_1, L_2). The voltage difference between the primary side (N_{p1} and N_{p2}) and secondary side (N_{s1}, N_{s2}) of the coupled inductors (L_1, L_2) is charged to the parasitic capacitor of S_1, and when it becomes $(4N/3{+}3N)V_o$, *Mode VII* is terminated.

7) *Mode VIII* [$t_7 - t_8$]

In the case of t_7, *Mode VIII* is started, and the current flow is outlined in Fig. 5(g). Accordingly, the flow of current charges $C_o$through one path ($C_2 \rightarrow L_s \rightarrow N_{s1} \rightarrow N_{s2} \rightarrow V_{in} \rightarrow N_{p1} \rightarrow D_o$), which dissipates power to R_o, and the equation for this *mode* can be written as follows:

$$i_{Lk1}(t) = i_{Ls}(t), \quad i_{Lk2}(t) = i_{Lm2}(t) + i_{Ls}(t) \quad (10)$$

$$i_{S2}(t) = i_{Lm1}(t) + i_{Lm2}(t) = i_{Lk2}(t) + i_{Ls}(t). \quad (11)$$

III. PERFORMANCE ANALYSIS

A. STEADY–STATE ANALYSIS: HIGH STEP–UP VOLTAGE GAIN

In Section II, a steady–state analysis of the proposed high step–up converter is conducted using *Modes II*, *IV*, *V,* and *VIII* and ON/OFF switches. Ignoring the transient characteristics (*Mode III* and *Mode VII*) of the circuit, the coupling coefficient (k) is defined as follows:

$$k = \frac{L_{mx}}{L_{mx} + L_{kx}}. \quad (12)$$

In *Mode II*, the primary and secondary voltages of the magnetizing inductors (L_{m1}, L_{m2}) and the voltage of the leakage inductors (L_{k1}, L_{k2}) for the coupled inductors can be expressed as follows:

$$V^{II}_{Lk1} = V^{II}_{Lk2} = \frac{L_{k1}}{L_{m1} + L_{k1}}V_{in} = \frac{L_{k2}}{L_{m2} + L_{k2}}V_{in} = (1 - k)V_{in} \quad (13)$$

$$V^{II}_{Lm1} = V^{II}_{Lm2} = \frac{L_{m1}}{L_{m1} + L_{k1}}V_{in} = \frac{L_{m2}}{L_{m2} + L_{k2}}V_{in} = kV_{in} \quad (14)$$

$$V^{II}_{Ns1} = V^{II}_{Ns2} = NkV_{in}. \quad (15)$$

The volt-second balance principle can be applied based on the voltage components of a coupled inductor (L_1), which can be written as follows:

$$\int_0^{DT_s} V^{II}_{Lk1}dt + \int_{DT_s}^{T_s} V^{VIII}_{Lk1}dt = 0 \quad (16)$$

$$\int_0^{DT_s} V^{II}_{Lm1}dt + \int_{DT_s}^{T_s} V^{VIII}_{Lm1}dt = 0 \quad (17)$$

$$\int_0^{DT_s} V^{II}_{Ns1}dt + \int_{DT_s}^{T_s} V^{VIII}_{Ns1}dt = 0. \quad (18)$$

By substituting (13)–(15) with (16)–(18), the voltage of the coupled inductors (L_1, L_2) can be written as follows:

$$V^{VIII}_{Lk1} = V^{IV}_{Lk2} = -\frac{D(1 - k)}{1 - D}V_{in} \quad (19)$$

$$V^{VIII}_{Lm1} = V^{IV}_{Lm2} = -\frac{Dk}{1 - D}V_{in} \quad (20)$$

$$V^{VIII}_{Ns1} = V^{IV}_{Ns2} = -\frac{NDk}{1 - D}V_{in}. \quad (21)$$

OFF period of switch S_2 — By analyzing *Mode IV*, the voltages of capacitors C_2 and C_1 are given as follows:

$$\begin{aligned} V_{C1} = V_{C2} &= V_{in} - V_{Lm2}^{IV} - V_{Lk2}^{IV} - V_{Ns2}^{IV} + V_{Ns1}^{II} \\ &= V_{in} + \frac{Dk}{1-D}V_{in} + \frac{D(1-k)}{1-D}V_{in} \\ &\quad + \frac{NDk}{1-D}V_{in} + NkV_{in} = \frac{1+Nk}{1-D}V_{in}. \end{aligned} \tag{22}$$

The OFF period of switch S_1 — In the analysis of *Mode VIII*, the energy is transferred to capacitor C_o, and the load side output voltage (V_o) is given as follows:

$$\begin{aligned} V_o &= V_{C2} - V_{Ns1}^{VIII} + V_{Ns2}^{II} + V_{in} - V_{Np1}^{VIII} - V_{Lk1}^{VIII} + V_{C1} \\ &= \frac{1+Nk}{1-D}V_{in} + \frac{NDk}{1-D}V_{in} + NkV_{in} + V_{in} \\ &\quad + \frac{Dk}{1-D}V_{in} + \frac{D(1-k)}{1-D}V_{in} + \frac{1+Nk}{1-D}V_{in} \\ &= \frac{3+3Nk}{1-D}V_{in}. \end{aligned} \tag{23}$$

Excluding the coupling coefficient (k), the ideal voltage gain (M) of the proposed high step–up converter can be written as follows:

$$M = \frac{V_o}{V_{in}} = \frac{3+3N}{1-D}. \tag{24}$$

It is confirmed that the proposed converter has a high step–up voltage gain (M) without an extreme D or a high N. For example, if $D = 0.7$ and $N = 1$, V_o can obtain a voltage gain (M) that is twenty times higher than V_{in}.

B. STEADY–STATE ANALYSIS: VOLTAGE STRESS

Based on the voltage applied to *Mode IV*(S_2) and *Mode VIII*(S_1), the voltage stress of the switches is obtained as follows:

$$V_{S2} = V_{S1} = V_{in} - V_{Lm2}^{IV} = V_{in} + \frac{D}{1-D}V_{in} = \frac{1}{1-D}V_{in} \tag{25}$$

$$V_{S2} = V_{S1} = \frac{V_{in}}{1-D} = \frac{1}{3+3N}V_o. \tag{26}$$

In Section II (*Mode III*, *Mode VII*), the voltage spike problem of the switches (S_1, S_2) may occur through the resonance phenomenon between the leakage inductors (L_{k1}, L_{k2}) and the parasitic capacitor of the switch. The voltage spike was reduced by adding a snubber network of the switches (S_1, S_2), and 200V was designed in consideration of this problem.

A low voltage stress results in low switching losses. Moreover, low voltage rated MOSFETs with a small ON–resistance can be used, resulting in low conduction losses.

Since the voltage stress of the diodes is determined by the charged voltage of the capacitors, it is obtained as follows:

$$V_{Do} = V_{D1} = V_{D2} = V_o - V_{C1} = \frac{2+2N}{3+3N}V_o = \frac{2}{3}V_o. \tag{27}$$

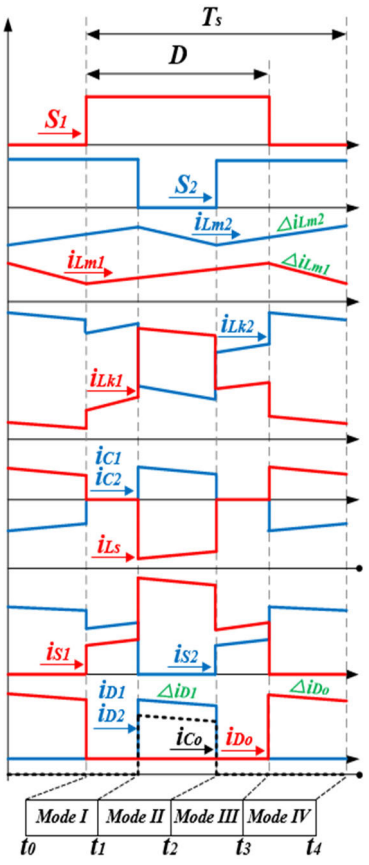


FIGURE 6. Key current waveforms of the proposed converter [$i_{Lk1} = i_{Lk2} = i_{Ls} \approx 0$].

C. STEADY–STATE ANALYSIS: CURRENT STRESS

Based on the voltage applied to *Mode IV*(S_2) and *Mode VIII*(S_1), the voltage stress of the switches is obtained as follows:

The steady–state current stress of the proposed converter excludes transient analysis through leakage inductance, and comprises four *Modes*(I, II, III, IV), as shown in Fig. 6. Furthermore, the current stress was analyzed based on the actual experimental parameters (V_{in} =20V, V_o =400V, I_{in} =16A, I_o =0.8A, D = 0.7, f_s =80kHz, L_{m1} = L_{m2} =60μH, R_o =500Ω, P_o =320W). Based on the charge balance of the capacitors (C_1, C_2), the following equations were obtained:

$$I_{C1} + I_{C2} = \frac{1}{1+N}I_{Lm2}(1-D)\Big|_{I_{C1}=I_{C2}} \tag{28}$$

$$\begin{aligned} I_{C1} &\rightarrow \frac{1}{2(1+N)}I_{Lm2}(1-D) \\ &= \frac{1}{1+N}I_{Lm1}(1-D)\Big|_{N=1} \rightarrow I_{Lm2} = 2I_{Lm1} \end{aligned} \tag{29}$$

Based on the input current and (29), the *average* current in the magnetizing inductors (I_{Lm1}, I_{Lm2}) can be written as

follows:

$$I_{in} = I_{Lm1} + I_{Lm2} = 16A \tag{30}$$

$$I_{Lm1} = \frac{1}{3}I_{in} = 5.33A, I_{Lm2} = \frac{2}{3}I_{in} = 10.67A. \tag{31}$$

Also, through the charge balance according to the D of the capacitor (C_o), the output current can be written as:

$$I_{Co} \rightarrow I_o D = \left(\frac{I_{Lm1}}{1+N} - I_o\right)(1-D)\Big|_{I_{Lm1}=\frac{1}{3}I_{in}} \tag{32}$$

$$I_o = \frac{1-D}{3(1+N)}I_{\text{in}} = 0.8\ A. \tag{33}$$

OFF periods of S_1 and S_2 — The *average*currents of all diodes through the two *Modes*(II, IV) are as follows:

$$I_{D1\_avg.}(1-D) = I_{D2\_avg.}(1-D) = I_{Do\_avg.}(1-D) = I_o. \tag{34}$$

Also, the *peak* currents of all diodes can be written as:

$$\Delta i_{D1} = \Delta i_{D2} = \frac{I_{in}(1-D)}{6}, \Delta i_{Do} = \frac{I_{in}(1-D)}{3} \tag{35}$$

$$I_{D1\_peak} = I_{D2\_peak} = \frac{4+(1+N)(1-D)}{4(1-D)}I_o - \frac{\Delta i_{D1}}{2} = 2.67A \tag{36}$$

$$I_{Do\_peak} = \frac{2+(1+N)(1-D)}{2(1-D)}I_o - \frac{\Delta i_{Do}}{2} = 2.67A. \tag{37}$$

ON period of S_1 — It comprises three *Modes*(I, II, III), and the *average* current of S_1 through the current ripple (Δi_{Lm}) of the magnetizing inductor and the leakage inductor currents is as follows:

$$\Delta i_{Lm} = \Delta i_{Lm1} = \Delta i_{Lm2} = \frac{V_{in}D}{L_{m1}f_s} = 2.92A \tag{38}$$

$$I_{Lk1\_avg.}^{Mode\ I} = \left(\frac{4DI_{Lm1} - \Delta i_{Lm1}}{4D}\right)(D-0.5) = 0.85A \tag{39}$$

$$I_{in\_avg.}^{Mode\ II} = I_{in\_avg.}^{Mode\ IV} = I_{in}(1-D) = 4.8A \tag{40}$$

$$I_{Lk1\_avg.}^{Mode\ III} = \left(\frac{4DI_{Lm1} + \Delta i_{Lm1}}{4D}\right)(D-0.5) = 1.27A \tag{41}$$

$$I_{S1\_avg.} = I_{Lk1\_avg.}^{Mode\ I} + I_{in\_avg.}^{Mode\ II} + I_{Lk1\_avg.}^{Mode\ III} = 0.85 + 4.8 + 1.27 = 6.92A. \tag{42}$$

Also, the *rms* current of S_1 can be written as (43)–(45), shown at the bottom of the next page.

ON period of S_2 — It entails three *Modes*(I, III, IV), and the *average* current of S_1 through (40) and the leakage inductor currents is as follows:

$$I_{Lk2\_avg.}^{Mode\ III} = \left(I_{Lm2} - \frac{\Delta i_{Lm2}}{4D}\right)(D-0.5) = 1.9A \tag{46}$$

$$I_{Lk2\_avg.}^{Mode\ I} = \frac{(0.5\cdot\Delta i_{Lm2} + 2DI_{Lm2})(D-0.5)}{2D} = 2.34A \tag{47}$$

$$I_{S2\_avg.} = I_{Lk2\_avg.}^{Mode\ III} + I_{in\_avg.}^{Mode\ IV} + I_{Lk2\_avg.}^{Mode\ I} = 1.9 + 4.8 + 2.34 = 9.04A. \tag{48}$$

Also, the *rms* current of S_2 can be written as (49)–(51), as shown at the bottom of the next page.

ON/OFF periods of S_1 and S_2 — It comprises four *Modes*(I, II, III, IV), and through (39), (41), (46), and (47), the *average*currents of the leakage inductors can be written as:

$$I_{Lk1\_avg.}^{Mode\ II} = (I_{Lm1} + 2I_{D1})(1-D) = 3.2A \tag{52}$$

$$I_{Lk1\_avg.}^{Mode\ IV} = I_{Do}(D-0.5) = 0.534A \tag{53}$$

$$I_{Lk1\_avg.} = I_{Lk1\_avg.}^{Mode\ I} + I_{Lk1\_avg.}^{Mode\ II} + I_{Lk1\_avg.}^{Mode\ III} + I_{Lk1\_avg.}^{Mode\ IV} = 0.85 + 3.2 + 1.27 + 0.534 = 5.85A \tag{54}$$

$$I_{Lk2\_avg.}^{Mode\ II} = 2I_{D1}(1-D) = 1.6A \tag{55}$$

$$I_{Lk2\_avg.}^{Mode\ IV} = I_{Lm2} + I_{Do}(1-D) = 4A \tag{56}$$

$$I_{Lk2\_avg.} = I_{Lk2\_avg.}^{Mode\ I} + I_{Lk2\_avg.}^{Mode\ II} + I_{Lk2\_avg.}^{Mode\ III} + I_{Lk2\_avg.}^{Mode\ IV} = 2.34 + 1.6 + 1.9 + 4 = 9.84A \tag{57}$$

Also, the *rms* currents of the leakage inductors through (35), (43), (44), (49), and (50) can be written as (58)–(61), shown at the bottom of the next page.

OFF period of S_1 and S_2 — It consists of two *Modes*(II, IV), and capacitors (C_1, C_2) *rms* currents can be obtained through the diodes (D_1, D_o) currents. In addition, the ON/OFF period of switches S_1 and S_2 consists of four *Modes*(I, II, III, IV), and the capacitor (C_o) *rms* current is obtained as follows:

$$I_{C1\_rms} = I_{C2\_rms} = \sqrt{\left(I_{D1\_rms}\right)^2 + \left(I_{Do\_rms}\right)^2} = 2.08A \tag{62}$$

$$I_{Co\_rms} = \sqrt{(I_{Do} - I_o)\sqrt{1-D}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_{Do}}{(I_{Do} - I_o)}\right)^2} + I_o^2(D)} = 1.22A \tag{63}$$

D. KEY PERFORMANCE COMPARISON

Table 1 and Fig. 7 provide a performance comparison between the proposed converter and the non–isolated high step–up DC/DC converter. The converters in [8], [19], [20], [30], [40], [41], [42], [44], [45], and [46] can achieve high voltage gain (M) through coupled inductors, switched capacitors, VMC and voltage lift techniques. Moreover, it is possible to use switches and diodes with low withstand voltages by lowering the voltage stress of the semiconductor device. Through the leakage inductance energy of the coupled inductor, the soft switching performance can reduce the switching losses and alleviate the diode reverse recovery problem.

The converter in [8], [19], and [20] have high voltage gain and low voltage stress, by using the charging mode of the VMC circuit in the ON section of a single switch. Also, the D can be used in the entire range (0<D<1). However, the VMC circuit has a high component count, uses extreme duty cycles, and high input current ripple is unavoidable in the gain cell

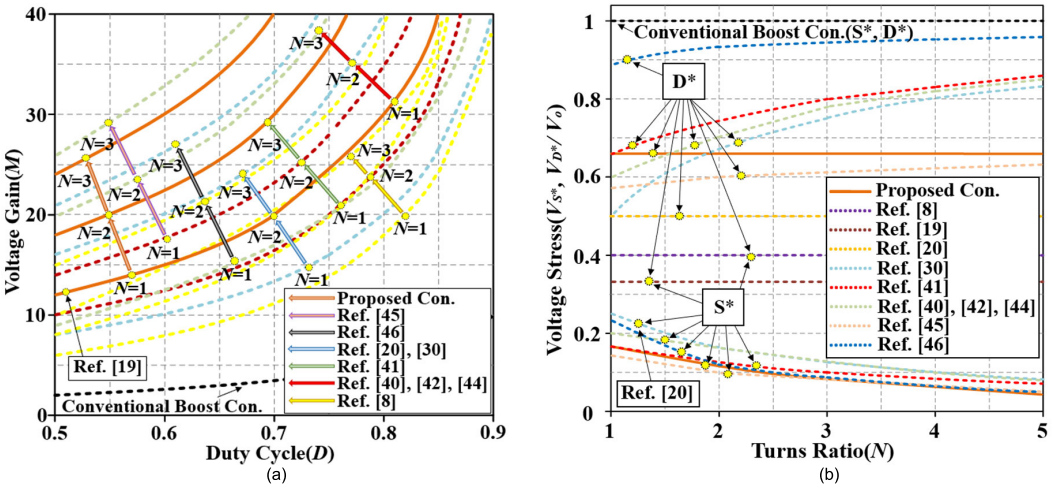


FIGURE 7. Comparison of high step-up converters. (a) M vs. D according to N; (b) voltage stress vs. N based on V_o.

and charge pump circuit connected in parallel on the input side.

The converter in [41] can achieve a high M by taking advantage of interleaved, coupled inductor, and switched

$$X_{S1}^{Mode\,I} = I_{Lm1} - \frac{\Delta i_{Lm1}}{2} + \frac{(D-0.5)\,\Delta i_{Lm1}}{2D} = 4.25A \tag{43}$$

$$Y_{S1}^{Mode\,III} = I_{Lm1} + \frac{\Delta i_{Lm1}}{2} - \frac{(D-0.5)\,\Delta i_{Lm1}}{2D} = 6.34A \tag{44}$$

$$\begin{aligned} I_{S1\_rms} &= \sqrt{\left(X_{S1}^{Mode\,I}\right)^2 (D-0.5) + (I_{in})^2\,(1-D) + \left(Y_{S1}^{Mode\,III}\right)^2 (D-0.5)} \\ &= \sqrt{4.25^2\,(0.2) + 16^2\,(0.3) + 6.34^2\,(0.2)} = 9.4A \end{aligned} \tag{45}$$

$$X_{S2}^{Mode\,III} = I_{Lm2} - \frac{\Delta i_{Lm2}}{2} + \frac{(D-0.5)\,\Delta i_{Lm2}}{2D} = 9.62A \tag{49}$$

$$Y_{S2}^{Mode\,I} = I_{Lm2} + \frac{\Delta i_{Lm2}}{2} - \frac{(D-0.5)\,\Delta i_{Lm2}}{2D} = 11.71A \tag{50}$$

$$\begin{aligned} I_{S2\_rms} &= \sqrt{\left(X_{S2}^{Mode\,III}\right)^2 (D-0.5) + (I_{in})^2\,(1-D) + \left(Y_{S2}^{Mode\,I}\right)^2 (D-0.5)} \\ &= \sqrt{9.62^2\,(0.2) + 16^2\,(0.3) + 11.71^2\,(0.2)} = 11.08A. \end{aligned} \tag{51}$$

$$Z_{S1}^{ModeII} = I_{Lm1} + 2I_{D1} = 10.67\,A \tag{58}$$

$$\begin{aligned} I_{Lk\ 1\_rms} &= \sqrt{\begin{array}{c}\left(X_{S1}^{ModeI}\right)^2 (D-0.5) + \left(Z_{S1}^{ModeII}\right)^2 (1-D) \\ + \left(Y_{S1}^{ModeIII}\right)^2 (D-0.5) + (I_{Do})^2\,(1-D)\end{array}} \\ &= \sqrt{4.25^2(0.2) + 10.67^2(0.3) + 6.34^2(0.2) + 2.67^2(0.3)} = 6.9\,A \end{aligned} \tag{59}$$

$$\begin{aligned} I_{Lk\ 2\_rms} &= \sqrt{\begin{array}{c}\left(X_{S2}^{ModeIII}\right)^2 (D-0.5) + (I_{in} - I_{Do})^2\,(1-D) \\ + \left(Y_{S2}^{ModeI}\right)^2 (D-0.5) + (2I_{D1})^2\,(1-D)\end{array}} \\ &= \sqrt{9.62^2(0.2) + 13.33^2(0.3) + 11.71^2(0.2) + 5.34^2(0.3)} = 10.15\,A \end{aligned} \tag{60}$$

$$\begin{aligned} I_{Ls\_rms} &= \sqrt{(I_{Do})^2\,(1-D) + (2I_{D1})^2\,(1-D)} \\ &= \sqrt{2.67^2(0.3) + 5.34^2(0.3)} = 3.27\,A \end{aligned} \tag{61}$$

capacitor technologies. The proposed converter has about 16% improved M compared to [41]. Moreover, the voltage stress of the switch was 20% lower and the number of key components was 6% lower.

The converter in [40], a hybrid cascade DC/DC converter is proposed that combines a coupled inductor and switched capacitor technology. The switches can achieve ZCS Turn–ON performance by utilizing the leakage inductance of the coupled inductor, and the output diodes are ZCS Turned–OFF. The converters in [30], [42], [44], [45], and [46] are high step–up converters in which a diode-capacitor circuit and a VMC are combined. These converters not only increase the M, but also reduce the current ripple, magnetic core size and switch conduction losses. In addition, the leakage energy of the coupled inductor can be recycled into the load. The proposed converter has the highest increase rate of M and the lowest increase rate of voltage stress (S∗, D∗) when the N of the coupled inductor is increases compared to [30], [42], [44], and [46]. Also, the number of components is from the maximum (33%, [45]) to the minimum (6%, [40], [42]), which will help to improve the power density of the system. The converter [45] has higher voltage gain and lower voltage stress than the proposed converter. However, the proposed converter has a low component count. Adding switches–PCB layout, gate drivers, control strategy, and DSP (coding and control) is added, hindering the power density improvement.

IV. COMPARISON AND EXPERIMENTAL RESULTS

A. DESIGN

Prototypes with V_{in} =20V, V_o =400V, P_o =320W, D ≈0.7 were manufactured and tested to verify the performance of the proposed converter. The key parameters of the experimental circuit are listed in Table 2.

L_1 and L_2 design — The coupled inductors (L_1, L_2) of the proposed converter operate in a *CCM*, and N is limited in the following manner for normal operation characteristics:

$$N = \frac{M(1-D)}{3}. \tag{64}$$

The N of the coupled inductors (L_1, L_2) is designed using M and D, and because D is greater than 0.5, the following expression can be written:

$$N \le \frac{1}{6}(M-1). \tag{65}$$

In addition, the minimum value of the magnetizing inductance (L_m) is obtained using (30) and (38), which is derived as follows:

$$L_m > \frac{V_{in}D\,(1-D)}{3\,(1+N)\,I_o f_s}. \tag{66}$$

Semiconductors S_1, S_2, D_1, D_2, and D_o can be selected using (26) and (27). The switching (ON/OFF) process can produce voltage peaks (overshoot and ringing) because the parasitic parameters of the circuit and the voltage level should be chosen to be higher than the theoretical value.

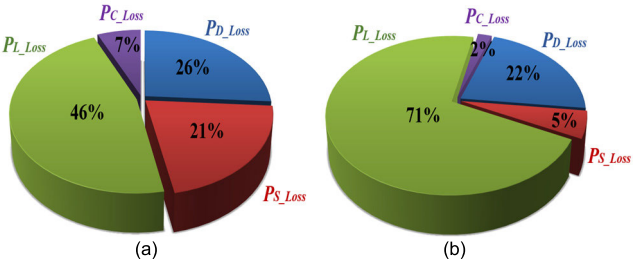


FIGURE 8. Loss breakdown of the proposed converter. (a) 320W(500Ω); (b) 75W(2000Ω).

In the proposed converter, a voltage spike problem may occur because of the resonance phenomenon through the leakage inductor and parasitic capacitor of the switch. A simple RCD snubber circuit was added to the switches to compensate for this problem.

C_1 and C_2 design — The capacitance can be designed using (22) and (24), based on V_{C1} and V_o. The switched capacitors (C_1, C_2) of the proposed converter should exhibit DC voltage clamping performance, and if the capacitance is small, resonant tanks may be formed with leakage inductance. Therefore, it should be designed such that the resonant frequency is significantly higher than the switching frequency. However, because an excessive capacitance increases the power density and cost of the system, an appropriate capacitance design is required.

$$C_1 = C_2 > \frac{I_o}{\Delta V_{C1} f_s} = \frac{P_o}{\Delta V_{C1} f_s V_o} = \frac{3P_o}{\Delta V_{C1} f_s V_o^2}. \tag{67}$$

B. LOSS BREAKDOWN

Loss analysis was conducted using four main components (diode, switch, coupled inductor, and capacitor) of the proposed prototype.

$$P_{Loss} = P_{D\_Loss} + P_{S\_Loss} + P_{L\_Loss} + P_{C\_Loss} \tag{68}$$

Based on the data used in the actual experiment, loss analysis was performed through the *average* and *rms* currents (Section III) applied to each component. Fig. 8 presents the power loss breakdown of the four main components through full load and light load power based on the proposed prototype. In the proposed prototype, most of the losses occurred in the coupled inductor because it carried a high current. Moreover, it can be observed that the semiconductor devices have reduced switching loss through ZCS Turn-ON/OFF, and the main power losses are P_{D_Loss}, P_{S_Loss}, and P_{L_Loss}.

The total loss (P_{D_Loss}) of diodes (D_1, D_2, D_o) — Based on the conduction losses ($P_{D1\_con.}$, $P_{D2\_con.}$, $P_{Do\_con.}$) and reverse recovery losses ($P_{D1\_rev.}$, $P_{D2\_rev.}$, $P_{Do\_rev.}$), it can be obtained as: (V_{FD1} =0.78V, I_{D1_avg} =0.8A)

$$\begin{aligned} P_{D\_Loss} &= P_{D1\_con.} + P_{D1\_rev.} \cdots P_{Do\_con.} + P_{Do\_rev.} \\ &\simeq V_{FD1}\left(3 \cdot I_{D1\_avg}\right) = 1.8W. \end{aligned} \tag{69}$$

TABLE 1. Performance comparison of the high step-up topologies. (n: number of cells; S∗: Switch; D∗: Diode; C∗: Capacitor; I∗: Inductor; L∗: Coupled Inductor; W∗: Windings; n: number of cells; N_1:1st-Coupled Inductor-Turn Ratio; N_2:2nd-Coupled Inductor-Turn Ratio; Se.: Sensor).

Con.	M D	Voltage stress		Ripple (Δi_{in})	No. of Component								S^* - Soft Switching	Peak Efficiency(%) V_{in}→V_o
		S^*/V_o	D^*/V_o		S*	D*	C*	I*	L*	W*	Se.	Total		
[8]	$\frac{2+2nD}{1-D}\Big\vert_{n=2,D=0.75}$ $0<D<1$	$\frac{2n+M}{(1+n)M}$		Large	2	4	6	4	-	8	1	25	-	96.8 [145W] 30V→310V
[19]	$\frac{6}{1-D}$ $0<D<1$	$\frac{1}{3}$		Large	1	7	7	3	-	6	1	25	-	94.8 [106W] 20V→400V
[20]	$\frac{2+2N}{1-D}$ $0<D<1$	$\frac{1}{2+2N}$	$\frac{1}{2}$	Large	1	4	4	-	1	2	-	12	-	96.4 [132W] 36V→400V
[30]	$\frac{2+2N}{1-D}$ $0.5\le D$	$\frac{1}{2+2N}$	$\frac{N}{1+N}$	Small	2	6	5	-	2	4	-	19	ZCS	96.5 [140W] 24V→400V
[40]	$\frac{4+2N}{1-D}$ $0.5\le D$	$\frac{1}{4+2N}$	$\frac{1+N}{2+N}$	Small	2	4	4	-	2	4	-	16	ZCS	95 [250W] 20V→400V
[41]	$\frac{3+2N}{1-D}$ $0.5\le D$	$\frac{1}{3+2N}$	$\frac{1+2N}{3+2N}$	Small	2	4	4	-	2	4	-	16	ZCS	- 16V→200V
[42]	$\frac{4+2N}{1-D}$ $0<D<1$	$\frac{1}{4+2N}$	$\frac{1+N}{2+N}$	Small	2	4	4	-	2	4	-	16	ZCS	95 [150W] 18V→300V
[44]	$\frac{4+2N}{1-D}$ $0.5\le D$	$\frac{1}{4+2N}$	$\frac{1+N}{2+N}$	Small	2	4	4	2	1	6	-	19	ZCS	95 [250W] 40V→580V
[45]	$\frac{4+3N}{1-D}$ $0.5\le D$	$\frac{1}{4+3N}$	$\frac{2+2N}{4+3N}$	Small	4	3	7	-	2	4	-	20	ZVS	97.2 [250W] 28V→460V
[46]	$\frac{1+N_1+2N_2+D}{1-D}\Big\vert_{N_1=2,N_2=1}$ $0.5\le D$	$\frac{1}{1+N_1+2N_2+D}$	$\frac{1+N_1+2N_2}{1+N_1+2N_2+D}$	Small	2	6	7	2	3	9	-	19	ZCS	94.8 [500W] 48V→800V
Pro. Con.	$\frac{3+3N}{1-D}$ $0.5\le D$	$\frac{1}{3+3N}$	$\frac{2}{3}$	Small	2	3	3	-	2	4	1	15	ZCS	96.5 [75W] 20V→400V

TABLE 2. Specifications of the proposed converter.

Components	Parameters
Input Voltage (V_{in})	20V
Output Voltage (V_o)	400V
Out Power (P_o)	320W
Switching Frequency (f_s)	80kHz
Turns Ratio (N)	1
Magnetizing inductance (L_{m1}, L_{m2})	62.24μH, 62.32μH
Leakage inductance (L_{k1}, L_{k2})	2.1μH, 2.2μH
Switches (S_1, S_2)	IRF200P222
Diodes (D_1, D_2, D_3)	RF1501
Capacitance (C_1=C_2, C_o)	4.4μF, 220μF
DSP	TMS320F28335

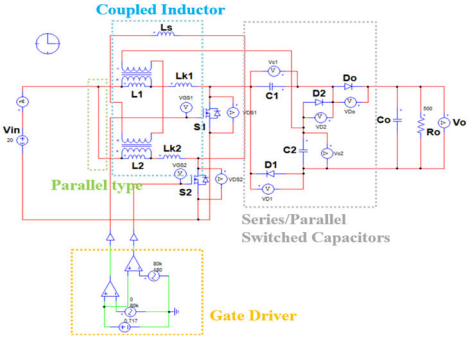


FIGURE 9. PSIM simulation schematic diagram of the proposed converter.

The total loss (P_{S_Loss}) of switches S_1 and S_2 is divided into conduction losses ($P_{S1\_con.}$, $P_{S2\_con.}$) and switching losses ($P_{S1\_sw.\_OFF}$, $P_{S2\_sw.\_OFF}$). The switches of the proposed converter have a reduced switching loss due to the ZCS Turn–ON performance, which can be obtained as follows: (R_{DS_ON} =6.6mΩ, V_{DS} =66V, I_{S1_rms} =9.4A, I_{S2_rms} =11.08A, tri=850ps, tfv=720ps, $Y_{S1}^{ModeIII}$= 6.34A,

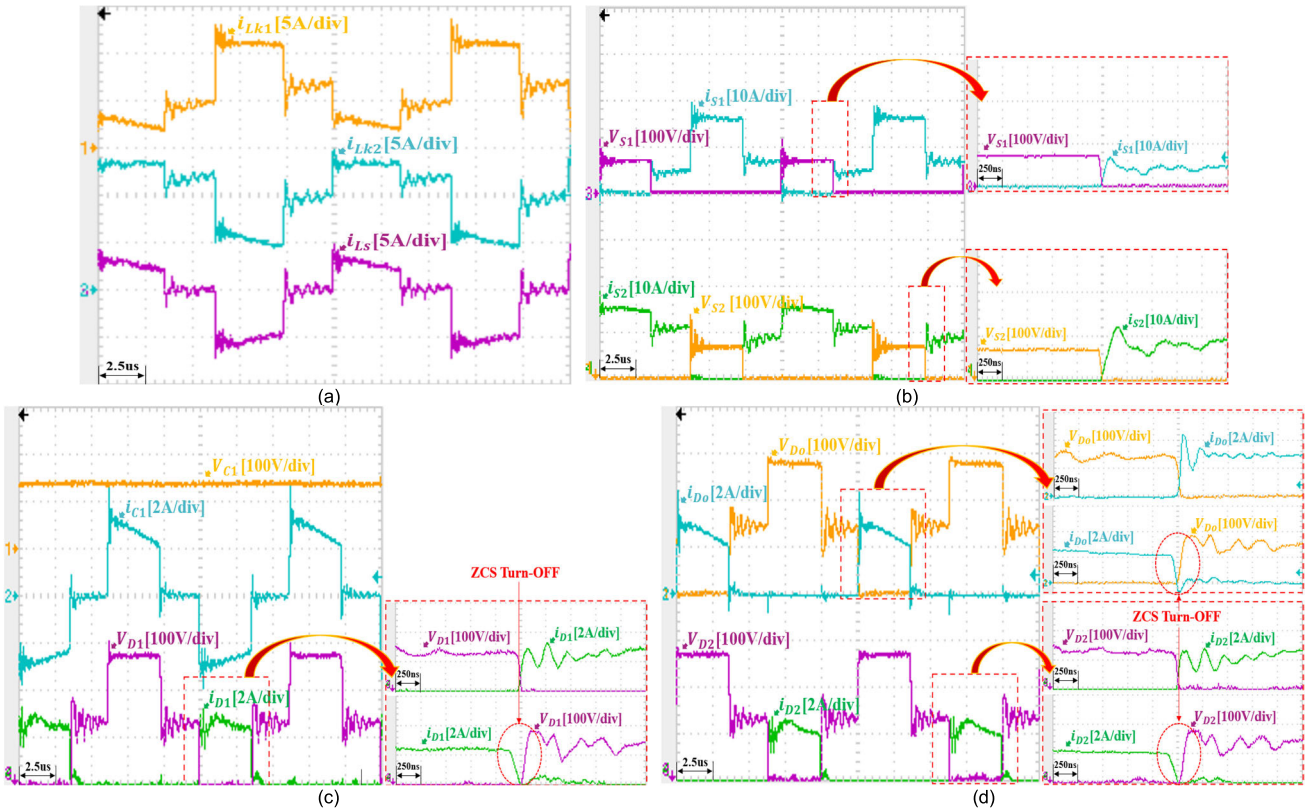


FIGURE 10. Experimental results of the proposed prototype. (a) Current waveforms of L_{k1}, L_{k2}, L_s; (b) Voltage and Current waveforms of S_1, S_2; (c) Voltage and Current waveforms of C_1, D_1; (d) Voltage and Current waveforms of D_o, D_2.

$Y_{S2}^{ModeI} = 11.71\text{A}$)

$$\begin{aligned} P_{S\_Loss} &= P_{S1\_con.} + P_{S1\_sw.\_OFF} + P_{S2\_con.} + P_{S2\_sw.\_OFF} \\ &= R_{DS\_ON}\left(I_{S1\_rms}^2 + I_{S2\_rms}^2\right) \\ &\quad + V_{DS}\frac{f_s(tri+tfv)}{2}\left(Y_{S1}^{Mode\,III} + Y_{S2}^{Mode\,I}\right) \\ &\simeq 1.5W. \end{aligned} \tag{70}$$

The losses of coupled inductors L_1 and L_2 are divided core losses (P_{L1_core}, P_{L2_core}) by core and copper losses (P_{L1_copper}, P_{L2_copper}) by winding. The core losses (P_{L1_core}, P_{L2_core}) are expressed as hysteresis losses, which can be calculated using the steinmetz equation as [49]: (k_1 =1.47, k_2 =1.44, k_3 =2.25, ΔB =0.0622Gauss, f_s =80kHz V_L =15.58cm^3)

$$P_{L1\_core} = k_1 \cdot f_s^{k_2} \cdot (\Delta B)^{k_3} \cdot V_L = 0.715W \tag{71}$$

$$P_{L1\_core} + P_{L2\_core} = 1.43W. \tag{72}$$

The copper losses (P_{L1_copper}, P_{L2_copper}) are determined through the *rms* currents of the leakage inductors (I_{Lk1}, I_{Lk2}, I_{Ls}) and the total winding series resistance (R_{dc}), which are given by: (N = 21 Turn,ρ=1.7·10^{-5}Ω·mm, MLT=56mm, r = 0.66mm, N_N =1.5Turn, I_{Lk1_rms} =6.9A, I_{Lk2_rms} =10.15A, I_{Ls_rms} =3.27A)

$$R_{dc} = \frac{N \cdot \rho \cdot MLT}{\pi \cdot r^2 \cdot N_N} = 0.0097\Omega \tag{73}$$

$$\begin{aligned} P_{L1\_copper} + P_{L2\_copper} &= \left(I_{Lk1\_rms}^2 + I_{Lk2\_rms}^2\right) R_{dc} \\ &\quad + 4\left(I_{Ls\_rms}^2 \cdot R_{dc}\right) = 1.9W. \end{aligned} \tag{74}$$

Therefore, the total loss (P_{L_Loss}) of the coupled inductors can be written as:

$$\begin{aligned} P_{L\_Loss} &= P_{L1\_core} + P_{L1\_copper} + P_{L2\_core} + P_{L2\_copper} \\ &= 3.33W. \end{aligned} \tag{75}$$

Based on the *rms* current of the capacitors and the *ESR* of the component, the total loss (P_{C_Loss}) of capacitors (C_1, C_2, C_o) can be obtained as follows: (ESR_{C1} = ESR_{C2} =7.2mΩ, ESR_{Co} =370mΩ)

$$\begin{aligned} P_{C\_Loss} &= P_{C1\_Loss} + P_{C2\_Loss} + P_{Co\_Loss} \\ &= 2 \times \left(ESR_{\_C1}/2 \times I_{C1\_rms}^2\right) \\ &\quad + \left(ESR_{\_Co} \times I_{Co\_rms}^2\right) = 0.47W. \end{aligned} \tag{76}$$

C. COMPARISON OF SIMULATION RESULTS

Table 3 shows the PSIM simulation result data of Table 1. Fig. 9 shows the schematic diagram of the simulation

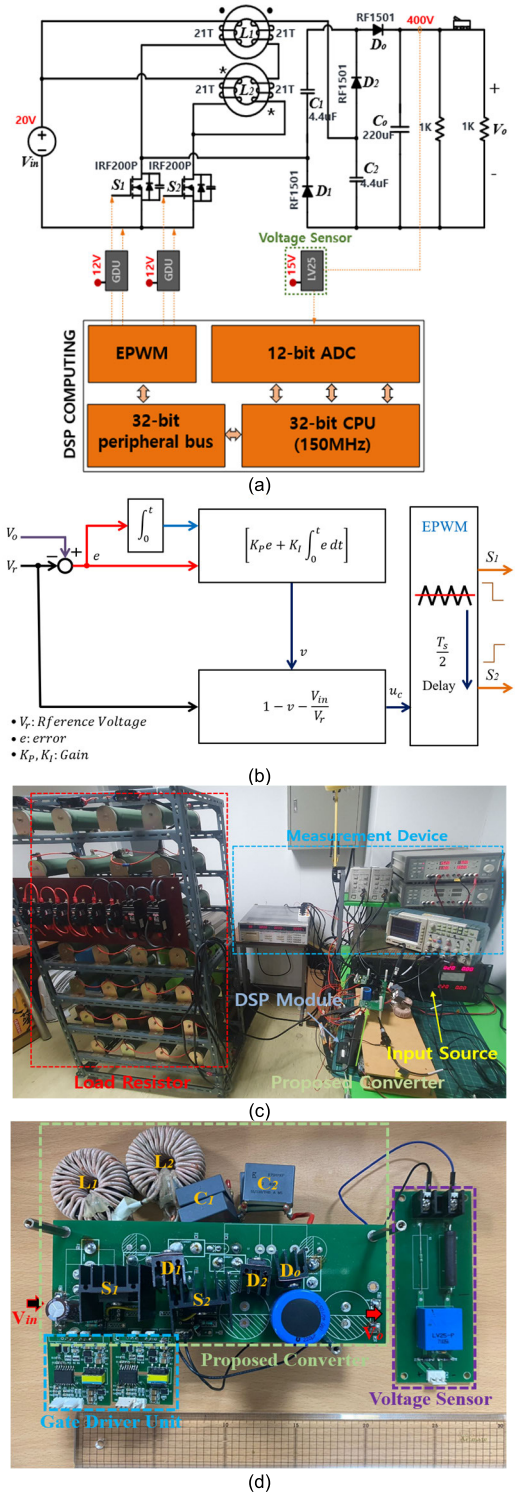


FIGURE 11. Experimental configuration of the proposed converter. (a) Circuit diagram; (b) PI control algorithm block diagram; (c) Device and equipment photos; (d) Prototype photo.

of the proposed converter, and by performing simulations based on the same parameters (V_{in} =20V, V_o =400V, P_o =320W, f_s =80kHz, N = 1, L_{m1} = L_{m2} =100μH, R_{DS_ON} =5.3mΩ, tri=850ps, tfv=720ps, V_{FD1} =0.78V),

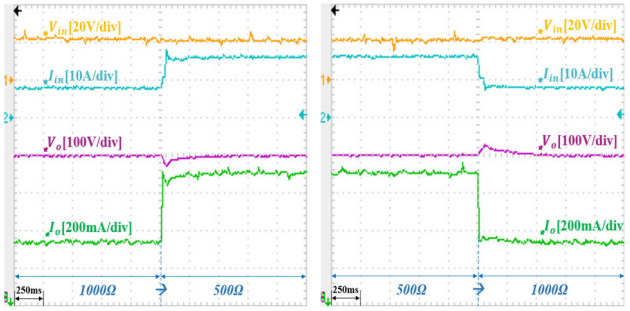


FIGURE 12. Transient response characteristics: R_o (1000Ω → 500 Ω → 1000Ω) fluctuation.

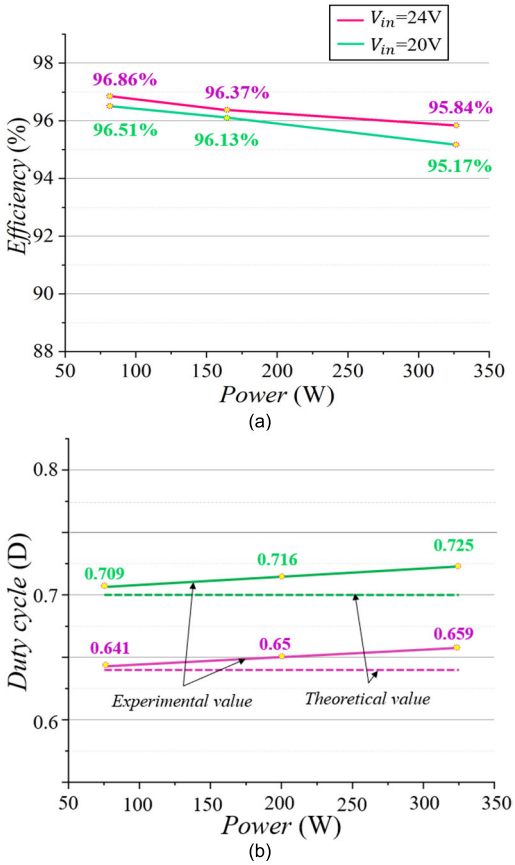


FIGURE 13. Experimental measurement data [CCM]. (a) Efficiency vs. Power; (b) Duty cycle vs. Power.

it was confirmed that the duty ratio (D), switch voltage stress, and input current ripple (Δi_{in}) were similar to the theoretical data values. In [8], [19], and [20] can obtain high voltage gain (M) through the ON operation period of a single switch and the VMC circuit. However, since the input current ripple is large, it is not suitable for high power systems. The proposed converter has small input current ripple (Δi_{in}) and low voltage stress, low number of components, high power density, and low loss rate in semiconductor devices.

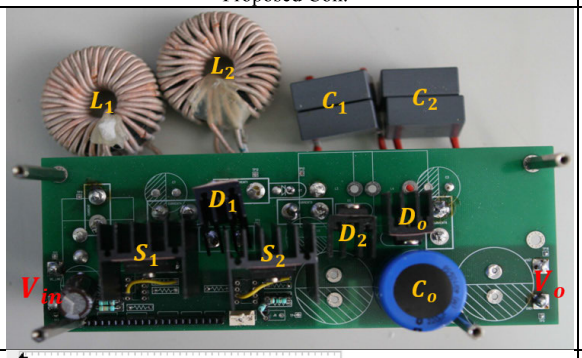
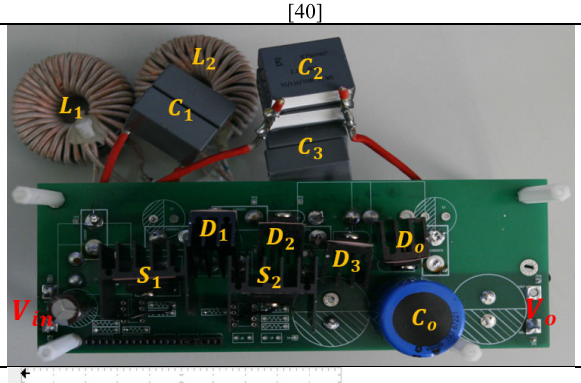
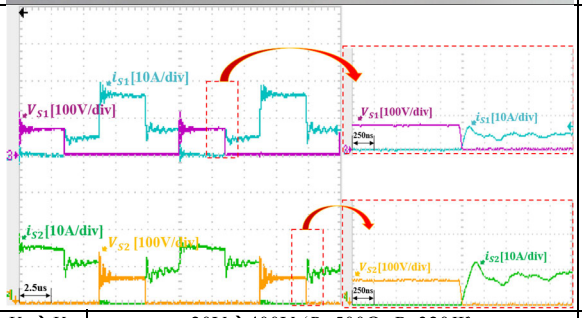
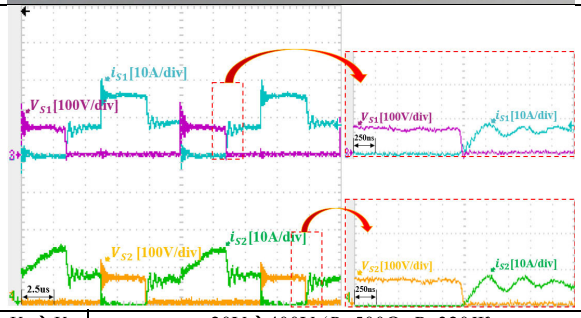
D. EXPERIMENTAL WAVEFORMS

To validate the performance of the proposed converter, a 320W prototype was built and tested based on the parameters

TABLE 3. Simulation comparison of the high step-up topologies. (S∗: Switch; D∗: Diode).

Topologies	Duty cycle(D)	Δi_{in}(A)	Semiconductor Device					
			S*				D*	
			rms(A)	Turn–ON/OFF(A)	V_{DS}(V)	Loss(W)	*average* current(A)	Loss(W)
[8]	0.77	11	19.2, 1.7	26, 21, 1.8	158, 158	2.4	0.84, 0.84, 9, 9	15.3
[19]	0.73	19	33	31, 31	136	6.2	0.7, 0.77, 0.79, 0.79, 12, 12, 2.1	22.7
[20]	0.81	23	17.8	15, 23.1	100	1.9	0.78, 0.79, 0.8, 0.8	2.4
[30]	0.81	1.5	9.2, 9.2	9.1	101, 101	1.1	0.38, 0.39, 0.4, 0.4, 0.83, 0.83	2.5
[40]	0.71	1.3	9.3, 10.4	9.1, 9.1	73, 73	1.2	0.78, 0.8, 0.81, 0.81	2.4
[41]	0.76	1	8.1, 11	8.3, 10.8	81, 81	1.2	0.78, 0.81, 0.82, 0.82	2.5
[42]	0.72	1.1	9.2, 10.4	9.1, 9.1	76, 76	1.2	0.77, 0.8, 0.81, 0.81	2.4
[44]	0.71	1.1	9.4, 10.5	9.3, 9.3	71, 71	1.3	0.39, 0.41, 0.41, 0.41	1.2
[45]	0.66	0.8	9.5, 11, 2.3, 1.6	17.6, 18	58, 58	1.4	0.76, 0.84, 0.8	1.8
[46]	0.77	1.2	8.9, 8.9	9.7, 9.7	60, 60	1	0.43, 0.43, 0.4, 0.4, 0.41, 0.41	1.9
Pro. Con.	0.71	1	9.7, 11.6	6.4, 12.1	68, 68	1.5	0.8, 0.8, 0.79	1.8

TABLE 4. Comparison of Characteristics Between Similar Topologies. z (W: Width, D: Depth, H: Height, R: Radius).

Topologies	Proposed Con.				[40]			
Circuit board								
Experiment (S_1, S_2)								
Parameters	V_{in}→V_o	20V→400V (R_o:500Ω, P_o:320W)			V_{in}→V_o	20V→400V (R_o:500Ω, P_o:320W)		
Component	S*	IRF200P222×2 (200V, 5.3mΩ)	W·D·H×2 (15·5·36×2)	5400mm^3	S*	IRF200P222×2 (200V, 5.3mΩ)	W·D·H×2 (15·5·36×2)	5400mm^3
	D*	RF1501×3 (300V, 1.35V)	W·D·H×3 (10·4·29×3)	3480mm^3	D*	RF1501×4 (300V, 1.35V)	W·D·H×4 (10·4·29×4)	4640mm^3
	C*	R75MR422050×4	W·D·H×4 (32·13·25×4)	41600mm^3	C*	R75MR422050×6	W·D·H×6 (32·13·25×6)	62400mm^3
		MAL219367221E3	R^2·π·H (15^2· π ·35)	24727mm^3		MAL219367221E3	R^2·π·H (15^2· π ·35)	24727mm^3
	L*	OD468125×2	R^2·π·H×2 (23^2·π·15×2)	49831mm^3	L*	OD468125×2	R^2·π·H×2 (23^2·π·15×2)	49831mm^3
Total volume	S*+ D*+ C*+ L*			125038mm^3	S*+ D*+ C*+ L*			146998mm^3

listed in Table 2. Fig. 10(a) illustrates the currents in L_{k1}, L_{k2}, and L_s of the coupled inductors (L_1, L_2). It can be observed that they operate in an interleaved manner, which is identical to the key waveforms of the operating principle. Therefore, the input-side coupled inductors (L_1, L_2) are connected in parallel to further reduce the input current ripple through a 180 ° phase operation.

Fig. 10(b) depicts the voltage and current stress waveforms of S_1 and S_2. The D values of S_1 and S_2 are approximately 0.7 and the steady-state voltage stresses are approximately 66V, which is much less than V_o. Therefore, it can be confirmed that M can be increased without extreme D. Additionally, as the leakage inductor limits the rate of change of current, the current in the switch gradually increases when the switch is Turned–ON, which helps to significantly reduce switching losses. It was confirmed that the conduction loss and switching loss can be lowered by using low voltage–rated MOSFETs with low ON–resistance along with the partial ZCS Turn–ON performance of S_1 and S_2.

Fig. 10(c) and 10(d) show the voltage and current waveforms of D_1, D_2, D_o and C_1, which are identical to the key waveforms of the operating principle. The diodes are approximately 266V, which is much lower than V_o, and their current drop rate is controlled by the leakage inductor to Turn–OFF the ZCS. It can be observed that the reverse recovery current is significantly reduced and the EMI performance of the proposed topology can be enhanced [43]. The capacitors (C_1, C_2) were charged for the same amount of time, and the clamping voltage was 133V, which corresponds to (27) at one–third of V_o.

Fig. 11(a) depicts the experimental setup including the proposed converter and DSP control circuit. The input side supplied V_{in} through two power supplies (200V/10A), and the output side had a resistance of 500Ω (320W) due to a load resistance of 1000Ω connected in parallel. Furthermore, the two switches generate PWM gate signals using a DSP TMS320F28335 chip from Texas Instruments, and these signals are applied to MOSFETs through gate driver units (GDUs). DSP TMS320F28335 chip is a C28X Core 32[bit] FPU, which enables high–speed processing of decimal data and has a processing capacity of 150[MHz]. The ADC circuit can be sampled with 16 channels, 12.5MSPS, and the analog input range is 0∼3[V]. Voltage sensor (LV–25) has a maximum voltage of 500V. For the sensor, DSP ADC circuit distributed 3V through a resistor divider. The coupled inductors connected in parallel with the input side were wound around the toroidal core (OD468125) using four windings. Fig. 11(b) depicts the control algorithm of the proposed converter, which senses V_o and performs output constant voltage through PI (Proportional–Integral) control algorithm. Fig. 11(c) and Fig. 11(d) are photographs of the experimental equipment used in the experiment, the measuring device, and the proposed converter prototype.

Fig. 12 illustrates the transient response according to the load resistance (R_o) 1000Ω →500Ω →1000Ω. Fig. 13(a) is the measurement data of the efficiency according to the load of the proposed converter based on *CCM*. It is calculated by measuring the voltage/current of the input/output using a power analyzer. When the V_{in} is 24V, the maximum efficiency is 96.86% and the *average* efficiency is 96.35%. When the V_{in} is 20V, the maximum efficiency is 96.51% and the *average* efficiency is 95.9%. Fig. 13(b) depicts the theoretical duty cycle value and the duty cycle value applied to the experiment. As the power increases, the duty cycle increases linearly.

In Table 1, the topology with the most similar characteristics to the proposed converter was experimentally verified in Table 4. The proposed converter and in [40] have the same voltage gain (M) and voltage stress as the semiconductor device, and the circuit is configured using the same PCB board. Moreover, the characteristics were confirmed through the same parameters (V_{in} =20V, V_o =400V, I_{in} =16A, I_o =0.8A, $D = 0.7$, f_s =80kHz, $N = 1$, $L_{m1} = L_{m2}$ =62μH, R_o =500Ω, P_o =320W). Similar topologies confirmed the ZCS Turn–ON switching performance of the switches and the ZCS Turn–OFF performance of the diodes. The proposed converter exhibited a power density improvement of 14%.

V. CONCLUSION

This study proposes a high density–high step–up interleaved DC/DC converter applicable to sustainable energy applications. The proposed converter takes a simple form, with two coupled inductors and passive elements added without requiring an additional winding method or bulky and heavy transformer. In this study, the interleaved method is used to combine coupled inductor and switched capacitor technologies, achieving high step–up voltage gain with low current ripple, increased power density, and reduced voltage stress of semiconductor devices. During the alternating OFF mode of the switches, the coupled inductors and switched capacitors are charged in parallel or discharged in series to deliver power to the output side. This design achieves a high voltage gain and low voltage stress of the semiconductor device, making it possible to select low voltage–rated MOSFETs with low ON–state resistance. As a result, conduction losses and cost are reduced, leading to improved efficiency. Moreover, the efficiency is enhanced by utilizing the leakage inductor energy of the coupled inductor to realize the ZCS Turn–ON/OFF of the semiconductor device. Finally, the proposed converter was verified by implementing and comparing prototypes in the laboratory and a maximum efficiency of 96.86% was obtained.

REFERENCES

[1] *Transforming Our World: The 2030 Agenda for Sustainable Development*, UN Gen. Assembly, New York, NY, USA, 2015.

[2] J. Wu, S. Guo, H. Huang, W. Liu, and Y. Xiang, "Information and communications technologies for sustainable development goals: State-of-the-art, needs and perspectives," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 3, pp. 2389–2406, 3rd Quart., 2018.

[3] M. H. Todorovic, L. Palma, and P. N. Enjeti, "Design of a wide input range DC–DC converter with a robust power control scheme suitable for fuel cell power conversion," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1247–1255, Mar. 2008.

[4] Y. Zheng, B. Brown, W. Xie, S. Li, and K. Smedley, "High step-up DC–DC converter with zero voltage switching and low input current ripple," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9416–9429, Sep. 2020.

[5] O. Ellabban, H. Abu-Rub, and F. Blaabjerg, "Renewable energy resources: Current status, future prospects and their enabling technology," *Renew. Sustain. Energy Rev.*, vol. 39, pp. 748–764, Nov. 2014.

[6] M. Islam, S. Mekhilef, and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," *Renew. Sustain. Energy Rev.*, vol. 45, pp. 69–86, May 2015.

[7] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-efficiency high step-up DC–DC converter with dual coupled inductors for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5967–5982, Jul. 2018.

[8] H. Pourfarzad, M. Saremi, and T. Jalilzadeh, "An extended high-voltage-gain DC–DC converter with reduced voltage stress on switches/diodes," *Electr. Eng.*, vol. 102, no. 4, pp. 2435–2452, Jun. 2020.

[9] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.

[10] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano, and A. Rufer, "Design and control of a modular multilevel DC/DC converter for regenerative applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3970–3979, Aug. 2013.

[11] X. Zhang and T. C. Green, "The modular multilevel converter for high step-up ratio DC–DC conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015.

[12] Y. Hu, R. Zeng, W. Cao, J. Zhang, and S. J. Finney, "Design of a modular, high step-up ratio DC–DC converter for HVDC applications integrating offshore wind power," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2190–2202, Apr. 2016.

[13] F. L. Luo and H. Ye, "Positive output cascade boost converters," *IEE Proc.-Electr. Power Appl.*, vol. 151, no. 5, pp. 590–606, Sep. 2004.

[14] R. J. Wai and R. Y. Duan, "High-efficiency DC/DC converter with high voltage gain," *IEE Proc.-Electr. Power Appl.*, vol. 152, no. 4, pp. 793–802, Jul. 2005.

[15] S. D. Johnson, A. F. Witulski, and R. W. Erickson, "Comparison of resonant topologies in high-voltage DC applications," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 24, no. 3, pp. 263–274, May 1988.

[16] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.

[17] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC–DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[18] R.-J. Wai and R.-Y. Duan, "High step-up converter with coupled-inductor," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1025–1035, Sep. 2005.

[19] R.-J. Wai, C.-Y. Lin, R.-Y. Duan, and Y.-R. Chang, "High-efficiency DC–DC converter with high voltage gain and reduced switch stress," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 354–364, Feb. 2007.

[20] Y.-P. Hsieh, J.-F. Chen, T.-J. Liang, and L.-S. Yang, "Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.

[21] T. Jalilzadeh, N. Rostami, E. Babaei, and M. Maalandish, "Ultra-step-up DC–DC converter with low-voltage stress on devices," *IET Power Electron.*, vol. 12, no. 3, pp. 345–357, Mar. 2019.

[22] Y. Ye, S. Chen, and Y. Yi, "Switched-capacitor and coupled-inductor-based high step-up converter with improved voltage gain," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 754–764, Feb. 2021.

[23] Y. Zheng and K. M. Smedley, "Analysis and design of a single-switch high step-up coupled-inductor boost converter," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 535–545, Jan. 2020.

[24] K. Kanathipan, R. Emamalipour, and J. Lam, "A single-switch high-gain PV microconverter with low-switch-voltage-to-high-voltage-bus ratio," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9530–9540, Sep. 2020.

[25] S. B. Santra, D. Chatterjee, Y. P. Siwakoti, and F. Blaabjerg, "Generalized switch current stress reduction technique for coupled-inductor-based single-switch high step-up boost converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1863–1875, Apr. 2021.

[26] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 689–704, Jun. 2016.

[27] W. Li and X. He, "Review of nonisolated high-step-Up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[28] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[29] G. A. L. Henn, R. N. A. L. Silva, P. P. Praça, L. H. S. C. Barreto, and D. S. Oliveira, "Interleaved-boost converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2753–2761, Nov. 2010.

[30] K.-C. Tseng, C.-C. Huang, and W.-Y. Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3047–3057, Jun. 2013.

[31] K.-C. Tseng and C.-C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1311–1319, Mar. 2014.

[32] K.-C. Tseng, J.-Z. Chen, J.-T. Lin, C.-C. Huang, and T.-H. Yen, "High step-up interleaved forward-flyback boost converter with three-winding coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4696–4703, Sep. 2015.

[33] T. Nouri, N. Nouri, and N. Vosoughi, "A novel high step-up high efficiency interleaved DC–DC converter with coupled inductor and built-in transformer for renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6505–6516, Aug. 2020.

[34] M. Y. Hassani, M. Maalandish, and S. H. Hosseini, "A new single-input multioutput interleaved high step-up DC–DC converter for sustainable energy applications," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1544–1552, Feb. 2021.

[35] Y. Zhao, X. Xiang, W. Li, X. He, and C. Xia, "Advanced symmetrical voltage quadrupler rectifiers for high step-up and high output-voltage converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1622–1631, Apr. 2013.

[36] B. Akhlaghi, N. Molavi, M. Fekri, and H. Farzanehfard, "High step-up interleaved ZVT converter with low voltage stress and automatic current sharing," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 291–299, Jan. 2018.

[37] H. Moradisizkoohi, N. Elsayad, and O. A. Mohammed, "An integrated interleaved ultrahigh step-up DC–DC converter using dual cross-coupled inductors with built-in input current balancing for electric vehicles," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 644–657, Mar. 2020.

[38] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2397–2408, Sep. 2010.

[39] S.-W. Seo, D.-K. Lim, and H. H. Choi, "High step-up interleaved converter mixed with magnetic coupling and voltage lift," *IEEE Access*, vol. 8, pp. 72768–72780, 2020.

[40] Y. Zheng, W. Xie, and K. M. Smedley, "Interleaved high step-up converter with coupled inductors," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6478–6488, Jul. 2019.

[41] X. Hu, G. Dai, L. Wang, and C. Gong, "A three-state switching boost converter mixed with magnetic coupling and voltage multiplier techniques for high gain conversion," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2991–3001, Apr. 2016.

[42] X. Hu, P. Ma, J. Wang, and G. Tan, "A hybrid cascaded DC–DC boost converter with ripple reduction and large conversion ratio," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 761–770, Mar. 2020.

[43] K. Mainali and R. Oruganti, "Conducted EMI mitigation techniques for switch-mode power converters: A survey," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2344–2356, Sep. 2010.

[44] T. Nouri, N. V. Kurdkandi, and M. Shaneh, "A novel interleaved high step-up converter with built-in transformer voltage multiplier cell," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4988–4999, Jun. 2021.

[45] J. Semiromizadeh, E. Adib, and H. Izadi, "A ZVS high step-up DC–DC converter for renewable energy systems with simple gate drive requirements," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11253–11261, Nov. 2022.

[46] M. F. Guepfrih, G. Waltrich, and T. B. Lazzarin, "Unidirectional step-up DC–DC converter based on interleaved phases, coupled inductors, built-in transformer, and voltage multiplier cells," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2385–2395, Mar. 2023.

[47] J.-S. Kim, J.-M. Kwon, and B.-H. Kwon, "High-efficiency two-stage three-level grid-connected photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2368–2377, Mar. 2018.
[48] S. K. Kuncham, K. Annamalai, and N. Subrahmanyam, "A two-stage T-type hybrid five-level transformerless inverter for PV applications," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9510–9521, Sep. 2020.
[49] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1055–1061, 2001.

SANG-WHA SEO received the B.S. degree in electronic engineering from Seokyeong University, Seoul, South Korea, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from Dongguk University, Seoul, in 2010 and 2017, respectively. From 2019 to 2022, he was a Postdoctoral Researcher with the Propulsion System Research Team, Korea Railroad Research Institute, Uiwang-si, South Korea. In 2023, he joined the Future Automobile Innovation Education Center, Dankook University, Yongin-si, South Korea.

JOON-HYOUNG RYU was born in Anyang, South Korea, in 1972. He received the B.S., M.S., and Ph.D. degrees in control and instrumentation engineering and electronics engineering from Ajou University, Suwon-si, South Korea, in 1997, 1999, and 2005, respectively. He is currently a Principal Researcher with the Propulsion System Research Team, Korea Railroad Research Institute. His research interests include railway propulsion systems, power electronics, and hydrogen-powered railway systems.

HAN HO CHOI received the B.S. degree in control and instrumentation engineering from SNU, Seoul, South Korea, in 1988, and the M.S. and Ph.D. degrees in electrical engineering from KAIST, in 1990 and 1994, respectively. He is currently with the Division of EEE, Dongguk University, Seoul.

JAE-BUM LEE received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2010, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2012 and 2016, respectively. He was a Senior Researcher with the Korea Railroad Research Institute, Uiwang-si, South Korea, from 2016 to 2019. He is currently an Associate Professor with the Korea National University of Transportation, Uiwang-si. His research interests include high-voltage/power transformer design, high-efficiency ac/dc and dc/dc converters, and digital control method in high-power vehicles, such as electric vehicles and rolling stock and medium power, such as electronic equipment.