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RESEARCH ARTICLE

Experimental Characterization and Electro-Thermal Modeling of Double Side Cooled SiC MOSFETs for Accurate and Rapid Power Converter Simulations

PIERPAOLO DINI[1], SERGIO SAPONARA[1], (Senior Member, IEEE), SAJIB CHAKRABORTY[2,3], (Member, IEEE), FARZAD HOSSEINABADI[2,3], AND OMAR HEGAZY[2,3], (Senior Member, IEEE)

[1]Department of Information Engineering, University of Pisa, 56122 Pisa, Italy
[2]MOBI-EPOWERS Research Group, ETEC Department, Vrije Universiteit Brussel (VUB), 1050 Brussel, Belgium
[3]Flanders Make, 3001 Heverlee, Belgium

Corresponding author: Pierpaolo Dini (pierpaolo.dini@phd.unipi.it)

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ABSTRACT The paper presents a precise and efficient model of Double-Side Cooled (DSC) SiC MOSFET, which incorporates the dynamics of both electrical and thermal variables. It offers a suitable computational complexity for simulating transients in complex power converters. The objective is to define a model that enables multi-scale time simulations and facilitates rapid power converter design in system-level tools such as Simulink. Additionally, the model aims to achieve simulation accuracy comparable to device-level models for the next generation of SiC MOSFETs. The paper demonstrates the complete test bench measurement procedure for the device. This procedure is essential for experimentally extrapolating the intrinsic characteristics and developing a model-reduction approach based on electro-thermal modeling. The approach strikes a balance between computational complexity and level of detail. The proposed model has been seamlessly integrated into Simulink to simulate a 3-phase inverter for several grid cycles at the grid frequency. To evaluate the model's validity, the predicted inverter performance is compared with experimental measurements. These simulations require significantly less time compared to those based on LTspice models.

INDEX TERMS Model-based design, multi-scale, simulation, power measures, power converters, silicon carbide (SiC).

ABBREVIATION TABLE

Acronym/Abbreviation	Meaning
SiC	Silicon-Carbide.
Si3N4	Silicon-Nitride.
DSC	Double-Side-Cooled.
SPT	Single-Pulse-Test.
DPT	Double-Pulse-Test.
DUT	Device-Under-Test.
FPGA	Field-Programmable-Gate-Array.
LUT	Look-Up-Table.
RMS	Root-Mean.Square.
STD	Standard Deviation.
RMSE	Root-Mean-Square-Error.
PWM	Pulse-Width-Modulation.
GaN	Gallium Nitride.
HEMT	High-Electron-Mobility-Transistor
FET	Field-Effect-Transistor.

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I. INTRODUCTION

A. MOTIVATIONS

In recent years, there has been an increasing demand for high-efficiency power electronics systems, particularly for electric and hybrid vehicles. Firstly, energy efficiency has become an increasingly important factor in the design of power electronic devices. Due to the rising demand for electricity, energy efficiency has become a priority in many sectors, including industry, transportation, and computing. High-efficiency devices can reduce operating costs and improve system reliability, contributing to the reduction of CO2 emissions and environmental sustainability. Furthermore, semiconductor technology has advanced significantly in recent years, enabling the production of high-efficiency devices at increasingly lower costs. In particular, silicon (Si) and silicon carbide (SiC) semiconductor device technology has made great strides, making available devices with efficiencies above 98%. These devices also offer other advantages, such as greater robustness, faster switching speeds, and higher power density. One of the key components in such systems is the power switching device, and silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have emerged as a promising solution for this application due to their high power density and high-temperature operation capabilities [1], [2]. However, the design and optimization of power electronics systems that utilize SiC MOSFETs requires a detailed understanding of the device's behavior under different operating conditions, exploiting mathematical modeling. Firstly, SiC MOSFET devices are high-power semiconductor devices that operate under extreme conditions, such as high temperature and high voltage. These operating conditions can be difficult to replicate experimentally and often require expensive and specialized equipment. Therefore, numerical simulation can be a more economical and efficient alternative for analyzing the behavior of the device under these extreme operating conditions. Furthermore, mathematical models of SiC MOSFET devices are capable of providing detailed information on device behavior, such as the distribution of electric fields within the device, current distribution, and power dissipation. This information can be used to better understand device operation and to optimize device design for improved performance. Finally, mathematical models of SiC MOSFETs can be used to analyze device behavior quickly and efficiently over a wide range of operating conditions, which would be impossible or too costly to perform experimentally. This allows engineers to design devices with optimized performance and to identify any design issues before physically producing the devices themselves. In summary, the use of mathematical models to simulate the behavior of SiC MOSFET devices is important and sometimes essential in the design and optimization of these devices, as it allows for analysis of device behavior under extreme operating conditions, provides detailed information on device operation, and allows for rapid and efficient identification of any design issues. This is where the use of an electro-thermal model of the SiC MOSFET comes in. Such a model can provide a comprehensive and accurate simulation of the device's behavior, allowing for the prediction of its performance under different thermal and electrical conditions. The use of an electro-thermal model of a SiC MOSFET in the design and optimization of in-vehicle power electronics systems can provide several benefits. For example, it can be used to estimate the power loss in the device, which is important for the design of power electronic circuits, and to optimize the design of the device for specific applications such as reducing switching losses or increasing the efficiency of the circuit. Additionally, the use of a model developed in MATLAB/Simulink, a widely used simulation tool in the field of power electronics [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], allows for easy integration with other models and simulations, providing higher compatibility and flexibility, respect to other SW, often adopted in application of modeling single components of power electronics system. In summary, the development of an electro-thermal model of a SiC MOSFET in MATLAB/Simulink for in-vehicle power electronics can provide a powerful tool to analyze and optimize the performance of high-power systems, allowing for the design of efficient and reliable systems that can operate under high temperatures and high power density conditions.

B. STATE OF THE ART OVERVIEW

Recent research in modeling electro-thermal behavior in SiC MOSFETs aimed to provide a comprehensive and accurate simulation of the device's behavior under different operating conditions. However, several limitations still exist that can make it difficult to model SiC MOSFETs accurately. One of the main limitations is the complexity of the SiC MOSFET electro-thermal behavior [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. The behavior is multi-physics in nature and the effects of temperature, parasitic elements, device degradation, and the manufacturing process are difficult to model accurately. Additionally, the availability of experimental data for SiC MOSFETs is limited, which can make it difficult to validate models and extract device parameters [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35]. Another limitation is the scalability of the models. Many models developed for SiC MOSFETs are based on specific device geometries and operating conditions, and may not be easily scalable to other devices or conditions. Furthermore, many models developed for SiC MOSFETs are specific to a particular simulation tool or platform, and may not be easily portable to other tools or platforms [36], [37], [38], [39], [40]. Additionally, the temperature dependence of SiC MOSFETs is unique,and SiC MOSFETs are susceptible to degradation mechanisms such as dielectric breakdown and some models may not be able to take into account the effects of these mechanisms. In addition, the impact of package and interconnects on the device's behavior, and the impact of the manufacturing process spread on the device's behavior is not always considered in the models [18], [29],

[41], [42], [43], [44], [45], [46], [47], [48], [49], [50]. Possible packaging options for SiC MOSFETs in vehicle power electronics applications include plastic packages, ceramic packages, direct bond copper (DBC) packages, silicon nitride (Si3N4) packages, and metal-ceramic packages. The choice of packaging depends on various factors, such as cost, thermal performance, mechanical strength, and environmental factors. Double-sided cooling is another packaging technique that can be an effective option for high-power applications. It involves mounting a power semiconductor device on a substrate that has cooling channels on both sides. Double-sided cooling can help reduce the overall size and weight of the power electronics system while increasing reliability and lifespan, but it can be more complex and expensive to implement compared to other packaging options, and it requires additional design considerations [51], [52], [53], [54].

C. CONTRIBUTIONS

An innovative contribution of our work is that we have characterized a device not yet on the market, of which the datasheet is not present. This is why a whole section dedicated to experimental measurements is needed, followed by a section where the model is compared with the experimental data. In fact, our work first shows the characterization phase, followed by our analysis for modeling with reduced computational complexity, which is the other innovation aspect of our article which allows the insertion of the SiC model within the converter model as the simulation times allow the analysis of multiple switching cycles in a few minutes. The simulation times found within the converter model are in fact considerably reduced. The key point lies in having elaborated a model with a rather high degree of detail with reduced computational complexity starting from experimental measurements, combining algebraic relationships and LUTs to avoid differential/recursive ones. Furthermore, it is shown that it can also be retrofitted with minimal effort to GaN technology. Summarizing, the proposed article makes significant contributions in the development of an electro-thermal model for SiC switches in power converters, offering comparable accuracy to physics-level models while ensuring suitable simulation time and parameter complexity for Simulink-based power converter control. These contributions include comprehensive experimental characterization of the SiC MOSFET device's electrical and thermal behavior, a methodology for complexity reduction based on an analytical model combined with experimental data, an accurate analysis of model accuracy and reduced simulation times compared to existing literature, and the use of the electro-thermal model for precise evaluation of losses and converter efficiency in three-phase inverters. Section II presents experimental measurements conducted on DSC-based SiC MOSFETs for device characterization and electro-thermal model development. Section III outlines a model reduction workflow that strikes a balance between computational complexity and level of detail. Section IV demonstrates the performance of the electro-thermal model in a 3-phase inverter simulation within a Simulink environment, comparing it to experimental measurements. Section V deals with extension of the work to GaN power switch modeling. Conclusions are presented in Section VI.

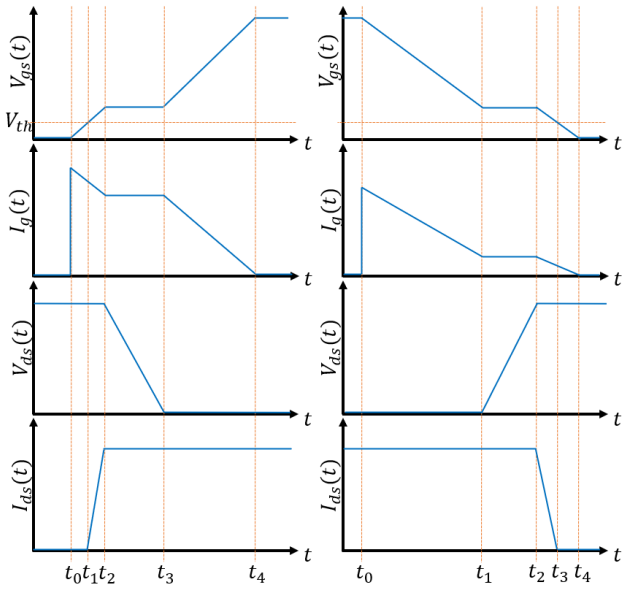


FIGURE 1. Schematic representation of turn-on/off transients modeling.

TABLE 1. Relevant instants in turn-on and turn-off transients.

Turn-on	Turn-off
$t_2(V_{ds})$ - 0.20 μs	$t_1(V_{ds})$ - 36.44 μs
$t_3(V_{ds})$ - 4.16 μs	$t_2(V_{ds})$ - 40.96 μs
$t_3(V_{gs})$ - 2.56 μs	$t_2(V_{ds})$ - 38.08 μs
$t_1(I_{ds})$ - 1.04 μs	$t_2(I_{ds})$ - 37.36 μs

TABLE 2. Delays between measured relevant signals.

delay($V_{gs} - I_{ds}$)	delay($V_{ds} - V_{gs}$)	delay($V_{ds} - I_{ds}$)
0.72μs	2.88μs	3.60μs

II. EXPERIMENTAL CHARACTERIZATION

With reference to a new family of SiC MOSFET by Infineon, this Section shows the following experimental measures carried out to extract key device figures to develop bottom-up the electro-thermal model. Dual Pulse Tests (DPT), characterization of threshold voltage, $R-I$ and $I-V$ curves, turn-on and turn-off transient tests, characterization of body-diode and parasitic capacitor and stray inductance and gate resistance, static and dynamic thermal measurements. The focus is on hybrid vehicles and full-electric light vehicles and hence the considered voltage and power ranges are: V_{dc} of 150 V and output power between 5 and 40 kW. The measurement activity is needed in case of devices, such this new SiC MOSFETs, missing a data sheet with detailed characterization. If the following characteristics are available in a device data sheet the proposed method can be applied by directly moving to the Section III.

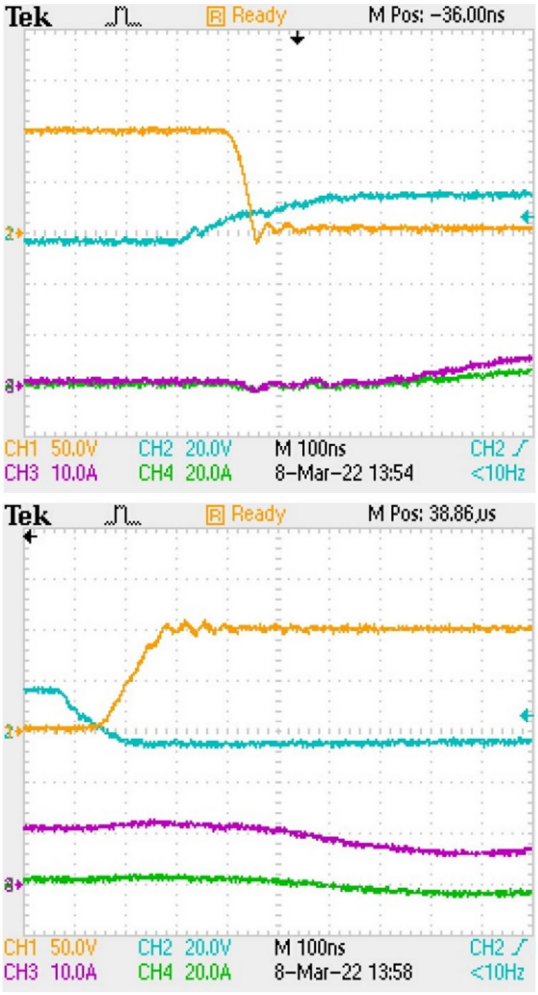
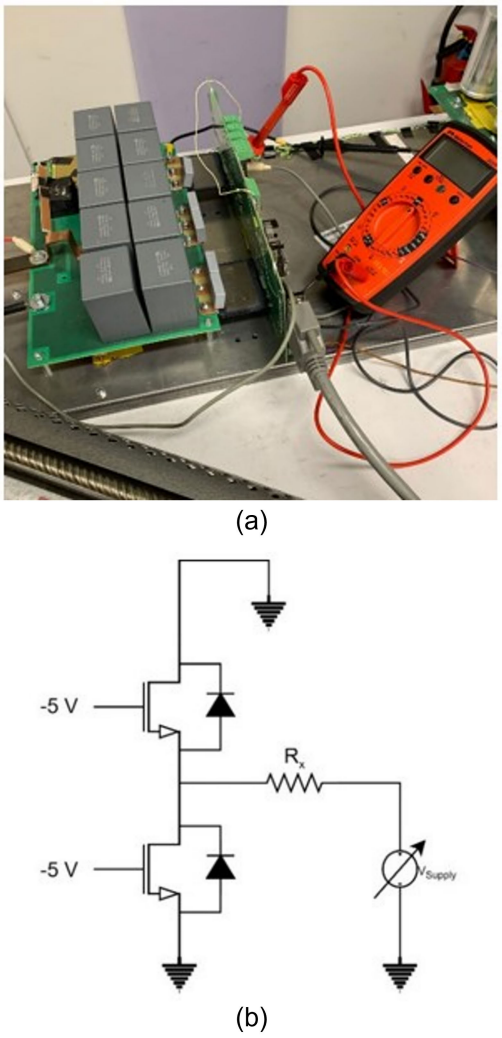


FIGURE 2. Experimental results of the DPT with 100 V, 10 A (CH1: V_{ds}, CH2: V_{gs}, CH3: I_{ds}, CH4: I_{supply_+}).



(a)

(b)

FIGURE 3. Experimental set-up for the static body diode test (a) and equivalent circuit description - $R_x \cong 10\Omega$ (b).

A. PROBE DELAY DERIVATION FOR V_{th} ESTIMATION

To determine the threshold voltage of the MOSFET, the following steps need to be taken: (i) Identify the moment when the load current (I_{load}) starts to rise during the turn-on phase (t_1); (ii) Subtract the delay between I_{load} and V_{GS} from t_1; (iii) Determine the value of V_{GS} at the identified instant, which represents the threshold voltage. The transients used for this purpose are obtained from either the Single Pulse Test (SPT) or the Double Pulse Test (DPT). Since we are working with an inverter, conducting the conventional test to evaluate the MOSFET's threshold voltage is not feasible due to the presence of the driver, which poses a risk of damage. Therefore, an alternative approach must be employed to obtain this threshold voltage. Initially, it is necessary to ascertain the delay between V_{GS}, V_{DS}, and I_{load}. To accomplish this, the instant at which the Miller plateau concludes during the turn-off phase (t_2) can be utilized.

As mentioned earlier, the determination of the MOSFET threshold voltage requires the utilization of transients obtained from either the Single Pulse Test (SPT) or the Double Pulse Test (DPT). In our case, we utilized the transients obtained from the DPT conducted at a supply voltage of 100 V and a load current of 10 A. Specifically, the transients used for analysis were the initial turn-on (beginning of the first pulse) and the first turn-off (end of the first pulse), depicted in Figure 2. Based on these waveforms, employing the same notation as shown in Figure 1, we obtained the corresponding results presented in Table 1. From the turn-off waveform, we were able to determine the delays caused by the probes, as detailed in Table 2.

By observing the moment $t_1(I_{DS})$ when the current starts to rise during the turn-on phase and accounting for the delay between I_{DS} and V_{GS}, we were able to determine the specific instant $t_x = 1.76\mu s$ at which V_{GS} reaches the threshold voltage. Consequently, by evaluating the value of V_{GS} during the turn-on phase at time t_x, we obtained the MOSFET threshold voltage V_{th}, which was found to be 4.036 V.

TABLE 3. Body diode static test results.

$V_{sd}[V]$	$I_{sd}[A]$	$V_{sd}[V]$	$I_{sd}[A]$	$V_{sd}[V]$	$I_{sd}[A]$
0	0	2.440	0.383	2.498	0.881
0.480	0	2.445	0.407	2.500	0.906
0.980	0	2.450	0.432	2.504	0.932
1.470	0	2.453	0.455	2.508	0.958
1.970	0	2.456	0.482	2.512	0.981
2.220	0	2.460	0.507	2.516	1.019
2.300	0.033	2.463	0.530	2.520	1.171
2.330	0.055	2.466	0.555	2.530	1.402
2.350	0.075	2.470	0.580	2.540	1.661
2.360	0.100	2.472	0.604	2.550	1.917
2.370	0.130	2.474	0.623	2.560	2.167
2.380	0.155	2.476	0.652	2.570	2.435
2.390	0.178	2.478	0.678	2.580	2.694
2.400	0.200	2.480	0.701	2.590	2.951
2.410	0.225	2.483	0.728	2.60	3.207
2.415	0.250	2.486	0.764	2.610	3.468
2.420	0.280	2.490	0.788	2.620	3.724
2.430	0.310	2.492	0.809	2.625	3.983

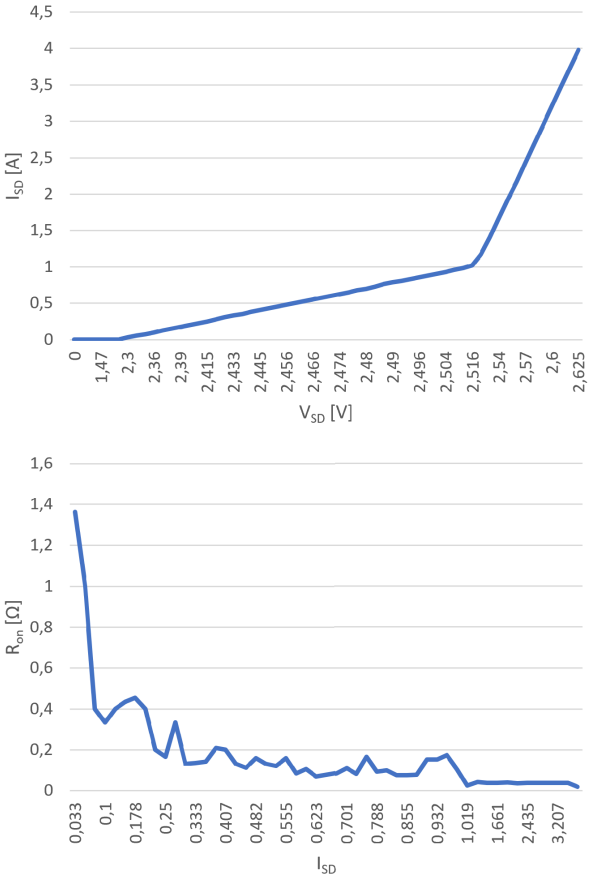


FIGURE 4. $I_{sd} - V_{sd}$ and $R_{sd,on} - I_{sd}$ body diode measured characteristics.

B. STATIC MEASUREMENT OF THE BODY-DIODE CHARACTERISTIC

To characterize the body diode, a static test can be conducted, provided that low currents are employed. Figure 3 illustrates the circuit configuration used for this test. It is essential to turn on the gate driver to keep the devices in the off state.

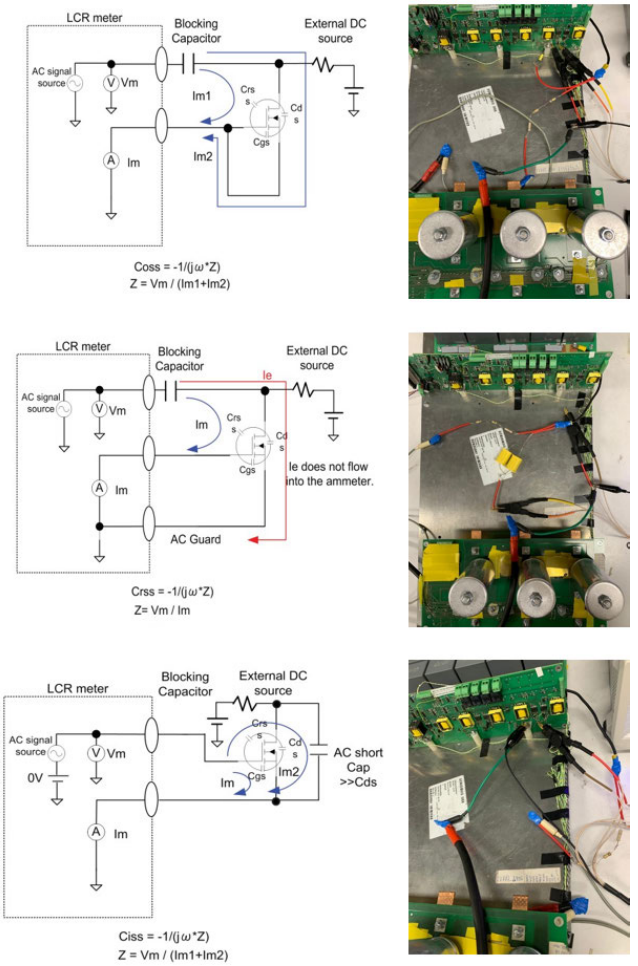


FIGURE 5. Test set-up for measuring C_{iss}, C_{oss}, and C_{rss}.

To test the upper device, the positive terminal of the power supply should be connected to the midpoint between the two MOSFETs, while the negative terminal is connected to the positive terminal of the inverter's supply voltage. The negative terminal of the inverter's supply voltage can either be left open or connected to the negative terminal of the power supply. For safety reasons, it is recommended to connect a resistance between the power supply and the midpoint. The value of this resistance, denoted as R_x, should satisfy the condition $R_x \geq 10\Omega$.To conduct the test, we simply need to adjust the power supply voltage and measure the voltage across the body diode as well as the current flowing through it. The gate driver is activated to ensure that the devices remain in the off state. For testing the upper device, we connect the positive terminal of the power supply to the midpoint between the two MOSFETs, while the negative terminal is connected to the positive terminal of the inverter's supply voltage. To ensure safety, a variable resistance is inserted between the power supply and the midpoint.

A resistance value of 20Ω is chosen for the test configuration. To perform the test, the power supply voltage is adjusted while simultaneously measuring the voltage across the body

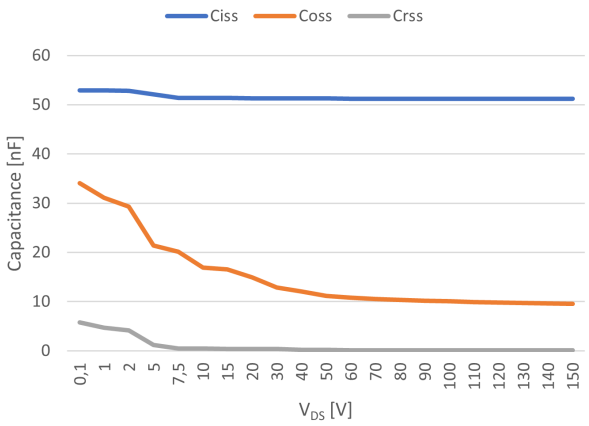


FIGURE 6. Experimental C-V Characteristics.

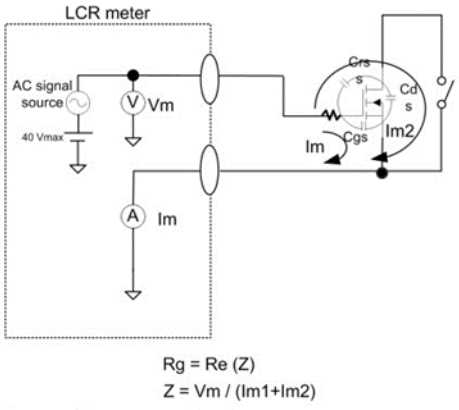


FIGURE 7. Schematic representation of the circuit used for R_g measurement.

diode (V_{SD}) using a multi-meter, and monitoring the current flowing through it (I_{SD}) supplied by the power source. The results obtained from the test are presented in Table 3. The graphical representation of the body diode characteristic can be seen in Figure 4. up, while Figure 4. bottom illustrates the relationship between the body diode on-resistance and varying current levels. Notably, the average on-resistance ($R_{on,avg}$) is found to be approximately 0.1Ω.

C. PARASITIC CAPACITORS CHARACTERIZATION

Parasitic capacitances have a significant impact on the performance of SiC MOSFETs and need to be considered in their design and analysis. These capacitances, including the output capacitance (C_{oss}), reverse transfer capacitance (C_{rss}), and input capacitance (C_{iss}), are measured using a capacitance-voltage (C-V) technique. This technique involves measuring the capacitance of the device as a function of the applied voltage. To perform these measurements, the circuits shown in Figure 5 are utilized along with an external power supply for biasing the device and an LCR meter. The results, depicted in Figure 6, were obtained under standard measurement conditions with an alternating voltage (V_{ac}) of 1 V and a frequency

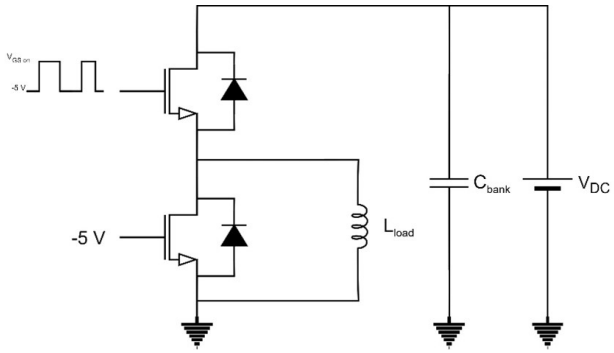


FIGURE 8. Test circuit for the DPT characterization.

FIGURE 9. Experimental setup of the DPT test for dynamic characterization.

(f) of 1 MHz. It is worth noting that the terminal capacitance of the SiC MOSFET, C_{gd}, corresponds to C_{rss}, while C_{gs} is calculated as the difference between C_{iss} and C_{gd}, and C_{ds} is determined as the difference between C_{oss} and C_{gd}.

D. INTERNAL GATE RESISTANCE CHARACTERIZATION

To find the internal gate resistance it was enough to use just one LCR meter (see Fig. 7). The drain terminal was left open and the LCR meter was set in Rs-Cs mode using measurement frequency of $1MH_z$ and a Vac equal to 1 V. The value of the internal gate resistance obtained is about $500m\Omega$.

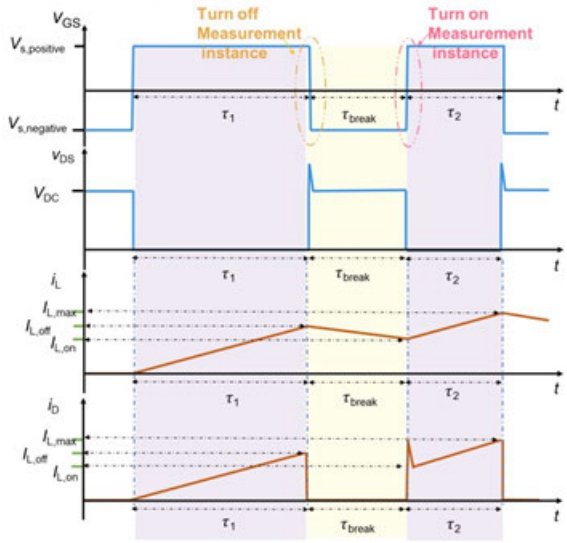


FIGURE 10. DPT waveforms.

E. DOUBLE PULSE TEST FOR DYNAMIC CHARACTERIZATION

In order to achieve the dynamic characterization of the DUT (upper device), it is essential to ensure that the lower device remains in an off state. This can be achieved by applying two carefully timed pulses to the gate of the DUT, with their duration precisely determined based on the desired test current. Figure 8 illustrates the test circuit utilized for conducting this evaluation. During the off period of the DUT, the body diode of the lower device serves as a freewheeling diode, allowing the current to flow through the load. The tests are conducted at specific values of V_{DS} and I_{load} to enable the dynamic characterization of the device. The quantities of interest that are measured include V_{GS}, V_{DS}, and I_{DS} of the DUT, as well as the load current (I_{load}). These measurements provide valuable insights into the device's behavior under dynamic conditions. To achieve the desired load current, the first on period is employed, allowing the current to gradually increase. The duration of this period, denoted as τ_1, is carefully selected to ensure the desired current level is reached. The duration τ_1 is determined based on various factors such as the load characteristics, the device parameters, and the desired settling time. By appropriately choosing τ_1, the load current can be precisely controlled and stabilized at the desired value (see Eq. 1).

$$\tau_1 \geq L_{load} \frac{I_{test}}{V_{DC}} \tag{1}$$

Subsequently, an off period is introduced to facilitate the measurement of the turn-off parameters of the DUT. It is essential to carefully select the duration of this off period, denoted as τ_{break}, to ensure that it does not significantly decrease the load current. By appropriately choosing τ_{break}, the load current can be maintained at a relatively stable level, allowing for accurate measurement of the turn-off characteristics of the DUT. The duration of τ_{break} is determined based on factors such as the required measurement accuracy, the load circuitry, and the characteristics of the DUT, ensuring that any potential decrease in load current during this period remains minimal (see Eq. 2).

$$\tau_{break} \leq L_{load} \frac{\Delta I_{test}}{V_{DC}} \tag{2}$$

To ensure proper turn-on operation at approximately equal load current, it is crucial to set the test current ΔI_{test} within a range of 1% to 5% of the desired load current. This range allows for a sufficient level of current stability during the turn-on process. During the first pulse, electrical energy is sourced from the capacitor bank and subsequently converted into magnetic energy in the load inductance. It is important to maintain a relatively constant voltage during this period to ensure stable operation. To determine the minimum required capacitance, an energy balance analysis between the capacitor and the load inductance is performed. This analysis takes into account the energy stored in the capacitor and the energy transferred to the load inductance, ensuring that the voltage remains within an acceptable range. By carefully considering the energy balance, the appropriate capacitance value can be determined to maintain voltage stability during the turn-on phase (see Eqs. 3 and 4).

$$C_{bank} \geq \frac{L_{load} I^2{}_{test}}{2V_{DC}\Delta V_{DC} - \Delta V^2{}_{DC}} \tag{3}$$

$$\Delta V_{DC} = V_{DC} - \sqrt{V^2{}_{DC} - \frac{L_{load}}{C_{bank}} I^2{}_{bank}} \tag{4}$$

Given that the value of C_{bank} is predetermined based on the design of the inverter, it is necessary to calculate the variation of V_{DC} during the test. The variation of V_{DC} should ideally be limited to a range of 1% to 5% of the nominal V_{DC} value. The second on period is specifically dedicated to obtaining the turn-on parameters of the Device Under Test (DUT). The duration of this period is determined by the limitations of the driver, particularly the maximum driving frequency (f_{max}). It is important to consider the capabilities and specifications of the driver to ensure that the turn-on parameters of the DUT can be accurately measured within the given time frame. By accounting for the maximum driving frequency, the appropriate duration for the second on period can be determined, allowing for efficient and accurate characterization of the DUT during turn-on (see Eq. 5).

$$f_{max} \geq \frac{1}{\tau_{break} + \tau_2} \tag{5}$$

To obtain the dynamic characterization of the upper device (DUT), it was necessary to design a real-time FPGA-based controller specifically for each test. This controller was then downloaded onto the dSPACE Micro-Lab-Box, enabling the gate driver to apply the desired V_{GS} to the devices. The tests were conducted at specific values of V_{DS} and I_{load}, with the goal of obtaining the dynamic characterization of the device. However, due to the limitations of the testing system,

TABLE 4. Experimental Characterization of the turn-on and turn-off behaviour.

	Turn on			Turn off		
Operating Condition	$I_{load}[A]$	$t_f[ns]$	$t_{d,ff}[ns]$	$I_{load}[A]$	$t_r[ns]$	$t_{d,on}[ns]$
(30V,3.2A)	4.1	167.0	119.6	3.9	33.0	89.0
(30V,5A)	7.0	102.8	81.2	6.8	36.4	88.8
(30V,7A)	9.6	65.6	72.4	9.4	39.0	86.0
(50V,5A)	6.8	125.2	83.6	6.6	36.2	89.2
(50V,6.8A)	8.0	120.0	86.4	7.8	36.4	88.4
(50V,10A)	13.2	50.4	77.0	13.0	40.4	84.0
(100V,5A)	7.8	182.8	107.6	7.6	41.4	92.4
(100V,10A)	12.0	110.0	94.0	11.8	42.4	91.2
(100V,13A)	13.4	87.2	94.4	13.2	44.8	86.8
(100V,15A)	18.6	62.8	80.0	18.4	46.0	88.8
(100V,20A)	25.6	39.0	70.0	25.4	47.0	88.0
(150V,10A)	12.2	220	100.0	12.0	39.0	87.0
(150V,15A)	17.8	120	81.8	17.6	44.4	84.8
(150V,20A)	23.4	62.0	79.2	23.2	48.0	82.8

TABLE 5. Pulses width for the various tests.

V_{dc}, I_{load}	$\tau_1[\mu s]$
30 V, 3.2 A	35
30 V, 5 A	69
30 V, 7 A	98
50 V, 5 A	39
50 V, 6.8 A	45
50 V, 10 A	85
100 V, 5 A	18
100 V, 10 A	38
100 V, 13 A	43
100 V, 15 A	60
100 V, 20 A	85
150 V, 10 A	25
150 V, 15 A	38
150 V, 20 A	53

we were only able to measure certain quantities, namely V_{GS}, V_{DS}, I_{load}, and $I_{supply,+}$. Considering the maximum driving frequency of the dSPACE Micro-Lab-Box, which is $40kHz$, the duration τ_{break} and τ_2 were set to the minimum possible value of $12.5\mu s$. This allowed for a suitable range of ΔI_{test}, which could be maintained between 1% and 5% of the test current. The duration of the first pulse (τ_1) was chosen to ensure that the load current increased to the desired value. While it was necessary for τ_1 to be greater than $12.5\mu s$, it was also important to adhere to the standards, which specified that it should not exceed $100\mu s$ to prevent device damage caused by self-heating (see Eq. 6).

$$12.5\mu s \leq \tau_1 \leq 100\mu s \tag{6}$$

During the first pulse, the electrical energy is sourced from the fixed capacitor bank with a value of $850\mu F$ that is designed into the inverter. This energy is subsequently converted into magnetic energy within the load inductance. It is crucial to maintain a relatively constant supply voltage during this period, or in other words, to ensure that the variation of V_{DC} (ΔV_{DC}) remains within the range of 1% to 5% of the nominal V_{DC}. All of these considerations play a significant role in determining the appropriate sizing of the load inductance. In addition to meeting the voltage variation requirements, the load inductance should also facilitate the desired increase in load current to the desired value (see Eq. 7).

$$L_{load} \leq \tau_1 \frac{V_{DC}}{I_{test}} \tag{7}$$

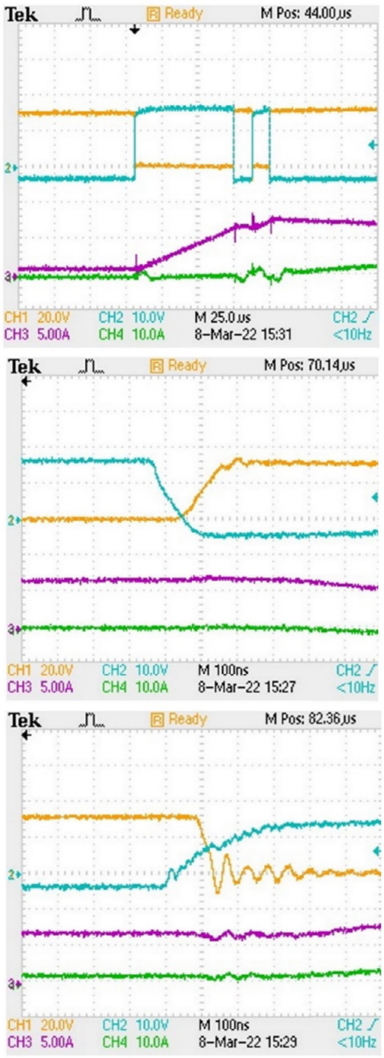


FIGURE 11. Total turn-on/off measurements in the DPT at with $V_{ds} = 50V$ and $I_{load} = 10A$.

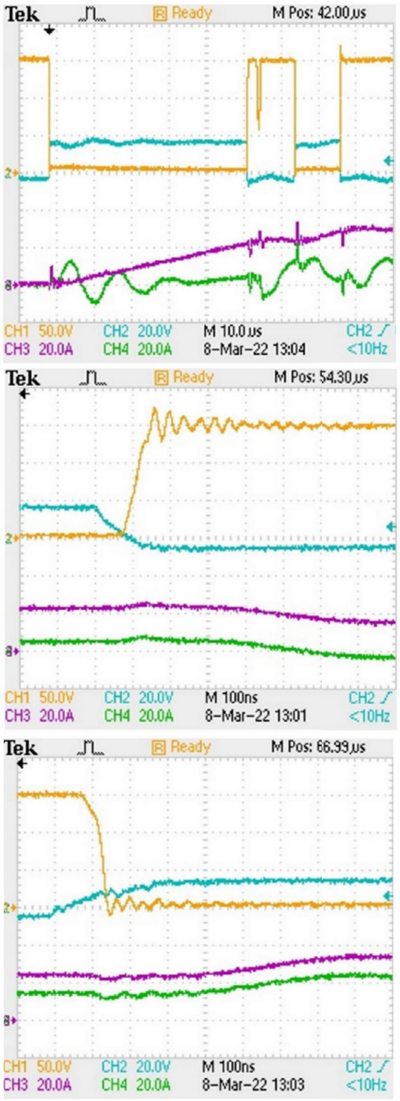


FIGURE 12. Total turn-on/off measurements in the DPT at with $V_{ds} = 150V$ and $I_{load} = 20A$.

Based on the planned tests, a load inductance of approximately $330\mu H$ was chosen. The series resistance of the load was measured to be less than 1Ω. Once the load inductance was determined, the next step involved designing various real-time FPGA-based controllers specifically tailored for each test scenario. Table 5, provides an overview of the pulse widths obtained for each test.

After assembling the setup, we measured the parasitic effects introduced by the cables that connect the system to the power supply using an LCR meter. The measurements revealed the following parasitic parameters for the cables: (a) The cable connected to the positive supply voltage exhibited the following parasitic characteristics: a.1) Parasitic resistance: 0.853 $m\Omega$; a.2) Parasitic inductance: 3.37 nH. (b) The cable connected to the negative supply voltage exhibited the following parasitic characteristics: b.1) Parasitic resistance: 0.862 $m\Omega$; b.2) Parasitic inductance: 3.61 nH.

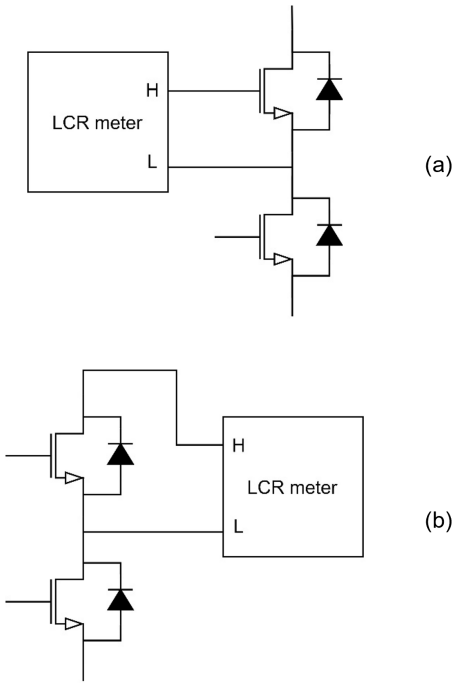


FIGURE 13. Circuit schematic for inductance measurement.

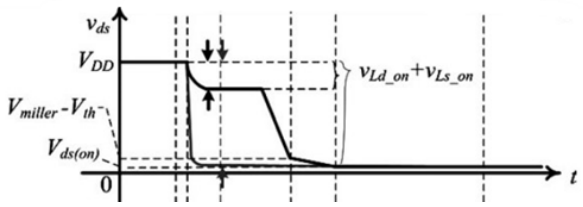


FIGURE 14. Turn-on switching waveform of the V_{DS}.

These measurements provide important information about the parasitic elements present in the system, which can have an impact on the overall performance and behavior of the circuit. By quantifying these parasitic parameters, we can implement appropriate compensation techniques to mitigate their effects and ensure accurate test results. Table 4 presents the results obtained from the conducted tests, specifically focusing on the turn-on and turn-off transients. The parameters $t_{f/r}$ and $t_{d_{off/on}}$ have been previously defined. Figures 11 and 12 depict waveforms obtained from selected tests. It is noteworthy that, due to safety considerations, a maximum V_{DC} of 150 V was employed, imposing limitations on the test conditions. These experimental findings offer valuable insights into the dynamic behavior of the DUT during turn-on and turn-off events, facilitating a deeper understanding of its performance characteristics.

F. STRAY INDUCTANCE CHARACTERIZATION

Two methods exist for determining the parasitic inductances at the drain, source, and gate terminals. The first method involves the use of an LCR meter, while the second method relies on analyzing the turn-on and turn-off

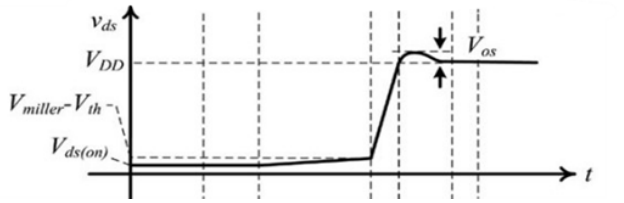


FIGURE 15. Turn-off switching waveform of the V_{DS}.

TABLE 6. Summary of measured Stray inductance value.

Turn-off			Turn-on		
$\frac{di_D}{dt}$	V_{os}	$L_S + L_D$	$\frac{di_D}{dt}$	$V_{Ld} + V_{Ls}$	$L_S + L_D$
40 $\frac{A}{\mu s}$	6 V	150 nH	8 $\frac{A}{\mu s}$	0.8 V	100 nH

transients. The appropriate connections for measuring the stray inductances of the upper device are illustrated in Figure 13. To measure the combined inductance of $L_G + L_S$, the test circuit shown in Figure 13(a) is utilized. Conversely, to determine the combined inductance of $L_D + L_S$, the test circuit depicted in Figure 13(b) is employed. These circuit configurations enable precise measurements of the respective parasitic inductances associated with the drain, source, and gate terminals of the device. An alternative method for determining $L_D + L_S$ involves analyzing the turn-on and turn-off switching waveforms obtained during the DPT. During the turn-on transient (see Figure 14), when V_{GS} exceeds the threshold voltage V_{th} and the drain current I_D starts to increase from zero to its peak value, the drain-source voltage V_{DS} decreases by $V_{L_{D,on}} + V_{L_{S,on}}$. This voltage drop is attributed to the rising drain current flowing through the inductances L_S and L_D. By measuring the voltage drop $V_{L_{D,on}} + V_{L_{S,on}}$ and the rate of change of I_D ($\frac{dI_D}{dt}$), it becomes possible to determine the combined inductance $L_D + L_S$ (see Eq. 8).

$$L_D + L_S = \frac{V_{L_{D,on}} + V_{L_{S,on}}}{\frac{dI_D}{dt}} \tag{8}$$

In the case of the turn-off transient (refer to Figure 15), once the diode stops blocking the voltage, the current starts to flow from the MOSFET to the diode. This stage continues until the drain current reaches zero and V_{GS} reaches the threshold voltage V_{th}. During this process, the decreasing drain current induces a voltage drop across the parasitic inductances, resulting in additional stress on the MOSFET. This leads to the appearance of a voltage overshoot V_{os} in V_{DS}. By directly measuring the voltage overshoot, it is possible to determine $L_D + L_S$ (see Eq. 9). To perform this characterization, we utilized the waveform obtained from the DPT conducted at $V_{DC} = 50V$ and $I_{load} = 10A$, in conjunction with the aforementioned equations. The results of this analysis are summarized in Table 6.

$$L_D + L_S = \frac{V_{os}}{\frac{dI_D}{dt}} \tag{9}$$

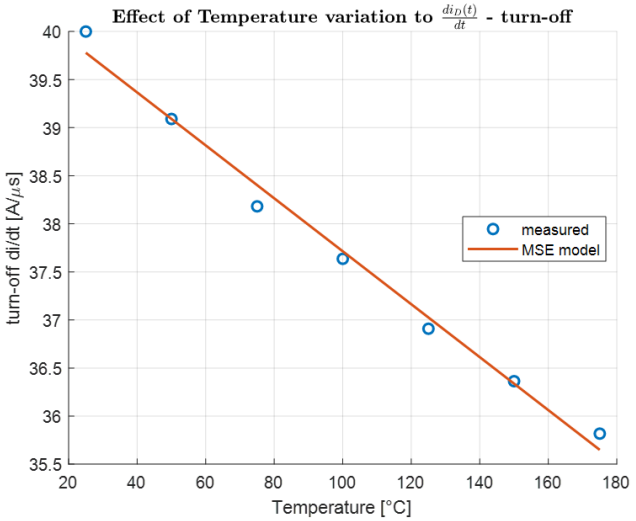


FIGURE 16. measurement of the dependence of the current derivative on the junction temperature, during the turn-off.

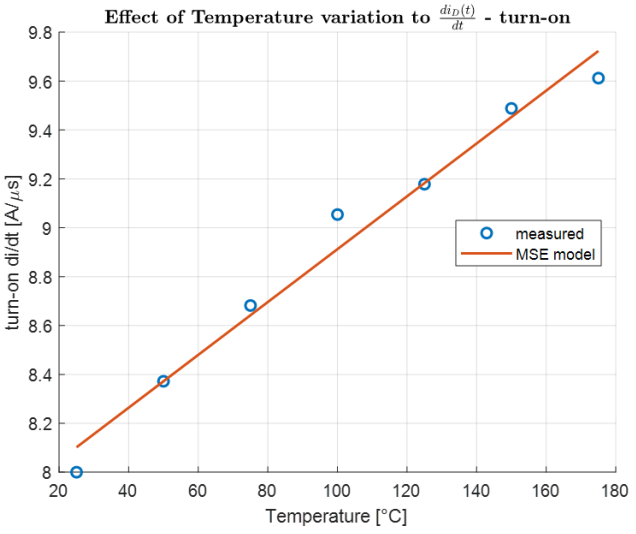


FIGURE 17. measurement of the dependence of the current derivative on the junction temperature, during the turn-on.

TABLE 7. Characterization of the Thermal Coefficient.

	$T_{case}[C]$	$V_{ds}[V]$	$I_{ds}[A]$	$K_{Vds}[mV/C]$
initial	25.0	2.54	1.661	
final	30.9	2.51	1.668	- 5.085

A fundamental aspect to analyze is certainly the thermal dependence of the stray components. For this purpose, the temperature was measured using a thermal chamber, maintaining the same operating conditions previously discussed ($V_{supply} = 50V, I_{load} = 10A$). By observing the V_{DS} measured in DPT, for a time long enough to reach even high temperatures (up to $T_j \cong 175^oC$), obtaining (indirectly) the estimate of $\frac{di_D}{dt}$. In this way we are able to estimate the dependence of the stray inductances (both in turn-off and

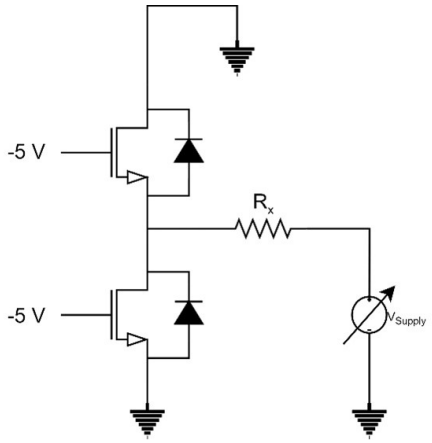


FIGURE 18. Test circuit for body diode the static thermal test.

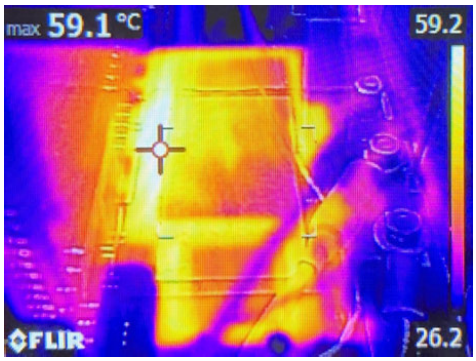


FIGURE 19. Measurement provided by the thermal imaging camera in the test with $V_{supply} = 40V$ after about 50 seconds of observation.

turn-onn), using the equations presented previously. Experimentally we were able to obtain measurements of the current derivative in the two switching transients, in the operating range $25-175[^oC]$. Figure 16 shows the overlap between the samples actually measured in the turn-off as the temperature varies, and the linear model obtained using the least squares method. Figure 17 shows the analogous result for the turn-on transient. It can be seen that a linear model is quite adequate to approximate the trend of the real measurements, therefore we assume that Eq.10 is valid.

$$\begin{aligned} \frac{di_D}{dt}|_{turn-off} &= m_{off}T_j + q_{off} \cong -0.0275\,T_j + 40.4675 \\ \frac{di_D}{dt}|_{turn-on} &= m_{on}T_j + q_{on} \cong 0.018T_j + 7.8317 \end{aligned} \tag{10}$$

$$\frac{L_{stray,on/off}(T_j+1)}{L_{stray,on/off}(T_j)} = \frac{m_{on/off}T_j + q_{on/off}}{m_{on/off}(T_j+1) + q_{on/off}} \tag{11}$$

It is therefore possible to estimate the inductance variation by applying the ratio principle, treating the variation of T_j as the argument of a sequence, with unitary ^oC increase (see Eq.11). Where L_{stray} it is defined as the sum of the stray contributions $L_S + L_D$. It can easily be verified that during the turn-off there is an increase of the L_{stray} inductance of about $70[pH/^oC]$, conversely, for the turn-on transient there is a decrease of the L_{stray} inductance of about $1.3[pH/^oC]$.

G. STATIC & DYNAMIC THERMAL CHARACTERIZATION

1) STATIC THERMAL TEST

To determine the junction-case thermal resistance of the device, the body diode can be employed. Although the obtained value will not be identical to the junction-case thermal resistance of the MOSFET due to the current flowing in a different region of the die, it will provide a close approximation. To determine the junction-case thermal resistance, the calculation of the diode temperature coefficient, denoted as $K_{V_{sd}}$, is the initial step. This coefficient quantifies the variation in the source-to-drain voltage of the body diode in response to temperature changes. By accurately assessing this coefficient, it becomes possible to estimate the junction temperature, which may not be directly measured using the available instrumentation (see Eq. 12).

$$K_{V_{sd}} = \frac{V_{SD}\left(T_{c,f}\right) - V_{SD}\left(T_{c,i}\right)}{T_{c,f} - T_{c,i}} \tag{12}$$

To determine the diode temperature coefficient, $K_{V_{sd}}$, several measurements need to be performed. Firstly, for a fixed current (I_{SD}), the case temperature ($T_{c,f}$) and the source-to-drain voltage (V_{SD}) of the device are measured when it is turned on. Subsequently, the system is allowed to stabilize, and another set of measurements is taken, recording the final case temperature ($T_{c,f}$) and the corresponding source-to-drain voltage (V_{SD}) at that temperature ($T_{c,f}$). These measurements provide the necessary data to calculate the diode temperature coefficient (see Eq. 13).

$$\Delta T_j = \frac{V_{SD}\left(T_{c,f}\right) - V_{SD}\left(T_{c,i}\right)}{K_{V_{sd}}} \tag{13}$$

Once the value of $K_{V_{sd}}$ has been determined, a similar test can be conducted by setting a different current value. The temperature ($T_{c,i}$) and the source-to-drain voltage (V_{SD}) of the device are measured when it is turned on, and the system is allowed to stabilize. The final values of V_{SD}, I_{SD}, and the case temperature ($T_{c,i}$) are recorded. By utilizing the previously obtained $K_{V_{sd}}$ value, it is possible to calculate the variation in junction temperature. This method allows for estimating the junction temperature using the diode temperature coefficient (see 14). Once the variation in junction temperature (ΔT_j) has been determined, it becomes possible to calculate the final junction temperature. By using this information, the junction-case thermal resistance $R_{th,jc}$ can be obtained. The junction-case thermal resistance provides insights into how efficiently heat is dissipated from the junction to the case of the device. It is an important parameter in assessing the thermal performance and reliability of the device under different operating conditions (see Eq. 15). Exploiting the above equations, it is possible to collect the data reported

TABLE 8. Results obtained from the body diode static thermal tests.

V_{supply}	$T_{c,i}$	$V_{SD,i}$	$I_{SD,i}$	$T_{c,f}$	$V_{SD,f}$	$I_{SD,f}$	$T_{j,f}$	$R_{th,jc}$
5V	25 ^oC	2.38 V	0.130 A	25.25 ^oC	2.37 V	0.143 A	26.97 ^oC	5.065 ^oC/W
10V	25 ^oC	2.44 V	0.383 A	26.00 ^oC	2.43 V	0.391 A	26.77 ^oC	0.810 ^oC/W
15V	25 ^oC	2.47 V	0.623 A	25.80 ^oC	2.46 V	0.645 A	26.97 ^oC	0.735 ^oC/W
20V	25 ^oC	2.49 V	0.881 A	27.30 ^oC	2.47 V	0.894 A	28.74 ^oC	0.651 ^oC/W
25V	25 ^oC	2.52 V	1.171 A	28.20 ^oC	2.49 V	1.150 A	30.90 ^oC	0.943 ^oC/W
30V	25 ^oC	2.53 V	1.402 A	29.20 ^oC	2.50 V	1.406 A	30.90 ^oC	0.484 ^oC/W
40V	25 ^oC	2.55 V	1.917 A	32.00 ^oC	2.51 V	1.930 A	32.87 ^oC	0.179 ^oC/W
45V	25 ^oC	2.56 V	2.167 A	32.35 ^oC	2.51 V	2.192 A	34.83 ^oC	0.451 ^oC/W
50V	25 ^oC	2.57 V	2.435 A	34.45 ^oC	2.52 V	2.454 A	34.83 ^oC	0.062 ^oC/W
55V	25 ^oC	2.58 V	2.694 A	35.85 ^oC	2.52 V	2.718 A	36.80 ^oC	0.139 ^oC/W
60V	25 ^oC	2.59 V	2.951 A	37.25 ^oC	2.52 V	2.994 A	38.77 ^oC	0.201 ^oC/W

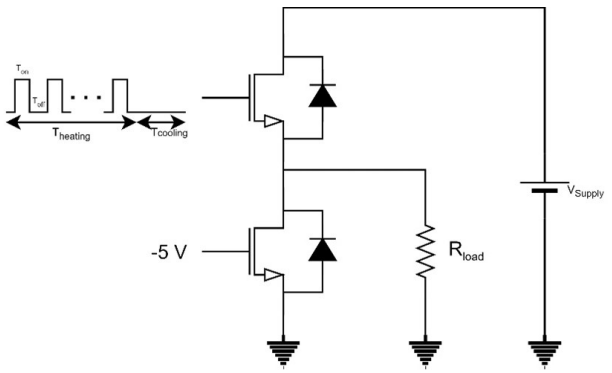


FIGURE 20. Test circuit for the dynamic thermal test.

in Table 8.

$$T_{j,f} = \Delta T_j + T_{init} \quad \left(T_{init} = 25^o C\right) \tag{14}$$

$$R_{th,jc} = \frac{T_{j,f} - T_{c,f}}{V_{SD,f} I_{SD,f}} = \frac{\Delta T}{P_{diss}} \tag{15}$$

2) DYNAMIC THERMAL TEST

To find the junction capacitance of the DUT, a dynamic thermal test must be carried out. For this purpose, the circuit in Figure 20 can be used. The test consists of turning on and off the DUT using a certain frequency and duty cycle so that it warms up, and then turning it off until it cools down. The load used is a resistance of about ten Ohms, the supply voltage can be changed to set the dissipated power by the device. The heating period $T_{heating}$ must be chosen so that the temperature of the device can reach a constant value, while the cooling period $T_{cooling}$ lasts as long as the device reaches the ambient temperature. A thermal camera is needed to perform this test. To conduct this test, we start by measuring the initial temperature of the device before the heating period begins. Subsequently, we record the case temperature at regular intervals to capture the temperature transient. During the test, we focus on measuring the electrical quantities of the upper device, namely V_{DS} (drain-to-source voltage) and I_{DS} (drain current). The case-ambient thermal resistance of the MOSFET can be determined from the heating transient when the system reaches a steady state. At steady state, the total power dissipated by the device can be calculated using Eqs.16. Then is obtained the case-to-ambient thermal resistance, as in Eq.17, To determine the case capacitance, we can utilize the case-to-ambient thermal resistance and the time constant of the case temperature heating transient ($\tau_{heating}\tau_c$). The time constant $\tau_{heating}$ corresponds to the time it takes for the case temperature to reach 63% of its total variation. By considering this, we can calculate the equivalent thermal capacitance of the case using Eq.18.

$$P_{diss,avg} = P_{cond,avg} + \underbrace{P_{on,avg} + P_{off,avg}}_{P_{switch,avg}}$$

$$P_{on,avg} = \frac{E_{on}}{T_{sw}}$$

$$P_{off,avg} = \frac{E_{off,avg}}{T_{sw}} \tag{16}$$

$$R_{th,ca} = \frac{T_{c,f} - T_a}{P_{diss,avg}} \ (steady - state\ condition) \tag{17}$$

$$C_c = \frac{\tau_{heating,\tau_c}}{R_{th,ca}} \tag{18}$$

To determine the junction capacitance, we can apply a similar method as used to find the junction temperature from the case temperature. First, we need to find the drain-to-source voltage temperature coefficient ($K_{V_{ds}}$). This coefficient indicates how the drain-to-source voltage of the device changes with temperature variations. It is crucial for accurately estimating the junction capacitance. Using the previously determined $K_{V_{ds}}$ and the measured values of V_{DS} at specific times and case temperatures, we can calculate the transient junction temperature. By considering the relationship between $K_{V_{sd}}$, V_{DS}, and the junction temperature, we can estimate the variation in junction temperature over time during the test. This information is crucial for further analysis and characterization of the device. The time constant of the junction temperature heating transient ($\tau_{heating,T_j}$) can be determined from the transient junction temperature profile. This time constant represents the time it takes for the junction temperature to reach 63% of its total variation during the heating process. By analyzing the junction temperature curve, we can identify this time constant, which is crucial for calculating the junction capacitance

(see Eqs. 19, 20 and 21).

$$K_{V_{ds}} = \frac{V_{DS}(T_{c,f}) - V_{DS}(T_{c,i})}{T_{c,f} - T_{c,i}} \tag{19}$$

$$\Delta T_j(t) = \frac{V_{DS}(T_c(t)) - V_{DS}(T_{c,i})}{K_{V_{ds}}} \tag{20}$$

$$C_j = \frac{\tau_{heating,T_j}}{R_{th,jc}} \tag{21}$$

Based on the results obtained from the previous static thermal test, we can analyze how the threshold voltage (V_{th}) and drain current (I_{DS}) depend on temperature. By comparing the values of V_{th} and I_{DS} at ambient temperature with those at higher temperatures, we can determine the parameters alpha (α) and temperature coefficient (K_{ftemp}) required for the first two models. To evaluate the α parameter, which represents the temperature dependence of the MOSFET threshold voltage, we assess the threshold voltage at a specific temperature using the waveforms of V_{GS}, V_{DS}, and I_{DS}, as previously performed in the characterization process (see Eq. 22). To determine the parameter K_{ftemp}, a numerical method was utilized in conjunction with the collected data of the drain-to-source current at different temperatures. By analyzing the correlation between temperature and the corresponding drain-to-source current values, the value of K_{ftemp} could be calculated. This approach provided valuable insights into the temperature dependency of the device characteristics and enabled the creation of accurate models to describe its behavior across various operating temperatures (see Eq. 23).

$$\alpha = \frac{V_{th}(T_{j,i}) - V_{th}(T_{j,f})}{T_{j,i} - T_{j,f}} \tag{22}$$

$$\left(\frac{T_{j,f}}{T_{j,i}}\right)^{K_{ftemp}} = \frac{I_{DS}(T_{j,f}) - I_{DS}(T_{j,i})}{I_{DS}(T_{j,i})} + \left(\frac{T_{j,f}}{T_{j,i}}\right)^{-\frac{3}{2}} \tag{23}$$

During the dynamic thermal test, experiments were performed to measure the thermal capacitances of the Device Under Test (DUT). The test involved cyclically switching the DUT on and off at a frequency of $20kHz$, corresponding to its operational frequency in the inverter. A variable resistance of 2Ω was used as the load (see 21). To simplify the test procedure, a real-time FPGA-based controller was developed. This controller allowed for the adjustment of the duty cycle of the driving signal sent to the gate driver, enabling precise control over the power dissipation of the DUT. Alternatively, the supply voltage could be modified to achieve the desired power dissipation. The controller also included options for setting the heating period ($T_{heating}$) and cooling period ($T_{cooling}$). However, for safety reasons, the decision was made not to utilize these features in order to avoid subjecting the device to excessive temperature rises. To perform the test, we measured the initial temperature of the device before starting the heating period. Then, at regular intervals, we recorded the case temperature to observe the temperature transient. We used an oscilloscope to measure the electrical quantities of the upper device, specifically V_{DS} and I_{DS}. The obtained temperature transients of the case are shown in Figure 21. Using the derived expressions for calculating the case-to-ambient thermal resistance ($R_{th,ca}$) and the average dissipated power ($P_{diss,avg}$), we collected the data presented in Table 10. Additionally, we determined the values of the case capacitance, as shown in Table 11. To determine the junction capacitance, we utilized the same method used previously to find the junction temperature from the case temperature. In this case, we first obtained the drain-to-source voltage temperature coefficient ($K_{V_{ds}}$) from the dynamic thermal test. This test involved applying a supply voltage of 30 V and a duty cycle of 0.5, combined with the static characteristics of the MOSFET obtained through the SPT. The resulting values of $K_{V_{ds}}$ are presented in Table 12. These values were crucial for accurately characterizing the temperature dependence of the junction capacitance and further enhancing our understanding of the device's behavior under different operating conditions. We proceeded to obtain the junction temperature transient by using the values of $K_{V_{sd}}$ and V_{DS} from the test conducted with a supply voltage of 40 V and a duty cycle of 0.5. This allowed us to determine the time constant of the junction temperature heating transient ($\tau_{heating,T_j}$), which we then used to calculate the junction capacitance. To perform this calculation, we relied on the junction to case thermal resistance ($R_{th,jc}$) obtained from the previous static thermal test. The resulting data and the junction capacitance values

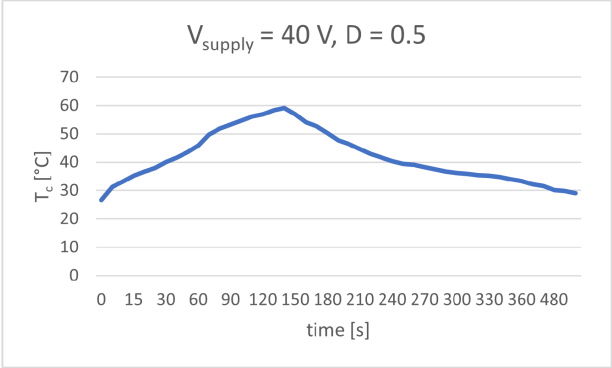


FIGURE 21. Case temperature transient for $V_{supply} = 40V$ and $D = 0.5$.

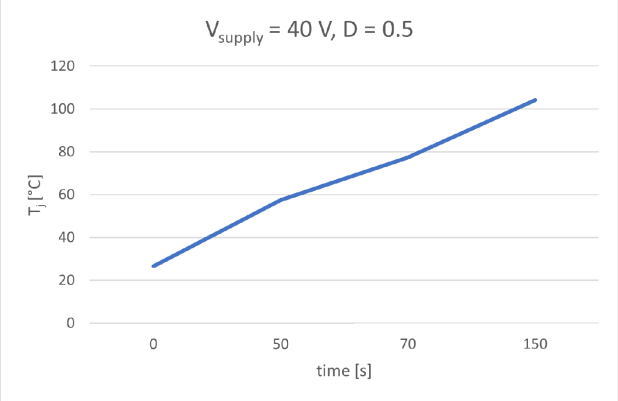


FIGURE 22. Junction temperature thermal transient.

TABLE 9. Data used to derive the thermal parameters needed by the models.

	$T_{j,s}$	$T_{j,f}$	$V_{th,s}$	$V_{th,f}$	I_{DS_s}	I_{DS_f}	α	K_{ftemp}
$V_s = 20V, D = 0.5$	25.0 ^oC	39.75 ^oC	4.036 V	3.536 V	12.77 A	9.60 A	-0.0339 $V/^oC$	-2.99
$V_s = 30V, D = 0.5$	25.0 ^oC	53.55 ^oC	4.036 V	3.472 V	17.94 A	14.0 A	-0.0198 $V/^oC$	-3.03
$V_s = 40V, D = 0.5$	25.0 ^oC	71.60 ^oC	4.036 V	3.412 V	22.80 A	18.4 A	-0.0134 $V/^oC$	-4.10

TABLE 10. Case-ambient thermal resistance values found with the tests.

	T_{amb}	$T_{c,f}$	$P_{diss,avg}$	$R_{th,ca}$
$V_s = 20V$	26.0 ^oC	43.7 ^oC	0.564 W	31.38 ^oC/W
$V_s = 30V$	27.3 ^oC	51.1 ^oC	0.856 W	27.80 ^oC/W
$V_s = 40V$	26.6 ^oC	47.0 ^oC	1.400 W	21.71 ^oC/W

TABLE 11. Case thermal capacitance values obtained.

	$T_c(t = \tau_{heating,T_c})$	$\tau_{heating,T_c}$	C_c
$V_s = 20V$	36.15 ^oC	79.50 s	2.533 $J/^oC$
$V_s = 30V$	39.99 ^oC	51.58 s	1.860 $J/^oC$
$V_s = 40V$	47.80 ^oC	64.74 s	2.980 $J/^oC$

TABLE 12. Values used to obtain $K_{V_{ds}}$ with $V_{supply} = 30V$ and $D = 0.5$.

$V_{DS}(T_{c,s} = 25^oC)$	$V_{DS}(T_{c,f} = 51.1^oC)$	$K_{V_{ds}}$
0.080 V	0.059 V	0.805 mV/^oC

TABLE 13. Values used to obtain the junction thermal capacitance.

$T_{j,i}$	$T_{j,f}$	$T_j(\tau_{heating,T_j} = 75.43s)$	C_j
26.6 ^oC	71.6 ^oC	54.95 ^oC	162.92 J/^oC

obtained from the test are presented in Table 13. These findings provided valuable insights into the thermal behavior of the junction and enabled us to accurately characterize its capacitance under different temperature conditions. Additionally, we used the results of this test to find the dependence of V_{th} and I_{DS} on temperature. By comparing the values obtained at ambient temperature with the SPT and the ones obtained at higher temperatures, we were able to determine the α and K_{ftemp} parameters needed for the first two models created. The α parameter was obtained using the previous definition, while K_{ftemp} was calculated using a numerical method combined with the data of the load current obtained at different temperatures. Table 9 shows the data obtained from the performed tests and the values of the parameters derived from them. Figure 22 shows the thermal trend of the junction during dynamic test.

III. MODELING FOR FAST SIMULATION

The article introduces a methodology aimed at simplifying the complexity of a SiC MOSFET model for converter simulations, while still accurately capturing its electro-thermal behavior, losses, and efficiency. This approach involves a gradual reduction of the model's level of detail by consolidating crucial aspects into maps that are activated by an ideal switch model. The initial step of the methodology involves parameter fitting of a comprehensive model through

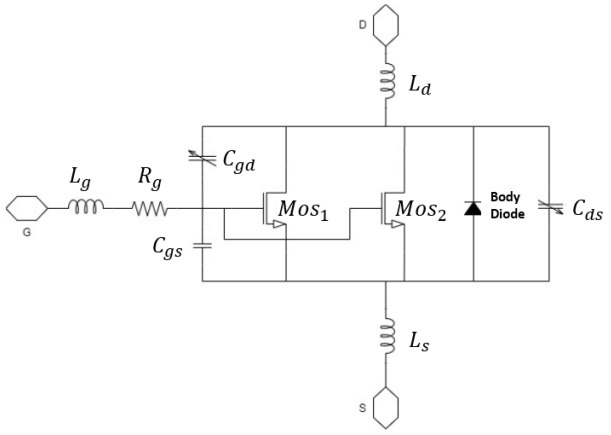


FIGURE 23. SiC MOSFET equivalent circuit.

experimental characterization. This ensures that the model accurately represents the behavior of the SiC MOSFET under different operating conditions. In the subsequent step, thermal estimation techniques are employed to streamline the electrical behavior of the model. This allows for a significant improvement in simulation speed while still preserving the essential thermal characteristics of the device. By following this methodology, the complexity of the SiC MOSFET model is effectively reduced without compromising the accuracy of the simulation results. This enables efficient and reliable evaluation of converter performance and aids in the design and optimization of power electronic systems. The mentioned reference refers to the equivalent circuit depicted in Figure 23, which is described by a set of differential equations. These equations include circuit parameters that are dependent on electrical quantities, resulting in a numerically stiff model that requires significant computational time for simulation. The characteristic equations for the three common operating regions (cut-off, linear, and saturation) are presented in Equation III. It is worth noting that the model necessitates the knowledge of parameters such as V_{th_i}, K_i, a_i, and λ_i, which are determined by fitting experimental measurements to the characteristic equations. Specifically, the equations below define the coefficients K_i and a_i (see Eqs. 24).

$$k_i = \frac{\frac{dI_D}{dt}}{(V_{GS} - V_{th_i})(1 + 2\lambda_i V_{DS}) - (1 + a_i)V_{DS}(1 + 1.5\ V_{DS})}$$
$$a_i = \frac{V_{GS} - V_{th_i}}{V_{DS,sat_i}} - 1 \tag{24}$$

To determine the value of λ, the following definitions are utilized, which are derived from the geometric interpretation

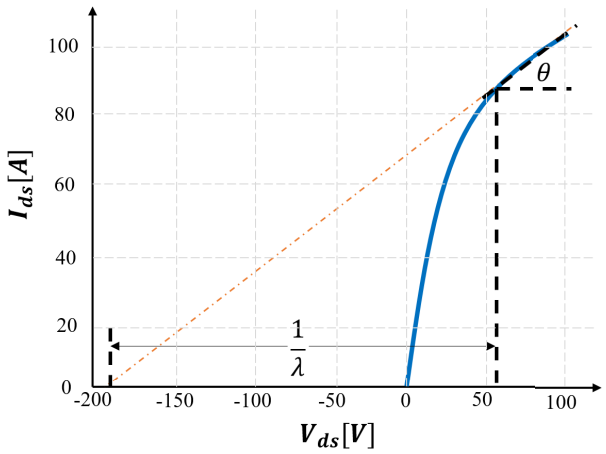


FIGURE 24. Schematic representation of the meaning of the parameter λ in relation to the angle θ of the I-V characteristic.

illustrated in Figure 24. This illustration demonstrates the relationship between the angle of curvature at the onset of the saturation zone and the parameter $1/\lambda$. In the given equations, $I_{D,T}$ represents the drain current corresponding to operation in the saturation zone, while $I_{D_{sat,T}}$ denotes the saturated value of this current. The experimental measurements provide the I-V function, allowing for the evaluation of the angle θ that characterizes this curve. Consequently, the required parameter can be derived from the constitutive equations of the model (refer to Eqs. 25, 26, and 27).

$$G_{DS} = \frac{\partial I_{D,T}}{\partial V_{DS,T}} = \\ = \frac{\partial}{\partial V_{DS,T}} \left[\frac{k(1+\lambda V_{DS,T})(V_{GS} V_{th,T})^2}{2(1+a)} \right] \quad (25)$$

$$I_{D_{sat,T}} = \frac{k(V_{GS} - V_{th,T})^2}{2(1+a)} \quad (26)$$

$$G_{DS} = \lambda I_{D_{sat,T}} = \tan(\theta) \quad (27)$$

The model also considers the influence of parasitic effects through capacitances and inductances, which are observed to be voltage-dependent according to the experimental characteristics. Furthermore, the model incorporates the characteristics of the body diode, which is described by the constitutive equation in Eq. 28. The parameters V_{th_d}, I_s, and n are determined through fitting the experimental data. It should be noted that this equation requires knowledge of $C_{iss}(V_{gs}, V_{ds})$, $C_{oss}(V_{gs}, V_{ds})$, and $C_{rss}(V_{gs}, V_{ds})$. This model takes into account the inherent relationships between electrical and thermal variables. By considering the equivalent circuit shown in Figure 25 and utilizing the following equations, it is demonstrated how the dependence of the device's junction temperature can be introduced for both the drain current I_D and the control voltage V_{GS} through the voltage generator E_{temp} (gate side) and the current generator F_{temp} (between drain and source).

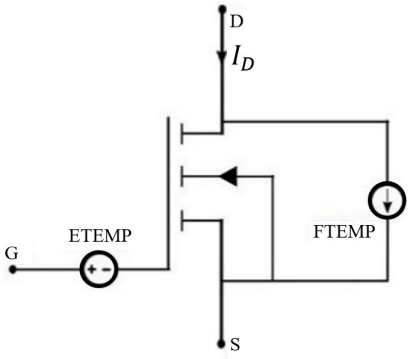


FIGURE 25. Equivalent circuit of electro-thermal relationships.

$$I_{SD} = \begin{cases} 0 & \text{if } V_{SD} < V_{thd} \\ I_S \left(e^{\frac{V_{SD} - V_{thd}}{n \frac{kT}{q}}} - 1 \right) & \text{if } V_{SD} > V_{thd} \end{cases} \quad (28)$$

$$Ftemp = I_{d,std} \left[\left(\frac{T_j}{T_{std}} \right)^{K_{Ftemp}} - \left(\frac{T_j}{T_{std}} \right)^{-1.5} \right]$$

$$Etemp = \frac{(T_j - T_{std})}{T_1 - T_2} (V_{th,1} - V_{th,2}) \quad (29)$$

One of the parameters to be determined through fitting the model to the experimental characterization data is the coefficient K_{ftemp}. Equations 29 present the thermal dependency model, where $I_{d,std}$ denotes the drain current under "standard" thermal conditions ($T_{std} = 25^o C$). This dependence is expressed as an additive disturbance in terms of the drain current and the control voltage at the gate, as illustrated in Eq. 30.

$$I_{d,tot} = I_{ch,1} + I_{ch,2} + Ftemp \\ V_{GS} = V_{GS,std} + Etemp \quad (30)$$

To account for the effects of parasitic capacitances, the model incorporates the experimental characteristics or datasheet information by utilizing maps that describe the capacitance-voltage (C-V) functions. The estimation of junction temperature employs a first-order linear model, which integrates the experimental thermal impedance characteristic Z_{th}. This characteristic is commonly provided in datasheets or obtained through experimental measurements and is expressed as a function of the duration of modulation pulses at a specific duty cycle. After obtaining the value of $R_{th,jc}$ from the thermal impedance characterization, the heat capacity is derived as shown in Equation 31. The linear thermal model is then "excited" by the estimated power dissipation, encompassing both conduction and switching losses (see Eq. 32).

$$Z_{th} = R_{th,jc} || C_{th,j} \longrightarrow C_{th,j}(f_{sw}) = \sqrt{\frac{\frac{1}{Z_{th}^2} - 1}{4\pi^2 R_{th,jc}^2 f_{sw}^2}} \quad (31)$$

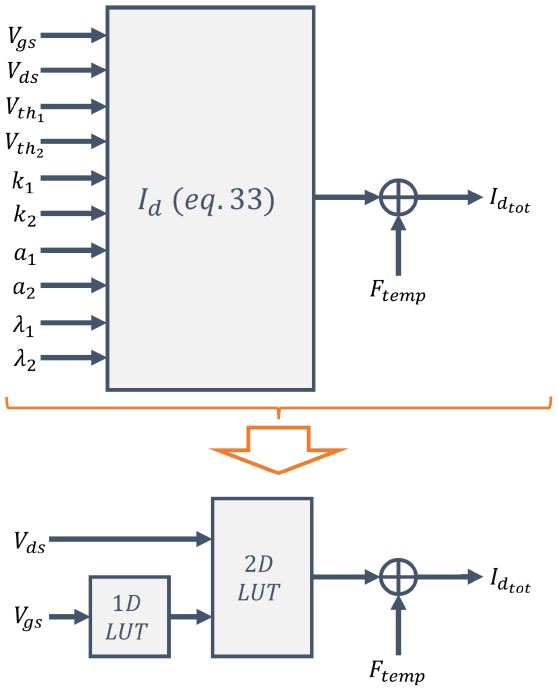


FIGURE 26. Substitution of constitutive equations of Drain current dynamics with 2-D maps in Simulink.

$$\begin{aligned} P_{loss} &= P_{mos} + P_{diode} + P_{C_{gs}} + P_{C_{ds}} + P_{C_{ds}} \\ &= V_{ds}I_d + V_{sd}I_{sd} + V_{gs}I_{C_{gs}} + \dots \\ &\quad \dots + V_{ds}I_{C_{ds}} + V_{gd}I_{C_{gd}} \end{aligned} \tag{32}$$

The current model is computationally intensive, which presents a challenge when simulating complete operating cycles of systems such as inverters, which can be lengthy. To overcome this challenge and reduce the required simulation step size, a simplification of the model is necessary. One approach to simplifying the model is to replace the constitutive equations of the two MOSFETs and the body diode, used in the previous model, with Look-Up Tables (LUTs). This is illustrated in Figures 26 and 27. By utilizing LUTs, the computational load of the simulations can be reduced while still maintaining the accuracy of the model's dynamic characteristics. Furthermore, this simplification streamlines the model creation process, as there is no longer a need to determine the parameters for the equations that define the device.

To create the LUTs, it is sufficient to discretize the relevant characteristics provided in the datasheet. The key aspect in reducing computational complexity is to preserve the

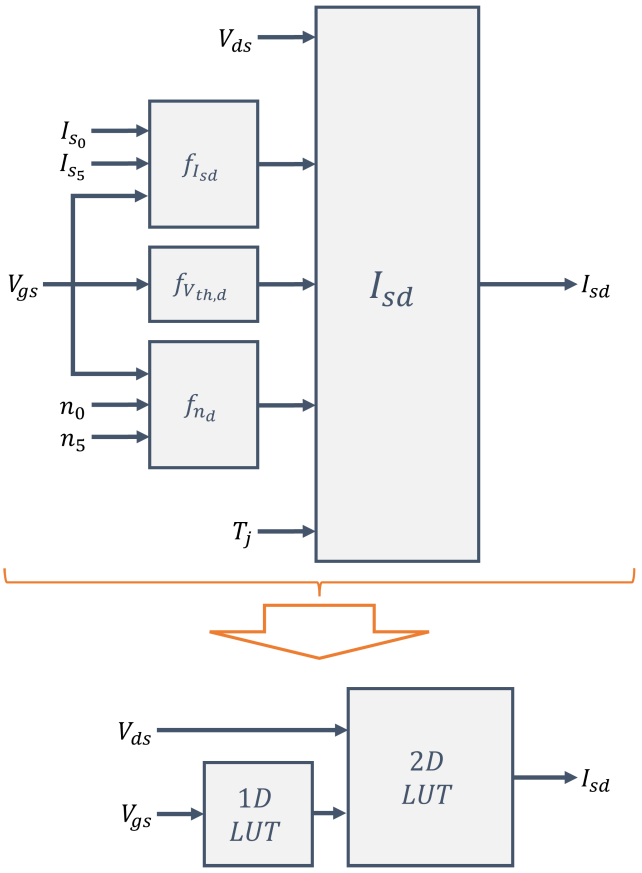


FIGURE 27. Substitution of constitutive of the body-diode behaviour equations with 2-D maps in Simulink.

dynamic I-V characteristic. Therefore, the proposed solution is to quantize the turn-on and turn-off transients using LUTs, while also incorporating the temperature dependency. This is achieved by utilizing an ideal switch model to trigger the switching states. By employing this approach, both the complexity and memory requirements of the model can be effectively managed. The power estimation process drives the linear thermal model to estimate the junction temperature. It is important to note that despite the trade-off between accuracy and simulation time, a certain level of detail is preserved in terms of the interdependence between electrical and thermal variables.

IV. PERFORMANCE OF MODEL IN FITTING EXPERIMENTAL DATA

In this section, the proposed model is evaluated through the simulation of an inverter behavior. The simulation results

$$I_{ch_i} = \begin{cases} 0 & \text{if } V_{GS} < V_{th_i} \\ K_i \left[\left(V_{GS} - V_{th_i}\right) V_{DS} - \dfrac{(1+a_i)\, V_{DS}^2}{2} \right] (1 + \lambda_i V_{DS}) & \text{if } 0 < V_{DS} < \dfrac{\left(V_{GS} - V_{th_i}\right)}{1+a_i} \\ \dfrac{K_i}{2\,(1+a_i)} (1 + \lambda_i V_{DS}) \left(V_{GS} - V_{th_i}\right)^2 & \text{if } 0 < \dfrac{\left(V_{GS} - V_{th_i}\right)}{1+a_i} < V_{DS} \end{cases}$$

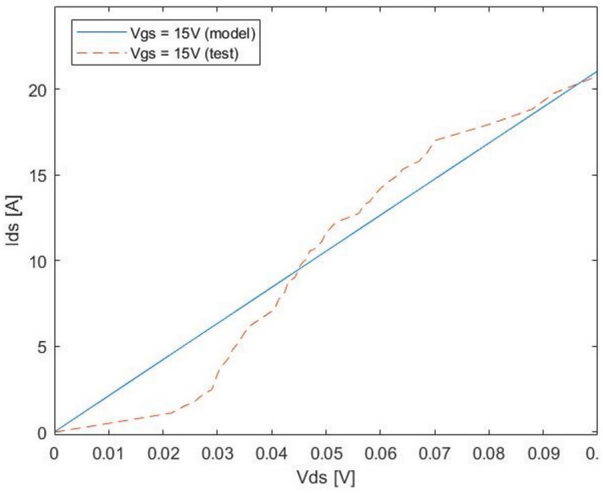


FIGURE 28. Comparison between model and experimental test in static output characterization (direct).

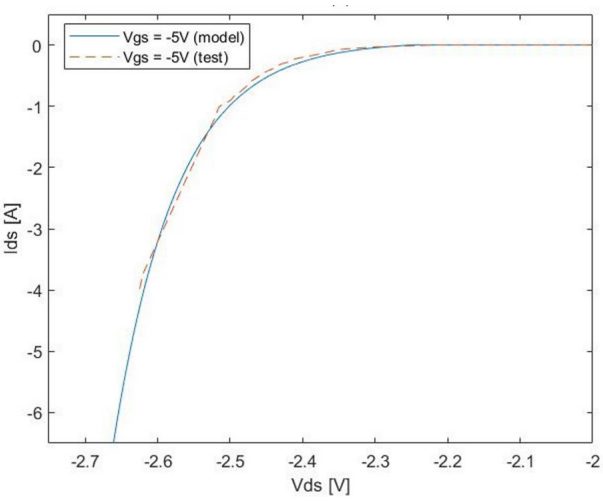


FIGURE 29. Comparison between model and experimental test in static output characterization (inverse).

are compared to experimental data, demonstrating the accuracy of the model and its ability to capture key features while reducing complexity for efficient analysis. Figure 30 illustrates the Simulink block diagram used to replicate the static characterization test of the device. The simulated output characteristics of the device, represented by solid lines, are compared to the experimental data, indicated by dashed lines, in Figures 28 and 29. The output characteristics are evaluated for two different gate voltage values: $V_{gs} = -5V$ and $V_{gs} = 15V$. The transition to the linear and breakdown zones is highlighted in these figures. The test was conducted by varying V_{ds} within the range of $[-3, 0.2]V$, while maintaining both V_{gs} and junction temperature T_j constant. Figure 31 presents the output characteristics of the proposed model at different temperature values, with $V_{gs} = 15V$. These results showcase the response of the model under varying temperature conditions. The model's accuracy in capturing dynamic behavior is demonstrated by comparing the simulated results

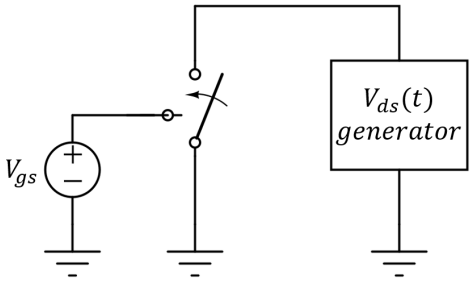


FIGURE 30. Circuit diagram (replicated in Simulink Environment) for generating the static characteristic.

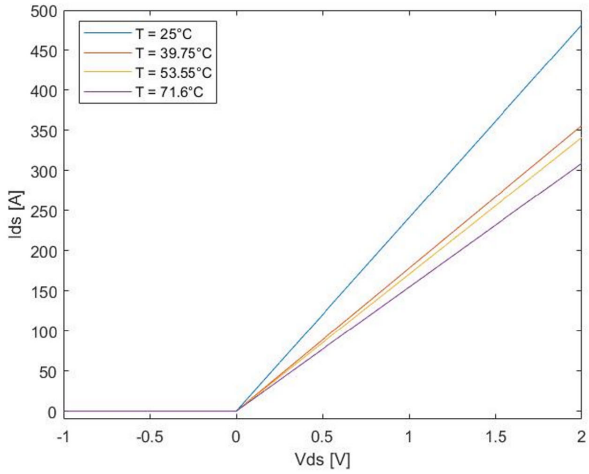


FIGURE 31. Simulation of the static output characteristic with $V_{GS} = 15V$, for $T_j = 25^oC; 39.75^oC; 53.55^oC; 71.6^oC$.

to experimental data for the DPT characterisation. Figure 32 presents the Simulink diagram used to emulate the DPT test conducted during the experimental characterisation. The accuracy of the model in approximating the dynamic behavior of the current on the load is shown in Figure 33. Additionally, Figure 34 compares the simulation results to the experimental measurements for the turn-off transient during DPT. In both figures, it is evident that the model efficiently captures the average current behavior on the load and accurately approximates the switching transients. The root-mean-square-error ($RMSE$) between simulation and measurements is approximately 1.24 A for the dynamic behavior of I_{load}, 2.39 V for the approximate V_{gs} results, and 5.81 V for the approximate V_{ds} results. Furthermore, a comprehensive analysis of the approximation error of switching times (which is necessary for loss estimation) was performed for various operating conditions. The approximation errors obtained for the turn-on and turn-off transients are presented in Tables 14 and 15, respectively. These tables provide valuable insights into the accuracy of the model in capturing the switching behavior of the device. To evaluate the proposed *SiCMOSFET* model's potential, a three-phase inverter circuit with an *LCR* load was simulated using custom blocks in Simulink. The circuit diagram is depicted in Figure 35. The input to the

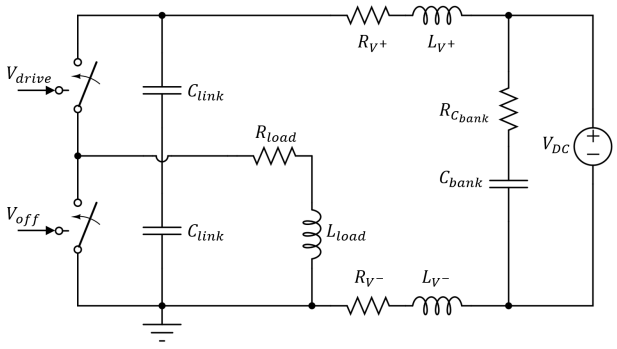


FIGURE 32. Circuit diagram (replicated in Simulink Environment) used to emulate the DPT test.

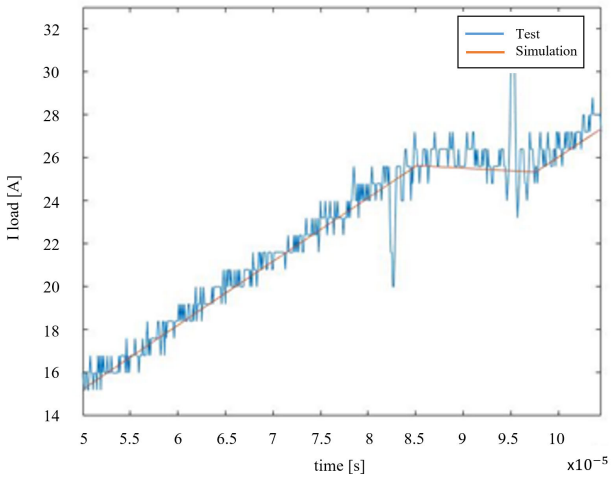


FIGURE 33. Comparison of measured and simulated current during the DPT test conducted at 100V with current $I_{load} = 20A$.

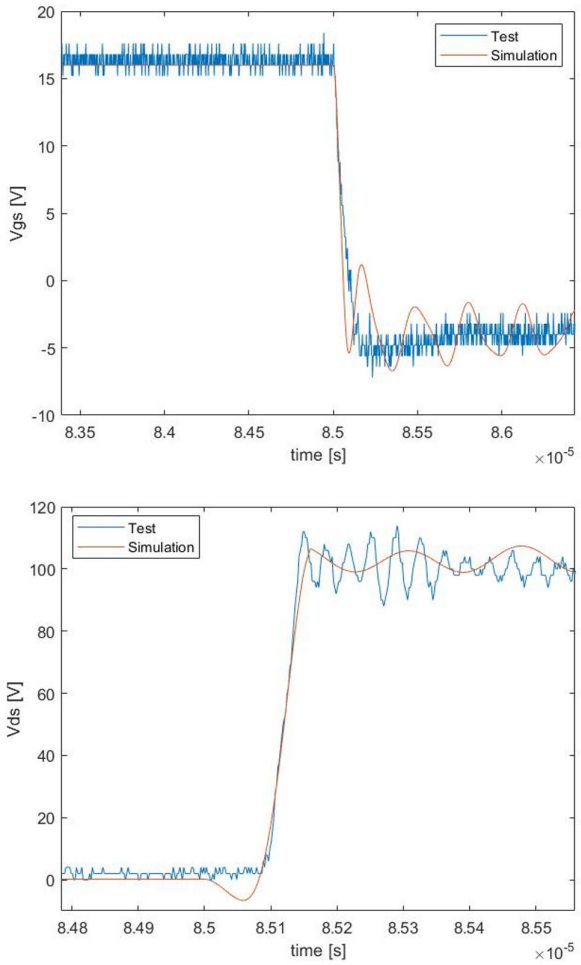


FIGURE 34. Comparison of simulated and experimental turn-off transient during the DPT test at 100V and $I_{load} = 20A$.

TABLE 14. Results from DPT (100 V, 20 A) simulation.

$t_{d,off}$	$t_{d,on}$	t_f	t_r
77.01 [ns]	100.01 [ns]	45.31 [ns]	53.85 [ns]
E_{off}	E_{on}	E_{rr}	
80.41 μJ	278.00 μJ	56.09 μJ	

TABLE 15. Relative turn-on/off errors: model vs. measures.

ϵ_{t_f}	$\epsilon_{t_{d,off}}$	ϵ_{t_r}	$\epsilon_{t_{d,on}}$
13.15 %	9.78 %	12.56 %	11.63 %

inverter is a DC voltage supply, and each phase is connected to an LC filter with a cutoff frequency of approximately $5kHz$ ($L = 100\mu H$, $C = 10\mu F$) and a resistance. The bank capacitance is $850\mu F$, and each link capacitance is $220nF$. The values of the DC voltage and the load resistances depend on the operating power of the system. In the initial operating condition, the output power is $5kW$, resulting in a DC voltage of $150V$ and three load resistances of 4.5ω each. The model's parameters are derived from the DPT conducted at $150V$ and $20A$. To generate the PWM (Pulse Width Modulation) signals for controlling the $MOSFETs$, a comparator receives a triangular waveform with a frequency f_m and three sine waveforms with a frequency of $50Hz$, each out of phase with the others by 120 electrical degrees. The simulations presented below utilize f_m values of $20kHz$ and $40kHz$, a modulation index of 0.8 or 1, a simulation time of 10 seconds, and an integration step time of $1\mu s$. The simulation took 40 minutes to complete, while $LTspice$ took 50 times longer for a similar analysis. Fig. 36 illustrates a system simulation with our integrated $SiCMOSFET$ model in the inverter. It showcases the estimation of instantaneous and average efficiency for a $5kW$ load transfer, operating at $20kHz$ with a modulation index of 0.8. The efficiency of the inverter is calculated using the definition given in Equation 33. Table 16 presents the simulation results for different power transfer conditions, where the switching frequency f_m ranges from $20kHz$ to $40kHz$, and the modulation index varies from 0.8 to 1.

$$\eta = \frac{P_{out,rms} - 6P_{diss,rms}}{P_{in,rms}} \tag{33}$$

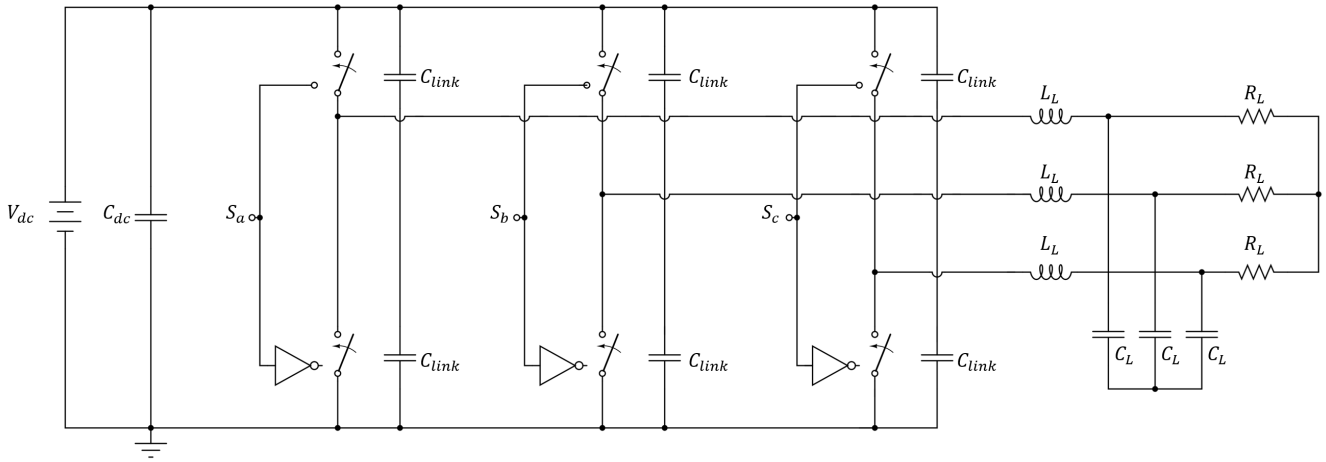


FIGURE 35. Circuit diagram of the Three-phase inverter (used in Simulink environment) including proposed SiC MOSFET model replacing classic switch components.

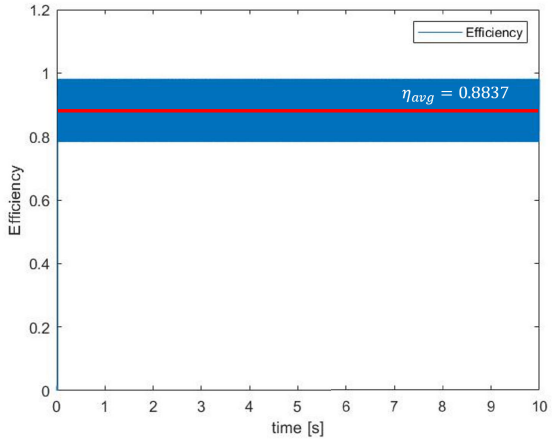


FIGURE 36. Simulation of instantaneous (blue) and average (red) inverter efficiency - in the operating condition of 5 kW transfer to load.

TABLE 16. Simulated inverter efficiency with $P_{out} = 5kW$, within variation of Mod.Index and modulation frequency.

f_m	$Mod.Index$	η	$T_j(t_f)$
20 kH_z	0.8	88.37 %	$\sim 31^oC$
20 kH_z	1.0	93.36 %	$\sim 30^oC$
40 kH_z	0.8	88.25 %	$\sim 31^oC$
40 kH_z	1.0	93.29 %	$\sim 30^oC$

The input power, denoted as P_{in}, is calculated by multiplying the DC voltage with the root mean square (RMS) value of the input current. The output power, represented as P_{out}, is determined by three times the product of the RMS values of current and voltage across the load for a single phase. To estimate the dissipated power, denoted as P_{diss}, only the switching losses of a single MOSFET are considered. To account for all MOSFETs in the inverter, the dissipated power is multiplied by 6. The RMS value of P_{diss} is used for further analysis.

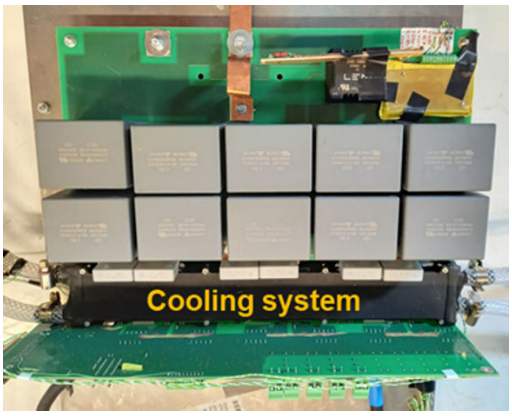


FIGURE 37. Real SiC-based 1200V-400A inverter, used for simulation comparison.

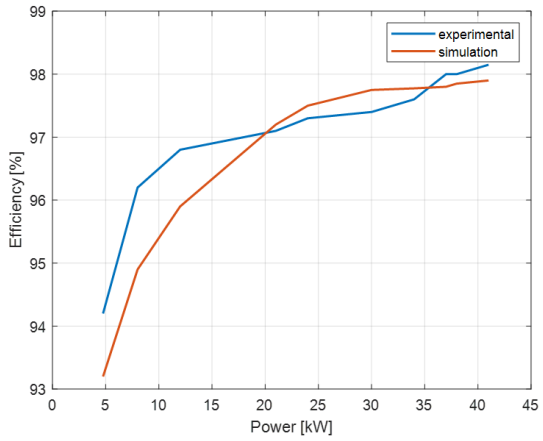


FIGURE 38. Inverter efficiency: experimental measures vs simulated (our model).

The estimated junction temperature $T_j(t_f)$, derived from the linear model T_j at the final simulation time $t_f = 10s$, is denoted as $T_j(t_f)$. It is worth noting that the values presented

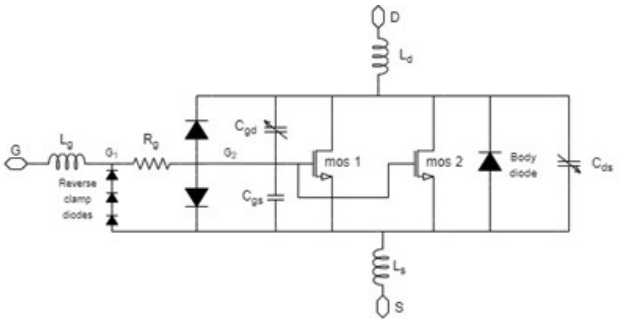


FIGURE 39. p-GAN equivalent circuit model.

in the table align well with the experimental characteristics. In Fig. 38, the efficiency obtained from experimental tests at different power levels transferred to the three-phase load (ranging from $5kW$ to $40kW$) is compared to the results of the circuit simulation using our model. The efficiency estimation obtained with our model exhibits a mean error of $\mu_{err} = \text{mean}(\eta_{\text{real}} - \eta_{\text{sim}}) \approx 0.78$ and a standard deviation of $\sigma_{err} = \text{std}(\eta_{\text{real}} - \eta_{\text{sim}}) \approx 1.85$.

V. EXTENSION TO GaN DEVICES

The GaN MOSFET model can be represented by connecting two NMOS (N-type MOSFET) transistors in parallel. This configuration allows for the division of the MOSFET's conduction operation into two distinct cases: low drain currents and high drain currents. The two NMOS transistors in the model have different threshold voltages and transconductance characteristics. By utilizing this configuration, the proposed model achieves a balance between complexity reduction, computational efficiency, and high accuracy. In the model, both NMOS transistors are represented as voltage-controlled current sources. While the GaN MOSFET model shares similarities with the SiC MOSFET model, there are also notable differences. These differences may arise from variations in the electrical properties, device structure, or other specific characteristics of the GaN MOSFET compared to the SiC MOSFET. The p-GaN HEMT (High Electron Mobility Transistor) exhibits certain unique characteristics compared to other devices. Firstly, the gate of the p-GaN HEMT features a diode structure that limits the gate-source or gate-drain voltage. Secondly, unlike a traditional SJ (Super Junction) MOSFET, the GaN HEMT does not have an intrinsic body diode connecting the source and drain. Instead, when the voltage across the drain-source (V_{DS}) becomes negative, the HEMT reactivates and functions as a diode with a forward voltage that depends on the gate voltage. To accurately capture the behavior in the third quadrant, an additional electrical component is connected in parallel to both MOSFETs, with its threshold voltage influenced by the gate-source voltage (V_{GS}). The dynamic characteristics of the GaN MOSFET can be attributed to three capacitances: the constant capacitance C_{GS}, and the nonlinear capacitances C_{DS} and C_{DG}. The model also incorporates stray inductances to account for parasitic elements at the device terminals. Furthermore, the model includes control mechanisms that monitor the operating conditions. These mechanisms are designed to detect over-voltages (breakdowns), over-currents, excessive temperatures, or prolonged operation outside the Safe Operating Area. The two N-MOS (N-type MOSFETs) in the model are represented as voltage-controlled current sources. The current values are obtained using the classical model that describes the MOSFET's output characteristics in its three possible regions of operation. To evaluate the accuracy of the model created for the *IGO60R070D1 CoolGaN enhancement-mode* Power Transistor by Infineon, the model was used to extrapolate the output static characteristics. Similar to the SiC model, the value of V_{DS} was varied from -9 V to 10 V, while V_{GS} and the junction temperature were fixed at specific values. The values of V_{GS} were obtained from the corresponding I_{GS} values using the I_{GS} vs V_{GS} characteristic. The resulting current values I_{DS} were plotted against V_{DS}. Figure 40 depicts the output characteristic of the model (solid line) compared to the datasheet values (dotted line) for different V_{GS} values. The two output characteristics closely align with each other. To obtain the transfer characteristic of the model, V_{GS} was varied from 0 V to 5 V, while keeping V_{DS} and the junction temperature fixed at specific values. The resulting current values I_{DS} were plotted against V_{GS}. Figure 41 illustrates the transfer characteristic of the model (solid line) compared to the datasheet values (dotted line) for $V_{DS} = 8V$ and $T_j = 125^oC$. The model's transfer characteristic closely matches the values provided in the datasheet. The reverse clamp diode characteristic of the model is obtained by varying the gate-source voltage (V_{GS}) from $-25V$ to $0V$ while keeping the drain-source voltage (V_{DS}) and junction temperature fixed at a certain value. The corresponding current values (I_{GS}) are recorded and plotted. Figure 42 shows the reverse body diode characteristic of the model (continuous line) compared to the one provided by the datasheet (dotted line) for a specific condition of $V_{DS} = 8$ V and $T_j = 25^oC$. It can be observed that the two output characteristics exhibit a significant similarity, indicating that the model accurately captures the behavior of the reverse clamp diodes. This agreement between the model and the datasheet validates the accuracy of the created model in representing the reverse body diode characteristics of the GaN MOSFET. To obtain the gate-source diode characteristic of the model, the gate-source voltage (V_{GS}) is varied from $0V$ to 4.5 V while keeping the drain open and the junction temperature fixed at a specific value. The corresponding current values (I_{GS}) are recorded and plotted. Figure 43 shows the gate-source diode characteristic of the model (continuous line) compared to the one provided by the datasheet (dotted line) for the condition of an open drain and $T_j = 25^oC$. The two output characteristics exhibit a high degree of similarity, indicating the accuracy of the model in capturing the gate-source diode behavior. To characterize the gate-drain diode behavior of the model, the drain-source voltage (V_{DS}) is varied from -4.5 V to $0V$ while keeping the gate-source voltage (V_{GS}) fixed at $0V$ and the junction temperature constant. The resulting

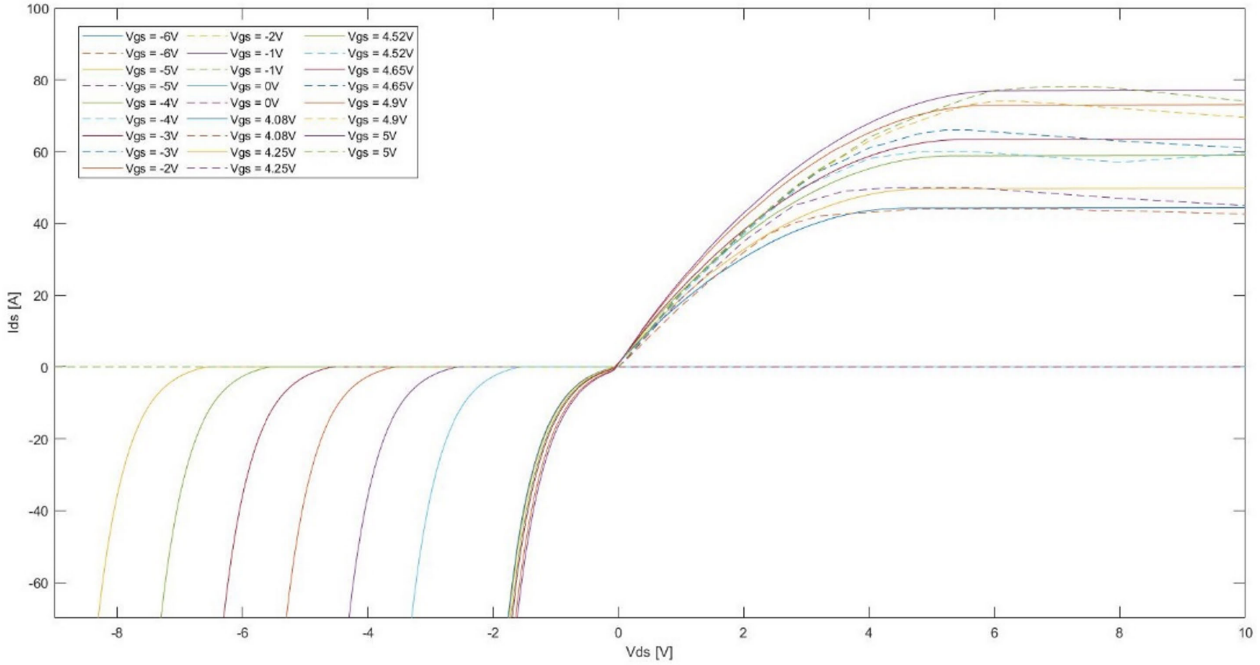


FIGURE 40. Output characteristic for $V_{GS} = -6V, -5V, -4V, -3V, -2V, -1V, 0\ V, 4.08V, 4.25V, 4.52V, 4.65V, 4.9V, 5V$.

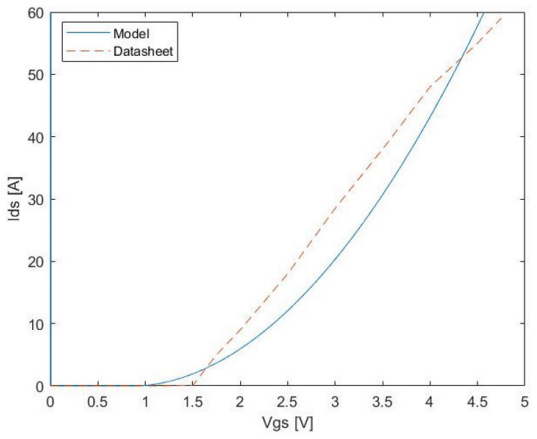


FIGURE 41. Transfer characteristic for T = 125 ^oC.

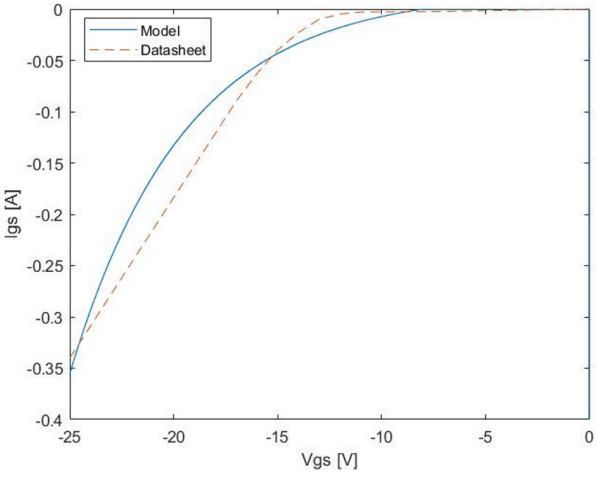


FIGURE 42. Reverse clamp diodes characteristic for $V_{DS} = 8V, T = 125^oC$.

current values (I_{GD}) corresponding to different V_{DS} values are plotted. Figure 44 illustrates the gate-drain diode characteristic of the model (continuous line) compared to the gate-source diode characteristic provided by the datasheet (dotted line), which in this case, is identical to the gate-drain diode characteristic. The plot demonstrates a close match between the two output characteristics, further affirming the accuracy and reliability of the model. To test the dynamic characteristic of the model created the simulation of a DPT was performed. In conclusion, the proposed model accurately captures the characteristics of both the gate-source diode and gate-drain diode of the GaN MOSFET. The model's output characteristics closely match the specifications provided in the datasheet, demonstrating its reliability and agreement with the device's behavior.

As free-wheeling diode was used the model provided by Simulink. The gate driver circuit is the one specified in the datasheet. It is composed by two resistances in parallel ($R_{on} = 5\Omega$ and $R_{off} = 5\Omega$) with a capacitor in series ($C_g = 3.3\ nF$) and a bridging resistance between them ($R_{ss} = 300\Omega$). The load is an inductance of $30nH$ and a resistance of 50Ω. Following the datasheet, V_{DS} is 400 V and V_{GS} is varied between the values 0 V and 12 V. The first pulse turns on the DUT for $2\mu s$. Then it is turned off for $1\mu s$ and turned on again for $1\mu s$. The waveform obtained reflects

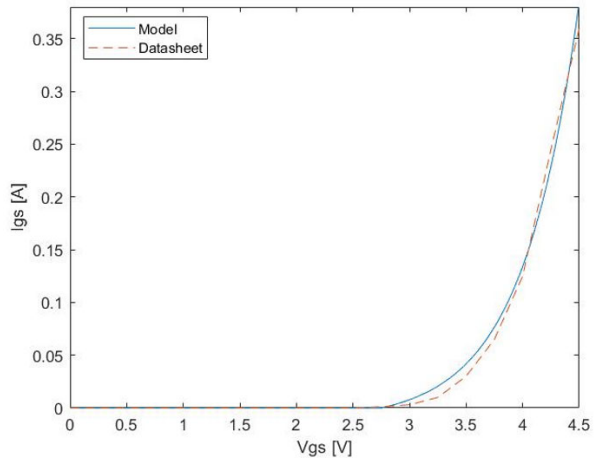


FIGURE 43. Gate-source diode characteristic for Drain open, $T = 25^oC$.

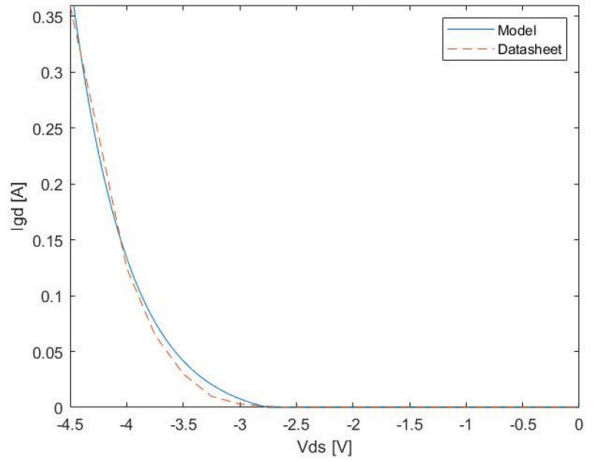


FIGURE 44. Gate-drain diode characteristic for $V_{GS} = 0V$, $T = 25^oC$.

TABLE 17. Obtained parameters for dynamic characteristic.

Turn off		
	Simulation	Datasheet
$t_{d\,\mathrm{off}}$	11.00 ns	14 ns
t_f	11.33 ns	15 ns

Turn on		
	Simulation	Datasheet
t_{don}	11.50 ns	10 ns
t_r	9.20 ns	8 ns

the dynamic behavior of a p-GaN HEMT. The gate current switching waveforms agree with the trend reported in the datasheet. When the device is on, a constant current entering the gate. The dynamic parameters obtained are reported in Table 17.

VI. CONCLUSION

The work presented a step-by-step experimental characterization of a DSC-based SiC MOSFET device for newly developed high-efficiency electric and hybrid vehicles. This characterization extracted key features for an electric-thermal model, aiming to enable multi-scale simulation and fast design of power converters. To overcome the issue of power MOSFETs circuit models, which are often implemented in specific tools and unsuitable for simulations of complex power systems due to excessive simulation time, the problem of computational complexity reduction was addressed. The discussion focused on reducing computational complexity by utilizing 2D maps (LUTs) to store essential characteristics and leveraging ideal switching to trigger the maps, along with algebraic relations that approximate the experimental characteristics. The proposed model integrates electrical and thermal dynamics, providing an approximation of both static and dynamic characteristics. This enables the evaluation of losses during turn-on/off transients and triggers thermal estimation through a reduced-order linear model. Simulation results of the SiC MOSFET model were compared with experimental measurements, demonstrating an error below 1% for efficiency estimation of a 3-phase power inverter ranging from 5 to 40 kW. The entire inverter functionality, simulated for 10 seconds, was completed in 40 minutes using the proposed model. In contrast, performing the same analysis in *LTspice* required a simulation time exceeding 33 hours.

REFERENCES

[1] A. Marzoughi, R. Burgos, and D. Boroyevich, "Investigating impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power industrial motor drives," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1371–1387, Jun. 2019.

[2] C. Ding, H. Liu, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11672–11680, Oct. 2021.

[3] P. Dini and S. Saponara, "Cogging torque reduction in brushless motors by a nonlinear control technique," *Energies*, vol. 12, no. 11, p. 2224, Jun. 2019.

[4] P. Dini and S. Saponara, "Design of adaptive controller exploiting learning concepts applied to a BLDC-based drive system," *Energies*, vol. 13, no. 10, p. 2512, May 2020.

[5] D. Benedetti, J. Agnelli, A. Gagliardi, P. Dini, and S. Saponara, "Design of an off-grid photovoltaic carport for a full electric vehicle recharging," in *Proc. IEEE Int. Conf. Environ. Elect. Eng., IEEE Ind. Commercial Power Syst. Eur.*, Jun. 2020, pp. 1–6.

[6] P. Dini and S. Saponara, "Design of an observer-based architecture and non-linear control algorithm for cogging torque reduction in synchronous motors," *Energies*, vol. 13, no. 8, p. 2077, Apr. 2020.

[7] P. Dini and S. Saponara, "Processor-in-the-loop validation of a gradient descent-based model predictive control for assisted driving and obstacles avoidance applications," *IEEE Access*, vol. 10, pp. 67958–67975, 2022.

[8] C. Bernardeschi, P. Dini, A. Domenici, M. Palmieri, and S. Saponara, "Formal verification and co-simulation in the design of a synchronous motor control algorithm," *Energies*, vol. 13, no. 16, p. 4057, Aug. 2020.

[9] D. Benedetti, J. Agnelli, A. Gagliardi, P. Dini, and S. Saponara, "Design of a digital dashboard on low-cost embedded platform in a fully electric vehicle," in *Proc. IEEE Int. Conf. Environ. Elect. Eng., IEEE Ind. Commercial Power Syst. Eur.*, Jun. 2020, pp. 1–5.

[10] F. Cosimi, P. Dini, S. Giannetti, M. Petrelli, and S. Saponara, "Analysis and design of a non-linear MPC algorithm for vehicle trajectory tracking and obstacle avoidance," in *Applications in Electronics Pervading Industry, Environment and Society*. Berlin, Germany: Springer, 2021, pp. 229–234.

[11] C. Bernardeschi, P. Dini, A. Domenici, and S. Saponara, "Co-simulation and verification of a non-linear control system for cogging torque reduction in brushless motors," in *Software Engineering and Formal Methods*. Oslo, Norway: Springer, 2020 pp. 3–19.

[12] C. Bernardeschi, P. Dini, A. Domenici, A. Mouhagir, M. Palmieri, S. Saponara, T. Sassolas, and L. Zaourar, "Co-simulation of a model predictive control system for automotive applications," in *Proc. Int. Conf. Softw. Eng. Formal Methods*. Cham, Switzerland: Springer, 2022, pp. 204–220.

[13] M. Jin, Q. Gao, Y. Wang, and D. Xu, "A temperature-dependent SiC MOSFET modeling method based on MATLAB/SIMULINK," *IEEE Access*, vol. 6, pp. 4497–4505, 2018.

[14] L. Ceccarelli, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "A fast electro-thermal co-simulation modeling approach for SiC power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2017, pp. 966–973.

[15] M. Alhalabi, A. Rashed, N. B. Iqbal, and A. A. Tarabsheh, "Modelling of SiC power MOSFET in MATLAB, Simulink, and LTSpice," in *Proc. IEEE Int. Conf. Environ. Electr. Eng., IEEE Ind. Commercial Power Syst. Eur.*, Jun. 2018, pp. 1–6.

[16] A. Mostefai and S. B. Abid, "Modeling and electrical characterization of the MOSFETs EKV model using MATLAB," *Carpathian J. Electr. Eng.*, vol. 12, no. 1, pp. 1–10, 2018.

[17] M. M. Hossain, L. Ceccarelli, A. U. Rashid, R. M. Kotecha, and H. A. Mantooth, "An improved physics-based ltspice compact electro-thermal model for a sic power MOSFET with experimental validation," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2018, pp. 1011–1016.

[18] A. Kempitiya and W. Chou, "An electro-thermal performance analysis of SiC MOSFET vs Si IGBT and diode automotive traction inverters under various drive cycles," in *Proc. 34th Thermal Meas., Model. Manage. Symp. (SEMI-THERM)*, Mar. 2018, pp. 213–217.

[19] L. Ceccarelli, R. Kotecha, F. Iannuzzo, and A. Mantooth, "Fast electro-thermal simulation strategy for SiC MOSFETs based on power loss mapping," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo. (PEAC)*, Nov. 2018, pp. 1–6.

[20] L. Ceccarelli, A. S. Bahman, and F. Iannuzzo, "Impact of device aging in the compact electro-thermal modeling of SiC power MOSFETs," *Microelectron. Rel.*, vols. 100–101, Sep. 2019, Art. no. 113336.

[21] T. Cheng, D. D. Lu, and Y. P. Siwakoti, "A MOSFET SPICE model with integrated electro-thermal averaged modeling, aging, and lifetime estimation," *IEEE Access*, vol. 9, pp. 5545–5554, 2021.

[22] Y. Wei and A. Mantooth, "Subcircuit based modelling of SiC MOSFET in MATLAB/SIMULINK," in *Proc. IEEE 12th Energy Convers. Congr. Expo.*, May 2021, pp. 2339–2344.

[23] Y. Wei, D. Woldegiorgis, X. Du, V. S. Machireddy, and A. Mantooth, "Comprehensive investigations on paralleling operation of SiC MOSFETs based on subcircuit model in MATLAB/SIMULINK," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, Aug. 2021, pp. 171–178.

[24] B. Mohamed, E. Elmostafa, and A. A. Imane, "A behavior electrical model of the MOSFET using MATLAB/SIMULINK," in *Proc. 4th Global Power, Energy Commun. Conf. (GPECOM)*, Jun. 2022, pp. 145–149.

[25] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, "Temperature-dependent characterization, modeling, and switching speed-limitation analysis of third-generation 10-kV SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4317–4327, May 2018.

[26] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.

[27] B. Hu, J. Ortiz Gonzalez, L. Ran, H. Ren, Z. Zeng, W. Lai, B. Gao, O. Alatise, H. Lu, C. Bailey, and P. Mawby, "Failure and reliability analysis of a SiC power module based on stress comparison to a Si device," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 727–737, Dec. 2017.

[28] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 71–83, Mar. 2019.

[29] Q. Wu, M. Wang, W. Zhou, X. Wang, G. Liu, and C. You, "Analytical switching model of a 1200 V SiC MOSFET in a high-frequency series resonant pulsed power converter for plasma generation," *IEEE Access*, vol. 7, pp. 99622–99632, 2019.

[30] Y. Wu, S. Yin, H. Li, and W. Ma, "Impact of RC snubber on switching oscillation damping of sic MOSFET with analytical model," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 163–178, Mar. 2020.

[31] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020.

[32] Y. Yan, Z. Wang, C. Chen, Y. Kang, Z. Yuan, and F. Luo, "An analytical SiC MOSFET switching behavior model considering parasitic inductance and temperature effect," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2020, pp. 2829–2833.

[33] V. Talesara, D. Xing, X. Fang, L. Fu, Y. Shao, J. Wang, and W. Lu, "Dynamic switching of SiC power MOSFETs based on analytical subcircuit model," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9680–9689, Sep. 2020.

[34] D. Yuan, Y. Zhang, X. Wang, and J. Gao, "A detailed analytical model of SiC MOSFETs for bridge-leg configuration by considering staged critical parameters," *IEEE Access*, vol. 9, pp. 24823–24847, 2021.

[35] M. Haider, S. Fuchs, G. Zulauf, D. Bortis, J. W. Kolar, and Y. Ono, "Analytical loss model for three-phase 1200 V SiC MOSFET inverter drive system utilizing Miller capacitor-based dv/dt-limitation," *IEEE Open J. Power Electron.*, vol. 3, pp. 93–104, 2022.

[36] A. H. Wijenayake, K. J. Olejniczak, D. Simco, S. Minden, M. Feurtado, B. Passmore, T. McNutt, A. Lostetter, and D. Martin, "Design of a 250 kW, 1200 V SiC MOSFET-based three-phase inverter by considering a subsystem level design optimization approach," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2017, pp. 939–946.

[37] A. B. Jørgensen, N. Christensen, D. N. Dalal, S. D. Sønderskov, S. Beczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM," in *Proc. 19th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Sep. 2017, pp. P.1–P.8.

[38] J. E. Cousineau, K. Bennion, K. Potty, H. Li, R. Na, L. Xu, and J. Wang, "Multi-scale thermal analysis for design of SiC-based medium voltage motor drive," in *Proc. Int. Electron. Packag. Tech. Conf. Exhib.*, vol. 59322, Oct. 2019, Art. no. V001T06A030.

[39] S. Race, T. Ziemann, S. Tiwari, I. Kovacevic-Badstuebner, and U. Grossner, "Accuracy of thermal analysis for SiC power devices," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2021, pp. 1–5.

[40] C. Scognamillo, A. P. Catalano, M. Riccio, V. d'Alessandro, L. Codecasa, A. Borghese, R. N. Tripathi, A. Castellazzi, G. Breglio, and A. Irace, "Compact modeling of a 3.3 kV SiC MOSFET power module for detailed circuit-level electrothermal simulations including parasitics," *Energies*, vol. 14, no. 15, p. 4683, Aug. 2021.

[41] M. F. Rahman, P. Niknejad, and M. R. Barzegaran, "Comparing the performance of Si IGBT and SiC MOSFET switches in modular multilevel converters for medium voltage PMSM speed control," in *Proc. IEEE Texas Power Energy Conf. (TPEC)*, Feb. 2018, pp. 1–6.

[42] H. Rasool, M. El Baghdadi, A. M. Rauf, A. Zhaksylyk, and O. Hegazy, "A rapid non-linear computation model of power loss and electro thermal behaviour of three-phase inverters in EV drivetrains," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion (SPEEDAM)*, Jun. 2020, pp. 317–323.

[43] W. Van De Sande, S. Ravyts, O. Alavi, P. Nivelle, J. Driesen, and M. Daenen, "The sensitivity of an electro-thermal photovoltaic DC–DC converter model to the temperature dependence of the electrical variables for reliability analyses," *Energies*, vol. 13, no. 11, p. 2865, Jun. 2020.

[44] Y. Xu, C. N. M. Ho, A. Ghosh, and D. Muthumuni, "Design, implementation, and validation of electro-thermal simulation for SiC MOSFETs in power electronic systems," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2714–2725, May 2021.

[45] H. Rasool, B. Verbrugge, A. Zhaksylyk, T. M. Tran, M. E. Baghdadi, T. Geury, and O. Hegazy, "Design optimization and electro-thermal modeling of an off-board charging system for electric bus applications," *IEEE Access*, vol. 9, pp. 84501–84519, 2021.

[46] P. Dini and S. Saponara, "Electro-thermal model-based design of bidirectional on-board chargers in hybrid and full electric vehicles," *Electronics*, vol. 11, no. 1, p. 112, Dec. 2021.

[47] P. Dini and S. Saponara, "Model-based design of an improved electric drive controller for high-precision applications based on feedback linearization technique," *Electronics*, vol. 10, no. 23, p. 2954, Nov. 2021.

[48] P. Dini, G. Ariaudo, G. Botto, F. L. Greca, and S. Saponara, "Real-time electro-thermal modelling & predictive control design of resonant power converter in full electric vehicle applications," *IET Power Electron.*, 2023.

[49] P. Dini and S. Saponara, "Review on model based design of advanced control algorithms for cogging torque reduction in power drive systems," *Energies*, vol. 15, no. 23, p. 8990, Nov. 2022.
[50] A. Begni, P. Dini, and S. Saponara, "Design and test of an LSTM-based algorithm for Li-ion batteries remaining useful life estimation," in *Proc. Int. Conf. Appl. Electron. Pervading Ind., Environ. Soc.* Cham, Switzerland: Springer, 2022, pp. 373–379.
[51] N. Zhu, H. A. Mantooth, D. Xu, M. Chen, and M. D. Glover, "A solution to press-pack packaging of SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8224–8234, Oct. 2017.
[52] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017.
[53] S. Pu, F. Yang, B. T. Vankayalapati, E. Ugur, C. Xu, and B. Akin, "A practical on-board SiC MOSFET condition monitoring technique for aging detection," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2828–2839, May 2020.
[54] J. S. Knoll, G. Son, C. DiMarino, Q. Li, H. Stahr, and M. Morianz, "A PCB-embedded 1.2 kV SiC MOSFET half-bridge package for a 22 kW AC–DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11927–11936, Oct. 2022.

PIERPAOLO DINI received the bachelor's degree in industrial engineering and the master's degree in robotics and automation engineering from the University of Pisa, in 2013 and 2016, respectively, and the Ph.D. degree in smart industry from the Department of Information Engineering, University of Pisa, Italy, 2021. He is currently a Researcher with the University of Pisa, and an expert in model-based design for industrial mechatronic systems. His research activity is focused on the development of control and monitoring algorithms, exploiting predictive and machine learning paradigms, for power electronic systems and electrical drives in industrial and automotive applications. He also collaborates in research and development activities with international companies, such as MARELLI, VITESCO, and MAGNA, and in the European Project Hi-Efficient. He is the coauthor of two industrial patents on cyber-security in the automotive environment, released for USA.

SERGIO SAPONARA (Senior Member, IEEE) received the master's (cum laude) and Ph.D. degrees from the University of Pisa, Italy. He is currently a Full Professor of electronics with the University of Pisa. He is also the Director of the I-CAS Laboratory, Crosslab Industrial IoT, the Summer School Enabling Technologies for the IoT. He coauthored more than 300 scientific publications and 18 patents. He is the leader of many funded projects by EU and by companies, such as Intel, Magneti Marelli, Ericsson, and PPC. In 2012, he was a Marie Curie Research Fellow of IMEC. He is an IEEE Distinguished Lecturer and co-founder of special interest group on the IoT of both IEEE CAS and SP societies. He is an associate editor of several IEEE and Springer journals.

SAJIB CHAKRABORTY (Member, IEEE) received the B.Sc. and M.Sc. degrees (Hons.) in electrical and electronic engineering from Independent University, Bangladesh, Dhaka, Bangladesh, in 2013 and 2016, respectively, and the Ph.D. degree (Hons.) from Vrije Universiteit Brussel, Belgium, in April 2022. Currently, he is working as a senior researcher and digital twin and reliability (DTR) division lead at the Efficient Power Electronics, powertrain, and energy solutions- EPOWERS research group in the MOBI research center. His activities include research and technical lead of EU and nationally funded projects focusing on the design-for-reliability, lifetime testing, and predictive health management of automotive converters, cloud-connected digital twin design and AI-based modeling of the powertrain components, and situationally-aware advanced battery management systems (BMS). He is the author and co-author of more than 60 scientific publications and is a young professional member of IEEE, IEEE PELS, and EPE.

FARZAD HOSSEINABADI was born in Isfahan, Iran. He received the B.Sc. degree in electrical engineering (power) from the University of Kashan and the M.Sc. degree in electrical engineering (power electronics and electric machines) from the Isfahan University of Technology (IUT), Isfahan, in 2018. He is currently pursuing the Ph.D. degree. From 2018 to 2019, he was a Researcher with the Industrial Electronics Laboratory, IUT. He is with the EPOWERS Research Group, MOBI Research Centre, Vrije Universiteit Brussel (VUB), Brussels, Belgium. He was involved in several industrial projects and a research and development engineer in industry for two years. His research interests include reliability assessment and electro-thermal modeling of power electronics converters.

OMAR HEGAZY (Senior Member, IEEE) received the Ph.D. degree (Hons.) from the Department of Electrical Engineering and Energy Technology (ETEC), Vrije Universiteit Brussel (VUB), Belgium, in July 2012. He is currently the Head of the Efficient Power Electronics, Powertrain and Energy Solutions (EPOWERS) Research Group, Power Electronics Innovation Laboratory (PEIL), Powertrain Innovation Laboratory (PIL), and Joint Smart Charging Laboratory (JSCL), Department of ETEC, and the MOBI Research Centre, where he coordinates the research activities in this field in several national projects, such as Flanders Make, VLAIO (ex. IWT), Innoviris, and Flux50, and European projects, such as SAFEDRIVE, UNPLUGGED, ELIPTIC, ORCA, ASSURED, HiFi-Elements, GHOST, HiPERFORM, CEVOLVER, OBELICS, ACHILES, LONGRUN, eCharge4drivers, iSTORMY, URBANIZED, HiEFFICIENT, NextETRUCK, SiC4GRID, ZEFES, EBRT2030, OpEVA, and NEMOSHIP. He is also the Manager of the MOBI Core-Laboratory, Flanders Make organization. He is the author of more than 200 scientific publications and two patent applications. His research interests include power electronics, electrical machines, electric and (plug-in) hybrid electric vehicles, digital twin (DT), charging infrastructure, power/energy management strategies, FC (hydrogen) powertrains, battery management systems (BMS), V2X systems, optimization techniques, and smart dc grid with renewable energy. He is a member of EGVIA, EARPA, Inside (ARTEMIS-IA), EPE, SAE, and IEC standards.