IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 14 July 2023, accepted 19 July 2023, date of publication 24 July 2023, date of current version 28 July 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3298052

RESEARCH ARTICLE

Simultaneous High-Efficiency Power Delivery and Energy-Efficient Forward Data Transmission Over Single Inductive Link

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This work was supported by the National Key Research and Development Program of China under Grant 2022YFF1202302.

ABSTRACT This paper presents a system for simultaneous wireless power and data transfer (SWPDT) over a single inductive link. We design the frequency-splitting inductive link to address the trade-off between high power transfer efficiency (PTE) and high data rate (DR). An active rectifier is designed for high power conversion efficiency. Forward data communication is based on frequency-shift keying (FSK) modulation to support high DR transmission while delivering uninterrupted power. Moreover, we proposed low-power FSK demodulation circuits to further improve the energy efficiency of the data demodulation. The system is implemented with 180nm CMOS process and occupies an area of 0.836mm^2. The post-layout simulation results show that the overall PTE (including the resonant tanks and the active rectifier) of the SWPDT system can be up to 76.5% while delivering 40mW power to the load. Meanwhile, a data rate of 1.11Mbps can be achieved. The power consumption for data demodulation is 69.1μW, showing an energy efficiency of 62.2pJ/bit. The proposed SWPDT system based on a single inductive link shows potential for implantable biomedical applications.

INDEX TERMS Simultaneous wireless power and data transfer (SWPDT), frequency splitting, energy efficient, active rectifier, injection lock, shifted limiter.

I. INTRODUCTION

IN the past few decades, wireless power transfer (WPT) technology has shown a wide range of applications in people's life, such as various mobile devices, home appliances, electrical vehicles, and especially in implantable medical devices (IMDs) [1], [2], [3]. Among all WPT technologies, inductive links are the most widely used compared to RF, optical, ultrasonic, and capacitive links [4], [5], [6]. Inductive links are simple, reliable, and highly secure, and are the commonly used technology in commercial IMDs. System on chip (SOC) is the trend in today's IMDs application for the low cost and high level of integration. Data and power can be transferred from the external system to the implant via inductive coupling to provide the stimulus signal and power. For most applications in IMDs, simultaneous wireless power and data transfer (SWPDT) is essential. However, designing an efficient SWPDT system can be challenging as we must consider the fundamental trade-offs between high data rates(DR), high power transfer efficiency(PTE), high power delivered to the load (PDL), and low power consumption [3], [7], [8]. For instance, to increase PTE, we require a higher quality factor (Q) of the inductive coils, but this will limit the bandwidth of the data transmission. Using multiple links for SWPDT is a possible solution for this trade-off, as we can design the power and data links separately. Some state-of-the-art works [10], [11], [12] have been reported using multiple links for SWPDT design, unfortunately, these designs are

The associate editor coordinating the review of this manuscript and approving it for publication was Ahmed F. Zobaa.

complex to implement and suffer from crosstalk between the different links [10]. Therefore, for the requirement of simpler design and smaller size of IMDs, it is necessary to design SWPDT over a single inductive link and to address this trade-off at the same time [13], [14], [15], [16], [17].

How to solve the trade-off between high PTE and high DR mentioned above in the single-link SWPDT is a popular study topic. Since data and power transmission in the SWPDT system is based on carrier modulation, the above trade-off can be considered to be solved in terms of modulation methods [7], [8]. For downlink data communication, the most common carrier modulation methods are amplitude-shift keying (ASK), frequency-shift keying (FSK), and phase-shift keying (PSK) [18], [19]. These modulation methods have their pros and cons. For example, ASK modulation is widely used for its simplicity and low power dissipation. However, its ability to suppress noise interference is weak. The on-off keying (OOK) can be used as a special type of ASK modulation with a modulation index of 100% for better immunity to interference. However, the bandwidth BW of data transmission for ASK and its derivation forms is limited by the carrier frequency and Q of secondary coil, which can be expressed as [7]

$$BW = \frac{f_c}{Q}. \tag{1}$$

where f_c is the carrier frequency. FSK and PSK can achieve continuous power transmission and have good anti-noise interference ability due to their constant envelope amplitude, and also support high data rate transmission. However, their demodulation circuits are often complex and power-hungry. Some new modulation methods are proposed such as pulse harmonic modulation (PHM) and Return-to-Zero modulation [20]. Although they support high DR (up to 200 Mb/s), they do not support simultaneous power transmission. The Carrier Width Modulation (CWM) mentioned in [9] achieves high DR and low-power consumption, but the PTE for power recovery is not high.

For the reverse transmission of data, a common modulation method is load-shift keying (LSK) [21], which has a simple design and low power consumption. In recent years, such as cyclic on-off keying (COOK) [7] and passive phase-shifting keying (PPSK) [8] are proposed. COOK is considered to be the most suitable solution, which solves the trade-off between PTE and DR. However, it is only applied to reverse data communication and the corresponding demodulation circuits haven't been designed.

The SWPDT methods presented above are based on the resonant frequency point of the inductive link and they operate in the weakly coupled region [22], [23]. In recent years, some SWPDT systems based on inductive links with frequency-splitting characteristics have been proven to be feasible and have demonstrated excellent performance [16], [17]. However, the point-point FSK (PP-FSK) in [16] makes the PTE degraded and its demodulation circuit is complex; the flat region FSK (FR-FSK) in [17] solves the trade-off between PTE and DR, but the system has some problems: (1) the system operation is limited by the close coil separation distance(5mm). (2) the output of the passive rectifier is not regulated. (3) the demodulator dissipates too much power.

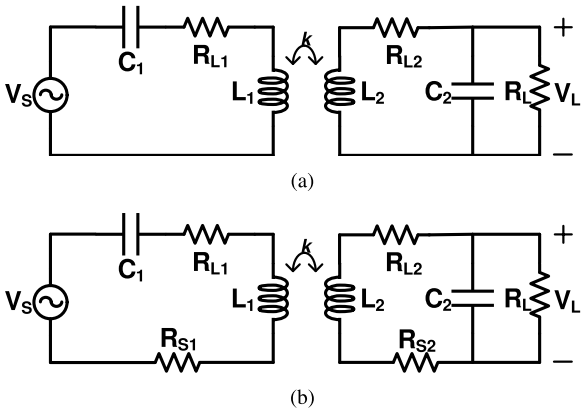


FIGURE 1. (a) general circuit diagram of the wireless series-parallel inductive link (b) circuit diagram of the wireless link for our design.

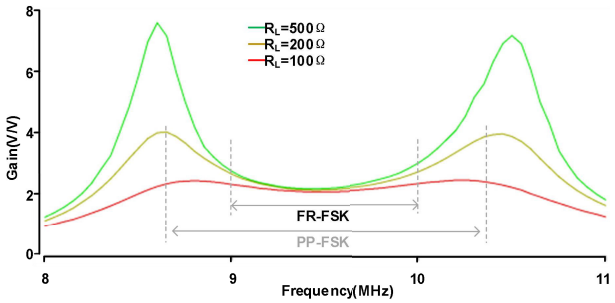
In this paper, we propose an SWPDT SOC to be used in RF front-end circuits of IMDs, such as electrically stimulated neural prostheses, cochlear implants, etc., where an external controller can send stimulus data and power to the implants. In order to reduce electromagnetic field absorption and human tissue safety considerations, the carrier frequency does not exceed 10MHz [12]. And in order to address the above-mentioned problems, the proposed SWPDT system inductive link is based on frequency splitting characteristics. Our SWPDT system achieves high PTE, high DR, and low power consumption. We use an active rectifier for power transmission and a low-dropout (LDO) regulator to regulate the DC output while supporting power for the whole system simultaneously. For data transmission, to reduce power consumption and improve energy efficiency, we mainly take advantage of injection-locked ring oscillators and a low-power ASK demodulation circuit. The proposed SWPDT system supports 1.11 Mbps data communication while dissipating only 69.1μW for data demodulation, showing an energy efficiency of 62.2 pJ/bit. Simultaneously, the overall power transfer efficiency is up to 76.5% (including the resonant tanks and the active rectifier losses) while delivering 40mW power to the load.

The rest of this paper is organized as follows. Section II presents the design and simulation result of the inductive link and the overall architecture of our proposed SWPDT system. Section III presents the related circuit implementations. Section IV shows the simulation results. Finally, the conclusions are drawn in Section V.

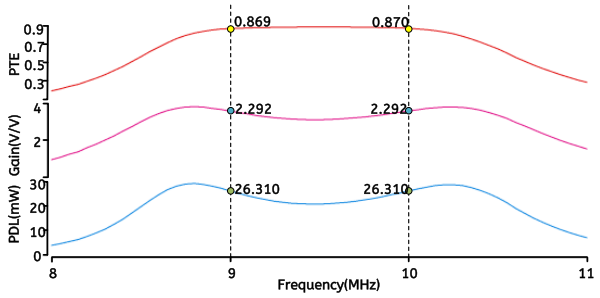
II. LINK CHARACTERISTICS AND SWPDT SYSTEM ARCHITECTURE

A. LINK CHARACTERISTICS

Conventional SPWDT systems operate on the resonant frequency of the inductive link and the inductive coupling is



(a)



(b)

FIGURE 2. (a) link gain curves with different loads (b) the PTE, link Gain, and PDL curves with load $R_L = 100\Omega$.

TABLE 1. The simulated value of the symbol in Figure1(b).

Symbol	Value	Symbol	Value
L_1	1.6uH	L_2	300nH
C_1	180pF	C_2	925pF
R_{L1}	0.8Ω	R_{L2}	0.2Ω
R_{s1}	0.2Ω	R_{s2}	0.2Ω
k	0.2	R_L	100Ω
$\|V_S\|$	1V		

in the weak coupling region. However, frequency splitting occurs in the strongly coupled region, where the maximum delivered power is available at two frequency splitting points [22], not at the resonant frequency. In this paper, we use the series-parallel resonance model to briefly illustrate the link characteristics of the frequency-splitting-based inductive coupling. A general circuit diagram of a series-parallel inductive link for the WPT system is shown in Fig. 1(a), where R_{L1} and R_{L2} are the parasitic resistances of inductors L_1 and L_2 respectively, and C_1 and C_2 are the resonant capacitors. When the coupling coefficient $k = 0$, the resonant frequency ω_0 satisfies

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}. \tag{2}$$

The quality factor Q_{L1} and Q_{L2} of the inductor L_1 and L_2 are defined as equation (3) respectively.

$$Q_{L_1} = \frac{\omega_0 L_1}{R_{L1}} \quad and \quad Q_{L_2} = \frac{\omega_0 L_2}{R_{L2}}. \tag{3}$$

When the coupling coefficient k satisfies $k > k_c$, two sides resonate at

$$\omega_{1,2} \approx \frac{\omega_0}{\sqrt{1 \pm k}}. \tag{4}$$

k_c is roughly inversely proportional to the Q_{RL} of the load impedance [16], which can be simply expressed as

$$k_c = \frac{1}{Q_2} \approx \frac{1}{Q_{RL}} = \frac{\omega_0 L_2}{R_L}. \tag{5}$$

when $Q_{RL} \ll Q_{L2}$, where Q_2 is the quality factor of secondary side. Therefore, to obtain a small and reasonable value of k_c, the load R_L should be slightly larger. The relationship between the coupling coefficient k and the distance d is considered as follows [16], [21]

$$k \approx \left(\frac{r_{\mathrm{TX}} r_{\mathrm{RX}}}{d^2 + r_{\mathrm{TX}}^2 + r_{\mathrm{RX}}^2} \right)^{3/2} \cos\theta. \tag{6}$$

where r refers to coil radius and d refers to the separation distance between the two coils, and θ is the angle between the planes of the coils. The k is larger than 0.3 in [17], which limits the separation distance of the coil to 5mm. To make the distance range of the link wider, k is not very large in our design. We choose $r_{L1} = r_{L2} = 1.5$cm for smaller coil sizes and $k = 0.2$ for a typical strong coupling range. According to equation (6), the coil distance $d \approx 1.45$cm when the center of the coils is coaxial. This distance is already suitable for most IMD applications. Misalignment of the inductor coils will reduce the k. However, the frequency splitting characteristic still exist when k satisfies $k > k_c$. Therefore, we need to adjust the coil distance to reduce the effect of misalignment depending on the situation in practice.

To make the link more realistic and conservatively estimate the link characteristics (especially the PTE), we consider the parasitic resistance of the power supply as well as the wires. The designed link model is shown in Fig. 1(b), where R_{s1} and R_{s2} are the parasitic resistances of the link respectively. The component parameters of the link are shown in Table 1. We simulated the characteristics of the designed link and the results are shown in Fig. 2. Fig. 2(a) shows the link gain curves with different loads R_L. We choose the flat region of the link gain (the frequency region where the gain does not exceed 10% of the lowest gain) for power and data transfer. In our design, the carrier frequencies are chosen as $f_{flat,low} = 9$MHz and $f_{flat,high} = 10$MHz so that the spacing in frequency is large enough to be distinguished by the subsequent demodulation circuit. Fig. 2(b) shows the curves of the PTE, link Gain, and PDL of the link at a load $R_L = 100\Omega$. The simulation result shows that the PTE of the designed link is 86.9%, while the gain is 2.29. It is worth noting that the efficiency of the link is affected by the Q of the inductor coils on two sides, whereas a change in capacitance will only affect the frequency of the two resonant peaks and do not affect the PTE.

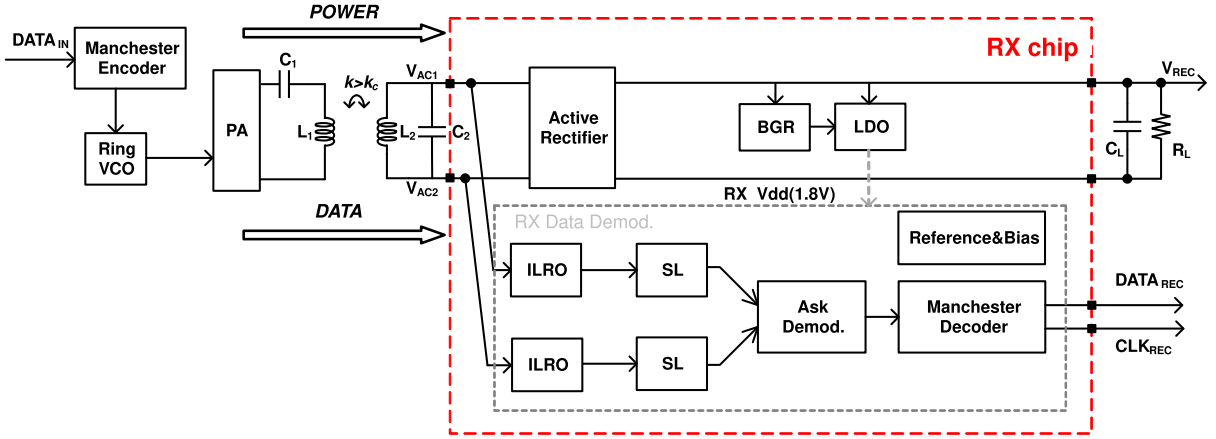


FIGURE 3. Overall architecture of the proposed SWPDT system.

The figure of merit (FOM) for power transmission of the designed link is [15]

$$FOM = \frac{(PTE)^2 \times PDL}{(V_S)^2} = 19.9 \tag{7}$$

For power transmission, we obtained the FOM value comparable to that in [17], which is 20.94 and it is 38.7 times compared to prior arts using a single inductive link [17]. For data transmission, our link also has sufficient bandwidth to support high DR communication. These results indicate that the link with frequency-splitting characteristics is suitable for SWPDT system.

B. OVERALL ARCHITECTURE

The proposed SWPDT system architecture is shown in Fig. 3. We utilized the link parameters discussed above and designed the Receiver chip for power and data transfer. We encoded the data in Manchester-coding so that the clock and data could be easily recovered in synchronization. Then the coding data converted into an FSK signal by the ideal voltage-controlled oscillators (VCO), which is transmitted to the RX side through an inductive coupling link with frequency-splitting characteristics. Since the voltage gain of the link is the same at two frequencies, it makes the power carrier envelope which contains data modulation information has no significant difference in amplitude and the rectifier can operate at the optimum input amplitude. The carrier is rectified as an output of DC voltage by the active rectifier with high power conversion efficiency(PCE) and high voltage conversion ratio(VCR). Then the low-dropout (LDO) regulator regulates the DC output and provides supply power for the whole data demodulation circuit. The carrier is also fed to two injection-locked ring oscillators (ILROs) for converting the FSK signal to the ASK signal and shifted limiter (SL) receives the ASK signal and deepens the modulation depth (MD). Then, the ASK demodulator decodes the ASK signal. Finally, the data and clock signal are recovered by the Manchester decoder.

III. CIRCUIT IMPLEMENTATION

A. ACTIVE RECTIFIER WITH ADAPTIVE DELAY COMPENSATION

As the main stage of power transmission, the rectifier converts the input AC voltage to the DC voltage source and it determines the dynamic performance of the whole system. Instead of conventional bridge rectifiers, an active rectifier is a better choice since it achieves high PCE and VCR [24]. For an active rectifier operating in mega-hertz, circuit propagation delays caused by comparators' limited bandwidth and large parasitic capacitors of power MOSFET severally decrease the dynamic performance. The MOSFET turn-on delay (on-delay) limited the effective conduction time (TCOND) and leads to lower VCR. The MOSFET turn-off delay (off-delay) results in reverse current and degrades PCE. Moreover, the propagation delays are various under different processes, voltage, and temperature (PVT) conditions [25]. Therefore, it is important to realize adaptive delay compensation to guarantee the performance of the active rectifier.

To gain high PCE and VCR and overcome the on/off-delay problems, an active rectifier with adaptive delay compensation is adopted, which schematic is shown in Fig. 4 (a). It contains a pair of cross-coupled PMOS M_{P1} and M_{P2}, a pair of active diode NMOS M_{N1} and M_{N2}. The push-pull comparator (CMP), which is shown in Fig. 4(b), controls M_{N1} and M_{N2} to realize zero voltage switching (ZVS) operations by V_{GN1} and V_{GN2} respectively through buffers. A pair of on/off-delay compensation loops are implemented to eliminate NMOS turn-on and -off delay, which is the same as [25]. In the design, we set $M_{N1} = M_{N2} = 1\text{mm}/180\text{nm}$ and $M_{P1} = M_{P2} = 2\text{mm}/180\text{nm}$. R_L and C_L is off-chip loading resistor and capacitor. A peaking current source (PCS), which is shown in Fig. 4 (c), is adopted to provide supply

voltage-independent current bias for the rectifier [26]. We set $R_{PCS} = 50\text{K}\Omega$ in this design and the I_B is approximately 2μA.

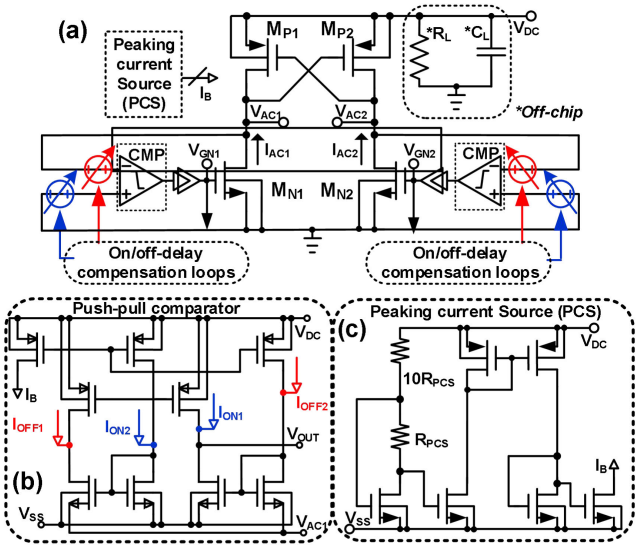


FIGURE 4. The schematic of (a) active rectifier (b) push-pull comparator and (c) peaking current source.

B. FSK-ASK CONVERSION WITH ILROS AND SHIFTED LIMITERS

The conventional method of FSK signal demodulation is relatively complex and has high power consumption [16]. In this paper, we utilized ILROs to realize the FSK-ASK conversion for simple and low-power consumption demodulation. This technique has been widely used in demodulation and frequency generation as it has obvious advantages in low-power applications [27], [28], [29]. The basic principle of ILRO is shown in Fig. 5. A free-running ring oscillator (RO) with a frequency of f_0 is injected with a signal of frequency f_{inj}, when f_{inj} is in the locking range (f_0-$f_L < f_{inj} < f_0 + f_L$), the output envelope of RO is constant, whereas in the injection pulling range ($f_{inj} < f_0 - f_L$ or $f_{inj} > f_0 + f_L$), the output envelope has the amplitude modulation phenomenon [29]. For studies on the injection locking range f_L, see [30], which is outside the scope of this paper. It is worth noting that during the injection locking state, the output amplitude "A" of the oscillator is inversely related to the injection frequency f_{inj}, satisfying [31]

$$A = K \cdot \left(\frac{1}{f_{inj}} - \frac{1}{f_0} \right) + A_0. \tag{8}$$

where A_0 is the output amplitude of the oscillator on the free operation and K is a constant, determined by the load charge and discharge. Unlike exploiting the difference in RO output envelope characteristics between the injection-locked and injection-pulled states in [29] and [31], we take advantage of the constant envelope characteristics in the injection-locked range to achieve FSK-ASK conversion. Therefore, our design makes the injection frequencies f_{inj} all lie within the injection-locked range.

As shown in Fig. 6, a three-stage injection-locked ring oscillator with low power consumption and a wide

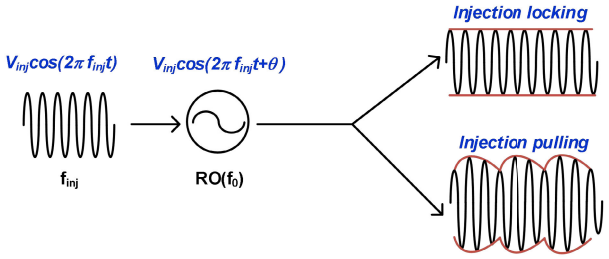


FIGURE 5. Injection locking and injection pulling state of ILRO.

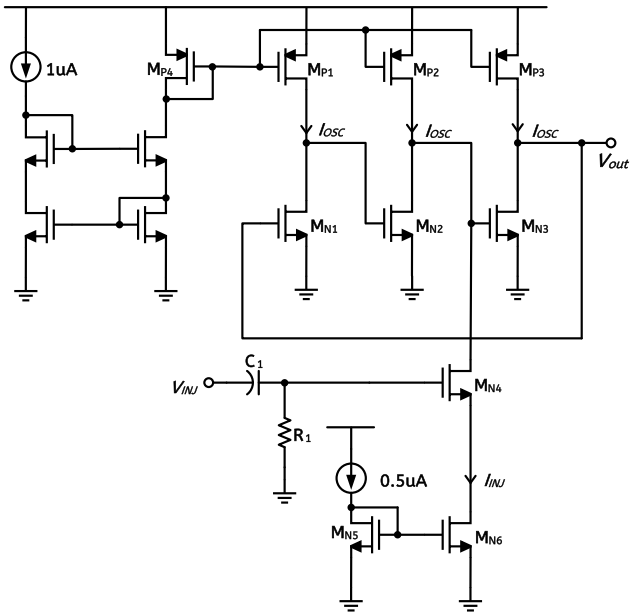


FIGURE 6. Circuit of the ILRO.

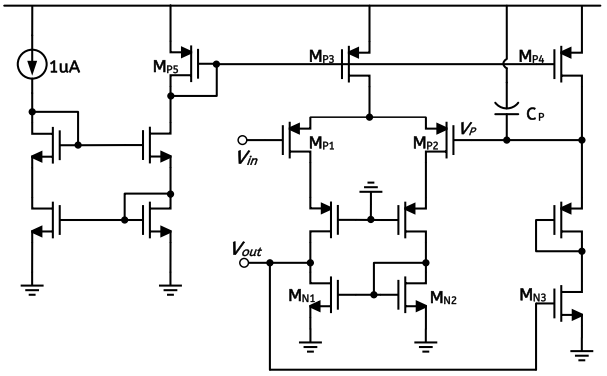


FIGURE 7. Circuit of the SL.

injection-locked range is designed [17], [29]. The free oscillation current of each RO stage is $I_{osc} = 1\mu$A. The carrier signal from the LC tank is filtered by a high-pass filter and injected into the ring oscillator by NMOS with the injection strength of $I_{inj} = I_{osc} = 1\ \mu$A, which is achieved by a simple current mirror. To avoid large deviations in the free oscillation frequency, resulting in the injected signal outside the injection locking range and losing the constant output envelope, the current of each stage is controlled by a Wilson current mirror. The FSK-ASK conversion is achieved by two phase-opposite ILROs for stability and high DR communication. This method for FSK demodulation takes advantage of

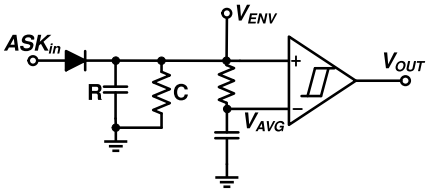


FIGURE 8. Typical ASK demodulator circuit.

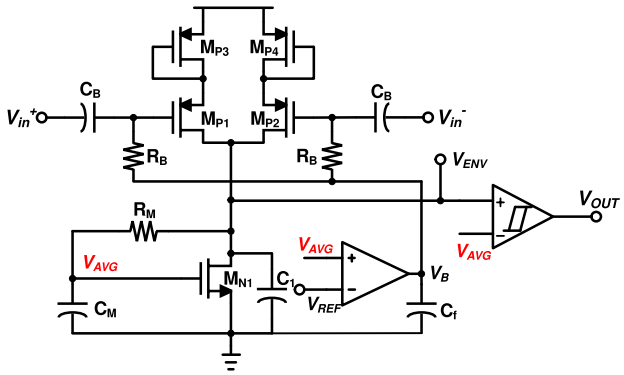


FIGURE 9. Proposed ASK demodulator circuit.

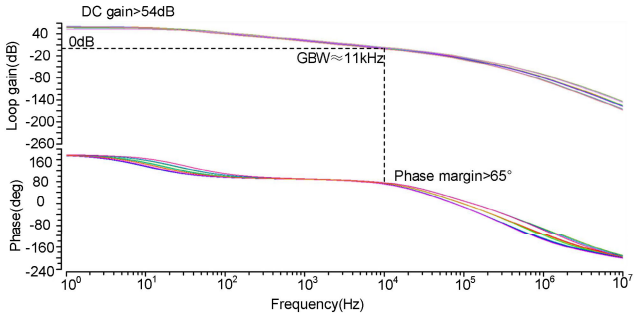


FIGURE 10. Bode plot of the demodulator under PVT variation.

both FSK and ASK modulation, thus not only enabling uninterrupted power transmission but also reducing demodulation complexity and power consumption. The average power consumption of an ILRO is 7.3μW with a 1.8V supply.

The modulation depth (MD) of the ASK signal is defined as MD = $(V_H$-$V_L)/(V_H + V_L)$, where V_H and V_L are the amplitude of data "1" and data "0" respectively. The consequence of low MD is that it is easy to bring demodulation BER. Therefore, as shown in Fig. 7, we use the shifted limiter similar to [14] to increase the MD. The circuit mainly consists of a differential pair of current mirror loads ($M_{P1,2}$, $M_{N1,2}$) and a feedback loop. The feedback loop consists of M_{N3} and capacitor C_P, and M_{P3} is used to vary the feedback loop current to control the bandwidth of the entire SL [32]. The amplification of the MD by the SL is mainly based on the principle that the envelope signal conversion gain is higher than the carrier conversion gain in the linear range. The MD of the ASK signal from ILRO is increased from 4.7% to 10.9% by the designed SL, which is a suitable depth for envelope demodulation, while the average power consumption of an SL is 7.7μW with a 1.8V supply.

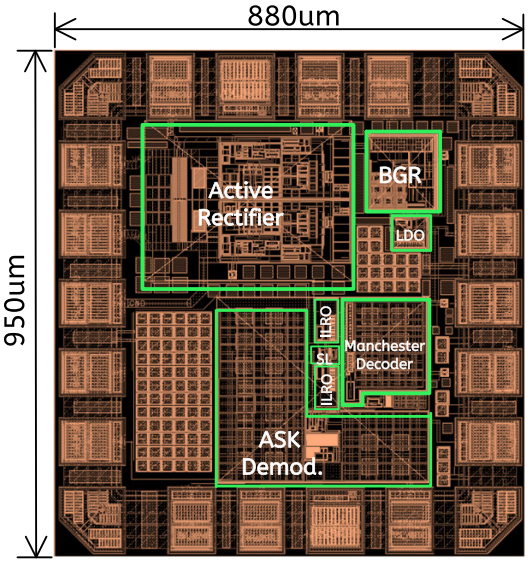


FIGURE 11. Layout of the proposed SWPDT system.

Our designed FSK-ASK conversion circuit, which does not require an exact frequency reference, is achieved by two phase-opposite ILROs with a wide injection locking range. It also reduces the MD requirement of the ASK demodulation circuit, which is achieved by a P-type shifted limiter.

C. ASK DEMODULATOR WITH LOW POWER CONSUMPTION AND HIGH DR

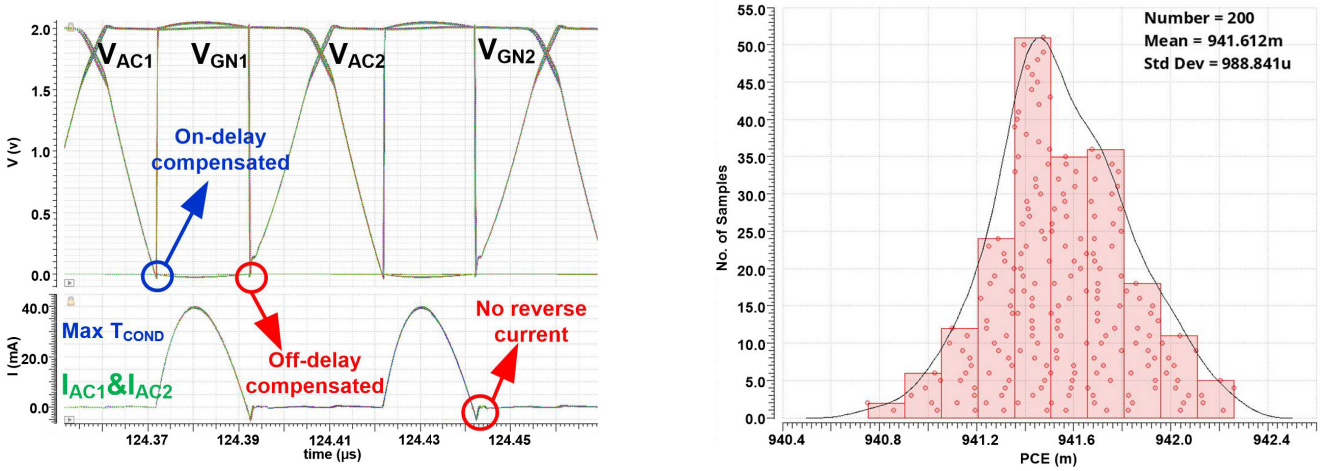
ASK modulation is a widely used method due to its simplicity and the demodulation circuit usually consists of an envelope detector (ED) and a comparator. However, implementing an envelope detector demodulation circuit with a high DR, low MD, high conversion gain, and low power consumption can be challenging [3], [21], [33], [34].

A typical ASK demodulation circuit is represented in Fig.8. It consists of an ED, a passive low-pass filter, and a hysteresis comparator. The ED is usually composed of a diode, a resistor, and a capacitor connected in parallel. This ED dissipates a lot of power when the diode is on and the time constant $\tau = RC$ limits the data rate. It should satisfy

$$\frac{1}{f_c} \ll \tau \ll \frac{1}{DR} \tag{9}$$

So, it is hard to improve the DR using this ED.

The ASK demodulation circuit with an adaptive bias we designed is shown in Fig. 9. The ASK demodulation circuit consists of an ED, an error amplification feedback loop, and a hysteresis comparator. When the input ASK signal passes through the high-pass filter consisting of R_B and C_B, it enters the differential symmetrical circuit (M_{P1}-M_{P4}) for rectification. The diode-connected PMOS M_{P3} and M_{P4} improve the efficiency of the rectifier so that the ED can operate correctly over a wider range of input amplitudes. The rectified output current generated by the input pair flows through a load consisting of M_{N1} and a low-pass filter (R_M, C_M) to form an envelope output V_{ENV}. The low-pass filter extracts the



(a) (b)

FIGURE 12. (a) The transient results under PVT corners (b) The simulated PCE with Monte-Carlo mismatches.

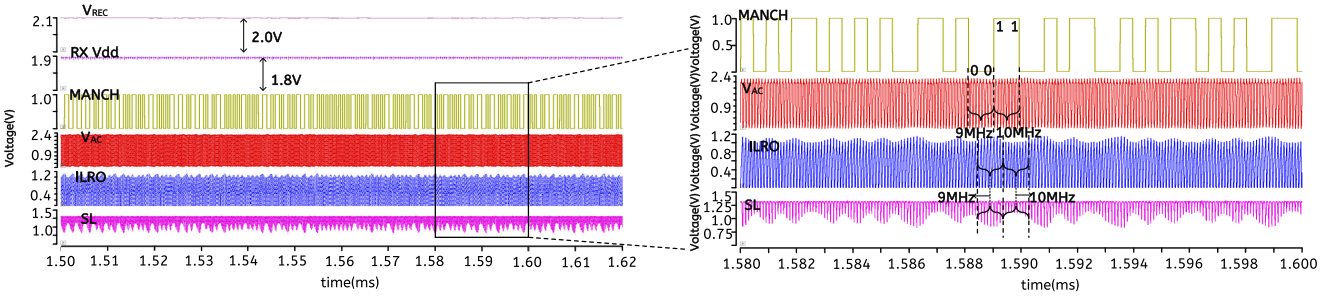


FIGURE 13. FSK-ASK conversion.

average value of the envelope V_{AVG} and sends it to an error amplifier, which feeds V_B back to the input bias voltage. Besides, V_{ENV} and V_{AVG} are fed to a hysteresis comparator to form a rail-to-rail output. The hysteresis voltage of the hysteresis comparator is designed to be larger than the output ripple of the envelope, which is important to reduce the BER of the demodulation [17]. Moreover, the appropriate loop bandwidth needs to be set in the circuit design to support high data rate demodulation without affecting the envelope output.

As shown in Fig. 10 is the simulation result of the loop gain and phase bode diagram under the PVT variation, the feedback loop always satisfies phase margin (PM)>65° and the DC gain is greater than 54dB, which can maintain the frequency stability and closed-loop feedback accuracy over a wide range of input variations. This is essential for our ASK demodulation circuit to work correctly and robustly.

Our ASK demodulation circuit is capable of supporting high data rate (>2Mbps) communication and consumes an average power consumption of only 14.4μW with a 1.8V supply, which shows an advantage for wireless data transmission applications.

IV. SIMULATION RESULTS

The proposed SWPDT system is implemented with the 180nm CMOS process. Fig. 11 shows a layout picture of the chip which occupies an area of 0.836mm^2 (0.88mm × 0.95mm). The performance of the proposed SWPDT system is verified by post-layout simulations. The simulations are carried out over a single inductive link with a coupling factor k of 0.2 (corresponding to a transmission distance of 1.45cm). The input Manchester encoded FSK signal is generated by the ideal VCO and amplified by the PA to the TX coil. Then carriers are transmitted to the RX side through inductive coupling with frequency-splitting characteristics for power and data transmission.

A. POWER TRANSMISSION

To verify the performance and robustness of the active rectifier with adaptive delay compensation loops, the transient simulation results under different PVT corners are shown in Fig. 12 (a). With V_{REC}=2V and R_L=100Ω, both on- and off-delay eliminations are accomplished. M_{N1} and M_{N2} have maximum effective conduction time and there is no reverse current. Further, Fig. 12(b) shows the simulated PCE with Monte-Carlo mismatches. The delay compensation technique is also insensitive to mismatches and a high PCE of 94.1% is achieved. Thus, the stability and feasibility of delay compensation are guaranteed. Meanwhile, the high PCE active rectifier and the designed frequency-splitting link ensure overall PTE of the SWPDT system is up to 76.5% while delivering 40mW power to the load.

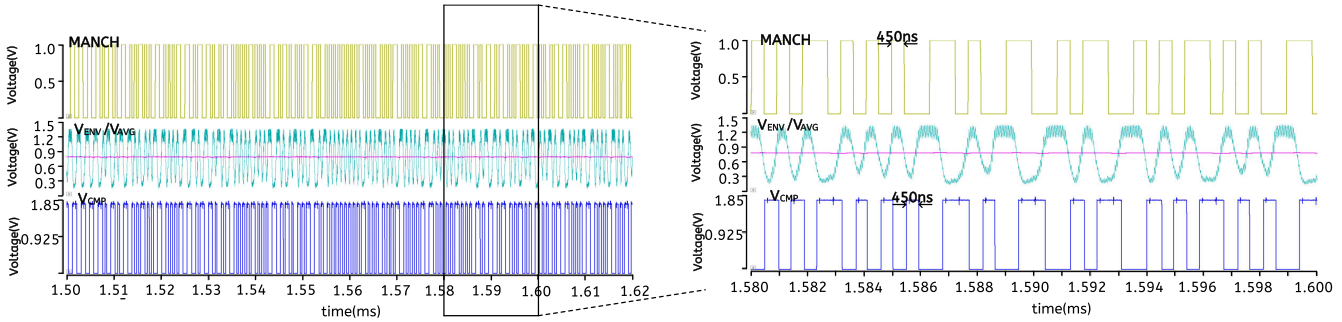


FIGURE 14. ASK demodulation.

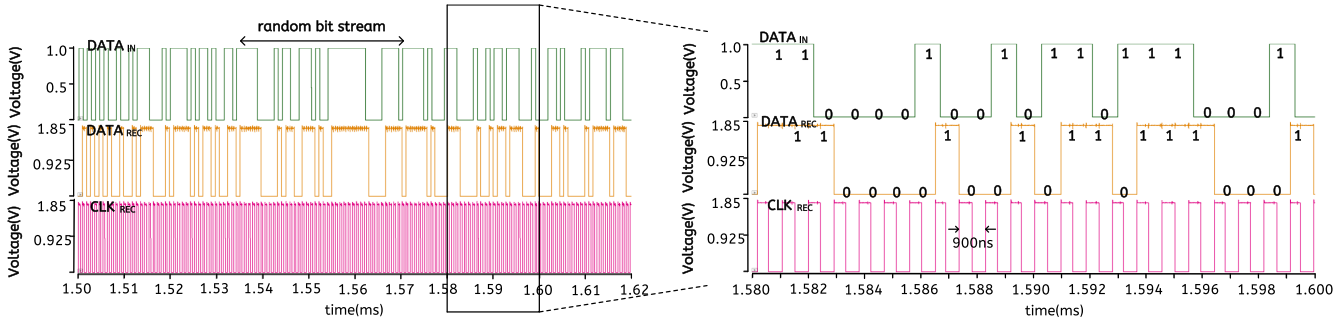


FIGURE 15. Data and clock recovery.

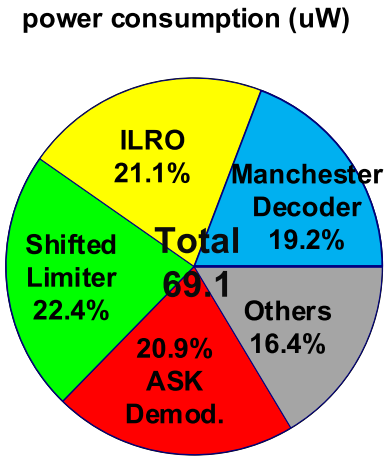


FIGURE 16. Power consumption breakdown of the data demodulation circuits.

B. DATA DEMODULATOR

Fig. 13 shows the transient waveforms of the FSK-ASK conversion. The V_{AC} is the FSK carrier signal, which contains 9MHz and 10MHz frequency information. The 9MHz frequency corresponds to Manchester code "0" and the 10MHz carrier frequency corresponds to Manchester code "1". Thanks to the designed frequency-splitting link, the link has almost the same link gain at 9MHz and 10MHz frequencies, making the amplitude of V_{AC} almost the same, so that the rectifier can operate at the optimum input amplitude. The modulated carrier is shown as the half waveform as it is also fed to the active rectifier. ILROs finish the FSK to ASK conversion as shown in Fig 13. The 9MHz signal (corresponding to code element "0") and the 10MHz signal (for code element "1"), both of which lie in the locking range of ILROs, differ in their output amplitude, which exhibits ASK modulation characteristics. As described in equation (8), the 9MHz signal corresponds to a high output amplitude (1.1V), while the 10MHz signal corresponds to a low output amplitude (1.0V), with an ASK MD of 4.7%. The output of the SL shows that both the ASK carrier signal and the envelope signal lie within their linear range, achieving different gain amplification for the ASK carrier signal and the envelope signal. MD of the ASK signal is increased to 10.9% by the P-type SL, which is a fit and robust modulation depth.

Fig. 14 shows the demodulation results for the ASK signal, from top to bottom are the Manchester code stream from TX coil, the envelope output V_{ENV}, the average output V_{AVG} of V_{ENV}, and the hysteresis comparator output V_{CMP}. The data stream of 1.11Mbps is encoded to form a 2.22Mbps Manchester code stream and the simulation results show that the envelope output has a large conversion gain and the circuit can demodulate the code stream correctly.

Fig. 15 shows the data and clock waveforms recovered by the Manchester decoder. At the top is a random bit stream with a DR of 1.11Mbps, in the middle is the recovered data, and at the bottom is the recovered clock signal. As can be seen from the results, the data and clock are recovered synchronously, with a clock period of 900ns, corresponding to a frequency of 1.11MHz. The demodulation of 1.11Mbps random data is completed correctly.

TABLE 2. Performance comparison with the state-of-the-arts.

Reference	JSSC [14]	TBIOCAS [12]	TCAS I [34]	TCAS I [18]	TCAS I [19]	TBIOCAS [17]	This work[a]
Technology(nm)	65	180	N.A.	180	1500	180	180
Link carrier(MHz)	13.56	13.56	10	10	5,10	6.5,7.5	9,10
Mode	ASK	ASK	ASK	BPSK	DFSK	FSK	FSK
Data rate(Mbps)	0.15	1	1	1.12	2.5	2.5	1.11
Data Rx power consumption(μW)	132	280	N.A.	610	380	300	69.1
FOM[b] (pJ/bit)	880	280	N.A.	544.6	152	120	62.2
Energy efficiency(%)	75.4[c]	N.A.	42[e]	N.A.	N.A.	56.7[e]	76.5[d]
PDL(mW)	9.2	N.A.	24	N.A.	25	115	40

[a] Simulation results.
[b] FOM = $\frac{Power\ consumption}{Data\ rate}$
[c] Only the rectifier efficiency.
[d] Link and rectifier efficiency.
[e] Transmitter efficiency is also included.

Fig. 16 shows the power consumption breakdown of the entire data demodulation circuit, consuming a total of 69.1μW on average, with an energy efficiency of 62.2pJ/b for data demodulation.

To further evaluate the reliability of the system, we performed a long-time simulation of the proposed SWPDT system, obtaining a total of over 10,000 data bits. The data demodulator correctly recovers the original data and achieves a BER lower than $1\times\ 10^{-4}$. It indicates that our SWPDT system can operate stably and reliably.

Certainly, the BER results are more dependent on experimental tests and the value given here is only a rough result. But it also shows that under normal operation, the system can operate stably and the BER meets the general IMDs requirements. It is worth noting that such as data rate, coil misalignment, coil separation distance, etc. can have an impact on the BER of the system. However, as stated in the descriptions of the link characteristics in section II, as long as the link satisfies the strong coupling condition ($k > k_c$) and its frequency-splitting characteristics are not destroyed, the system can operate stably without great changes in the BER.

Table 2 summarizes the overall performance compared to the state-of-the-art technology. From the comparison results, we can see that while delivering comparable power to the load, we achieve a high PTE of up to 76.5% for power transfer. And we also achieve high data rate communication while reducing the power consumption and improving energy efficiency significantly for data demodulation. In particular, compared to [17], we obtain higher transmission efficiency and lower power consumption for data demodulation despite the lower PDL and DR, which are achieved by the design of a high PCE active rectifier and low-power FSK demodulation circuit. These results show that the proposed SWPDT system has good performance and is suitable for implantable applications with low-power data demodulation and high-efficiency power transfer.

V. CONCLUSION

This paper presents an SWPDT system over a single pair of coils with high-efficiency power delivery and energy-efficient forward data transmission. We design an inductive link with frequency-splitting characteristics to achieve high PTE and support high DR communication at the same time. The link we designed extends the separation distance of the coils to the cm level, which is more suitable for implantable applications. Moreover, the energy efficiency for data demodulation is improved significantly due to the low-power FSK demodulator. Simultaneously, the active rectifier with high PCE and the frequency-splitting link ensure high overall efficiency of power transmission. The system is implemented in 180nm CMOS process, occupying an area of 0.836mm^2. The post-layout simulation results show that a DR of 1.11Mbps can be achieved on the condition that the coupling coefficient k between two coils is 0.2. Thanks to the low-power FSK-ASK conversion circuit and ASK demodulator, the power consumption of the whole data demodulation circuit is only 69.1μW and achieves an energy efficiency of 62.2pJ/bit. The overall PTE is up to 76.5% (including the link and the rectifier losses) while the delivered power to the 100Ω load is 40mW. In conclusion, the proposed SWPDT system demonstrates high performance in power and data transmission and has the potential for IMD applications that require high DR, low power consumption, and high PTE.

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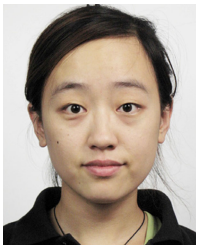

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