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RESEARCH ARTICLE

Thermal Performance Analysis of Carbon Materials Based TSV in Three Dimensional Integrated Circuits

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ABSTRACT This paper applies the carbon materials (i.e., SWCNT, MWCNT, and GNR) as new prospective filler materials of through silicon vias (TSV) for replacing the conventional copper (Cu) to improve the thermal performance of three-dimensional integrated circuits (3-D ICs). The thermal performance of 3-D ICs with integrated TSVs is investigated and the corresponding numerical calculation model is established in this work. Moreover, the thermal performance of 3-D ICs with integrated carbon materials based TSV is investigated by applying our proposed numerical calculation model. The calculation results illustrate that the 3D-ICs with integrated SWCNT based TSV have a greater thermal performance, as compared with the 3-D ICs integrated other materials (i.e., MWCNT, GNR, and Cu) based TSV. Furthermore, it is also manifested that the temperature of die layer in 3-D ICs can be reduced by increasing the thermal conductivity of package and heat sink, by increasing the radius of TSV and decreasing the spacing between TSV. In addition, it is found that the results of our proposed numerical calculation model are fairly consistent with COMSOL simulation and the maximum relative error for them is not exceeding 2%. The proposed new filler materials in this work has many potential applications in improving the heat dissipation performance of 3-D ICs, meanwhile the presented numerical calculation model can provide guidelines for thermal design of 3-D ICs.

INDEX TERMS 3-D ICs, TSV, thermal performances.

I. INTRODUCTION

The emergence of 3-D ICs has significantly promoted the development progress of semiconductor chips, which overcomes the weakness of traditional two-dimensional integrated circuits (2-D ICs) and the multiple chips can be stacked in three-dimensional space [1]. The 3-D ICs have much advantages over 2-D ICs in terms of interconnect length, propagation delay and system power consumption [2], [3], [4]. However, the structure of multi-die stacked chips can give rise to the high-power density, which lead to form the complex thermal problems. Therefore, effective thermal management is crucial to solve the thermal issues of 3-D ICs [5], [6], [7], [8], [9].

The 3-D ICs with integrated TSV can effectively improve the heat dissipation performance, which the heat generated by each die layer can vertically transported to the heat sink through TSV [10], [11]. Hence, TSV technology is significant to improve thermal management of 3-D ICs. To date, Cu is the most widely applied for the filler material of TSV. However, Cu as the TSV filler material can induce skin effect and electromigration at condition of high temperature and high frequency [12]. Hence, it is vital to explore new promising filler materials as substitute for replacing the traditional Cu. Carbon nanotubes (CNTs) and graphene nanoribbon (GNR) have gained significant attention from researchers due to their outstanding thermophysical properties [13], [14]. Moreover,

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CNTs can be classify into single-walled carbon nanotube (SWCNT) and multiwalled carbon nanotube (MWCNT) according to the difference of graphene layers [15]. In contrast to Cu, the thermal conductivity of high quality SWCNT, MWCNT and GNR can reach to 6600 W/mK, 3000 W/mK and 2000 W/mK, respectively [16], [17], [18]. Therefore, the carbon materials (i.e., SWCNT, MWCNT, and GNR) are adopted as filler materials of TSV in this work.

Currently, there have been some studies on the heat dissipation performance of 3-D ICs integrated with CNTs based TSV and GNR based TSV. Hossain et al. in [19] proposed a simulation model of the 3-D IC with integrated GNR based TSV to analyzed the performance of heat transmission in 3-D ICs by using COMSOL Multiphysics software. In [20], Xu et al. presented the CNTs based TSV model by ANSYS simulation and the experiment results indicated that CNTs based TSV exhibit better thermal performance than Cu based TSV and W based TSV in 3-D ICs. In [21], Sun et al. found that the 3D-ICs with integrated CNT-Cu based TSV can effectively improve the heat dissipation performance. In [22], Hossain et al. constructed the CNTs based TSV model through COMSOL Multiphysics and the experiment results suggested that CNTs based TSV have better thermal performance than Cu based TSV in 3-D ICs. In [23], Singh et al. found that the thermal performance of CNTs based TSV outperform GNR based TSV for 3-D ICs by the COMSOL Multiphysics simulation. Kumbhare et al. in [24] investigated the application prospect of TSV with carbon materials for 3-D ICs.

However, the aforementioned works are only paying attention to constructing the simulation model by the multiphysics software of COMSOL or ANSYS. Meanwhile, it is widely recognized that the numerical approximation model is highly CPU runtime efficient than the simulation model of COMSOL or ANSYS. To the best of our knowledge, it can be found that most literatures concerning carbon materials based TSV are implemented by the simulation model. Till date, there are few works to propose a numerical calculation model of 3-D ICs with integrated TSV for fast temperature calculation and optimization design. Hence, an equivalent numerical calculation model based on thermal resistance is proposed in this paper. Additionally, the lateral heat transfer is taken into account in our proposed thermal model because the thermal conductivity of TSV filler materials is far greater than BEOL, silicon substrate and bonding layer. In this paper, the thermal performance differences between carbon materials (i.e., SWCNT, MWCNT, and GNR) and Cu as filler materials of TSV in 3-D ICs are investigated. Moreover, our proposed numerical calculation model can be accurately and quickly to predict the temperature of each die layer of 3-D ICs, as compared with the simulation model.

II. EQUIVALENT CALCULATION THERMAL MODEL

The Fig. 1 illustrates the physical structure of 3-D ICs with embedded TSV, in which the bonding type of each die layer is adopted as face-to-back form.

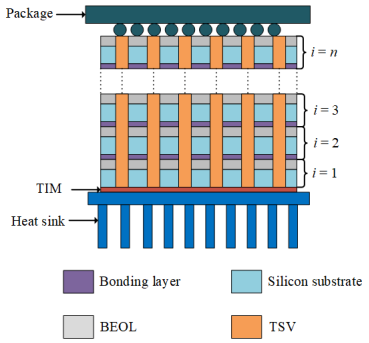

FIGURE 1. Structure diagram of 3-D ICs with integrated TSV.

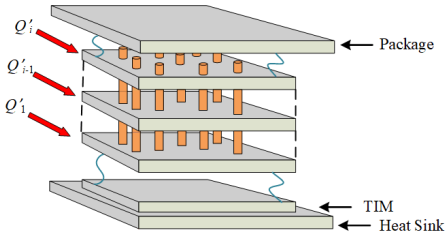

FIGURE 2. 3-D view of the 3-D ICs with integrated TSV structure.

Typically, in the case of 3-D ICs without TSV, the heat produced by the BEOL is conveyed vertically through heat sink or package to the external surroundings of chip. Due to the high thermal conductivity of TSV filler material, the heat can be transferred laterally to TSV in the scheme of 3-D ICs with integrated TSV.

Fig. 2 describes a 3-D view of 3-D ICs with embedded TSV structure, herein Q_i' denotes the total heat generated by the i^{th} ($i = 1, 2, \ldots, n$) BEOL layer.

The cylindrical shaped TSV filled with SWCNT are evenly embedded in 3-D ICs with the same pitch, where their perspective view is shown in Fig. 3(a). The 3-D ICs structure can be divided into cubic unit cells with side length P and the TSV is located at the central axis of the cubic unit cells. The cross-sectional view of a single square cell is exhibited in Fig. 3(b), where d and t_{ins} are the radius of TSV and the thickness of the insulation layer (usually SiO_2) of TSV, respectively.

This paper only investigated the single square cell (as $P \times P$ cell structure) of the 3-D ICs since the overall geometric structure displayed in Fig. 3(a) is a symmetric configuration. Consequently, we established a thermal resistance model of $P \times P$ cell structure to obtain the overall heat dissipation of the 3-D ICs. In order to facilitate the analysis of thermal performance of 3-D ICs with integrated TSV, all die layers are assumed as the same physical dimensions.

The equivalent thermal resistance model of the square cell is illustrated in Fig. 4. Here, $T_{i,1}$, and $T_{i,3}$ are the temperature of the i^{th} BEOL and the temperature for the segment of TSV parallel with i^{th} die layer ($i = 2, 3, \ldots\ldots, n$), respectively. $R_{i,1}$ is the thermal resistance of i^{th} die layer that is determined by the physical parameters of BEOL, silicon substrate, and boding layer. Similarly, $R_{i,2}$ and $R_{i,3}$ are the thermal

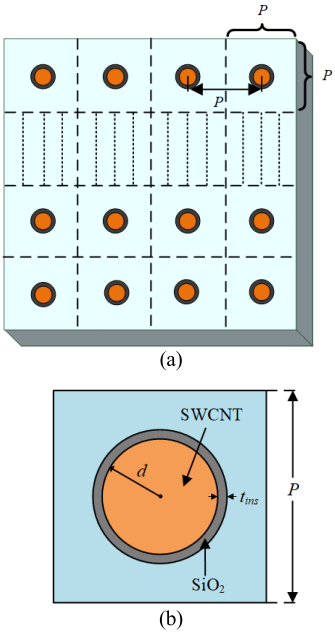

FIGURE 3. Distribution diagram of TSV in 3-D ICs: (a) Top view of 3-D ICs with integrated TSV; (b) Cross-section of 3-D ICs square cell.

resistance of insulation layer and TSV filler material in i^{th} die layer, which are formed by physical parameters of TSV. R_{pk} and R_{hs} are the thermal resistance of the package and heat sink of 3-D ICs, respectively. $q_{i,1}$ is the heat flow of i^{th} die layer to $(i - 1)^{th}$ die layer in vertical direction, $q_{i,2}$ represents the heat flow of i^{th} die layer to i^{th} insulation layer of TSV in lateral direction, $q_{i,3}$ denotes the heat flow of vertical transmission of TSV from i^{th} node to $(i - 1)^{th}$ node. q_{pk} and q_{hs} are the heat flow of top die layer to package and bottom die layer to heat sink, respectively. T_{amb} and Q_i represent the current ambient temperature and heat generate by each die layer in 3-D ICs square cell, respectively.

The thermal resistance of square cell of 3-D ICs is akin to the electrical resistance in a circuit and can be defined as [25],

$$R = \frac{t}{Ak} \tag{1}$$

Here, t denotes thickness of material. A represents the cross-sectional area of material with respect to the heat flow direction. k is the material's thermal conductivity. Thus, R_{pk}, R_{hs}, $R_{i,1}$, $R_{i,2}$, and $R_{i,3}$ $(i = 2, 3, \ldots\ldots, n)$ can be described as,

$$R_{pk} = \frac{t_{pk}}{P^2 k_{pk}} \tag{2}$$

$$R_{hs} = \frac{t_{hs}}{P^2 k_{hs}} \tag{3}$$

$$R_{i,1} = R_{BEOL} + R_{si} + R_{bond} = \frac{\left(\frac{t_{BEOL}}{k_{BEOL}} + \frac{t_{si}}{k_{si}} + \frac{t_{bond}}{k_{bond}}\right)}{P^2 - \pi (d + t_{ins})^2} \tag{4}$$

$$R_{i,2} = \int_0^{t_{ins}} \frac{dx}{2\pi k_{ins} \left(t_{BEOL} + t_{si} + t_{bond}\right)(d + x)} \tag{5}$$

$$R_{i,3} = \frac{t_{BEOL} + t_{si} + t_{bond}}{\pi d^2 k_{tsv}} \tag{6}$$

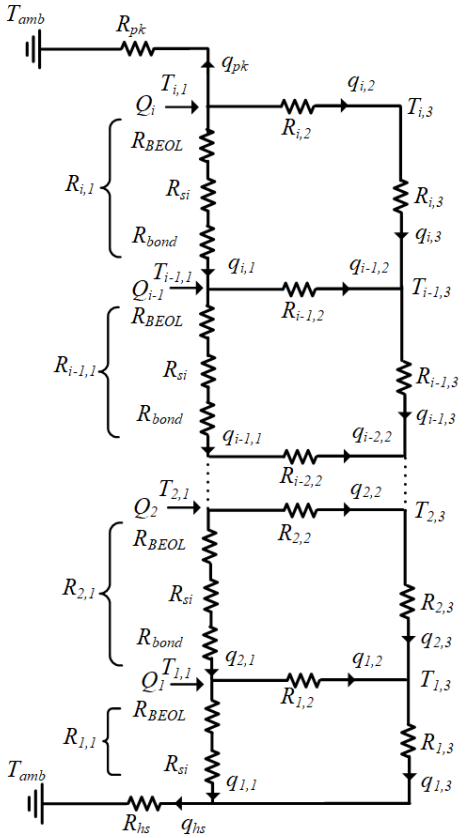

FIGURE 4. The thermal resistance model of 3-D ICs square cell.

Especially, for $i = 1$, the corresponding analytical expressions can be derived as,

$$R_{1,1} = R_{BEOL} + R_{si} = \frac{1}{P^2 - \pi (d + t_{ins})^2}\left(\frac{t_{BEOL}}{k_{BEOL}} + \frac{t_{si}}{k_{si}}\right) \tag{7}$$

$$R_{1,2} = \int_0^{t_{ins}} \frac{dx}{2\pi k_{ins} \left(t_{BEOL} + t_{si}\right)(d + x)} \tag{8}$$

$$R_{1,3} = \frac{t_{BEOL} + t_{si}}{\pi d^2 k_{tsv}} \tag{9}$$

Here, t_{pk} and t_{hs} are the thickness of package and heat sink, respectively. t_{BEOL}, t_{si}, and t_{bond} are the thickness of BEOL, silicon substrate, and bonding layer, respectively. k_{BEOL}, k_{si}, and k_{bond} are the thermal conductivity of BEOL, silicon substrate and bonding layer, respectively. t_{ins} and k_{ins} are the thickness of insulation layer and the thermal conductivity of insulation layer of TSV, respectively. k_{TSV} is the thermal conductivity of filler material of TSV.

In order to enable the calculation results of our proposed thermal model more accurate, the impacts of temperature on the thermal conductivity of TSV filler materials (including SWCNT, MWCNT, GNR, and Cu) are investigated in this section. The thermal conductivity of carbon material (i.e., SWCNT, MWCNT, and GNR) under different temperature can be derived from the [26], [27].

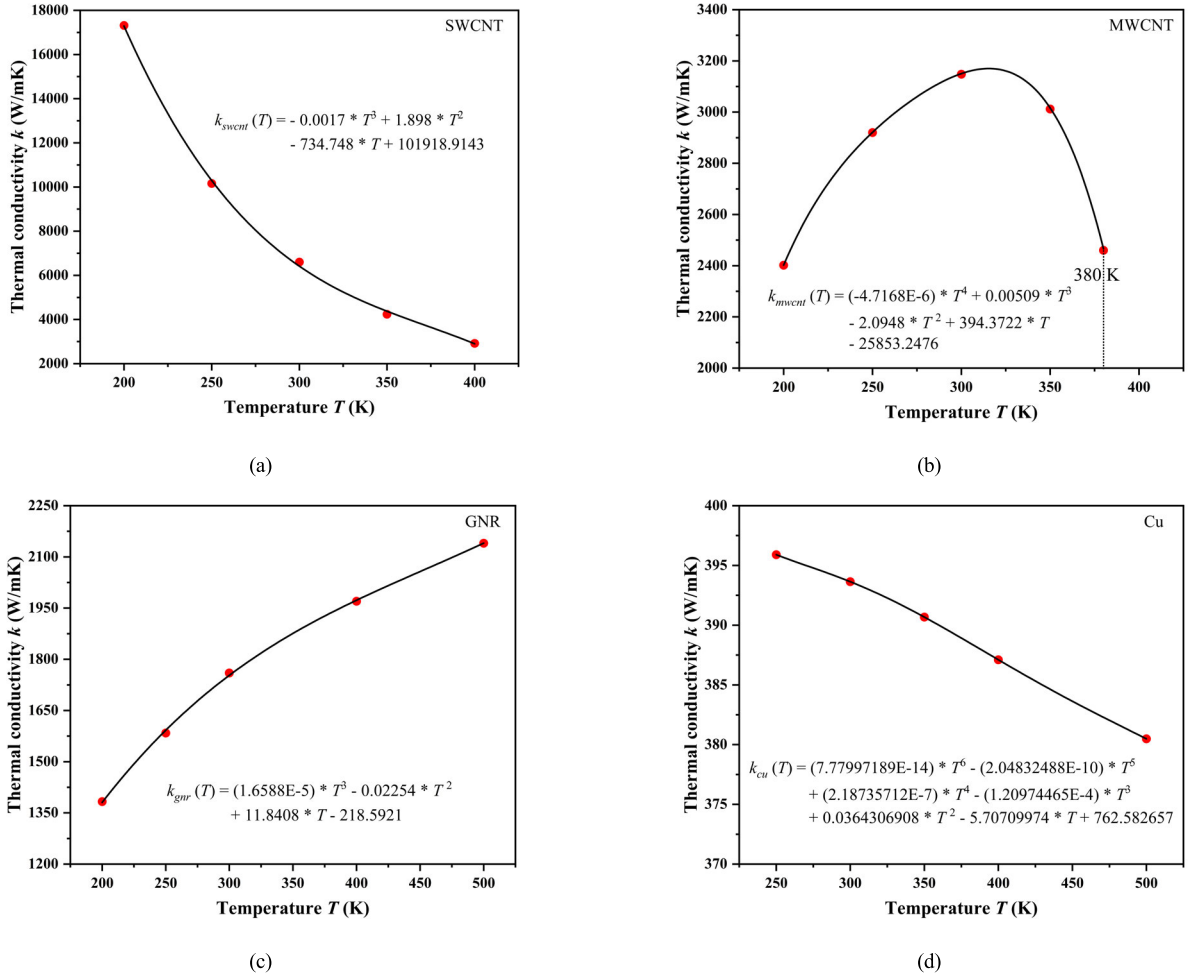

FIGURE 5. The relationship between the thermal conductivity of TSV filler materials and temperature: (a) SWCNT; (b) MWCNT; (c) GNR; (d) Cu.

Besides, the thermal conductivity of Cu versus temperature can be deduced from the [28], [29]. The function relationships between the thermal conductivity for different TSV filler material and temperature are shown in Fig. 5.

In the steady-state, the Kirchhoff's current law (KCL) can be utilized to express the relationship between heat flux and heat generated by each die layer. For i^{th} die layer ($i = 1, 2, \ldots, n-1$), the analytical expressions of heat flux and heat generated by each die layer can be expressed as follows,

$$q_{i+1,1} + Q_i - q_{i,1} - q_{i,2} = 0 \tag{10}$$

$$q_{i+1,3} + q_{i,2} - q_{i,3} = 0 \tag{11}$$

Furthermore, for $i = n$, the analytical expressions of heat flow can be concluded as below,

$$Q_n - q_{pk} - q_{n,2} - q_{n,1} = 0 \tag{12}$$

$$q_{n,2} = q_{n,3} \tag{13}$$

For $i = 0$, the equation of heat flow can be deduced as follow,

$$q_{1,1} + q_{1,3} - q_{hs} = 0 \tag{14}$$

The heat generate by each die layer in 3-D ICs square cell can be expressed by,

$$Q_n = Q_{i-1} = \ldots = Q_1 = \frac{Q'P^2}{S} \tag{15}$$

Here, S is the size of chip.

For i^{th} die layer ($i = 1, 2, \ldots, n$), the analytical expressions for the relationship between temperature and heat flow for each layer can be defined as,

$$q_{i,1} = \frac{T_{i,1} - T_{i-1,1}}{R_{i,1}} \tag{16}$$

$$q_{i,2} = \frac{T_{i,1} - T_{i,3}}{R_{i,2}} \tag{17}$$

$$q_{i,3} = \frac{T_{i,3} - T_{i-1,3}}{R_{i,3}} \tag{18}$$

Moreover, the heat flow through the package and heat sink can be expressed as follows,

$$q_{pk} = \frac{T_{n,1} - T_{amb}}{R_{pk}} \tag{19}$$

$$q_{hs} = \frac{T_{0,1} - T_{amb}}{R_{hs}} \tag{20}$$

Due to the structure of thermal interface material (TIM) configuring on the top surface of the heat sink, and its temperature can be expressed as,

$$T_{0,1} = T_{0,3} \tag{21}$$

The expressions from Eq. (10) to Eq. (21) are consisted of $(2n + 1)$ variables $T_{n,1}$, $T_{n,3}$, $T_{i-1,1}$, $T_{i-1,3}$, …, $T_{2,1}$, $T_{2,3}$, $T_{1,1}$, $T_{1,3}$, and $T_{0,1}$, and they can be expressed by the matrix equation as below,

$$CT = H \tag{22}$$

Herein, T denotes a $(2n + 1) \times 1$ matrix that corresponds to the temperature of each die layer and can be written as,

$$T = \left[T_{n,1}, T_{n,3}, T_{i-1,1}, T_{i-1,3}, \ldots, T_{2,1}, T_{2,3}, T_{1,1}, T_{1,3}, T_{0,1}\right]^T \tag{23}$$

The $(2n + 1) \times 1$ constant matrix H is deduced by applying the thermophysical parameters and initial conditions that can be expressed as,

$$H = \left[Q_n + \frac{T_{amb}}{R_{pk}}, 0, Q_{i-1}, 0, \ldots, Q_2, 0, Q_1, 0, -\frac{T_{amb}}{R_{hs}}\right]^T \tag{24}$$

C is a $(2n + 1) \times (2n + 1)$ matrix that can be defined as follows (25), as shown at the bottom of the next page.

For matrix C, the range of i is from 2 to $(n - 1)$ and the ξ_c $(c = 1, 2, \ldots, 7)$ can be expressed as follows,

$$\xi_1 = \frac{1}{R_{n,1}} + \frac{1}{R_{n,2}} + \frac{1}{R_{pk}} \tag{26-1}$$

$$\xi_2 = -\frac{1}{R_{n,2}} - \frac{1}{R_{n,3}} \tag{26-2}$$

$$\xi_3 = \frac{1}{R_{i+1,1}} + \frac{1}{R_{i,1}} + \frac{1}{R_{i,2}} \tag{26-3}$$

$$\xi_4 = -\frac{1}{R_{i+1,3}} - \frac{1}{R_{i,2}} - \frac{1}{R_{i,3}} \tag{26-4}$$

$$\xi_5 = \frac{1}{R_{2,1}} + \frac{1}{R_{1,1}} + \frac{1}{R_{1,2}} \tag{26-5}$$

$$\xi_6 = -\frac{1}{R_{2,3}} - \frac{1}{R_{1,2}} - \frac{1}{R_{1,3}} \tag{26-6}$$

$$\xi_7 = -\frac{1}{R_{hs}} - \frac{1}{R_{1,1}} - \frac{1}{R_{1,3}} \tag{26-7}$$

In order to obtain accurate calculation results of thermal model, the relationship between thermal conductivity of TSV filler materials and temperature is considered into matrix C. The thermal resistance of TSV for node i can be written as follows $(i = 2, 3, \ldots\ldots, n)$,

$$R_{i,3} = \frac{t_{BEOL} + t_{si} + t_{bond}}{\pi d^2} \frac{1}{k_{tsv}(T_{i,3})} \tag{27}$$

Especially, the thermal resistance for node $i = 1$ can be expressed as,

$$R_{1,3} = \frac{t_{BEOL} + t_{si}}{\pi d^2} \frac{1}{k_{tsv}(T_{1,3})} \tag{28}$$

In this work, the temperature results of each die layer at steady state can be derived by solving the T matrix using MATLAB software.

III. RESULTS AND DISCUSSION

This section delves into the thermal performance of eight die stacked chips by utilizing the proposed thermal resistance model, where the models with Cu based TSV and carbon (i.e., SWCNT, MWCNT, and GNR) based TSV are studied respectively. Furthermore, the size of chip is set as 4.5 mm × 4.5 mm, the size of unit is set as 30 μm × 30 μm, and the total heat generation of each die layer is set as 4 W.

In order to ensure the rationality and generalizability of our proposed model, the simulation model is implemented by COMSOL Multiphysics 6.0. The physical parameters of chip are exhibited in Table 1.

TABLE 1. The physical parameters of chip [30], [31], [32], [33], [34].

Physical parameters of chip	Values
Radius of TSV	2 μm
Thickness of insulation layer	0.5 μm
Thickness of package	1.8 mm
Thickness of heat sink	2 mm
Thickness of BEOL	20 μm
Thickness of silicon substrate	50 μm
Thickness of bonding layer	10 μm
Thermal conductivity of insulation layer	1.4 W/mK
Thermal conductivity of package	33 W/mK
Thermal conductivity of heat sink	400 W/mK
Thermal conductivity of BEOL	1.4 W/mK
Thermal conductivity of silicon substrate	130 W/mK
Thermal conductivity of bonding layer	0.15 W/mK

A. RESULTS OF OUR PROPOSED MODEL

In this section, the thermal performance differences between new materials (including SWCNT, MWCNT, and GNR) and conventional Cu as the filler materials of TSV in 3-D ICs are investigated. The results of temperature and temperature rise of SWCNT, MWCNT, GNR, and Cu based TSV are illustrated in Table 2 and Table 3 respectively, where the temperature rise ΔT_i can be defined: $\Delta T_i = \Delta T_{i,1}$ - T_{amb}. Moreover, the T_{amb} is defined as 300 K (i.e., 26.85 °C) in this work.

As exhibited in Table 2, it can be seen that the SWCNT based TSV case has lower temperature than that MWCNT, GNR, and Cu based TSV at all die layer. Taking die layer $i = 7$ as an instance, the temperature of 3-D ICs for SWCNT based TSV scheme is reduced by 7.599%, 15.742%, and 38.290% respectively, as compared to MWCNT, GNR, and Cu based TSV cases. This is due to the fact that SWCNT

TABLE 2. Steady-state temperature of each die layer for TSV based different filler materials.

$T_{i,1}$, [°C]	Filler materials of TSV			
	SWCNT	MWCNT	GNR	Cu
$i = 8$	38.615	41.670	45.396	57.949
$i = 7$	38.693	41.875	45.922	62.701
$i = 6$	38.518	41.657	45.754	64.880
$i = 5$	38.151	41.089	44.980	64.601
$i = 4$	37.594	40.172	43.601	61.862
$i = 3$	36.849	38.905	41.612	56.666
$i = 2$	35.918	37.287	39.009	49.016
$i = 1$	34.795	35.296	35.746	38.840

TABLE 3. Temperature rise of each die layer for TSV based different filler materials.

$\triangle T_i$, [°C]	Filler materials of TSV			
	SWCNT	MWCNT	GNR	Cu
$i = 8$	11.765	14.820	18.546	31.099
$i = 7$	11.843	15.025	19.072	35.851
$i = 6$	11.668	14.807	18.904	38.030
$i = 5$	11.301	14.239	18.130	37.751
$i = 4$	10.744	13.322	16.751	35.012
$i = 3$	9.999	12.055	14.762	29.816
$i = 2$	9.068	10.437	12.159	22.166
$i = 1$	7.945	8.446	8.896	11.990

based TSV case has a larger proportion of the lateral heat transfer toward TSV compared with other materials (i.e., MWCNT, GNR, and Cu) based TSV schemes.

According to Table 3, it is found that the temperature rise of SWCNT based TSV case is lesser than that other materials (i.e., MWCNT, GNR, and Cu) based TSV schemes. Giving $i = 7$ die layer as an example, the temperature rises of 3-D ICs for SWCNT based TSV scheme are 1.269, 1.610 and 3.027 times lesser than that MWCNT, GNR, and Cu based TSV cases respectively. Consequently, based on the discussions mentioned above, it is manifested that the SWCNT can be considered as a promising potential alternative to replace the traditional Cu.

B. RESULTS OF SIMULATION MODEL

In this section, the simulation model is constructed to ensure the accuracy of our proposed model by using COMSOL

$$C = \begin{bmatrix} \xi_1 & -\frac{1}{R_{n,2}} & -\frac{1}{R_{n,1}} & 0 & 0 & 0 & 0 & \overbrace{0\ldots0}^{2n-6} \\ \frac{1}{R_{n,2}} & \xi_2 & 0 & \frac{1}{R_{n,3}} & 0 & 0 & 0 & \overbrace{0\ldots0}^{2n-6} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \overbrace{0\ldots0}^{2(n-i-1)} & -\frac{1}{R_{i+1,1}} & 0 & \xi_3 & -\frac{1}{R_{i,2}} & -\frac{1}{R_{i,1}} & 0 & \overbrace{0\ldots0}^{2i-3} \\ \overbrace{0\ldots0}^{2(n-i-1)} & 0 & \frac{1}{R_{i+1,3}} & \frac{1}{R_{i,2}} & \xi_4 & 0 & \frac{1}{R_{i,3}} & \overbrace{0\ldots0}^{2i-3} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \overbrace{0\ldots0}^{2(n-3)} & 0 & 0 & -\frac{1}{R_{2,1}} & 0 & \xi_5 & -\frac{1}{R_{1,2}} & -\frac{1}{R_{1,1}} \\ \overbrace{0\ldots0}^{2(n-3)} & 0 & 0 & 0 & \frac{1}{R_{2,3}} & \frac{1}{R_{1,2}} & \xi_6 & \frac{1}{R_{1,3}} \\ \overbrace{0\ldots0}^{2(n-3)} & 0 & 0 & 0 & 0 & \frac{1}{R_{1,1}} & \frac{1}{R_{1,3}} & \xi_7 \end{bmatrix} \tag{25}$$

TABLE 4. The temperature of each die layer for COMSOL simulation.

$T_{i,1}$, [°C]	Filler materials of TSV			
	SWCNT	MWCNT	GNR	Cu
$i = 8$	38.080	41.212	44.983	56.974
$i = 7$	38.173	41.405	45.708	62.047
$i = 6$	37.985	41.180	45.579	63.913
$i = 5$	37.599	40.598	44.806	64.241
$i = 4$	37.019	39.659	43.395	61.717
$i = 3$	36.242	38.361	41.337	56.621
$i = 2$	35.275	36.703	38.631	48.896
$i = 1$	34.212	34.740	35.272	38.421

Multiphysics 6.0 software. All parameters of COMSOL simulation are configured as same with the proposed model.

In order to obtain the accurate simulation results, the mesh is set as extreme refinement. Furthermore, the thermal conductivity of the TSV filler material with temperature-dependent has also been considered for the COMSOL simulation. The comparison results of CPU runtime and memory usage for the proposed calculation model and COMSOL simulation model are presented in this section. The temperature results of each die layer for COMSOL simulation are described in Table 4. Here the central temperature of BEOL represents the temperature of each die layer of 3-D ICs.

The calculation results obtained by our proposed calculation thermal model and the COMSOL simulation results are shown in Fig. 6. In addition, the corresponding results of the relative deviation are also displayed in Fig. 6. Where, the relative deviation is defined as,

$$\delta = \frac{|T_{comsol} - T_{model}|}{T_{comsol}} \tag{29}$$

Herein, T_{comsol} and T_{model} are the results of COMSOL simulations and our proposed model, respectively.

As shown in Fig. 6, it is remarkable seen that the results of our proposed model are in great accordance with COMSOL simulation and the maximum relative error is not larger than 2%.

In order to verify that our proposed model can effectively improve the operating efficiency of the CPU, as compared with COMSOL simulation. Taking the solution process of temperature results of SWCNT based TSV as an example, the CPU runtime and memory usage for the proposed calculation model and COMSOL simulation are recorded in Table 5.

As exhibited in Table 5, it can be seen that the proposed calculation model can obviously reduce the CPU runtime and memory usage in comparison to COMSOL simulation.

Here the CPU runtime and memory usage of our proposed calculation model are 4.657 and 1.519 times lesser than the

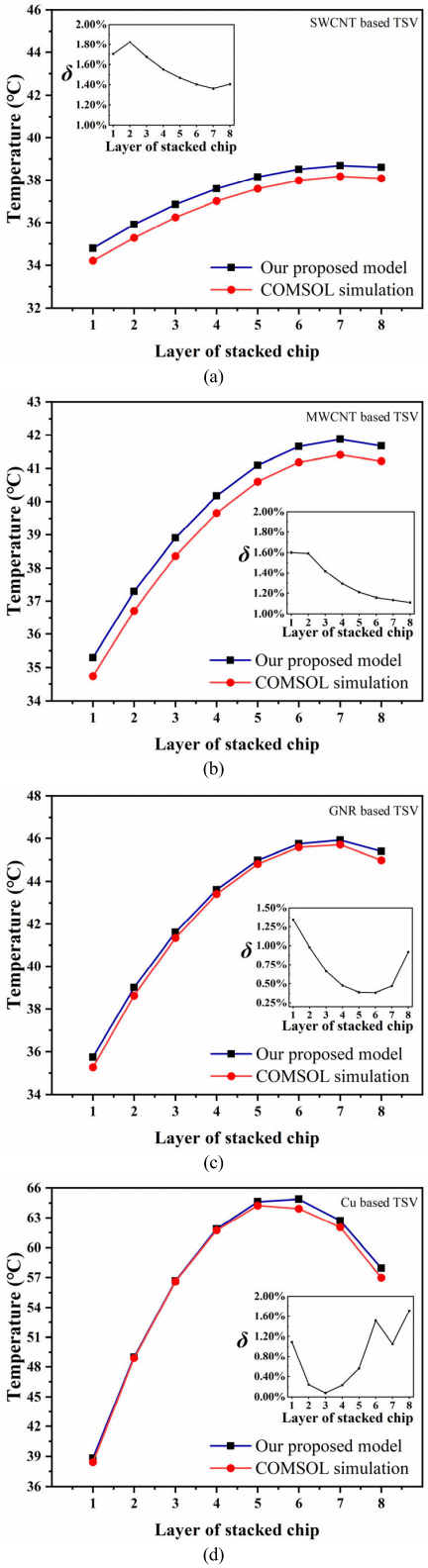

FIGURE 6. The comparison results of the proposed numerical calculation model and COMSOL simulation: (a) SWCNT based TSV; (b) MWCNT based TSV; (c) GNR based TSV; (d) Cu based TSV.

COMSOL simulation. Therefore, our proposed calculation model can effectively improve the efficiency of obtaining the temperature of die layer in 3-D ICs.

TABLE 5. The CPU runtime and memory usage for the proposed calculation model and COMSOL simulation.

PC configuration		CPU runtime and memory usage	
		Our proposed model	COMSOL
CPU	AMD 7735H	70 seconds	326 seconds
Memory Capacity	16 GB	5.4 GB	8.2 GB

C. EFFECT OF PHYSICAL PARAMETERS OF 3-D ICs ON TEMPERATURE

In order to explore the way for improving the heat dissipation performance of 3-D ICs. The effects of physical parameters (including thermal conductivity and physical geometric dimensions) of 3-D ICs are investigated in this section.

1) EFFECTS OF THERMOPHYSICAL PARAMETERS OF PACKAGE AND HEAT SINK ON THE TEMPERATURE OF EACH DIE LAYER

In order to accurately analyze the influences of the thermal conductivity of package and heat sink on the temperature of each die layer, we defined the three cases as follows:

Case 1: The thermal conductivity of heat sink is set to remain unchanged (i.e., $k_{hs} = 400$ W/mK) and the thermal conductivity of package is increased from 33 W/mK to 66 W/mK and decreased from 33 W/mK to 16.5 W/mK (i.e., k_{pk} is set as 16.5 W/mK, 33 W/mK, and 66 W/mK) respectively.

Case 2: The thermal conductivity of package is set to remain unchanged (i.e., $k_{pk} = 33$ W/mK) and the thermal conductivity of heat sink is increased from 400 W/mK to 800 W/mK and decreased from 400 W/mK to 200 W/mK (i.e., k_{hs} is set as 200 W/mK, 400 W/mk, and 800 W/mK) respectively.

Case 3: The thermal conductivities of package and heat sink are all changed (i.e., the thermal conductivity of package is increased from 33 W/mK to 66 W/mK and decreased from 33 W/mK to 16.5 W/mK respectively, meanwhile the thermal conductivity of heat sink is increased from 400 W/mK to 800 W/mK and decreased from 400 W/mK to 200 W/mK respectively.). In order to facilitate the analysis, the Case 3 is classified into three schemes, which can be defined as, scheme 1: $k_{pk} = 16.5$ W/mK & $k_{hs} = 200$ W/mK, scheme 2: $k_{pk} = 33$ W/mK & $k_{hs} = 400$ W/mK, scheme 3: $k_{pk} = 66$ W/mK & $k_{hs} = 800$ W/mK.

The results for the three cases mentioned above are depicted in Fig. 7.

As described in Fig. 7, it can be inferred from Fig. 7(a) that the temperature of all die layer for case 1 decreases with the increase of thermal conductivity of package when the thermal conductivity of heat sink is kept unchanged. Taking die layer $i = 7$ as an example, the temperature for $k_{pk} = 66$ W/mK are decreased by 4.461% and 7.216% respectively, as compared to $k_{pk} = 33$ W/mK and $k_{pk} = 16.5$ W/mK.

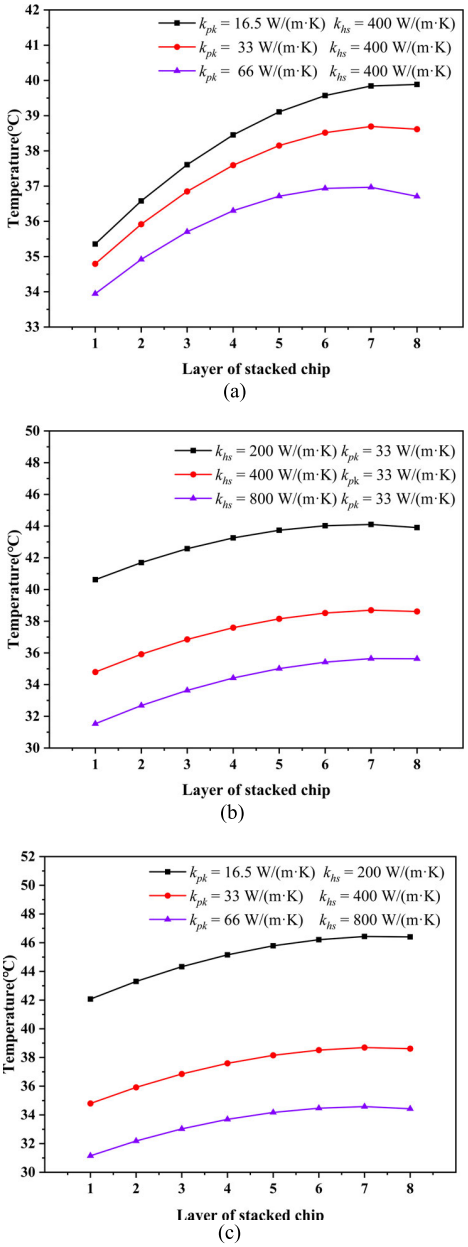

FIGURE 7. The temperature of die layer versus the thermal conductivity of package and heat sink: (a) Case 1; (b) Case 2; (c) Case 3.

The result of case 2 as shown in Fig. 7(b), it is suggested that the temperature of all die layer increases with the decrease of thermal conductivity of heat sink when the thermal conductivity of package is unchanged. Using die layer $i = 7$ as an instance, the temperature for $k_{hs} = 800$ W/mK are reduced by 7.883% and 19.188% in comparison to $k_{hs} = 400$ W/mK and $k_{hs} = 200$ W/mK, respectively.

The result of case 3 as illustrated in Fig. 7(c), it is found that collaborative increasing the thermal conductivities of heat sink and package can significantly reduce the temperature

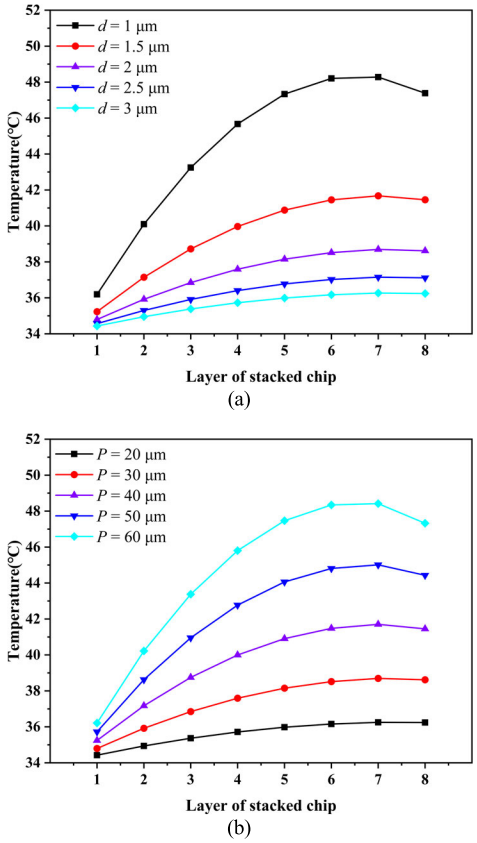

FIGURE 8. The temperature of die layer versus the physical geometric dimensions: (a) Under different radius of TSV; (b) Under different spacing between adjacent TSV.

of all die layer. Giving die layer $i = 8$ as an instance, the reduction percentages of temperature for scheme 3 (i.e., $k_{pk} = 66$ W/mK, $k_{hs} = 800$ W/mK) are 10.848% and 25.811% compared with scheme 2 (i.e., $k_{pk} = 33$ W/mK, $k_{hs} = 400$ W/mK) and scheme 1 (i.e., $k_{pk} = 16.5$ W/mK, $k_{hs} = 200$ W/mK), respectively. Apparently, it is beneficial to improve the thermal performance by increasing the thermal conductivity of package and heat sink in 3-D ICs.

2) EFFECTS PHYSICAL GEOMETRIC DIMENSIONS OF TSV ON TEMPERATURE OF EACH DIE LAYER

In order to analyze the effects of the physical geometric parameters on temperature of each die layer in 3-D ICs. In this work, the impacts of physical geometric dimensions (including of the radius of TSV and the spacing between adjacent TSV) on thermal performance of 3-D ICs are discussed. The effects of the different radius and spacing of TSV on temperature of each die layer are exhibited in Fig. 8.

Fig. 8 shows that the temperature of all die layer decreases with the increase of the radius of TSV, meanwhile the temperature of all die layer decreases with the reducing of the spacing between TSV. The reason for this phenomenon is that the area ratio of TSV in square cell increases as the radius of TSV increases, meanwhile the area ratio of TSV in square cell increases as the spacing between TSV decreases, hence these can enable to increase the proportion of horizontal heat transfer toward TSV. Consequently, it is suggested that the thermal performance of 3-D ICs can be enhanced by increasing the radius of TSV and reducing the spacing adjacent TSV.

IV. CONCLUSION

This work proposed a numerical approximation model of 3-D ICs with integrated different materials (including SWCNT, MWCNT, GNR, and Cu) based TSV, which take the lateral heat transfer into account. The calculation results show that thermal performance of TSV with SWCNT as the filler material are significantly better than that the other filler materials (i.e., MWCNT, GNR, and Cu). Moreover, it is found that the heat transfer performance of 3-D ICs can be enhanced by increasing the thermal conductivity of the package and heat sink materials, by increasing the radius of TSV and reducing the spacing between TSV. In addition, our proposed numerical approximation model illustrated excellent accuracy with the simulation model. Consequently, the SWCNT can be as a novel filler material of TSV to instead Cu, and our proposed numerical approximation model has greatly potential value in thermal management of 3-D ICs.

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