RESEARCH ARTICLE

Protection System for LVDC Distribution Networks Using a Fault Current-Limiting Converter and Protection Zones

JIN-SU KIM[1]**, (Member, IEEE), EUN-CHUL LEE**[2]**, AND SANG-YUN YUN**[3]**, (Member, IEEE)**
[1]LS Electric, Anyang-si, Gyeonggi-do 14118, South Korea
[2]EKOS Company Ltd., Gwangju-si, Gyeonggi-do 12731, South Korea
[3]Department of Electrical Engineering, Chonnam National University, Gwangju 61188, South Korea

Corresponding author: Sang-Yun Yun (drk9034@jnu.ac.kr)

ABSTRACT In this study, we propose a generalized protection system for low-voltage DC (LVDC) distribution networks based on fault current-limiting (FCL) and the concept of protection zones (PZs). The proposed system ensures fault resilience and sufficient operating time for protection devices (PDs) through the FCL of the power conversion device, and it performs protection coordination through fault zone isolation. FCL is achieved using a buck converter-type fault current-limiter to actively control the DC-side fault current contribution of the rectifier, as well as a phase-shift dual-active-bridge (DAB) converter, which exhibits inherent limiting effects during faults. This also enables PZ isolation. In addition, we propose a relaying method to coordinate protection in each PZ. The system distinguishes the types of arbitrary PDs that form each PZ according to their position within the PZ and defines predetermined relaying methods and operation criteria for each type. This enables the protection system to be easily configured for new systems or changing system topology. We configure an LVDC system using a general DC circuit breaker that does not rely on communication signals and generalize its relaying method for each PZ. We verified the applicability of the proposed method to real networks using MATLAB/Simulink simulations and in a hardware-in-the-loop simulation environment with actual manufactured DAB converter controllers and DC circuit breaker relays. In addition, a comparison with existing methods showed that the proposed method could contribute to improving supply reliability by reducing the frequency of system interruption despite lower infrastructure investment.

INDEX TERMS Dual active bridge converter, fault current limiting, hardware-in-the-loop test, low-voltage DC protection coordination, protection zone.

I. INTRODUCTION

Recently, the demand for DC transmission and distribution networks has dramatically increased owing to factors such as price reduction of major semiconductor components, expansion of DC renewable energy, and rapid development of power-conversion devices and their control technologies. Traditionally, electrical energy supplied through AC transmission and distribution networks has been converted into DC

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for use in loads such as computers, batteries, and DC motors. However, in recent years, the supply networks themselves have evolved as medium-/low-voltage DC (MVDC/LVDC).

Fault currents in DC distribution networks can flow through the semiconductor devices on the converter, and tend to rise faster than those in AC systems. Because these semiconductor devices have very low thermal durability, it is critical that faults be cleared quickly. Therefore, DC protection devices (PDs) such as circuit breakers require higher performance compared to their AC circuit counterparts and therefore tend to be larger and more expensive. Thus, to

continue the expansion of DC distribution systems, the development of appropriate protection technology with guaranteed economic feasibility is essential.

To effectively protect DC systems, the first step is analysis of the characteristics of fault currents. Meghwani et al. [1] formulated a model for the time-varying fault current after the occurrence of a fault at rectifier and converter terminals. Other researchers have defined the time-varying fault current characteristics such as the discharge stage of the DC-link capacitor at the beginning of the fault, energy release by the line inductor, and the contribution by the AC power source [2], [3]. Their results have revealed that the initial peak current is primarily related to the discharge stage of the DC-link capacitor, and its magnitude and duration are determined by the characteristics of the RLC circuit formed from the converter output to the fault point. Typically, the magnitude of this current is large but its duration is short (3 ms or less). Moreover, as it is directly transmitted from the converter output to the fault point without passing through the semiconductor switching element inside the converter, the peak current does not affect the converter itself. The inductor discharge section affects the converter to a far greater degree, and it is generally agreed that the fault current must be blocked before this section [1]. IEC61660 introduced a universal fault analysis method for DC distribution systems [4]. It calculates the total short-circuit current at a specific point by designating the partial short-circuit currents contributed by each fault current source and overlapping them. In cases where there are different current sources and a common network at a specific fault point, it calculates the correction factors of each current source. Feng et al. generalized the calculation of correction factors using the admittance matrix structure [5]. However, unlike AC distribution systems, whose fault current characteristics are determined by parameters such as the system impedance, the fault patterns of DC distribution networks can vary significantly. This variation can be due to the use of fault current limiting (FCL) elements that can directly control the current during an accident or new power- conversion device topologies.

Many studies have been conducted to find a fast and effective protection method for DC distribution systems. We classify existing studies according to the practical applications of protection systems, such as relaying methods and the use of communication functions, as follows.

The first group consists of methods that use magnitude changes (overcurrent, current change rate, and undervoltage) as relaying elements without using communication functions. Baran and Mahajan [6] proposed a relaying method based on overcurrent and undervoltage elements. This method essentially sets each converter section and DC line as separate protection zones (PZs) using a current-limiting converter as a circuit breaker for the converter section and multiple DC circuit breakers (DCCBs) for line faults. Tang and Ooi [7] proposed a ''handshaking method'' through the coordination of AC side circuit breakers and high-speed switches on the DC line.

This method has the advantage of isolating the fault section and restoring the remaining sections without transmitting communication signals, but has the drawback of causing a momentary blackout of the entire system. Meghwani et al. [8] presented a method that uses the current change rate as a relay element and transmits a transfer trip signal between PDs in each section for DC line faults. This method is used in loop-type AC distribution systems and involves exchanging follow-me commands between PDs on both sides of the line; however, it requires a trip signal-transmission circuit built into the cable. The above-mentioned methods focus on fault current blocking and location estimation. However, they cannot guarantee coordination between PDs in a general hierarchical distribution system structure.

The second group comprises methods that use the magnitude variation for relaying elements and communication functions. Emhemed and Burt [9] introduced an LVDC protection method using solid-state circuit breakers (SSCBs) based on communication between overcurrent relays and used used the current magnitude, direction, and DC bus voltage as relaying elements. Their method enables rapid detection and clearing of faults during the transient period and provides fast recovery. However, there are constraints due to the need for additional infrastructure such as for communication and SSCBs. Monadi et al. [10] presented an MVDC protection method in which the operation of the DCCB in the source side was coordinated with that of the switches inside the DC network. This method performs overcurrent-based relaying and uses communication signals to identify the fault location, similarly to the handshaking method in [7]. Emhemed et al. [11] suggested a method for detecting faults and estimating their locations by combining SSCB with multiple intelligent electronic device (IED) relays based on current direction. Their method performs high-speed fault blocking and location estimation by detecting the direction of the DC current at the initial stage of the fault and communicating with other IEDs. The communication employed in the above-mentioned methods ensures selectivity and coordination between PDs in different fault sections, but they ignore communication errors and delays. Furthermore, they require extensive infrastructure investment, limiting their economic feasibility, especially for small-scale LVDC systems.

In the third group, there are DC protection methods that employ the differential and distance relaying methods used in AC transmission systems. Fletcher et al. [12] reviewed the problems of non-unit protection methods and the effects of unit protection, and presented a framework for designing protection methods for target networks. They examined various protection methods and found communication-based differential current relaying to be the most suitable. Monadi et al. [2] also proposed a protection method using coordinated operation between DCCB and DC switches (the *cut and try* method). This method can only be applied in very specific LVDC system environments: it uses a source protection relay to quickly (within a few microseconds)

detect the current rise rate during capacitor discharge and uses the current differential method between PDs to block faults only at the sub-microgrid level. Further, Yang et al. [13] proposed a method to estimate both ground fault resistance and distance to the ground fault by analyzing the initial stage of the ground fault transient phenomenon. Christopher et al. [14] also presented a distance relay method based on impedance estimation. However, as general LVDC lines are very short, the impedance differences in fault sections are very small. Hence, the insertion of fault resistance and measurement sensor errors inhibit the application of this method to LVDC system protection.

Clearly, researchers have made various attempts to realize effective DC network protection. However, the size and cost of implementing the various topologies or high-specification PDs limit their practical applicability in LVDC distribution networks targeting DC consumers. Most LVDC networks still do not use communication signal-transmission methods, and traditional magnitude-based relaying is common. Moreover, there may be issues when performing complicated relay-calibration tasks whenever the system configuration changes. Therefore, developing a reliable and economically feasible protection system suitable for small-scale LVDC networks is necessary. Furthermore, for practicality, such a protection system must enable simple setting based on determination of the approximate load, renewable generation specifications, and equipment capacity (e.g., the energy-storage system, ESS), similarly to low-voltage AC (LVAC) systems.

In this study, we propose a protective coordination method based on a FCL and designated PZs for LVDC distribution networks with multiple branch circuits, including renewable energy and ESSs. The proposed method uses the FCL circuits of AC/DC rectifiers and dual-active-bridge (DAB)-type DC/DC converters to limit fault currents from the inductor discharge stage and ensure a time delay for circuit breakers and power-conversion devices. In addition, it creates separable PZs and enables protection coordination using directional overcurrent and undervoltage protection methods for faults in each PZ. This paper is organized as follows. Section II discusses the concept behind the proposed protection coordination system. Futher, Section III describes the system in details and includes verification results for a simulated system using MATLAB/Simulink. Section IV presents hardware-in-the-loop simulation (HILS) test results using Opal-RT, linking DAB converter and DCCB relay prototypes for an LVDC demonstration system built at Naju, Jeollanam-do, South Korea. Finally, Section V presents the conclusions.

This study makes the following contributions. First, the application of the proposed method is simple because it uses a simple magnitude-based protection method for protection coordination, rather than complicated communication functions and protection methods used in prior studies, which are difficult to apply to LVDC. Second, the PZ is determined on the basis of the position of the protection target and the PD, and the instantaneous and time-delay protection elements are

determined accordingly; therefore, in the proposed system, calibrating relays for new LVDC systems or changes in system topology is very easy. Third, by reducing the fault current magnitude in the LVDC system to a specified value, operating power-conversion devices and PDs with a time delay is possible, thus facilitating protection coordination between two or more PDs on a straight line. This also has the advantage of supporting economic feasibility because general DCCBs with an operating speed of 10–20 ms can be used, compared to the high-cost, high-speed SSCBs used in most prior studies.

II. CONCEPTUAL DESIGN OF THE PROPOSED LVDC PROTECTION SYSTEM

As mentioned earlier, DC systems commonly have a very high fault current rise rate. Additionally, fault current selectivity between PDs in LVDC systems is challenging owing to short line lengths. Consequently, previous studies have sought to secure protection selectivity through FCL. Such studies can be classified into two categories. The first includes studies on the use of superconducting fault current limiters (SFCLs), such as flux coupling-type, high-temperature superconducting-type, and hybrid-type SFCLs [15], [16], [17]. However, even in AC systems, superconducting technology is still at the prototype stage, and there are various limitations to its application in small-scale LVDC systems. The second category covers approaches that attach a DC/DC converter-type limiting circuit to the rectifier or use a DCCB with a limiting function. Ghisla et al. [18] proposed a device called a solid-state defender, which acts as a power buffer for upstream faults, discharging stored energy in the internal capacitor to the load, while for downstream faults, it limits the output current to a specific value to provide time for fault removal and isolation of the faulty load. Deng and Chen [19] proposed a series inductor for fault current reduction in HVDC cable accidents between offshore and onshore stations. However, losses and other inductor design issues challenge its application to LVDC. Cairoli et al. [20] presented a method for protection coordination using the current-limiting characteristics of the converter and a DC switch instead of a DCCB. In this method, when a fault occurs, the converter limits the fault current to a range in which the DC switch can operate, isolates the fault location through the operation of the DC switch, and then restores the system by controlling the converter to remove the current-limiting effect. Vanteddu et al. [21] proposed a technology that attaches a current-limiting circuit to the rectifier for a specific target system and protects the capacitor discharge section using high-speed SSCBs and fuses. However, the exact protection method is not described in this research, and the use of high-speed devices restricts its practical applicability. Rachi [22] also proposed connecting a current-limiting circuit to the rectifier for an independent DC microgrid system and installing an SSCB in each PZ. Wang et al. [23] conducted research on DC fault detection and location estimation through fault current reduction. In their method, a modular

multilevel converter with self-FCL and circuit-breaking function reduces the fault current. Further, Li et al. [24] proposed an SSCB with a self-adaptive FCL function and presented a protection method involving the combined operation of the proposed SSCB and a mechanical DCCB. All the above mentioned methods demonstrate a certain degree of practicality in that they apply FCL circuits to rectifiers. However, they require complex coordination between multiple high-speed PDs and are dependent on highly specialized limiting circuit breakers.

The overall concept of the proposed protection system is shown in Fig. 1. A separate limiting circuit is connected to the rectifier. A buck-type limiter is used as the limiting circuit. Moreover, a DAB-type converter is used as the limiting converter. This allows reduction of the fault current during a fault while also enabling separation of fault influences between fault points (F1 and F2 in Fig. 1). We call these PZs. The protections systems of PZ1 and PZ2 are thus separated from each other so that the F2 fault does not generate overcurrent and undervoltage in PZ1. Furthermore, the power-conversion devices can withstand the reduced fault current for a longer duration than they could if it were not reduced, securing time for DCCB operation to clear the fault current. This method enables coordination between the primary PDs responsible for fault removal and the backup PDs which act in case of failure or delay of the primary protection.

Implementation of the design in Fig. 1 requires several assumptions:

1) The LVDC distribution network considered in this study has a radial structure, with multiple potential fault current sources, such as distributed generation and energy-storage devices, interconnected and operating simultaneously.

2) Protection coordination is performed by PDs within each PZ; devices either exhibit instantaneous operation factors, or devices closer to the fault point operate first, with the remaining devices providing backup protection. Because of its previously mentioned constraints, protection through inter-device communication is not considered.

3) When a fault occurs, both the AC/DC rectifier and the load-side DC/DC converters perform FCL functions to reduce the fault current to below a certain level and secure
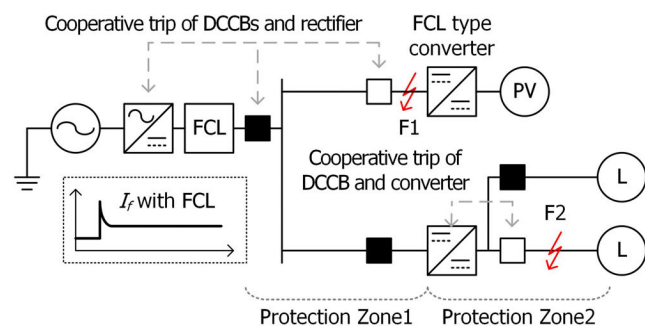
the withstand rating of the power-conversion devices; this ensures a time delay for coordination between devices.

4) Devices that perform protective actions use mechanical DCCBs (breaking speed within 20 ms) and block fault currents through the turning-off operation of power-conversion devices.

The current-limiting devices used in this study are configured as follows.

A. BUCK-TYPE CURRENT LIMITER

The buck converter, the most common DC/DC converter, uses the on/off ratio of the duty signal applied to the insulated-gate bipolar transistor (IGBT) to adjust its output voltage. Current-mode control can be achieved by sensing the output current thought the inductor and using a feedback controller to adjust the duty cycle accordingly [25]. To configure the buck converter for FCL, the duty ratio should be set at 100% during normal load current so that the IGBT is always on and the load is supplied without switching losses. Conversely, during a system fault, the duty ratio must be maintained close to 0%, controlling the supply of current only by the loss component due to residual resistance in the line. However, PDs such as DCCBs should be able to detect faults; thus, if the fault current falls below a certain threshold, the control system should activate switching to allow some current to flow again. Therefore, the buck-type FCL circuit was attached immediately behind the output stage of the power converter to limit the fault current originating from the supply. The configuration of the buck-type FCL circuit is shown in Fig. 2. I_{limit} represents the threshold value for the current-limiting control.

Fig. 3 compares the fault current behavior in an example DC system depending on whether FCL was applied. Fig. 3(a) illustrates the location of each fault current source during a fault in the sample LVDC system, and Fig. 3(b) shows the contribution of each source. In Fig. 3(b), ① indicates the total fault current at the fault point, which is the sum of the fault current supplied by each fault current source, and the discharge current of the capacitor at the converter output; ② denotes the fault current supplied from the DC/DC converter connected to the distributed power source; and
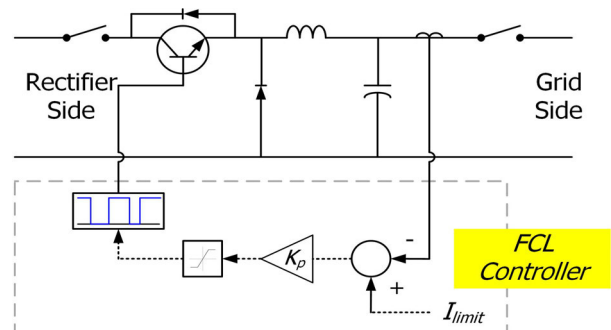

FIGURE 1. Conceptual design of the proposed protection system.

FIGURE 2. Configuration of the buck-type FCL circuit.

(a) One-line diagram of simulation network

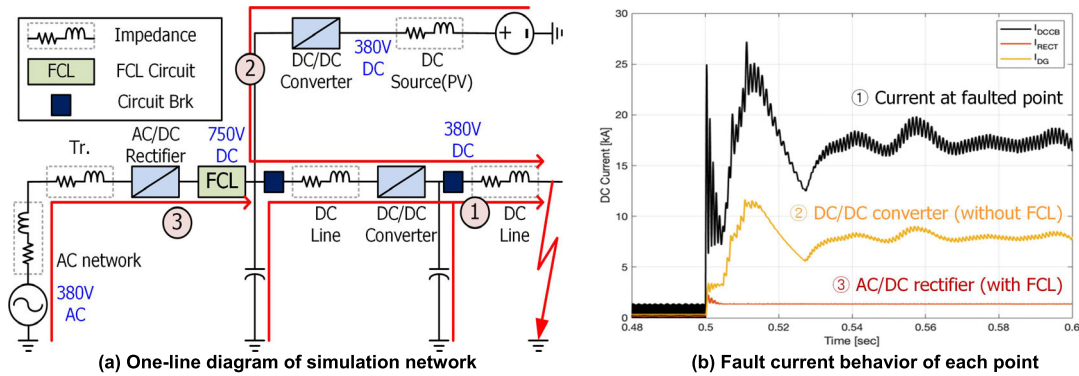**(b) Fault current behavior of each point**

FIGURE 3. Effects of buck-type FCL.

③ represents the fault current supplied from the rectifier with the FCL circuit. Typically, even considering the line impedance of the DC system, the fault current contributed by the converter is in the range of several to tens of kiloamperes without FCL. However, when FCL is applied, it is possible to maintain the fault current at around 1 kA through inductor current control without burdening the converter switches.

B. PHASE-SHIFT DAB CONVERTER

As seen in Fig. 4(a), the DAB converter performs the same function as a DC/DC converter. However, internally, it houses a circuit that transfers power using a section that is typically found in AC systems. On the primary and secondary sides of the AC transformer, there are inverters and rectifiers composed of IGBT switches and diodes, and power is transmitted through the inductance included in the AC circuit. We used a phase-shift DAB converter, which controls the output voltage and power by controlling the phase of the AC voltage generated by the primary- and secondary-side bridge with an inductor in between. This is similar to the transmission of active power due to the voltage phase difference between the sending and receiving ends in an AC system [26].

Fig. 4(b) shows an LLC converter circuit with a series LC resonant circuit inserted on the primary side of the transformer. There are two main differences between the DAB converter and the LLC converter. First, from a circuit perspective, the secondary side is not composed of IGBT switching devices but a resonant tank with a full-wave rectifier diode and a series capacitor for LC resonance in addition to the transformer reactance. Second, from a control perspective, instead of phase control, the load current is controlled by adjusting the primary-side frequency to control the composite impedance of the LLC resonant tank [27]. To compare the fault mechanisms in the DAB and LLC converters during output-stage faults, we consider some equivalent circuits including components that commonly contribute to faults.

In the DAB converter, before a fault, the secondary-side capacitor voltage controls the phase of the secondary-side transformer voltage (Fig. 4(c)). When a fault occurs, the capacitor first discharges, as shown in Fig. 4(d), and the

output terminal voltage drops significantly. Subsequently, as shown in Fig. 4(e), the secondary-side voltage phase controller is effectively disabled, and the magnitude of the fault current is determined solely by the reactance of the inductor.

In the pre-fault equivalent circuit of the LLC converter (Fig. 4(f)), the LLC resonant tank replaces the secondary-side phase controller. When a fault occurs at the output stage of the LLC converter, as shown in Fig. 4(g), the output-stage capacitor discharges, and the voltage drops significantly, as in the DAB case. Thereafter, as shown in Fig. 4(h), the magnitude of the fault current is determined by the LLC resonant tank. However, to recover the lowered voltage in the constant-voltage control mode on the secondary side, the switching frequency on the primary side is lowered, reducing the composite impedance of the LLC resonant tank. Thus, owing to its circuit structure, the self-current limiting function in the LLC is less reliable than that in the DAB converter.

These behaviors are analyzed in more detail below. In a circuit that generates a square-wave voltage with a specific frequency through DAB switching on both ends, the output power is defined as follows [26]:

$$P_o = \frac{V_i V_o}{2 f_s L_s} \left(\frac{\Phi}{\pi} \right) \left(1 - \frac{\Phi}{\pi} \right), \tag{1}$$

where V_i, V_o, and P_o are the magnitudes of the input voltage, output voltage, and power converted from the primary side to the secondary side, respectively; L_S is the internal inductance; f_S is the switching frequency; and Φ is the voltage phase difference. The transmitted current at the output I_o is calculated as follows:

$$I_o = \frac{P_o}{V_o} = \frac{V_i}{2 n f_s L_s} \frac{\Phi}{\pi} \left(1 - \frac{\Phi}{\pi} \right) \tag{2}$$

where n is the transformer turns ratio.

When the phase difference between the primary- and secondary-side transformer voltages is 90°, i.e., $\Phi = \pi/2$, I_o (rms) is at its maximum; hence,

$$I_{o,90°(rms)} = \frac{V_i}{8 n f_s L_s} \tag{3}$$

When applying V_{in} as a square wave through the primary-side switching circuit, the current waveform exhibits
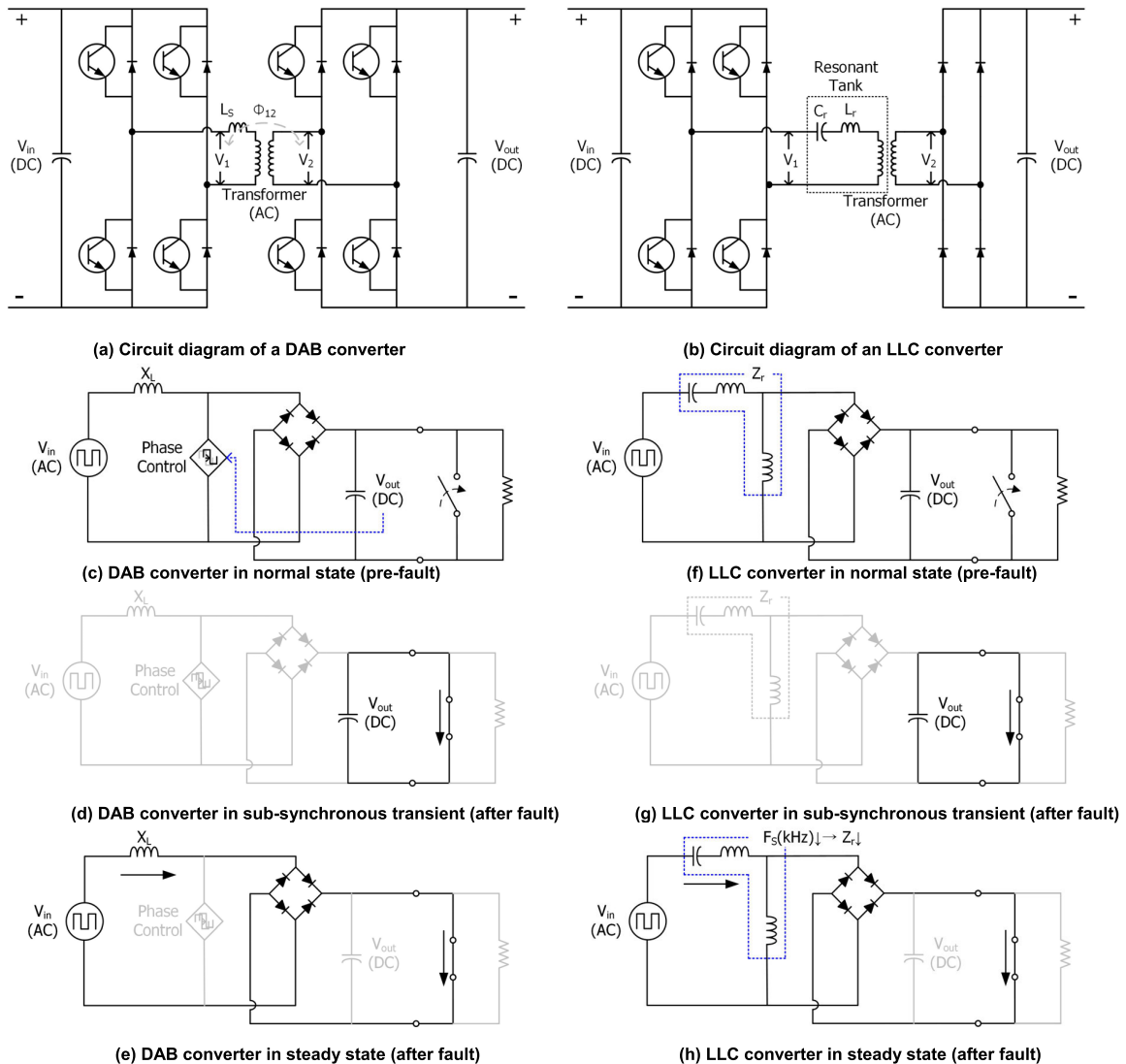
FIGURE 4. Comparison of FCL characteristics for converters.

a sawtooth shape, and the maximum steady-state current value is $\sqrt{3}$ times the rms value, as follows:

$$I_{o,90°(peak)} = \frac{\sqrt{3}V_i}{8nf_sL_s} \tag{4}$$

If the L_s value is selected so that the rated current flows when the phase difference is 60° ($\Phi = \pi/3$), the ratio of the rated current to the maximum transferable current and the ratio of the rated current to the peak fault current are calculated as follows. Note that the peak mentioned here is not the peak due to the discharge of the output capacitor, but the maximum value of the current supplied through the rectifier in the steady state.

$$\frac{I_{o,90°(rms)}}{I_{o,60°(rms)}} = 1.125 \tag{5}$$

$$\frac{I_{o,90°(peak)}}{I_{o,60°(rms)}} = 1.9486 \tag{6}$$

Hence, even if a fault occurs while operating at maximum load, the current increase rate is approximately 1.125 times the rated load current based on the rms value, which is within the range observed during a slight overload in non-fault situations. Table 1 summarizes the fault current increase ratio for the main design range.

In a conventional DAB converter design, the inductance (L_S) value is selected so that the rated power occurs within around 60° of the voltage phase difference. Therefore, the inductance in the AC circuit has a considerably high impedance value of approximately 50%–85%. In an LLC-type converter with such a high internal impedance, the large resulting voltage drop makes it difficult to supply the current normally needed for the load. However, a DAB converter can provide series compensation for the internal inductor by simultaneously controlling the voltage phase on both the primary and secondary sides; thus, normal voltage and power can be transferred to the load side. Furthermore, in such

TABLE 1. Current ratio between maximum and rated value according to rated phase shift.

Rated Phase Shift (°)	$I_{o,90^o(rms)}/I_{o,\text{rated}}$	$I_{o,90^o(peak)}/I_{o,\text{rated}}$
30	1.8	3.1177
45	1.3333	2.3094
60	1.125	1.9486
90	1.0	1.7321

conventional designs, the fault current of the DAB converter stays at approximately twice the load current, which is lower than that occurring in a buck converter without FCL (which can be 20 times the load current). In other words, the DAB prevents the generation of a large fault current due to the internal passive element, the inductor, even without any special control during a fault. Therefore, in the protection of a system including a DAB converter, it may be difficult to clearly distinguish between overload situations and fault currents and additional fault-related factors such as low voltage must be considered in addition to the current.

III. PROPOSED LVDC PROTECTION SYSTEM

Fig. 5 shows the proposed design procedure for setting the PDs in the LVDC distribution system. The procedure can be loaded onto the LVDC operating system or a dedicated controller for PD calibration. It can be summarized as follows:

1) Perform fault current calculations for the target system using various simulation tools. This calculates the expected fault currents for faults in each part of the system.

2) Use system topology data to distinguish PZs within the network and identify the type of each PD.

3) Combine the results of 1) and 2) to determine the required current-limiting settings of the power-conversion devices for protection coordination in each PZ.

4) Combine 2) and 3) to determine the operating setpoints for each PD and power-conversion device. This can be transmitted to the field device through a communication network or changed manually.

5) If there is a change in the system topology, repeat steps 1)–4).

To apply the above mentioned calibration procedure, the operational data of the general LVDC system are required, which can be implemented in an operation system database or controller memory. This includes the topology information for each facility (rectifier, converter, load, distributed power, battery, circuit breaker, switch, etc.), open/close information for circuit breakers and switches, impedance (R, L, and C) of each facility, length of each transmission line section, capacity of rectifiers and component facilities (converter, load, distributed power, etc.), rated voltage of each system point, and current-limiting characteristics of rectifiers and converters.

The PZs and PDs in Fig. 5 can be explained using a typical LVDC distribution system, as shown in Fig. 6. Fig. 6(a) shows the PZs divided according to distributed power sources, bidirectional converters, DC loads, and circuit breakers, which
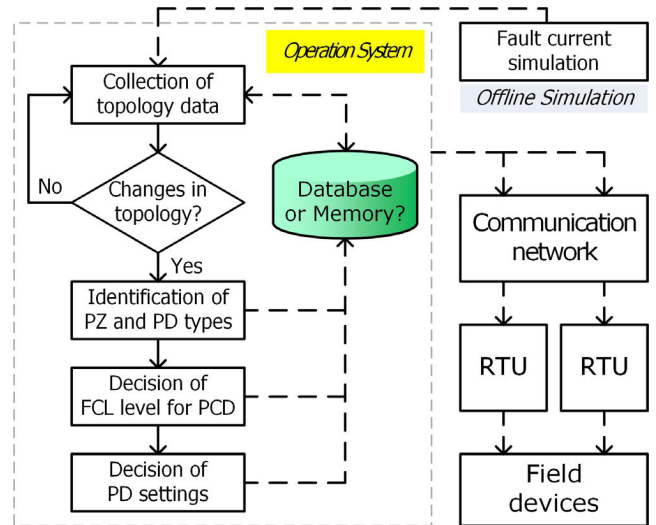

FIGURE 5. Procedure for engineering the proposed protection system.
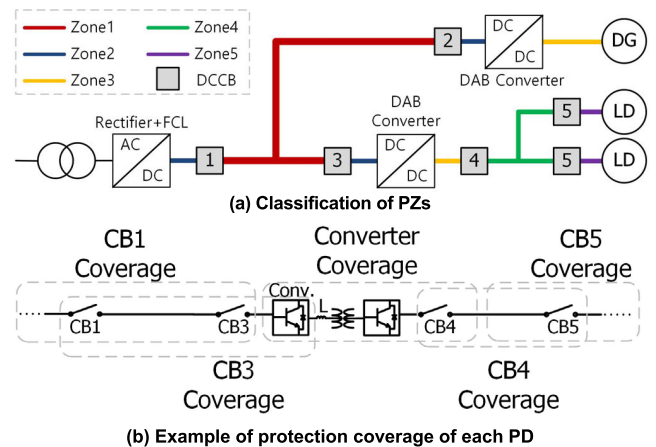

FIGURE 6. Conceptual diagram for LVDC protection coordination with PZs and PD coverage.

become fault current sources or paths in the event of a DC system fault. The division of PZs is designed considering two aspects. First is fault section isolation by the FCL function. When a fault occurs on the secondary side of the DAB converter, the control power for the phase shift control of the secondary-side voltage collapses, and most of the apparent power input from the primary side changes into reactive power owing to the change in AC power factor ($S \approx jQ$). However, this affects the power factor rather than the magni-

tude of the input power; hence, the magnitude of the fault current observed at the primary-side input stage does not increase significantly compared to the load current. In other words, the fault on the secondary side (Zone3 fault) is isolated from the primary side (Zone1 and Zone2) because of the circuit characteristics of the DAB converter. The second consideration in division of PZs is setting the protection coverage of circuit breakers and converters. Fig. 6(b) shows the protection coverage of each circuit breaker and converter based on the circuit in Fig. 6(a). Each PZ overlaps with the primary and backup PDs, and 2-3 PDs are associated with each zone.

For example, DCCB3 must respond to both Zone1 and Zone2 faults when distributed power is connected to the converter. More precisely, it manages up to the front end of the inductor on the primary side of the internal transformer of the DAB converter. In Zone3, which is the area after the inductor, the DAB limiting function operates, making it difficult to observe faults using only the current passing through CB2. Hence, the protection function can be implemented by also detecting the voltage drop on the secondary side of the converter and stopping the primary-side switching.

Considering the above facts, the protection-related devices in the sample LVDC system in Fig. 6(a) including FCL are defined as follows:

1) $DCCB_B$ (DCCB for DC bus): This includes DCCB1, DCCB2, and DCCB3, which are devices capable of blocking rectifiers and converters.

2) $DCCB_{ML}$ (DCCB for multiple load lines): This includes DCCB4, which is a device capable of blocking multiple load branch lines supplied by load-side converters.

3) $DCCB_L$ (DCCB for each load line): This includes DCCB5, which is a device capable of blocking a single load branch line supplied by a load-side converter.

4) Rectifiers and converters: Faults can also be removed by turning off the rectifiers and converters. In the case of bidirectional converters such as DAB converters, when a fault occurs, the direction of current flow reverses depending on whether a load or a generator is connected. Hence, to perform protection coordination including the converter, both primary and secondary zones on either side of the converter must be considered as protection areas.

As shown in Fig. 6(a), each PZ is distinguished according to the following criteria:

1) Zone1 is defined as the section where the power flow is integrated and distributed. It includes the downstream of the $DCCB_B$ for the AC/DC rectifier and the upstream of the $DCCB_B$ for the load and distributed generation.

2) Zone2 is defined as the section between Zone1 and the nearest fault current source or DC/DC converter, in this case, the area between the AC/DC rectifier or DC/DC converter and $DCCB_B$.

3) Zone3 is defined as the section from the output terminal of the converter to the DCCB, in this case being the area between the DC/DC converter and $DCCB_{ML}$.

4) Zone4 is defined as the front end of the load line and branch circuit section, which is the area between $DCCB_{ML}$ and $DCCB_L$ in this example.

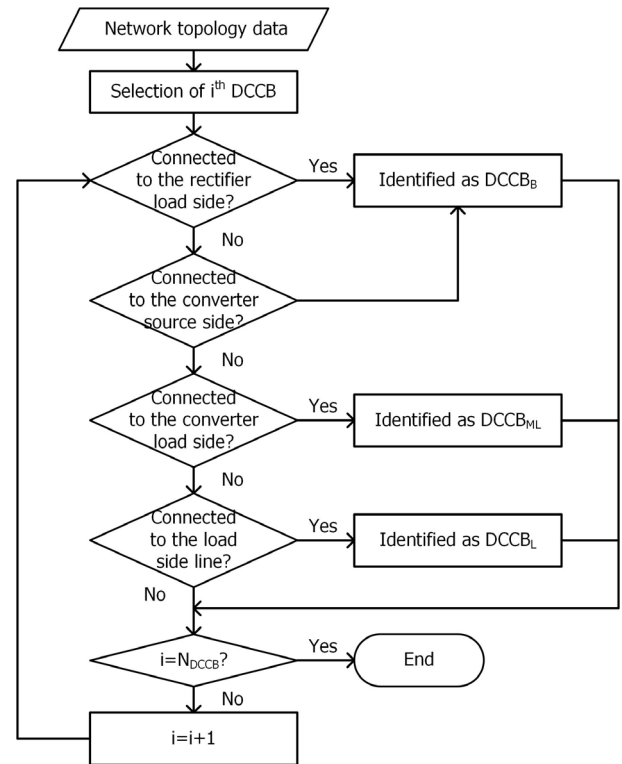5) Zone5 is the end section of the load line, which is the load-side area of $DCCB_L$ here.

FIGURE 7. Classification of the type of DCCB.

The types of DCCB can easily be identified with the flowchart shown in Fig. 7, and if there are any changes in the system topology or configuration of the equipment, immediate modification and identification are possible using the same flowchart.

For faults in each protection area, the protection coordination requirements to minimize the fault section are summarized as follows:

1) Zone1 fault (Fig. 8(a)): The primary protection blocks the fault current contributors by opening all $DCCB_B$s adjacent to Zone1. DCCB1 and DCCB2 experience forward fault currents, and DCCB1-DCCB3 experience a low voltage because the limiting function of each converter side cannot send sufficient current to maintain the bus voltage. Therefore, $DCCB_B$ should have relay elements for a low voltage or forward overcurrent to operate for Zone1 faults. In addition, each DAB converter should be able to operate owing to the low voltage of the primary side as backup protection. This requires time-delayed operation for protection coordination with the primary PDs of Zone2 faults (explained next).

2) Zone2 fault (Fig. 8(b)): For proper protection, only the nearest DCCB2 among the $DCCB_B$s and DC/DC converter needs to operate. To achieve this, they must determine the
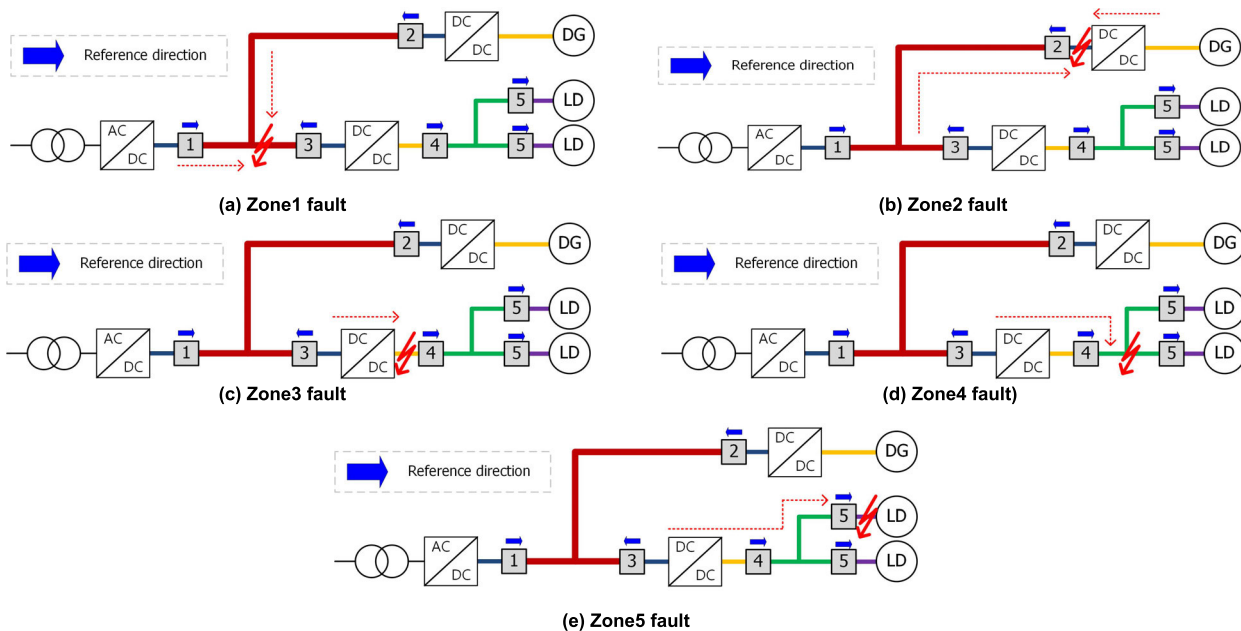
FIGURE 8. Fault current flow for faults in each PZ.

fault direction (forward or reverse, relative to the reference direction) along with the overcurrent and operate accordingly. When reverse (converter direction) overcurrent is experienced with the bus-side direction as the reference direction, the primary protection should operate instantaneously. For backup protection, the response to the primary-side low voltage of the corresponding DAB converter can be used.

3) Zone3 fault (Fig. 8(c)): If the DC/DC converter does not have a limiting function, DCCB3, a DCCB$_B$, can operate instantaneously for proper protection. However, the internal reactance of the DAB converter limits the fault current, making it difficult for DCCB3, upstream of the DAB, to experience a low voltage or overcurrent caused by the fault. Therefore, the DC/DC converter should block and stop the primary-side switching after detecting the low voltage or overcurrent of the secondary side. Backup protection can operate by detecting a reduction in the input power factor to DCCB3 from the DAB converter side. However, this power factor change is only applicable to phase-shift control-type DAB converters. If there are other converters with FCL functions, a suitable converter backup protection fault-detection method should be applied.

4) Zone4 fault (Fig. 8(d)): For proper protection, the load circuit breaker DCCB4 needs to operate instantaneously by detecting an overcurrent in the load direction. To prevent the converter from operating simultaneously, the DAB converter adjacent to Zone3 upstream performs a delayed operation, avoiding simultaneous operation and serving as backup protection. The circuit breaker for Zone4 protection should perform a time-delayed operation for protection coordination with the primary PDs of Zone5 (described next).

5) Zone5 fault (Fig. 8(e)): For proper protection, the branch circuit breaker DCCB5 should operate instantaneously for overcurrent.

By reviewing Fig. 8 for each PZ, the relaying methods and operation criteria for each PD (DCCBs and power-conversion devices) were determined, as presented in Table 2. For the PD setting in Fig. 5, the criteria in Table 2 can be applied simply according to the PD type identification results in Fig. 7.

The overcurrent calibration criterion among the relay elements is as follows:

$$I_{pi} = I_r \times \alpha, \tag{7}$$

where I_{pi} is the pickup current for the operation criterion of the PD, and I_r is the rated maximum current, which is based on the rated capacity of each connected AC/DC rectifier or DC/DC converter in the case of a DCCB$_B$. For DCCB$_{ML}$ and DCCB$_L$, it is based on the load capacity of the corresponding protection zone. Further, α is the setting factor, which is set in the range of $1 < \alpha < I_{max}(PU)$, and $I_{max}(PU)$ is the per unit value of the effective maximum fault current penetrating each PD with a duration of at least 1ms, considering the fault current calculation value and the FCL effects of the DAB converter and FCL. The low-voltage calibration criterion is as follows:

$$V_{pi} = V_{nor} \times \beta, \tag{8}$$

where V_{pi} is the operation criterion voltage for the PD (or rectifier/converter), V_{nor} is the nominal voltage at the installation point of the corresponding PD, and β is the setting factor, which is set in the range of $0 < \beta < V_{nor}(PU)$. The phase angle calibration criterion is set as follows:

$$D_{pi} = 1, \text{ if } (P_{vol} \times P_{cur}) \neq D_{set}, \tag{9}$$

TABLE 2. Relaying elements and trip operation for each protection device.

Types of PD	Relaying elements	Trip operation
DCCB$_B$	Low-voltage OR forward overcurrent	Definite time delay
	Low-voltage AND reverse overcurrent	Instantaneous
DCCB$_{ML}$	Forward overcurrent	Instantaneous
DCCB$_L$	Forward overcurrent	Instantaneous
Converter	Low-voltage OR forward overcurrent	Definite time delay

(a) Demonstration site at Naju
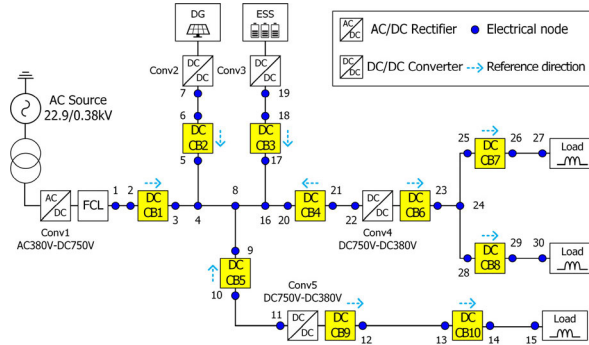
(b) Schematic of the demonstration site

FIGURE 9. Photo and schematic of the LVDC demonstration site at Naju.

where D_{pi} is the reverse direction detection flag: the initial value is 0 (false), but when the product of the voltage polarity (P_{vol}) and current polarity (P_{cur}) at the corresponding point differs from the criterion (D_{set}), it changes to 1 (true).

IV. CASE STUDY EVALUATION OF THE PROPOSED LVDC PROTECTION SYSTEM

From 2019 to 2022, the ''Development of DC micro grid system equipment technology capable of system autonomous control and protection cooperation for DC consumer'' project was carried out with the support of the Korean government for the overall development of LVDC technology and related equipment. In relation to this project, a demonstration site was established in Naju City, South Korea, to enable verification of developed technologies, as shown in Fig. 9(a). Fig. 9(b) shows a schematic of the demonstration site. This site was utilized for evaluation of the LVDC distribution protection system proposed in this study.

The target LVDC network includes five converters and 10 DCCBs, with each converter connected around a 750 V bus. A 500-kW-rated rectifier (Conv1) is located on the left side of the system diagram, serving as the source of the 750 V DC main power supply. It is connected to the 750 V bus through a buck-type fault current limiter capable of limiting fault current to approximately 1 kA (1.5 times the rated current). Conv2 and Conv3 are both 250 kW DAB converters with photovoltaic (PV) units and ESSs as their sources, respectively. Conv4 is a 500 kW DAB converter for supplying load power, generating an output voltage of 380 V. Conv5 uses a multi-channel DAB converter with a maximum input

power of 20 kW and a maximum output of 5 kW per channel. DCCB1- DCCB5 are DCCB$_B$s for protecting the 750 V bus and branch circuits, with the reference current direction set as the bus-side direction. DCCB6 and DCCB9 are DCCB$_{ML}$s, and the remaining circuit breakers are DCCB$_L$s. In each case, the circuit breaker operates with a delay of 50 ms for both forward overcurrent (at least 150% of rated current) and low voltage. For instantaneous operation, the circuit breakers activate when reverse overcurrent persists for more than 3 ms. The undervoltage protection activates when the voltage drops to $\leq$ 50% of the rated voltage. Tables 3 and 4 summarize the line data, converter capacity, and parameters of the test system.

The case study for the demonstration system in Fig. 9 was conducted in two ways: one using MATLAB/Simulink simulation, and the other using a HILS test.

A. VERIFICATION OF THE PROPOSED PROTECTION SYSTEM USING MATLAB/SIMULINK

For the test, the LVDC system shown in Fig. 9 was implemented as a MATLAB/Simulink model as shown in Fig. 10. Each DCCB and converter includes logic that senses the magnitude of the respective input and output voltage and current and uses it to determine faults independently; this was achieved through a user-defined model block implemented in the script. In this work, calculations were performed with a timestep of 0.1 μs to minimize waveform distortion due to low sampling frequency.

To determine whether the protective function could be operated by relay elements such as voltage and current

TABLE 3. Line parameter data of test network.

From	To	Length (m)	Resistance (Ω)	From	To	Length (m)	Resistance (Ω)
1	2	4.5	3.42×10^{-4}	16	17	0.1	1.0×10^{-7}
3	4	0.1	1.0×10^{-7}	18	19	3	5.49×10^{-4}
4	5	0.1	1.0×10^{-7}	16	20	0.1	1.0×10^{-7}
6	7	5.4	9.88×10^{-4}	21	22	7	5.32×10^{-4}
4	8	0.1	1.0×10^{-7}	23	24	0.1	1.0×10^{-7}
8	9	0.1	1.0×10^{-7}	24	25	3	1.96×10^{-4}
10	11	30	0.1614	26	27	5.2	0.0016
12	13	20	0.31	24	28	3	1.96×10^{-4}
14	15	0.1	1.0×10^{-7}	29	30	5.2	0.0016
8	16	0.1	1.0×10^{-7}	-	-	-	-

TABLE 4. Capacity and parameter data of each converter.

Name	Type	Capacity (kW)	Voltage (V)	Output capacitor (mF)	Inductance (μH)	Purpose
Conv1	Rectifier	500	380/750	30	-	Main source
FCL	Buck type	500	750/750	1	200	Current limiting
Conv2	DAB	250	600/750	1	2.5	PV
Conv3	DAB	250	600/750	1	2.5	ESS
Conv4	DAB	500	750/380	8	1.25	DC loads
Conv5	DAB	20	750/380	1.32	50	DC loads

(a) LVDC grid Simulink model

(b) DCCB model
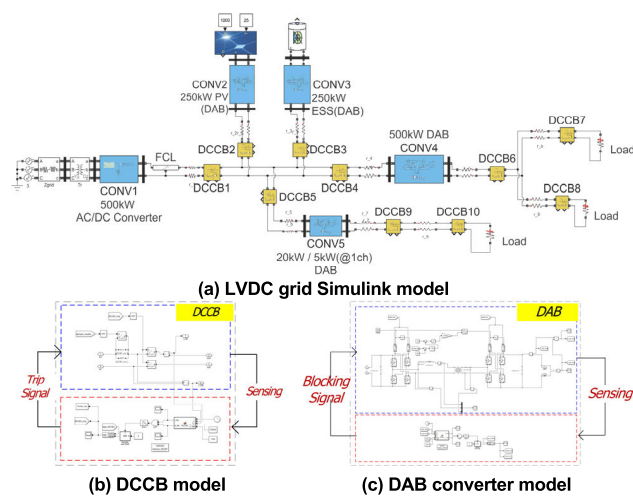
(c) DAB converter model

**FIGURE 10.** Demonstration network implemented in MATLAB/Simulink.

in LVDC systems based on the FCL and DAB converters, it was simulated using the MATLAB/Simulink model shown in Fig. 10; the results are presented in Fig. 11.

To compare each result from various cases briefly, the time of fault occurrence was set to the same at 0.2 s, and the units of voltage and current were standardized as per unit so that they could be compared at once.

The simulation results are summarized as follows. First, in Fig. 11(a), the PZ1 and PZ2 faults for each case that can occur in a 750 V system are simulated, and the voltage and current waveforms are shown. In this figure, V_{PZ1} (F_{PZ1}) and V_{PZ1} (F_{PZ2}) are the voltage measurements at PZ1 for the PZ1 and PZ2 faults, respectively. I_{CB2} (F_{PZ1}) and I_{CB2} (F_{PZ2}) are the current flows through DCCB2 for the cases of the PZ1 and PZ2 faults, respectively.

The PZ1 fault should be detected from a comparison of I_{CB2} (F_{PZ1}) and V_{PZ1} (F_{PZ1}). If it is a typical power system fault, it can be detected only by overcurrent; however, the simulation shows that the magnitude of the fault current I_{CB2} (F_{PZ1}) (black solid line) was not far from the rated load current. This is the result of the FCL effect of the DAB converter. In this case, the voltage V_{PZ1} (F_{PZ1}) (black circle symbol) was changed to nearly zero after the fault. In the PZ2 fault, as in the PZ1 fault, the voltage magnitude V_{PZ1} (F_{PZ2}) immediately dropped close to zero after the fault. Therefore, even if the voltage magnitude enabled the determination of the fault occurrence, it could not be used to distinguish the fault location of PZ1 and PZ2. In the case of the current magnitude, the current of DCCB2, I_{CB2} (F_{PZ1}), was maintained in the reference direction (positive) after the fault, but I_{CB2} (F_{PZ2}) (yellow line) changed in the reverse direction (negative) right after the fault in PZ2. The current magnitude also increased to around four times (∼1.3 kA) of the rated current. This can be seen as the result of the sum of another DAB converter current (∼0.3 kA) and the current of FCL (set as 1kA) which is connected at the output port of the rectifier (CONV1). Therefore, to detect and isolate the fault in PZ1 and PZ2, it is preferable that the device between PZ1 and PZ2 (e.g., DCCB2) first detects and blocks the fault by using its reverse overcurrent. Further, if the first protection fails, the
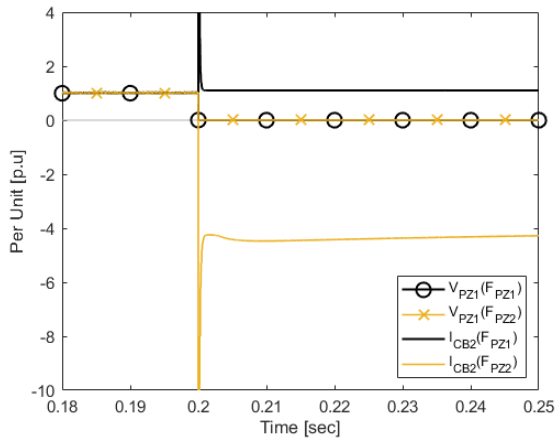
(a) Voltage/current profiles of the fault cases in PZ1 and PZ2
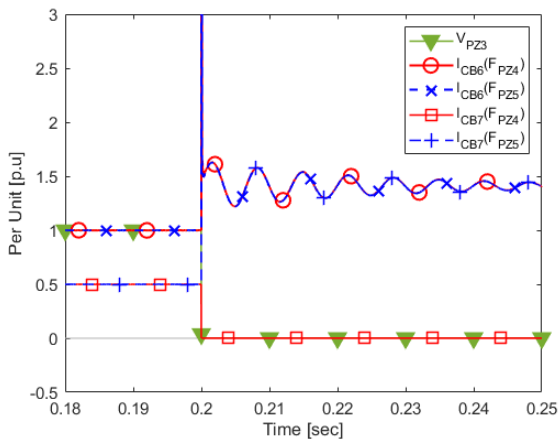
(b) Voltage/current profiles of the cases of faults in PZ4 and PZ5

FIGURE 11. Results of MATLAB/Simulink case study simulation.

FIGURE 12. Overall configuration for the HILS test.

protective devices adjacent to PZ1 must provide coordinated backup protection by using low voltages.

Next, in Fig. 11(b), voltage and current waveforms are shown by simulating faults in PZ3, PZ4, and PZ5 for each case that may occur in the 380 V system, which is the downstream grid of the load supply DAB converter (CONV4). Similar to the fault case of PZ1 and PZ2 described above, PZ3, PZ4, and PZ5 showed zero voltage immediately after the fault. For the PZ5 fault, the currents of DCCB6 and DCCB7, namely, I_{CB6} (F_{PZ5}) (blue X symbol) and I_{CB7} (F_{PZ5}) (blue plus symbol), respectively, were almost the same after fault. However, for the PZ4 fault, the current of DCCB6, I_{CB6} (F_{PZ4}) (red circle symbol), increased by 1.5 times the load current, but the fault current did not pass through DCCB7; thus, the current of DCCB7, I_{CB7} (F_{PZ4}) (red square symbol), dropped to zero. Therefore, for the DCCB that protects PZ4 and PZ5, the fault is detected by the overcurrent element, but the terminal breaker (between PZ4 and PZ5) must block the PZ5 fault first, and in the case of the branch breaker (between PZ3 and PZ4), it must provide protection coordination with sufficient time to clear the fault. Regarding the fault of the converter output terminal (PZ3), the converter must provide
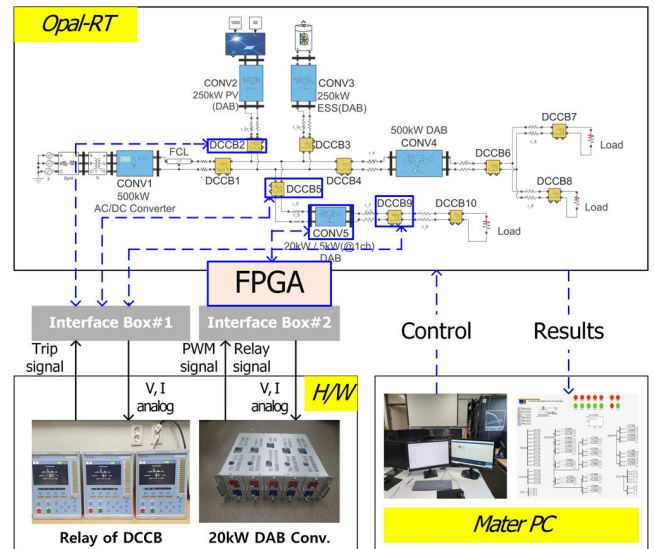
delayed off protection by detecting a low voltage as in the fault case of PZ1 and PZ2.

The operation of PDs and converters for each PZ fault after summarizing and generalizing the results of the case studies is summarized in Table 5. As seen in Table 5, only the devices that remove the fault current source operate for each fault, minimizing the propagation range of the fault and improving supply reliability.

B. VERIFICATION OF THE PROPOSED PROTECTION SYSTEM IN HILS ENVIRONMENT

In addition to the software simulation, we conducted experiments using a HILS simulator to verify the proposed protection method in actual systems. Opal-RT was used as the simulator for HILS, and the DCCB relay and DAB-type converter applied to the demonstration system shown in Fig. 9(a) were tested in conjunction. For this purpose, the LVDC demonstration system tested with MATLAB/Simulink was ported to the Opal-RT software environment, RT-LAB, and the environment was configured to perform calculations with a multicore CPU. The overall test environment configuration is shown in Fig. 12.

Although the maximum calculation timestep supported by Opal-RT is 10 μs, the 20 kW DAB converter used in the experiment required a calculation time of about 0.2 μs for proper pulse width modulation (PWM) performance. We resolved this issue by implementing the internal circuit of the DAB converter in a field programmable gate array (FPGA) with a 0.2 μs calculation capability. The FPGA received the DAB input voltage as a digital signal from the system model mounted on Opal-RT and directly input a 40 kHz high-frequency PWM optical signal generated by the DAB hardware control board, processing and analyzing it as IGBT switching signals for the primary and secondary bridges within the Conv5 shown in Fig. 12. The FPGA then

TABLE 5. Behaviors of protection and protection control devices for each PZ fault.

Fault	DCCB							Converter				
	750V					380V		Source			Load	
	1	2	3	4	5	6/9	7/8/10	1	2	3	4	5
PZ1	DV	DV	DV	DV	DV	-	-	DV	DV	DV	-	-
PZ2	IC	IC	IC	IC	IC	-	-	DV	DV	DV	-	-
PZ3	-	-	-	-	-	-	-	-	-	-	DV	DV
PZ4	-	-	-	-	-	DC	-	-	-	-	DV	DV
PZ5	-	-	-	-	-	DC	IC	-	-	-	DV	DV

("-": not tripped, "DC"/"DV": delay-tripped by current/voltage, "IC": instantaneously tripped by current)
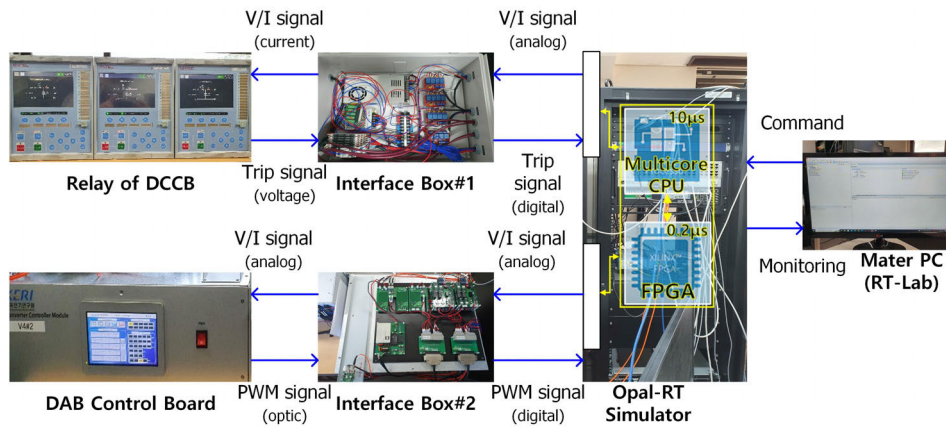

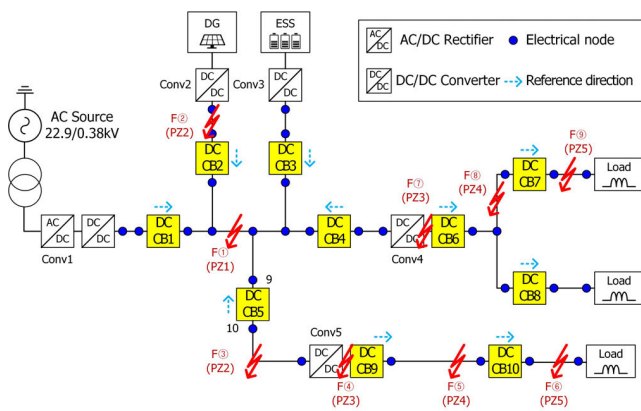**FIGURE 13.** Overall signal transmission for the HILS test.

FIGURE 14. Fault simulation points for the HILS test.

output the secondary-side output voltage and primary-side input current values as the results of the circuit analysis to the CPU. Accordingly, the FPGA directly performed the short-cycle DAB circuit analysis without going through the CPU, and the DAB-integrated HILS processed by the CPU was configured to enable long-cycle analysis. Furthermore, the input signal of the DCCB relay was a current within 20 mA, and the PWM of the 20 kW DAB converter control board was transmitted through an optical signal. However, Opal-RT requires voltage signals for input/output; therefore,

separate interface devices were fabricated and tested for signal transmission between both devices. The overall signal-transmission system is shown in Fig. 13; Interface Box#1 is configured to match the input/output analog signal types and levels between the Opal-RT signal and the DCCB protection relay, and Interface Box#2 includes a converter that changes the PWM optical signal generated by the DAB converter H/W controller and input/output voltage and current signals into analog signals exchangeable with the FPGA.

The fault simulation points for HILS are shown in Fig. 14. As indicated, faults were simulated for nine cases including all PZs. Among them, Cases 1–6 are relevant for determining the direct protection coordination of the connected hardware PDs.

Figs. 15–19 show the test results for fault cases 1, 2, 4, 5, and 6 corresponding to PZ1-PZ5, respectively. In each figure, individual tile-type graphs are provided, along with pictures of the trip alarm section of the RT-LAB monitoring screen and the actual hardware, making it easy to check the operation status of the PDs composed of hardware and software models. A green light indicates that the device is on, and a red light signifies an open state due to a trip. The yellow circles mark the trip alarm lights in the hardware device photos.

The results of fault point 1 in Fig. 15 show that the PZ1 fault was resolved by the tripping of each relay element with DCCB$_B$s (DCCB1 to DCCB) that protect against 750 V bus
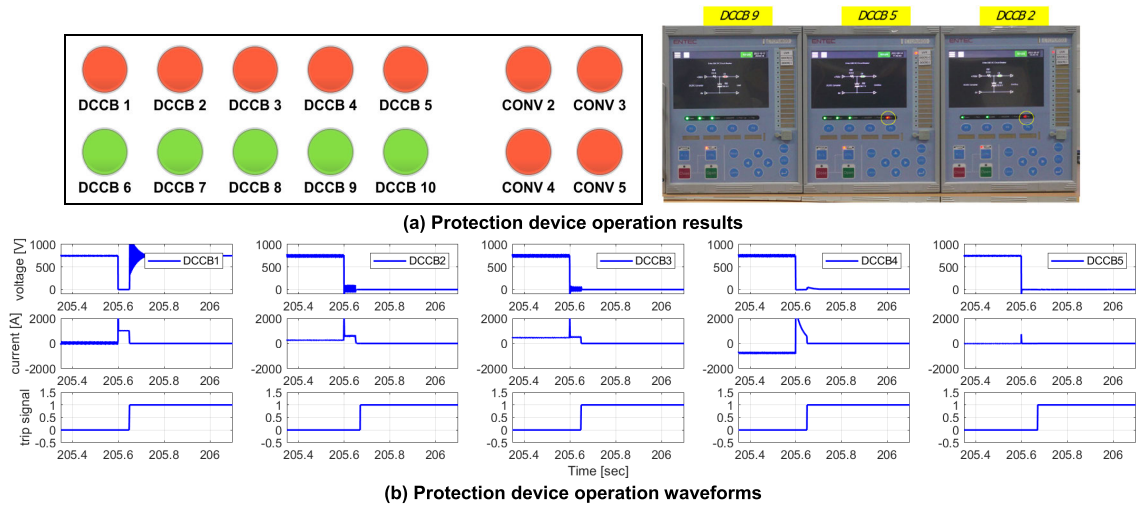
(a) Protection device operation results

(b) Protection device operation waveforms

FIGURE 15. Test results of fault case① for PZ1.

(a) Protection device operation results

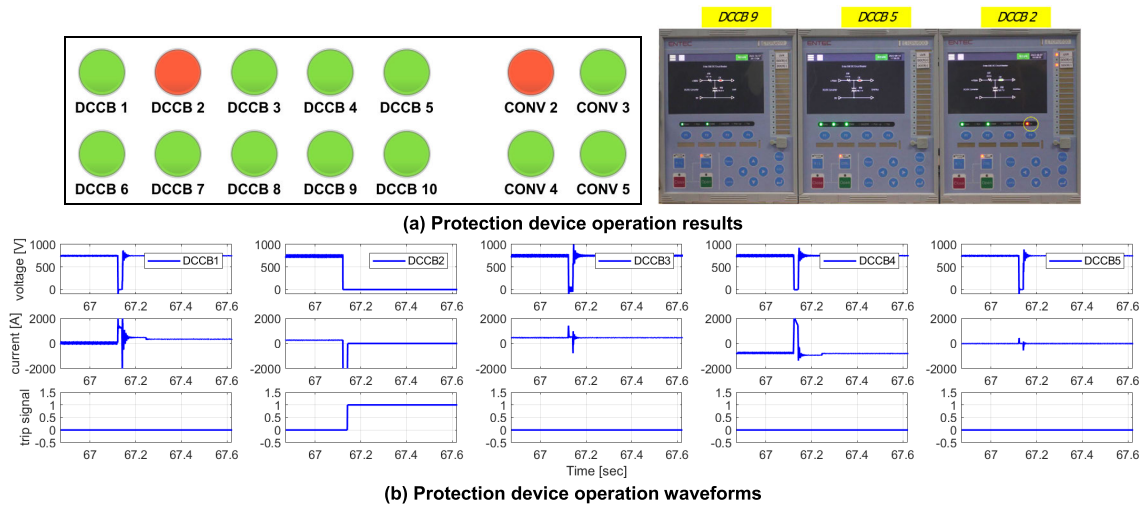(b) Protection device operation waveforms

FIGURE 16. Test results of fault case② for PZ2.

accidents. In Fig. 15(a), the hardware-based DCCB2 and DCCB5 indicator lights are red, and the trip signal alarm reference value can be found to have operated owing to low voltage (the yellow circles in the top right insets). The remaining software models also successfully generated trip signals and blocked the circuit, as evidenced by the trip signal graphs (the bottom line of graphs) in Fig. 15(b).

Fig. 16 shows the results of fault point 2 between DCCB2 and the PV-side converter Conv2. In Fig. 16(a), it can be confirmed that the hardware-based DCCB2 detected reverse overcurrent and operated instantaneously. Consequently, the fault section PZ2 was isolated from other healthy sections, and, in Fig. 16(b), it can be confirmed that the circuit breakers in other sections remained in the on state, ensuring a normal power supply.

Fig. 17 shows the results for fault point 4 of PZ3, a case in which the operation of the DAB converter (Conv5) controller

hardware can be verified. In Fig. 17(a), the DAB converter controller detected a forward overcurrent and a low voltage lasting for 50 ms, generating a fault state alarm and halting switching. In Fig. 17(b), only Conv5 generated a trip signal, and the current waveforms of other converters or DCCBs show that the fault current did not propagate owing to the limiting effect of the DAB itself.

Fig. 18 shows the results of fault point 5 of PZ4. In Fig. 18(a), the hardware-based DCCB9 detected a forward overcurrent of more than 150% of the load current for 3 ms and blocked the fault. In Fig. 18(b), there was no trip occurrence because the ripple effect of the fault did not propagate to other devices.

Fig. 19 shows the results for fault point 6 of PZ5. Fig. 19(a) shows that the software model DCCB10 resolved the fault at the load terminal, and the hardware-based PDs did not perform any breaking actions. In Fig. 19(b), the load disappeared
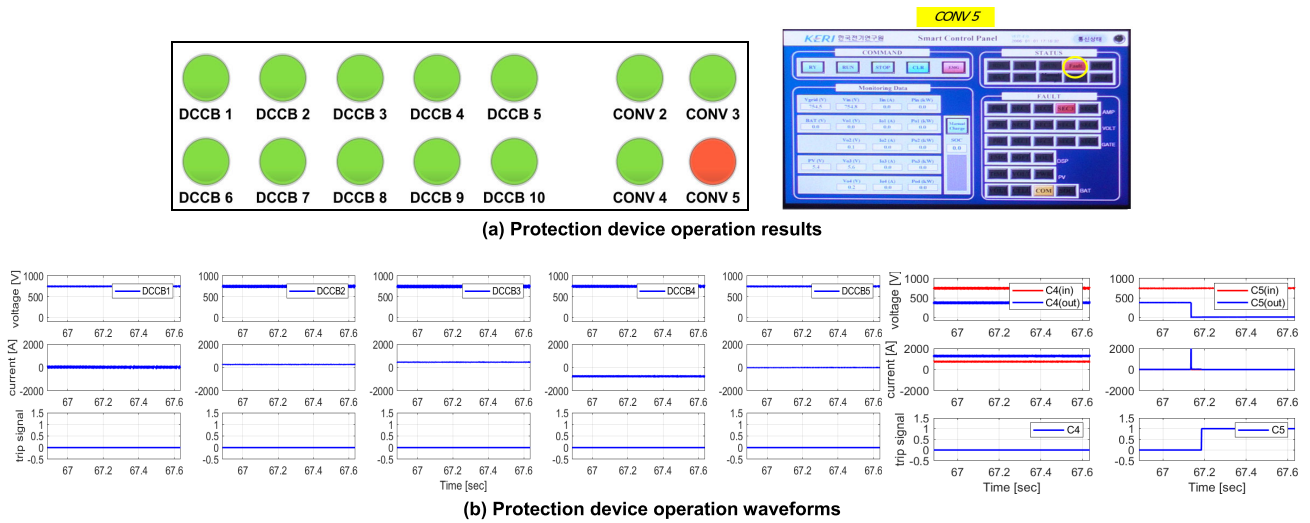
(a) Protection device operation results

(b) Protection device operation waveforms

FIGURE 17. Test results of fault case④ for PZ3.

(a) Protection device operation results
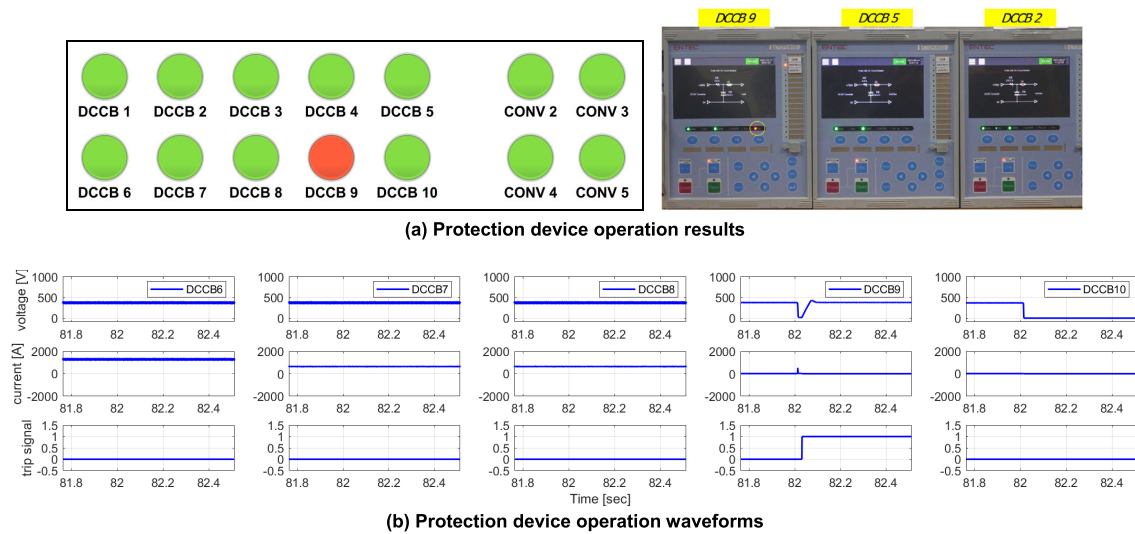

(b) Protection device operation waveforms

FIGURE 18. Test results of fault case⑤ for PZ4.

because of the opening of DCCB10, but it was restored to the rated voltage of 380 V through the constant-voltage control of the converter.

A quantitative performance comparison was performed between the proposed method and the protection methods from the previous research. The comparison included previous studies such as Tang and Ooi's handshaking method [7] and the method proposed by Monadi et al. [10], which share similarities with the proposed method based on directional overcurrent. In both methods, once a fault is detected, all the fault current sources are blocked. Next, the fault section is isolated by opening the switches on both sides of the line sections. Finally, the faultless sections are restored by closing AC or DC circuit breakers and restarting the DC converters. The method of Tang and Ooi [7] does not utilize communication among devices, whereas the method of Monadi et al. [10]

employs communication among devices to identify the fault section.

For a quantitative comparison, reliability indices are used to express the stochastic failures observed at the load side. In this paper, the system average interruption frequency index (SAIFI), which represents the count of power outages, and the system average interruption duration index (SAIDI), which measures the average outage duration per load per year, were used. These indices are widely used as reliability evaluation indicators for distribution systems. The performance analysis of the test system shown in Fig. 9(b) was conducted. Unlike AC systems, failure rate statistics for DC distribution systems have not yet been clearly published. Therefore, the failure rate of the longest section (30 m) in the test system, which is the section between node10 and node11, was assumed to be 1.0 per year. Further, the failure rates of the remaining
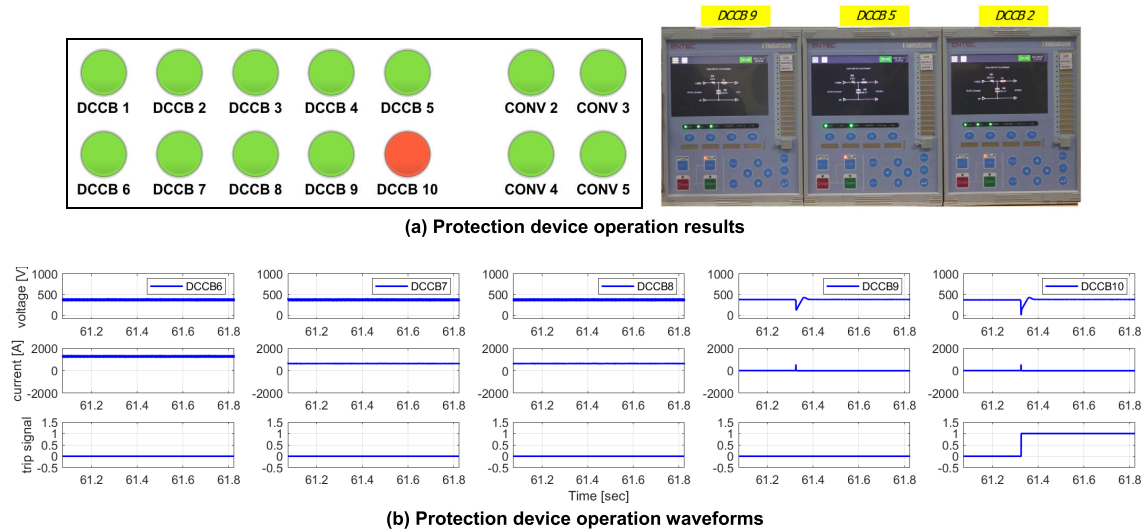
(a) Protection device operation results

(b) Protection device operation waveforms

FIGURE 19. Test results of fault case⑥ for PZ5.

TABLE 6. Quantitative performance comparison of the proposed method with previous studies.

Methods		Ref. [7]			Ref. [10]			Proposed method		
Load points		L1	L2	L3	L1	L2	L3	L1	L2	L3
Number of interruptions for each load point	Temporary	2.2367	2.2367	1.0800	2.2367	2.2367	1.0800	0	0	0
	Permanent	0.6767	0.6767	1.8333	0.6767	0.6767	1.8333	0.7867	0.7867	1.8467
	Summary	2.9133	2.9133	2.9133	2.9133	2.9133	2.9133	0.7867	0.7867	1.8467
Interruption duration (min)		22.5	22.5	56.1	20.5	20.5	55.1	23.6	23.6	55.4
Reliability index	SAIFI	2.91			2.91			1.14		
	SAIDI (min)	33.7			32.1			34.2		

sections were assumed to be directly proportional to their length. To calculate the power outage time, a permanent fault duration of 30 min was assumed, resulting from the operation of a protective device or a switch. In addition, in the methods of Tang and Ooi and the method of Monadi et al., the assumed durations of instantaneous faults were 1 and 0.1 min, respectively. These durations are determined by restarting the sources and reclosing the switches, taking into account whether communication is used or not. Table 6 presents the results of failure simulations in all line sections for each load shown in Figure 9(b).

Table 6 indicates that the interruption duration does not show a significant difference among the proposed and existing methods. However, in the case of SAIFI, the frequency index of interruptions, the proposed method has a reduction effect of more than 50% compared to the existing methods. This is because the proposed method selectively isolates the faulted section through cooperation between protection devices, whereas the existing methods cause momentary power interruptions to the load by shutting down the entire power source. According to Gates et al. [28], the outage cost is not directly proportional to the duration. Additionally, there is no significant difference between a few seconds and tens of minutes of outages. Therefore, reducing the number of

short-term power outages can significantly improve the reliability of the power supply for consumers. This improvement makes the contribution of the proposed method to the actual system operation valuable.

V. CONCLUSION

In this study, we propose a system for protection and protection coordination in radial LVDC distribution systems based on FCL. The proposed protection system uses a buck-type FCL circuit at the rectifier terminal and a phase-shift DAB converter for FCL, while protection coordination is achieved through isolation of PZs. Moreover, we present an engineering procedure for calibrating the protection system, such that the system can easily be applied to any LVDC system. The conclusions obtained from this study can be summarized as follows:

1. The PZs are defined according to the converter and DCCBs by utilizing the characteristics of fault impact isolation between the primary and secondary sides of the DAB converter during a fault. In addition, to minimize the fault zone, a relaying method is proposed for the PDs to enable protection coordination between PZs. A major advantage of the defined PZs is that they can be applied to an LVDC network with arbitrary branch circuits using the same rules.

2. A method is presented to distinguish the arbitrary PDs constituting each PZ as bus circuit breakers, load circuit breakers, and branch circuit breakers according to their position within the PZ. Furthermore, by allowing the system operators to set predetermined relay methods and operating criteria for each type, they can easily calibrate the PDs for new systems or when the system topology changes.

3. By using directional overcurrent and undervoltage relay elements that can be determined by individual PDs themselves without relying on communication signals, the design is simplified, and the economic issues faced by previous studies can be improved. Thus, the proposed solution is highly practical for protecting LVDC systems built for small-scale consumers.

4. The FCL characteristics of the system increase the withstand time during faults in rectifiers/converters. This enables the use of conventional DCCBs for protection coordination instead of the expensive, high-speed semiconductor-type DCCBs used in previous studies.

Finally, we conducted various simulations using MATLAB/Simulink and verified the developed protection coordination scheme through HILS tests based on Opal-RT. Through this process, the accuracy and practical applicability of the proposed method were confirmed. In addition, the verification process confirmed that compared to the existing studies, the proposed method remarkably reduced the frequency of outages while maintaining a load outage duration at a similar level. Accordingly, it was confirmed that high reliability level could be maintained despite lower infrastructure investment compared to existing methods. This can be a very important strength in actual LVDC operation.

In the case of LVDC distribution systems built for small- and medium-scale consumers, it is possible to predict a somewhat standardized system topology (similarly to LVAC systems). They commonly use a multi-branch form, including rectifiers for converting AC power supply from utilities into DC and converters for connecting loads and DC power, such as energy-storage devices and distributed generation. Therefore, the protection system proposed herein has the advantage of being immediately applicable to most LVDC systems. However, because fault characteristics are constantly changing owing to improvements in power-conversion devices, the proposed protection method also requires continuous improvements. Moreover, the most important factor in designing protection coordination for DC distribution systems is the system topology structure. Nevertheless, excluding the architectural aspects of buildings, the power system structure is generally considered a separate design domain. Accordingly, it should generally be feasible to design and construct a topology suitable for applying the proposed protection system.

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JIN-SU KIM (Member, IEEE) received the B.S. degree in electrical engineering and the M.S. and Ph.D. degrees in power systems from Soongsil University, Seoul, South Korea, in 2011, 2013, and 2021, respectively. Since 2013, he has been a Researcher of the industrial applications for energy storage system (ESS) and smart grid. He has collaborated intelligent LVDC system development as a Postdoctoral Researcher with Chonnam University, Gwangju, South Korea, from 2021 to 2022. He is currently developing the next generation energy management system (EMS) as a Senior Research Engineer with LS Electric, Anyang, South Korea. His research interest includes advanced grid management systems for future smart grids.

EUN-CHUL LEE received the B.S. and M.S. degrees in electronics and information engineering from Kunsan National University, Kunsan, South Korea, in 2006, and the Ph.D. degree in electronics system engineering from Hanyang University, Seoul, South Korea, in 2019. From 2006 to 2016, he was a Section Chief with the Renewable Energy Laboratory, Research and Development Center, WILLINGS, Yongin, South Korea. He is currently the Director of the Research and Development Department, EKOS Company Ltd., Gwangju, Gyeonggi-do, South Korea. His research interest includes the design of power electronics.

SANG-YUN YUN (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Soongsil University, Seoul, South Korea, in 1996, 1998, and 2002, respectively. From 2002 to 2009, he was a Senior Researcher with the Electrotechnology Research and Development Center, LSIS, Cheongju, South Korea. From 2009 to 2016, he was a Senior Researcher with the KEPCO Research Institute, Daejeon, South Korea. He is currently a Professor with the Department of Electrical Engineering, Chonnam National University, Gwangju, South Korea. His research interests include the design of EMS, DMS and MGMS, and protection technologies for active distribution networks.

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