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RESEARCH ARTICLE

A 10 Gb/s Line Driver in 65 nm CMOS Technology for Radiation-Pervaded and High-Temperature Applications

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ABSTRACT Links able to sustain high-speed data transfer while exposed to radiation phenomena are required by several applications, including aerospace and high-energy physics experiments. To satisfy this need, this paper outlines the design of a radiation-hard line driver for communication up to 10 Gb/s. The driver design is focused on the techniques adopted to increase its radiation hardness, namely the use of long-channel transistors, the avoidance of p-type MOSFETs and thick oxide devices. Circuital strategies to boost driver speed, such as inductive peaking, buffer chaining, and optimal layout placement and routing, are discussed and implemented to compensate for the downsides caused by adopted radiation-hard techniques. The driver, fabricated in 65 nm technology, has been experimentally tested demonstrating its ability to operate up to 10 Gb/s in a radiation-pervaded environment. In particular, after exposure to 1 Grad(SiO_2) X-ray, the line driver exhibits an output signal amplitude reduction of 18.3% and a jitter increase of 5.53%. Performed temperature tests highlight that the line driver is capable to operate at 125 °C with 15.9% and 6.7% output signal swing reduction and jitter increase, respectively. The temperature tests also demonstrate the driver's ability to work up to 160 °C with an output signal swing reduction below 25% and a jitter increase below 12%.

INDEX TERMS Aerospace, high energy physics, high speed, high temperature, integrated circuit, line driver, radiation hardening by design, total ionization dose.

I. INTRODUCTION

Several applications pose challenges to the use of CMOS technology in harsh conditions such as high radiation levels and high-temperature environments. The introduction of all-electric propulsion spacecrafts has made the radiation tolerance requirements for geosynchronous satellites even more severe. Indeed, all-electric propulsion spacecrafts having low weight enable savings on launch costs, but it takes them 200 to 400 days to cross the heart of the Van Allen radiation belts. This slow ascension results in an increase in the level of radiation dose cumulated on onboard electronics [1], [2]. Looking farther into space exploration, the Europa satellite requires electronics that can withstand cumulative dose levels of 5 Mrad in 2 weeks, with 2.54 mm of aluminum shielding [3]. Naturally, the greater the radiation hardness of the onboard electronics, the thinner the shielding could be to save on launch costs.

Besides the challenges posed by space applications, high-energy physics experiments demand electronic equipment with high levels of radiation tolerance as a key point for reliable results. As an example, in the current setup of the Large Hadron Collider, electronic integrated circuits fabricated in commercial silicon technologies are qualified for hundreds of

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Mrad [4]. According to the current CERN schedule, the more powerful Future Circular Collider (FCC) will start operating by 2035 with a forecasted electronics radiation hardness of about 1 Grad(SiO_2) [5].

Both space and HEP applications necessitate high-speed communication links. Current trends in satellite design indicate a substantial growth in onboard data traffic and digital processing. The throughput of next-generation satellites for digital telecom applications, as well as for scientific missions, surveillance, and remote sensing, will exceed terabits per second of data that must be processed on board. For instance, high-resolution cameras and synthetic aperture radars need high-speed communications between the instruments and the onboard data storage system [6]. The particle tracking inside the FCC will rely on thousands of sensors placed around the beam collision point, requiring parallel links with several Gb/s speeds to collect information data from the inner tracker [5].

In this paper, the design and experimental verification of a full-custom line driver able to sustain a high-speed communication link in a radiation-pervaded environment is presented. In particular, a summary of the main radiation effects on silicon devices is presented in Section II with a focus on advanced CMOS technology. In the same section, the main design techniques employed in the line driver design to counteract the effects of radiation are also discussed.

The driver architecture is discussed in Section III with a thorough description of the design of each stage. Section IV concerns the layout design phase with the description of the solutions adopted to design the driver for a **r**adiation-pervaded environment. Section V describes the simulation results of the proposed line driver for different corners. In Section V, the results obtained by the experimental test of the fabricated driver are reported and analyzed. In particular, results for both standard and radiation environment tests are discussed. Section V deals with the analysis of the state-of-the-art line drivers and their performance compared with the proposed device. Conclusions are drawn in Section VI.

II. TID EFFECTS ON INTEGRATED DEVICES

Radiation effects on silicon devices can be either sudden or cumulative. The former produces a temporary system disturbance usually denoted as single event effect (SEE), which is caused by high-energy particle collisions with the silicon chip. The latter, on the other hand, degrades system performance over time, such as total ionizing dose (TID) accumulation in device insulators.

Considering the nature of the proposed driver device, which lacks memory cells that could be corrupted by SEE events, this paper focuses on the cumulated dose effects [7], [8], [9], [10].

A. TID EFFECTS ON CMOS TECHNOLOGIES

Due to radiation, electron ionization can occur in insulating layers, leading to charge accumulation, and resulting in unintended local fields. In MOSFET transistors, after electron-hole pairs generations in oxide, they are separated by the electric field rapidly drifting toward the gate and the Si/SiO_2 interface. As the holes approach this interface (a few nm away from it), some fraction of them will be trapped, leading to positive oxide-trapped charge accumulation. In addition, another effect of ionizing radiation in MOSFET devices is the formation of trap states at the interface, which can capture charge carriers [11], [12]. The amount of trapped charge and its effects are typically proportional to the square of the oxide thickness. For thickness oxide below 10 nm, there is an even greater benefit thanks to the hole annealing through tunneling. Therefore, the use of advanced technologies with thin gate oxide is expected to improve device and circuit performance in terms of radiation hardness [13]. However, on closer inspection, other thick oxide layers near the MOSFET devices may affect their behavior [14]. Indeed, charge buildup can occur in gate spacers for the creation of lightly doped drain (LDD) regions and in the shallow trench isolation (STI) oxide used for device separation. Being the LDD and STI located near the channel, the electrical fields generated by the charge trapped in these thick oxide structures have a direct effect on the carriers in the channel.

Considering the 65 nm CMOS technology targeted in this work, a severe impact is expected in N- and P-type diode-connected MOSFETS when exposed to high radiation levels [15], [16]. In particular, the on-current loss in minimum length devices reaches 52% and 98% for N and P devices, respectively, when exposed to 1 Grad(SiO_2).

This current decrease is mainly due to the shift of the threshold voltage and the reduction of carrier mobility. Since transistor threshold voltage is defined as the minimum gate-source voltage required to create the channel, its value is particularly impacted by the parasitic charge generated by ionizing radiation in the gate-oxide, oxide interface, gate-spacers, and STI.

Charge nature is what distinguishes the performance of N- and P-type devices. Indeed, for P-MOSFETs all trapped charges are positive, hindering the channel creation (threshold voltage increases in the module). For N-MOSFETs, all charges are positive except those trapped on the interface, providing a partial compensation on the threshold voltage variation (to be noted that positive charge leads to threshold voltage decrement for N-MOSFETs). Concerning the carrier mobility inside the MOSFET, it is mainly reduced by the traps generated in the channel near the Si/SiO_2 interface and by the increase of LDD resistance. Indeed, the charge buildup in the gate spacers and at their interfaces can modify the effective doping of LDD increasing the channel series resistance [16].

B. TID RHBD TECHNIQUES

Considering all these effects, some radiation hardening by design (RHBD) techniques have to be adopted to extend the operability of MOSFET devices in environments pervaded by radiation [12], [17].

In the proposed driver, presented in Section III, three main RHBD solutions are adopted to improve its radiation hardness.

The first solution, which also guides the selection of the driver architecture, is to avoid employing P-MOSFET devices. This approach is derived from the noticeable performance reduction of these devices when exposed to high-level radiation, as discussed in the previous section.

Note that this solution was not dictated by the limit to the selected technology to achieve 10 Gb/s. In fact, 65 nm CMOS drivers operating over 10 Gb/s in standard conditions are already presented in the literature [18].

The second solution adopted relies on the use of long-channel devices. This choice allows us to physically separate the gate spacer from the channel center, thus making the effect of the spacer accumulated charge on the channel less significant. On the one hand, this approach improves the device radiation hardness but, on the other hand, it lowers the MOSFET cutoff frequency, thus reducing the circuit speed. As a result, for the high-speed driver design, a tradeoff between radiation hardness and speed performance is achieved by selecting a minimum transistor length equal to 120 nm. This value corresponds to twice the minimum length available in the selected technology (minimum length equal to 60 nm).

The third solution is based on the engineering of the MOSFET layout. It consists of designing the transistor gate as a closed shape to obtain the so-called enclosed layout transistors (ELTs) [19], [20], [21], [22]. This layout solution has the advantage to remove the interface between the transistor gate and the STI, limiting the impact on the device channel of charge generated in STI structures due to the radiation.

III. DRIVER ARCHITECTURE

A. DRIVER ARCHITECTURE

The line driver is designed to feed 50 Ω transmission lines with a 100 Ω differential termination. It is composed of three stages: an output stage, two predriver stages, and an input stage. As stated in the previous section, the achievement of both high-speed and high-radiation hardness characteristics is strongly limited if P-MOSFET devices are used. For this reason, the proposed high-speed driver is based on Current Mode Logic (CML). It enables high-speed applications to operate in this harsh environment thanks to the use of only N-MOSFETs and passive devices.

The core supply voltage of the targeted technology is 1.2 V, which is suitable for low-power digital systems. However, a higher supply voltage for the input-output stages is more appropriate for achieving a higher signal-to-noise ratio in harsh environments. Indeed, having differential output signals with wide swings helps address the issues relevant to the considered harsh environment (e.g., radiation and temperature as shown in Sections V.B and V.C), and improve the reliability of high-speed communication links operating in this environment. Considering these requirements, two different supply voltages are adopted for the driver: VDD-L equal to 1.4 V for the input and predriver stages, and VDD-H equal to 2.4 V for the output stage, as shown in Fig. 1.

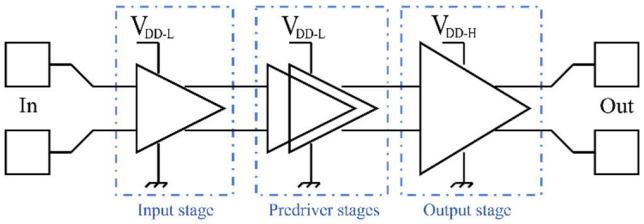

FIGURE 1. Driver architecture. From the left to the right: input pads, input stage, predriver stages, output stage, and output pads.

A multi-stage architecture composed of three main blocks is adopted for the driver to face the speed and voltage requirements. Below, the description of every single stage is reported following the natural design process, from the output toward the input stage.

B. OUTPUT STAGE

Considering the adoption of a 2.4 V supply voltage, a differential cascode architecture is implemented in the last stage, as illustrated in Fig. 2.

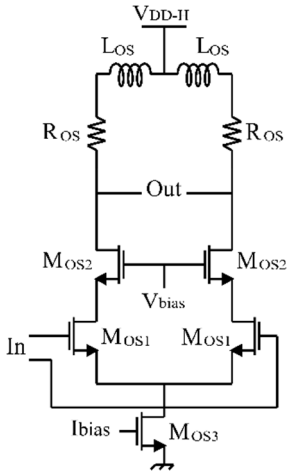

FIGURE 2. Output stage schematic.

Indeed, different from typical applications where high-voltage MOSFETs could be adopted for wide voltage range management [23], [24], [25], the high level of radiation that the driver should sustain makes this approach not worth considering. Indeed, being these devices fabricated with thick gate oxide, they exhibit low radiation hardness. In addition, the cascode architecture, by minimizing Miller's effect on the output capacitance, allows for a reduction in the stage's input capacitance. An internal termination of 50 Ω connected to the power supply is inserted to accomplish load matching across the entire frequency range. Considering this choice and the targeted 1 V_{p-p} differential output voltage swing, the stage is designed for a tail current of about 28 mA. To sustain this current level wide MOSFETs are employed, i.e., 84 μm

(8.4 μm × 10 fingers) wide devices for the common source couple, and 168 μm (8.4 μm × 20 fingers) wide for the common gate ones.

Additionally, a shunt peaking technique is introduced in the output stage to counteract the detrimental impact of large load capacitance of the electro-static discharge protections on the bandwidth. This technique, thanks to the use of an inductor connected in series with the pull-up resistor, allows for the extension of the output stage bandwidth. Particularly, the inductor acting as a high impedance for high frequency directs the output signal toward the output port instead of the power supply.

In terms of the zero-poles approach, the inductor generates a zero and a couple of conjugated poles changing the frequency response from

$$\mathrm{H}(\omega) \approx -\frac{\mathrm{g_m R}}{1+\mathrm{j}\omega\mathrm{RC}} \tag{1}$$

to

$$H(\omega) \approx -g_m R \frac{\left(1+j\omega\frac{L}{R}\right)}{1+j\omega RC+\omega^2 LC} \tag{2}$$

In (1) and (2), g_m is the transconductance of the differential MOSFET, L is the value of the inserted inductor, and R and C are the resistance and capacitance viewed at the output node. This solution enables a 4-5 times bandwidth extension that is paid with a wider layout area [26], [27]. The common value for the inductor that enables the bandwidth extension while providing the maximally flat gain is $L = R^2C/0.4$. However, in the proposed driver a greater inductor value is used to compensate for the bandwidth loss caused by connection parasitics. After the first sizing of the proposed line driver, post-layout simulations are performed to properly define the required inductor values.

For system bandwidth enhancement, other broadband techniques such as series peaking, T-coil peaking, and transformer peaking could be applied. However, compared with the adopted shunt peaking, the series peaking techniques result in a lower bandwidth extension. Instead, although the use of T-coils and transformers could generate a wider increase in bandwidth than the adopted solution, they need nearly twice as much area [28].

Fig. 3 depicts the image of the integrated inductor for the shunt peaking technique. The inductor structure is composed of a differential inductor with a central tap to minimize the layout area. In this configuration, both the inductors of the CML stage branches (L_{os} in Fig. 2) are interleaved in a concentric octagonal shape sharing the electromagnetic flux. High metal layers are employed in the inductor design because they have a lower resistivity due to their greater thickness compared to lower metal levels.

Squares of lower-level metals are placed in the empty area under the inductor for planarity purposes. In Fig. 4 the inductor value and its quality factor as a function of the frequency are shown. The inductance is about constant up to 10 GHz achieving a high-quality factor of 14.8 at 12.8 GHz.

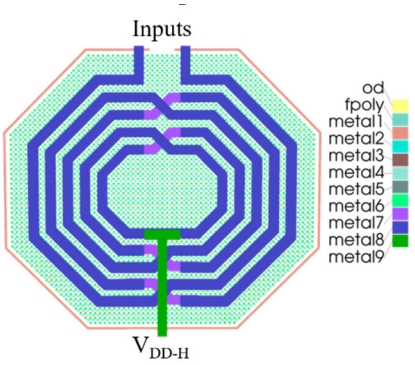

FIGURE 3. Image of the symmetrical inductor with a center tap used in the driver output stage.

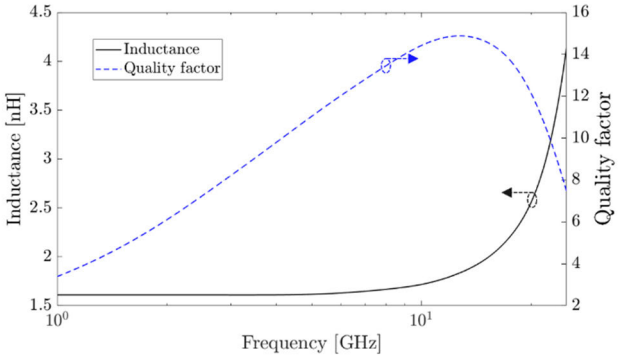

FIGURE 4. The inductance and quality factor of the inductor that are shown in Fig. 3. Data are extracted by electromagnetic simulations.

Differently from classical RF applications, for the shunt peaking technique adopted in the proposed line driver, the main inductor parameter is having the inductor value constant throughout a broad frequency range. Instead, a high-quality factor is not essential since the inductor is connected in series with the CML pull-up resistance. Hence, the inductor series resistance could be compensated by reducing the pull-up resistance accordingly.

C. PREDRIVER STAGES

As a consequence of the output stage sizing, the previous stage is loaded with a 356 fF capacitor making it difficult to achieve the target speed. Therefore, a two-stage CML tapered chain is used to properly drive the output stage. It is designed considering a tapered factor of two, scaling the MOSFETs, pull-up resistors, and tail current consequently. A logic swing value of about 600 mV with a common mode of 0.9 V is chosen for the buffer stages of the pre-driver to guarantee the complete swing of the differential couple.

The second predriver stage is sized for a tail current of 14 mA, a differential couple width of 48 μm, and a pull-up resistor of 45 Ω. Consequently, the first stage is sized with a tail current of 7 mA, a differential couple width of 24 μm (6 μm × 4 fingers), and a 90 Ω pull-up resistor.

To extend the driver bandwidth, a shunt inductive peaking technique is employed in both stages using 1.4 nH inductors similar to those used in the output stage. The schematic view of the predriver is shown in Fig. 5.

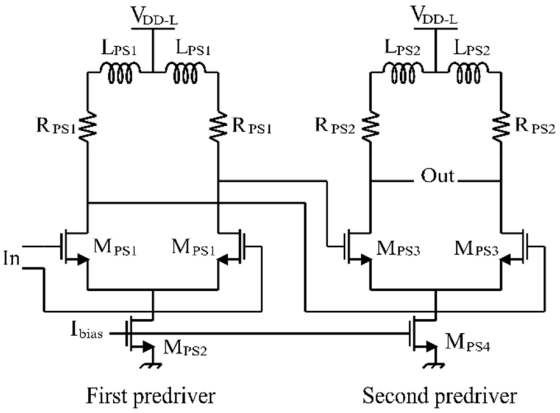

FIGURE 5. Schematic of the predriver stages.

D. INPUT STAGE

An additional stage is introduced at the driver input to fulfill three tasks: further reducing the input capacitance, adjusting the common mode level of the input signals, and creating a differential 100 Ω termination for the input signals. Since the driver is assumed to be coupled with AC signals, the common mode of the input signal is generated inside the chip with a partition of the supply voltage in the first stage. This allows the constraints of the available test instruments to be released from those of the driver. This enables testing of the driver using equipment without common mode control.

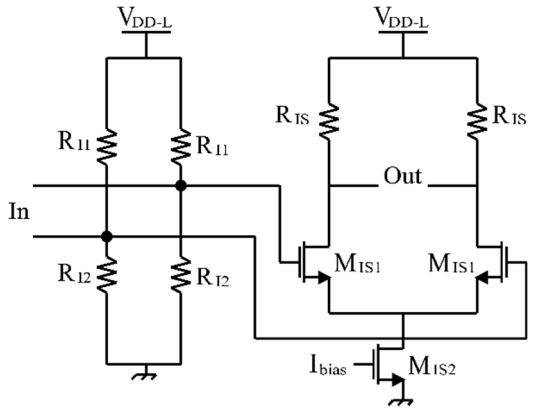

FIGURE 6. Input stage schematic.

The input stage is sized with a tail current equal to 5 mA, a differential couple width of 15 μm (2.1 μm × 4 fingers), and 120 Ω pull-up resistors. The Input stage schematic is depicted in Fig. 6.

IV. DRIVER LAYOUT

The layout of the driver is based on a full custom approach. It is meant to fit in a 1 mm × 1 mm chip with the driver outputs on the opposite side than the input signals. The layout of every single device adopts techniques aimed at mitigating the radiation and high-temperature effects. The layout of all MOSFETs and resistors is realized with an interdigitated structure for matching purposes, which also allows us to reduce the effects of TID. Indeed, this structure allows having a uniform TID charge on the devices, which helps to increase the TID radiation hardness thanks to the adopted differential architecture.

One of the main challenges in the layout phase is related to the metal electromigration that limits the minimum metal widths and via numbers. This effect is particularly relevant when operating at high temperatures. Indeed, according to technology data, the maximum current density in metal paths and vias should be reduced by a factor of 8.8 when passing from 85 °C to 125 °C to avoid electromigration phenomena [29].

At first glance, designing very wide metal tracks to connect the single driver devices appears to be the solution to the electromigration problem when running at high temperatures. However, the wider the path, the greater the parasitic capacitance of the connection, which reduces the driver's speed. In the driver's layout design, two solutions are adopted to overcome this issue. The first solution, particularly adopted for short connections, is the routing of the signals on parallel stacked metals. This solution satisfies the electromigration rules with a limited increase of the parasitic capacitance. Indeed, the upper and lower capacitances of the metal remain unchanged and only the lateral capacitance increases with a limited impact on the total capacitance.

The second solution is the use of the thicker top metals available in the technology (metals six, seven, and eight) to route the signal between adjacent stages. Since these metals are thicker than bottom metals, they have a higher current density limit preserving the same parasitic capacitance. A drawback of this solution is that the signals should pass through several vias to reach the top metals, and each via has its parasitic resistance and capacitance that degrade signal quality.

In order to ensure substrate ground potential and drain out parasitic charge generated by TID, all the free layout space is filled with a grid of substrate contacts connected to the GND pads.

Fig. 7 shows the layout of the driver, whose area is dominated by the inductors and by metal paths used for signals and power routing. The whole area is about 0.181 mm^2 and is constrained by the placement of the pads; a layout optimization could be performed for area reduction.

Fig. 8 depicts the picture of the 1 mm x 1 mm chip fabricated in commercial 65 nm technology. The driver is located on the right-hand side with input pads at the top, and output pads at the bottom, whereas supply voltages and biases are connected to the pads on the right.

V. DRIVER POST-LAYOUT SIMULATIONS

In this section, the driver post-layout simulation results are described. These simulations are performed after the

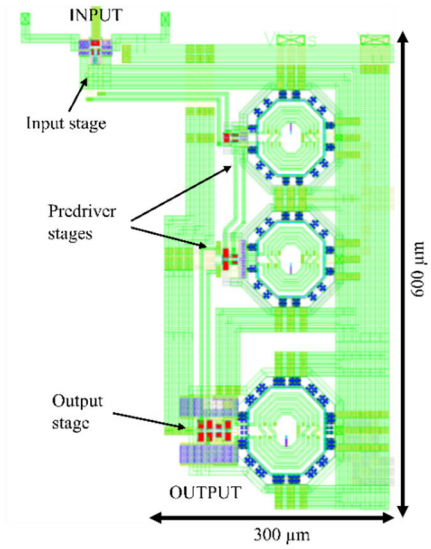

FIGURE 7. Image of the whole driver layout.

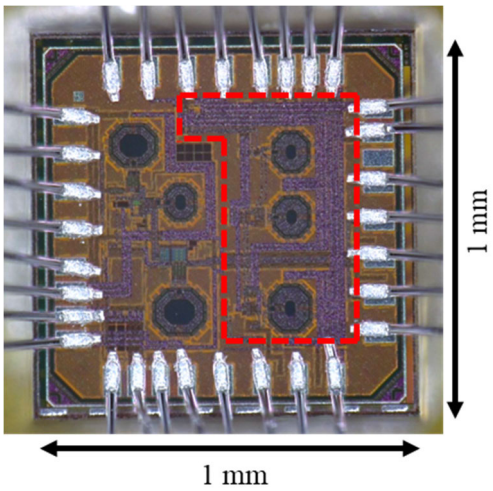

FIGURE 8. Microphotograph of the 1 mm^2 chip fabricated in 65 nm CMOS technology.

extraction of parasitic elements of the interconnections. Several simulations were performed considering different technology processes, supply voltages, and temperature (PVT). In particular, for the process variations, typical-typical (TT), fast-fast (FF), and slow-slow (SS) corners are used. For the supply voltage, a variation of ±10% from the nominal voltage values is considered. With regard to temperature, models of the devices of the used technology were characterized for a temperature ranging between −40 °C and 125 °C, hence this whole range was used for the proposed line driver characterization.

In order to simplify the data visualization, only the most extreme PVT parameter combinations are shown in this paper. In particular, the ''typical'' case is obtained with TT process, temperature of 27 °C, and nominal supply voltages. The ''slow'' case is represented by SS process, temperature of 125 °C, and −10% variation of the supply voltages. The ''fast'' case is obtained with FF process, temperature of −40 °C, and +10% Variation Of Both Supply Voltages.

Fig. 9 shows the simulation results of the eye diagrams of the output signals for the three different corners: typical, slow, and fast. As expected, it is possible to observe that the eye diagram of the slow case is closer than the others. This is due to the longer rise and fall times of the output signals and to the eye amplitude reduction. In contrast, the fast case has the widest open eye diagram. However, for all corners, the post-layout simulations show the driver ability to operate at 10 Gb/s with an eye-diagram amplitude greater than 1 V.

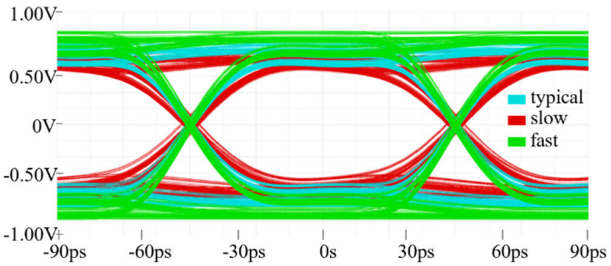

FIGURE 9. Eye diagrams of the line driver output signals for three limits cases: typical (TT process, 27 °C, and nominal supply voltages); slow (SS process, 125 °C, and −10% variation on the supply voltages); fast (FF process, −40 °C, and +10% variation on the supply voltages).

Considering that the line driver should be driven by other devices able to generate high-speed serial data, such as SerDes devices, the post-layout simulation results of the output signal amplitude as a function of the amplitude of the input signals are reported in Fig. 10. The figure shows that to achieve an output voltage greater than 1 V in all three corners, the input voltage should be greater than 0.3 V.

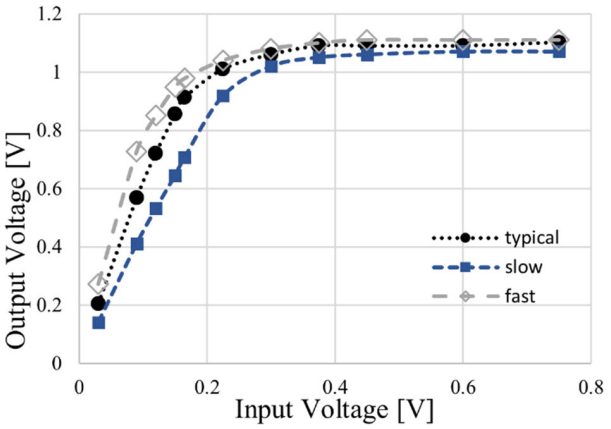

FIGURE 10. Simulation results of the eye amplitude of the output voltage signals as a function of the input voltage for the three considered corners.

VI. DRIVER MEASUREMENTS

The experimental characterization of the driver is performed by gluing the chip directly on a test board and by wire

bonding the chip pads to the board traces. A four-layer board, shown in Fig. 11, has been designed and equipped with commercial off-the-shelf (COTS) components dedicated to the generation of supply voltages and bias current. A free space area of 2×2 cm^2 is kept around the chip to confine the radiation test to the targeted chip preventing radiation impacts on COTS devices. High-speed traces that connect the driver's input and output pads with the SMA connectors are properly designed on a Rogers4003C substrate to present 50 Ω transmission line characteristic impedance up to 15 GHz.

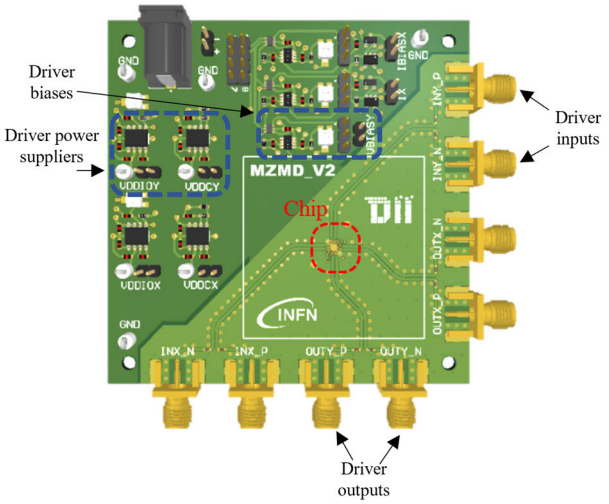

FIGURE 11. Image of the testing board with the chip directly bonded on it.

A. ELECTRICAL MEASUREMENTS

Nominally, the driver should be inserted in a data transmission chain integrated into a single IC and composed of a module for data processing, a data serializer, and then the designed line driver [30]. Therefore, the input data for the driver should be generated inside the same chip. However, considering the importance of the test of the single data transmission blocks, for the test of the driver the data are provided by an external generator. In particular, a pseudo-random binary sequence generator (PRBS) was implemented on a Kintex Ultrascale FPGA and used to feed the driver. The output data of the driver are then acquired by a 23 GHz 100 GS/s Tektronix oscilloscope with an internal 50 Ω termination and analyzed.

Fig. 12 shows the comparison between the eye diagram of the signal generated by the FPGA used to feed the driver and the eye diagram of the driver output signal at 10 Gb/s.

The two measured eye diagrams show differences in terms of shape and amplitude; indeed, the driver output shows a more rounded shape with an amplitude that is twice that of the FPGA output.

A frequency-domain characterization is also carried out by feeding the driver with the PRBS-31 signals at different bit rates. Compared to classical frequency characterization using Vector Network Analyzer (VNA), this solution yields more accurate transmission results. Indeed, although VNA measurements are less time-consuming, they feed the system with a single tone swept across the frequency range, thus not considering the intermodulation issue.

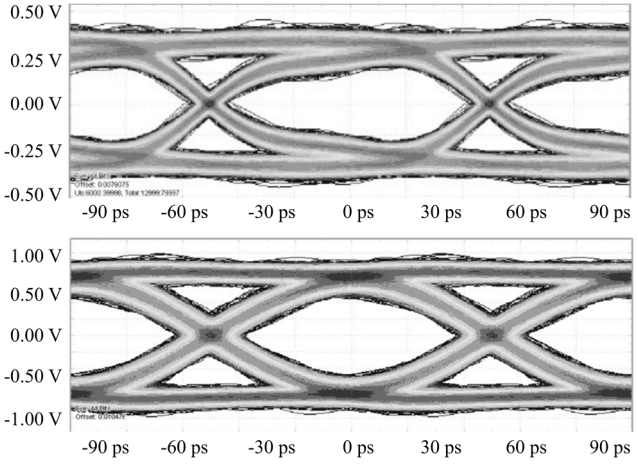

FIGURE 12. Eye diagram images for 10 Gb/s data rate for the signal at the FPGA output (top) and the driver output (bottom).

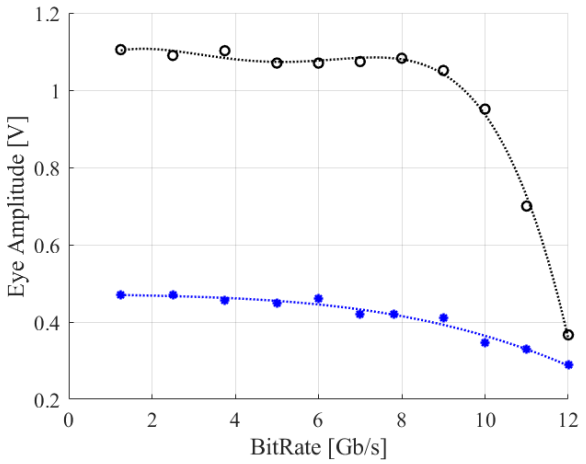

FIGURE 13. Eye amplitude of the driver output signals (in black) and of the driver input signals (in blue) as a function of the bit rate.

Fig. 13 shows the comparison between the eye diagram amplitude of the FPGA and driver output signals as a function of the bit rate values, from 1.25 Gb/s to 12 Gb/s. Considering a 3 dB bandwidth definition, a driver bandwidth limit of 10 Gb/s can be considered. To be noted that the results depicted in Fig. 13 are not de-embedded from the frequency limiters, such as testing boards, connectors, and cables. In addition, the FPGA output signals used for the driver feeding present a bandwidth limitation near 10 Gb/s.

B. RADIATION HARDNESS MEASUREMENTS

The driver radiation hardness is evaluated by exposing the test chip to X-rays at room temperature. The TID measurement is performed using the X-ray Seifert RP149 machine at the

X-ray facility at CERN. A high dose rate of about 8.2 Mrad/h is used for the test to reduce the testing time and the valuable machine uptime. Since the charge build-up in the oxide layers does not have enough time to recombine through annealing processes, this TID test is more conservative than the real case where the targeted dose is achieved in several years. The test is conducted with the same setup described in Section V.A.

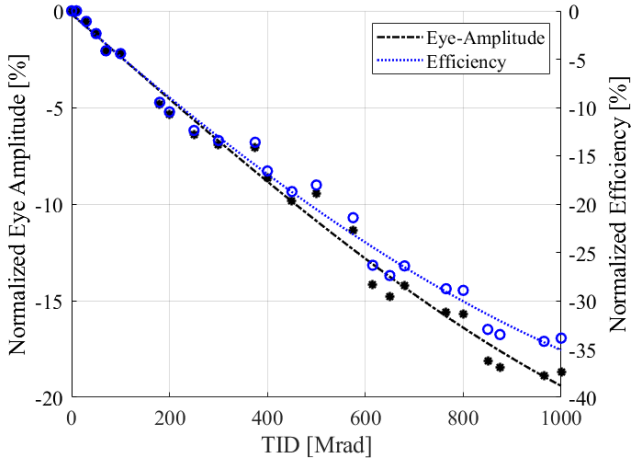

FIGURE 14. Eye amplitude variation (black) and efficiency variation (blue) as a function of TID at room temperature.

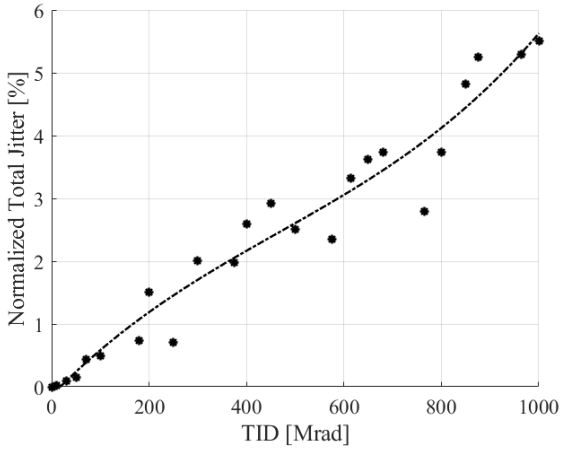

FIGURE 15. Total Jitter variation of the driver output as a function on TID at room temperature.

The driver is fed with a PRBS pattern signal while it is exposed to X-rays. The driver output signals are acquired by the oscilloscope and read out at different dose levels. In Fig. 14, the eye amplitude reduction as a function of TID from 0 to 1 Grad(SiO_2) is plotted. In particular, an amplitude reduction of about 18.3% is shown at 1 Grad(SiO_2). It is worth noting that without the adoption of the radiation hardness techniques shown in Section II, an eye amplitude reduction of about 80% would be expected [14]. In addition, in the same figure, the line driver efficiency variation as a function of TID is plotted. It is calculated as the ratio between the power delivered to the load and the line driver power consumption.

The total jitter measurement results are reported in Fig. 15 as a function of TID from 0 to 1 Grad(SiO_2). It shows an increase of only 5.53% when the driver is exposed to 1 Grad(SiO_2).

C. THERMAL MEASUREMENTS

Considering the stringent temperature requirements of space missions and the problems associated with silicon devices operating at high temperatures, such as the metals electromigration addressed in the layout phase in Section IV, studies of the driver exposed to different temperatures are performed. Concerning the driver behaviour at low temperatures, down to −40 °C, simulations confirm that no performance degradation is expected compared to room temperature. Furthermore, the electromigration problem is significantly reduced at low temperatures. Therefore, experimental measurements of the driver exposed to high temperatures are performed. For these measurements, to minimize the problems related to the exposition of COTS devices hosted on the testing board to high temperatures, a localized constant flux of hot air is used to heat the driver chip. The air temperature was controlled by an automatic system thanks to the use of a thermocouple sensor glued on the board as close to the driver chip as feasible and in the same small hot chamber. During the test, the driver was fed with PRBS signals and its outputs were acquired by the oscilloscope.

In Fig. 16, the output signal eye amplitude is reported as a function of the temperature from 25 °C up to 160 °C. Considering that the standard temperature for electronics in space missions is up to 125 °C, the output signal eye amplitude is reduced by 15.9% at that temperature.

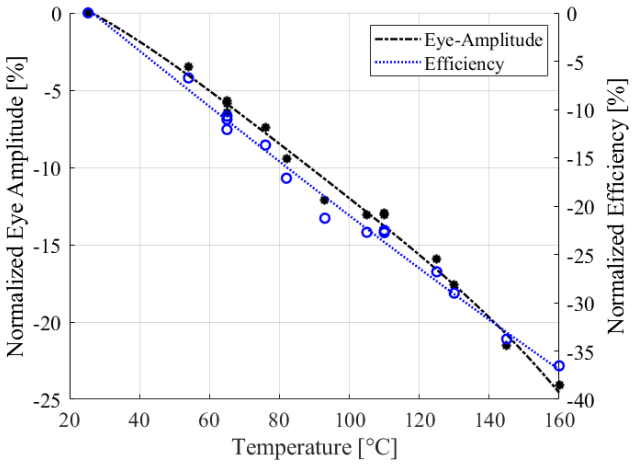

FIGURE 16. Eye amplitude variation (black) and efficiency variation (blue) as a function of temperature.

However, the driver continues to work for higher temperatures with a quasi-linear decrement of the eye amplitude. Indeed, an eye amplitude reduction of 24.3% is measured

TABLE 1. State-of-the-art comparison.

	[31]	[32]	[33]*	[34]	[35]	[36]+	[18]	[37]	[38]	This work
Technology	Commercial SOI	Commercial SOI	180 nm	180 nm	180 nm	65 nm	65 nm	28 nm	28 nm	65 nm
Bit rate	400 Mb/s	400 Mb/s	1 Gb/s	1.2 Gb/s	3.2 Gb/s	2.56 Gb/s	12.5 Gb/s	1 Gb/s	12.5 Gb/s	10 Gb/s
Maximum Temperature	125 °C	85 °C	125 °C	-	-	125 °C	-	-	-	160 °C
Electrical output swing	800 mV	900 mV	3.3 V	900 mV	500 mV	200 mV	400 mV	450 mV	135 mV - 703 mV	1.15 V
Area	-	-	3.15* mm^2	-	1.8 mm^2	Schematic	0.24 mm^2	0.0085 mm^2	0.0196 mm^2	0.18 mm^2
Power Consumption	75.9 mW	76 mW	105.6 mW	-	135 mW	0.5 mW	4.85 mW	7.56 mW	13.52 mW 21.49 mW	99.3 mW
TID tolerant	100 krad	100 krad	300 krad	1.68 Mrad	4.5 Mrad	500 Mrad	-	-	-	1 Grad

*Quad-driver: it is composed of four parallel drivers. +Only results of schematic simulations are reported.

at 160 °C. In addition, in the same figure, the line driver efficiency variation as a function of temperature is plotted.

Fig. 17 also shows the jitter increase as a function of the chip temperature from 25 °C up to 160 °C. A jitter increase of 6.7% and 11.9% are measured at 125 °C and 160 °C, respectively.

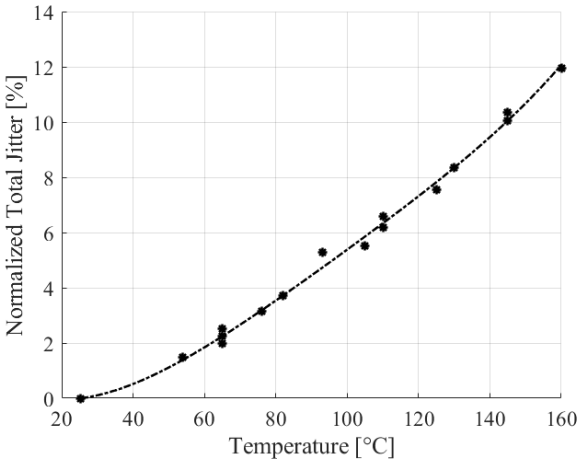

FIGURE 17. Total jitter variation as a function of the temperature.

VII. STATE-OF-THE-ART REVIEW

In this section, the line drivers found in the literature and market are compared with the driver proposed in this paper. As a result, in order to extend the comparison, designs on different technology nodes are considered, such as 180 nm, 65 nm, and 28 nm. In addition, for an exhaustive comparison also line drivers not designed for space applications are included. A summary of the compared line driver is reported in Table 1.

In [31], a commercial 400 Mb/s transmitter SPLVDS031, certified for radiation hard applications, is tested up to 100 krad, showing that the full performance is satisfied up to 56 krad. Over that level, the transmitter can be still used, but with some limitations. Another commercial transmitter with similar performance, the TF90LVDS031, is exposed to radiation in [32] showing a 12% performance degradation at 100 krad.

Compared to these two commercial solutions, the proposed line driver overperforms them with twenty-five times higher speed and four orders greater radiation hardness. Focusing the attention on research works, in [33] a 1 Gb/s quad-driver for LVDS communication is proposed. Each driver is based on three CMOS stages fabricated in 180 nm technology. The experimental tests show a radiation hardness of up to 300 krad. On the same technology node, in [34], a higher communication speed and radiation hardness are achieved, 1.2 Gb/s and 1.68 Mrad, respectively. Unfortunately, no area and power comparisons are possible for a lack of data. Instead, a comparison can be made with the 3.2 Gb/s driver reported in [35]. This driver, fabricated in the same 180 nm technology, is able to achieve a higher speed and radiation hardness than [33] and [34]. Indeed, the radiation tests with the chip exposure to X-ray show that the chip is able to operate up to 3.5 Mrad. On the other hand, the achievement of this result is paid for with greater power consumption.

Considering that the TID radiation hardness improves with the technology scaling, in [36] the simulation results of a driver in 65 nm are reported. The schematic simulations show a 2.56 Gb/s speed and an estimated radiation hardness of 500 Mrad.

The driver proposed in this work, which is realized with the same technology node, shows experimental evidence of a nearly four times faster link and twice the radiation hardness. However, this improvement is paid for with an increase in power consumption. Thanks to the use of flip-chip technology a speed of 12.5 Gb/s is achieved in 65 nm technology in [18]. It shows a reduced power thanks to the CMOS approach, a slightly wider area, but any data concerning the space environments, such as radiation and temperature are reported.

Concerning the technology scaling related to the line driver, [37] shows the design of a 1 Gb/s driver in 28 nm technology. It features a small area and power consumption but, since it is not designed for space applications, no radiation hardness data are reported.

In the same technology, increasing the area and power consumption, the line driver design in [38] is able to achieve 12.5 Gb/s. However, also in this case no radiation hardness data and temperature tests are reported.

A few drivers for optical communications capable of dealing with high radiation levels have been identified in the literature. Although optical communications support higher speed connections than electrical transmission lines, they require high voltage or high current to power electro-optic modulator devices.

Electro-optic drivers are designed to power small, non-terminated electro-optic modulators, such as vertical surface cavity lasers (VCSELs), Mach-Zehnder interferometers, and ring resonators, whose requirements differ from those of a 100 Ω differential transmission line. For these reasons, they are only briefly compared with the proposed driver.

A driver for VCSELs operating at up to 10 Gb/s is presented in [39]. It is designed to provide an output of up to 14 mA. However, its radiation hardness is limited to 100 Mrad. Higher radiation hardness of up to 600 Mrad was obtained in [40]. In which the VCSEL is supplied with 15 mA. Higher levels of radiation hardness can be achieved using ring resonators and Mach-Zehnder modulators [41]. These devices indeed have higher radiation hardness than VCSELs, but they are particularly sensitive to temperature variations, which makes their use prohibitive in high-temperature applications such as the one proposed in this paper [42]. In [21], 5 Gb/s current and voltage drivers are proposed for optical links. They are capable of supporting communications up to 800 Mrad, but no temperature data are given. A Mach Zehnder driver capable of supporting 10 Gb/s at 1 Grad is reported in [19]. It was designed in 65 nm technology with a power consumption of 114.8 mW, but no thermal measurements are reported.

VIII. CONCLUSION

In this paper, we presented the design and experimental characterization of a line driver able to operate up to 10 Gb/s in space environments. The great radiation level at which the new all-electric propulsion spacecraft are exposed during their raising poses challenges in the onboard electronics. Indeed, considering the significant impact that TID has on the performance of silicon devices, some RHBD techniques have been developed and applied to the design of the proposed driver. In particular, design methodologies such as the use of a scaled technology node, the adoption of long-channel transistors, the use of ELT devices, and the avoidance of p-type MOSFETs and thick oxide devices have all been adopted to improve the radiation tolerance of the line driver.

Considering the high-speed communication requirement, some broad-band circuit solutions have been implemented, e.g., inductive peaking, CML buffer chaining, and proper layout placement and routing. The driver has been fabricated in a 1 mm × 1 mm chip and experimentally tested to verify its electrical performance in standard and harsh conditions. In particular, the driver radiation and temperature hardness have been tested by exposing the device to X-rays and a localized hot air flux, respectively. The experimental measurements highlighted a line driver operating range up to 1 Grad(SiO_2) with an 18.3% output signal eye amplitude loss and a 5.53% jitter increase, emphasizing the effectiveness of the adopted RHBD techniques.

Concerning the behavior with temperature, the proposed driver exhibited an output signal amplitude loss of 15.9% and a jitter increase of 6.7% at 125 °C, which is a typical temperature space standard. However, the proposed device has been tested up to 160 °C showing a further slight performance degradation. An eye amplitude reduction of 24.3% and a jitter increase of 11.9% are measured at 160 °C.

Comparing the performance of the proposed driver with that of line drivers in the literature and market, it is possible to highlight that it overperforms all other solutions in terms of radiation hardness and speed. The only exception is the line driver designed in [38] that is able to sustain a 12.5 Gb/s communication link, but without adopting any specific design techniques to face radiation and temperature effects. On the other hand, the performance of the proposed driver comes at the expense of a wider area and larger power consumption over some of the line drivers reported in Table 1. These characteristics could be further investigated and optimized in future studies.

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