IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 24 June 2023, accepted 15 July 2023, date of publication 20 July 2023, date of current version 26 July 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3297496

RESEARCH ARTICLE

Reduced Voltage Stress and Spikes in Source Current of 7-Level Switched-Capacitor Based Multilevel Inverter

SHIRAZUL ISLAM[1], MARIF DAULA SIDDIQUE[2], (Member, IEEE), MD. REYAZ HUSSAN[3], (Student Member, IEEE), AND ATIF IQBAL[1], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Qatar University, Doha, Qatar
[2]Department of Electrical Engineering, National University of Singapore (NUS), Singapore 117583
[3]Department of Electrical Engineering, Aligarh Muslim University, Aligarh 202002, India

Corresponding author: Shirazul Islam (shiraz.ulislam@qu.edu.qa)

This publication, was made possible by the National Priorities Research Program (NPRP) grant # [13S-0108-200028] from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors. The APC for this manuscript is funded by the Qatar National Library, Doha, Qatar.

ABSTRACT Various 7-level switched-capacitor (SC) based converters are reported in the literature which furnishes a voltage gain of 1.5. However, in these topologies, the voltage rating of switches is high and the switch count is more. Further, the charging and discharging action of the switched capacitors, lead to the production of spikes having a large magnitude in source current and charging currents supplied to switched capacitors. Due to this limitation, the SC-based Multilevel Inverter (SC-MLI) cannot be used for high-power applications. To resolve these issues, an SC-MLI in an Active-Neutral-Point-Clamped (ANPC) configuration is proposed in this paper which requires switches having reduced value of voltage stresses and the switch count of the proposed converter is less. Further, to reduce the magnitude of spikes in the source and charging current supplied to switched capacitors, a soft switching circuit is included in the proposed converter. The soft charging circuit includes an inductor and a diode in the charging path of the proposed converter which ensures soft charging of the switched capacitors. The proposed converter can significantly suppress the spikes appearing in the source current by including a small value of inductance connected to the soft charging circuit. The proposed topology requires a single dc source, 2 switched capacitors, and 8 switches to generate 7-level and does not require an auxiliary diode. The absence of an auxiliary diode leads to a further reduction in losses. If the value of the modulation index is reduced to a low value, the proposed topology can maintain the self-balancing of the capacitor voltage. To highlight the various key features of the proposed 7-level topology, its comparison with the recent converter topologies suggested in the literature is carried out. To validate the efficacy of the proposed 7-level SC-MLI, experimental results are included which are captured using a laboratory prototype for different values of soft charging inductor.

INDEX TERMS Soft charging, switched capacitors, multilevel inverters.

I. INTRODUCTION

Multilevel Inverters (MLIs) are preferred due to the ease of integration of photovoltaic (PV) sources based on Renewable Energy Systems (RESs) to the grid. These converters eliminate the need for the front dc-dc converter stage which is required in conventional inverters for voltage boost-up action. The elimination of the first front-end converter increases the overall efficiency of conversion [1]. Further, the MLIs lead to improvement in the harmonic profile of the output voltage, electromagnetic interference is reduced, voltage stress across the switches included in MLIs is reduced and the operation of MLIs becomes more fault tolerant as compared to conventional inverters [2]. Due to these key features, the MLIs find their dominant applications in electric vehicles, uninterruptible power supplies, motor drives, microgrids power

The associate editor coordinating the review of this manuscript and approving it for publication was Fengjiang Wu.

systems requiring power factor corrections, HVDC transmission, etc. [3].

Over the course of the past few decades, several configurations of MLIs are discussed in the literature. Basic topologies reported in the literature to produce multilevel output are based on cascaded H-bridge (CHB), diode clamped, and flying capacitor-based configurations. For high-voltage applications, the cascaded H-bridge-based MLIs are considered a good option due to their modularity. A modified Selective Harmonic Elimination technique implemented using Pulse Amplitude Modulation used to improve the harmonic profile of the converter in CHB configuration and furnishing 7-level ac output voltage is suggested in [4]. However, the CHB-based converter topologies require a large number of input sources to be connected in the system which may not be feasible in practical scenarios. Further, the switch count is more [5]. To resolve this issue, diode clamped and flying capacitor-based configurations of MLIs are suggested. However, the component count is more in the case of diode-clamped-based multilevel converters. Further, the voltage balancing across the capacitor is a major issue in the case of flying capacitor-based converter topologies, [6], [7]. To balance the voltage across the capacitors in a 7-level FC-MLI, a wavelet modulation-based technique is suggested in [8]. Further, to enhance the active voltage balancing across the capacitors, phase-shift and carrier swapping-based PWM technique is suggested in [9]. The complexity of the techniques discussed in [8] and [9] increases with an increase in voltage levels in ac output voltage. Further, the requirement for a large number of components outweighs the advantages of FC-MLIs.

To resolve these issues, switched-capacitor-based Multilevel Inverters (SC-MLIs) are considered the most appropriate candidate to produce multilevel output without requiring multiple input sources and more component count. Due to the above-mentioned advantages, the SC-MLI are preferred choice for the integration of renewable energy sources like fuel cells, battery storage, solar photovoltaic (PV) sources, etc. [10]. The SC-MLI offers improved waveforms of multilevel ac output, lower electromagnetic interference and lower device stress [11]. However, Active-neutral-point-clamped (ANPC) based SC-MLIs having voltage-boosting capabilities are preferred as compared to the other SC-MLIs. It is due to their requirement for low dc-link voltage. This leads to improvement in the efficiency, power density and reliability of the SC-MLI [12].

Due to the above-mentioned advantages offered by SC-MLI, various recent variants of SC-MLIs are included in the literature. To produce a 7-level single-phase ac output voltage, the SC-MLIs are suggested in [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], and [26]. The topologies suggested in [13], [14], and [15] are two-stage SC-MLI. In these MLIs, the dc voltage is boosted up in the first stage and finally, the conversion to ac output takes place in the second stage. However, the voltage stress across the switches is more in the case of SC-MLIs requiring two-stage conversion. Due to the requirement of switches having large voltage ratings, the cost of the converter increases. Further, the topologies suggested in [13] and [15] require two input sources which may not be available in certain applications. The SC-MLI topologies requiring a single dc input source are suggested in [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], and [26] require only one dc input source. The SC-MLI with 7-level ac output is suggested in [16], [17], [18], [19], [20], [21], [22], [23], [24], and [26] while with 5-level ac output voltage is suggested in [25]. The topologies suggested in [16], [17], [18], and [19] require switches having reduced value of voltage stresses across them. This leads to a decrement in losses in the converter and its cost. However, the switch count of these topologies is high. The topologies suggested in [20], [21], [22], [23], [24], [25], and [26] require less number of switches. However, these converter topologies require switches having high voltage ratings. The topologies suggested in [22], [24], and [26] require switches having voltage stress of three times the magnitude of the dc input source. From the above discussion, a trade-off is observed between the number of switches and the voltage rating of switches.

The topologies suggested in [13], [14], [15], [19], [20], and [24] include auxiliary diodes. These diodes produce losses in the converter and lead to a reduction in converter efficiency. The converter topology suggested in [19] requires 4 auxiliary diodes, thereby furnishing low efficiency. Therefore, the converter topologies suggested in [13], [14], [15], [19], [20], and [24] cannot be used in applications requiring high efficiency.

In the case of SC-MLIs configurations, the switched-capacitors are connected in parallel with the input dc voltage source for their charging and connected in series with the input dc voltage source while discharging. Due to the charging action of switched capacitors, spikes of large magnitude appear in the source current and charging current of switched capacitors. The magnitude of these spikes further increases with an increase in the power rating of the SC-MLIs. Excessive spike charging current may damage the capacitors and reduce the efficiency of the converter [27]. This may hamper the reliability of the electrolytic capacitors included in SC-MLI. Due to the above-mentioned limitations, the SC-MLIs cannot be used in high-power applications. However, some of the solutions are reported in the literature to resolve this issue. In [28], capacitors of high equivalent series resistance (ESR) value are used to limit the magnitude of spikes in the source. However, the high ESR value of capacitors reduces the effective value of output voltage and the efficiency of the converter is reduced. To accommodate the high magnitude of current spikes, the oversizing of the power switches having an over-current rating is suggested as a solution in [1]. Further, snubber circuits connected across the switches may be used to protect the switches. However, these options increase the cost of the proposed SC-MLI. Therefore, a trade-off exists between the cost and the performance of SC-MLIs having high power rating.

To reduce the magnitude of spikes source and charging currents, various soft switching-based techniques are discussed in the literature. These techniques include the connection of the inductor in the charging path of SC-MLI and ensuring the soft charging of the capacitors. Soft charging of the capacitors leads to a significant reduction in the magnitude of current spikes present in the source current and charging current supplied to capacitors. In [25], an ANPC-based T-type SC-MLI is discussed in which two identical soft charging legs are used to limit the magnitude of spikes present in the source current. Each soft-switching circuit includes two switches and one inductor. The suggested converter ensures a reduction in the magnitude of current spikes. However, the value of the inductance included in the soft charging circuit is large and the cost of the converter is more due to the use of two inductors. The inclusion of more inductors in soft switching circuits may reduce the efficiency of the converter. Further, the voltage stress across the switches is more. To reduce the value of soft charging inductance and the number of inductors used in soft switching circuits and voltage stress across the switches, a generalized n-level SC-MLI is discussed in [19]. The suggested converter includes only one inductor of reduced value in the soft switching circuit. The suggested converter requires two identical switched-capacitor-based legs required for each phase of the suggested 7-level SC-MLI. The inclusion of two legs increases the cost and size of the converter. Further, the operation of the converter may become complex. To make the operation of the converter simple, a modified 7-level switched-capacitor-based converter topology is suggested in [26]. The topology included in [26] ensures the reduction in the magnitude of spikes which appears in the source current. However, the total number of components required in the suggested converter is more.

To overcome these limitations, a 7-level SC-MLI in Active-Neutral-Point-Clamped (ANPC) configuration is proposed in this paper. The key features of the proposed 7-level MLI confutation are as follows:

- The total number of components required in the proposed converter is reduced. The proposed converter requires a single input source, 8 switches, 2 switched capacitors, 1 inductor, and no additional diode.
- The suggested topology includes switches with decreased voltage stresses and generates 7-level ac output voltage with a voltage gain of 1.5. The reduction in the value of voltage stress across the switches leads to a reduction in TSV across the switch string.
- A diode and an inductor are included in the charging path of the proposed converter which ensures soft charging of the capacitors. The soft-charging circuit leads to a significant reduction in the magnitude of spikes present in the source current. However, the low value of inductance is required to reduce the magnitude of current spikes.
- The proposed converter ensures self-voltage balancing across the capacitors with variations in the value of the modulation index and the operating frequency of the converter.
- The key features of the proposed converter are highlighted with the help of a comparative analysis of the proposed converter with state-of-the-art converters discussed in the literature. To validate the efficacy of the proposed converter, the lab prototype is fabricated and the experimental results are included.

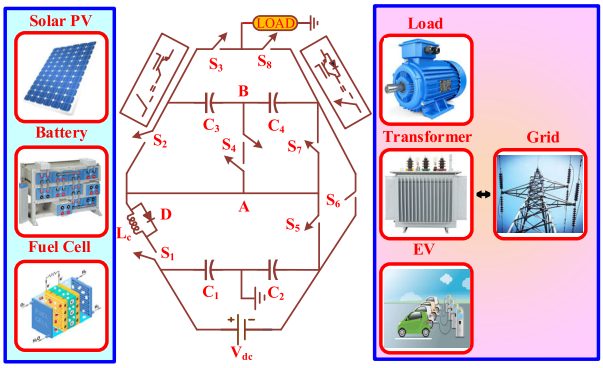


FIGURE 1. Schematic of the proposed 7-level SC-MLI.

II. PROPOSED TOPOLOGY

A. DESCRIPTION OF THE PROPOSED SC-BASED 7-LEVEL MLI

Fig. 1 shows the proposed switched capacitor-based ANPC 7-level inverter configuration used to produce a single ac output voltage. This configuration includes a single input dc source (V_{dc}), 8 switches (S_1-S_5 and S_7-S_8) including antiparallel diodes, 1 switch (S_6) without antiparallel diode, 2 dc-link capacitors (C_1-C_2), and 2 switched-capacitors (C_3-C_4) to generate seven levels at the output with a voltage gain of 1.5. The dc-link capacitors, C_1 and C_2 are used to split the voltage of the dc source into two halves and provide the facility for connection of the neutral terminal of the load. The switched capacitors, C_3 and C_4 are charged by the input voltage supply, V_{dc} and discharged alternately through the load to produce a 7-level ac output voltage. The ANPC arrangement leads to a reduction in common mode voltage to a very low value, which reduces the leakage current in the system. Further, the ANPC connection leads to a reduction in voltage stresses across the switches which are limited to source voltage (V_{dc}). As illustrated in Fig. 1, the inductor, L_c, is connected in the charging route of the capacitors, C_3 and C_4, to reduce the size of spikes that may arise in the source current during the charging operation of capacitors. However, the interruption of inductor current in the charging path may lead to the production of voltage spikes across the switches, S_1 and S_2. This can be avoided by operating the switches under zero current conditions. However, this condition imposes an upper bound on the value of the inductor. A freewheeling diode is connected in parallel to the inductor to alleviate this problem. Further, the freewheeling diode prevents the overcharging of

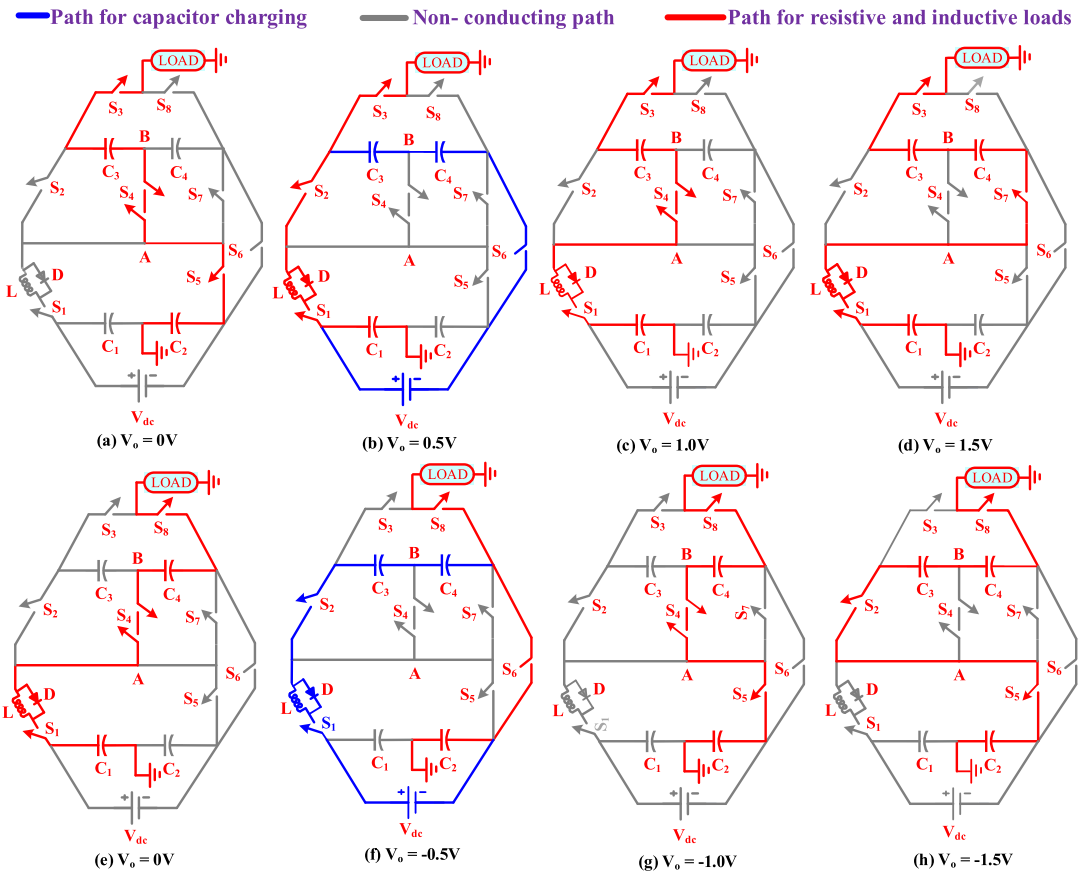


FIGURE 2. Different stages of the proposed single-stage SC-MLI topology, which produces 7-level ac output voltage.

the capacitors, C_3 and C_4 to safeguard the switches S_1 and S_2 during the fault occurrence. The inclusion of a diode enhances the fault-tolerant capability of the proposed SC-MLI. In the next subsection, the operation of the proposed 7-level SC-MLI is discussed.

B. OPERATION OF THE PROPOSED CONVERTER

The voltage gain of 7-level SC-MLI is decided by the voltage gain of the switched capacitors, C_3 and C_4 included in the proposed converter. The voltage appearing across the capacitors, C_3 and C_4 is $0.5V_{dc}$. Here, V_{dc} is the magnitude of the input voltage. These capacitors are charged to 0.5 V_{dc} by using the switches, S_1, S_2 and S_6. The red colour is used to indicate the direction of current flow during discharging of capacitors in various switching states as shown in Fig. 2. The charging operation of capacitors is depicted in blue, and the capacitors taking part in voltage boost action are depicted in red. The proposed converter can generate 7 levels, with the levels that can be produced being 0Vdc, ±0.5Vdc, ±1.0Vdc, and ±1.5Vdc. There are eight different ways the proposed converter can operate to produce these levels. Various switching states during these operating conditions are shown in Fig. 2. The voltage stress across switches S_1-S_3 and S_5-S_8 is V_{dc} while the voltage stress across switch S_4 is $0.5V_{dc}$.

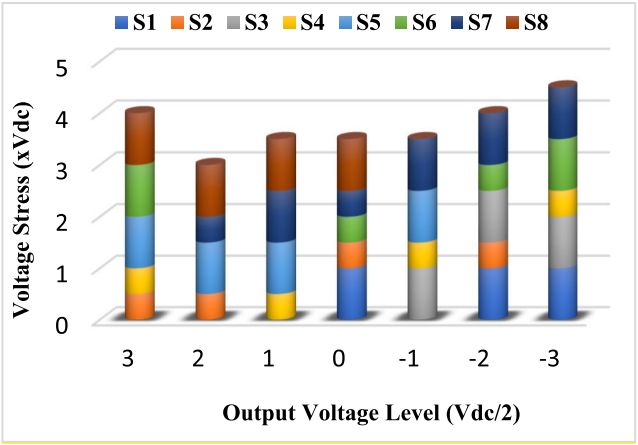


FIGURE 3. Voltage stress across the switches.

Fig. 3 depicts the voltage stress that develops across each switch at various ac output voltage levels. From Fig. 3, it is noted that the total PIV (Peak Inverse Voltage) spanning switches S_1 through S_3, S_5 through S_8, and S_4 is 66% of the peak value of output ac voltage and 34% of the peak value of ac output voltage, respectively. This leads to the value of Total Standing Voltage for the proposed 7-level SC-MLI being equal to 5.33. Here TSV is defined as the sum of

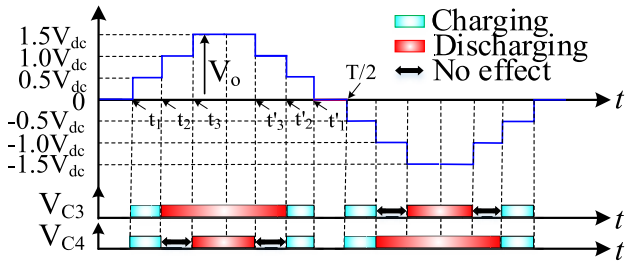


FIGURE 4. Output voltage of the proposed 7-level SC-MLI as well as the capacitors' charging and discharging patterns.

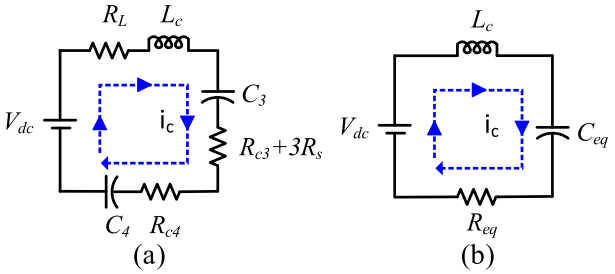


FIGURE 5. (a) Charging path of the capacitors, C_3 and C_4. (b) Equivalent circuit of charging path of C_3 and C_4.

voltages appearing across the switches divided by the peak value of output ac voltage.

C. SELECTION OF SWITCHED CAPACITORS, C_3 AND C_4

In the case of SC-MLI, the capacitors are connected in parallel during charging and in series during discharging with the dc input source. This charging and discharging action in the case of SC-MLI leads to the production of ripples in capacitor voltages. The value of flying capacitors, C_3 and C_4 connected across the load is evaluated using the value of, ΔQ_c charge supplied by the capacitors C_3 and C_4 during the discharge period. From the discharge pattern of capacitors, C_3 and C_4 shown in Fig. 4, the capacitor, C_3 is discharged during the time interval t_3 to t_3'. The magnitude of ripple voltage, Δv_{c3} appearing across the capacitor, C_3 during this the time interval t_3'- t_3 is

$$\Delta v_{c3} = \frac{\Delta Q_{c3}}{C_3} = \frac{1}{C_3}\int_{t_3}^{t_3'} i_o dt \tag{1}$$

The discharge period of the capacitor C_3 is t_3'- t_3, which corresponds to θ_3 to π-θ_3. The desired value of C_3 selected using (1) for a specific range of Δv_{c3}, is given by

$$C_3 > \frac{1}{2\pi f_s \Delta v_{c1}} \int_{\theta 3}^{\pi-\theta_3} I_o \sin(\omega t - \phi) d(\omega t) = \frac{I_o \cos\theta_3 \cos\phi}{\pi f_s \Delta v_{c3}} \tag{2}$$

where I_o is the peak value of the fundamental load current component, ϕ is the phase angle and f_s is the frequency of the MLI output voltage. The value of the capacitance of C_4 is

$$C_4 > \frac{I_o \cos\theta_3 \cos\phi}{\pi f_s \Delta v_{c4}} \tag{3}$$

As per the standards discussed in the literature [29], 5–10% of the nominal capacitor voltage is considered the allowable range of ripple voltage in the case of MLI.

D. SELECTION OF SOFT CHARGING INDUCTOR, L_c

After including the soft charging inductor L_c, the capacitor is charged during each half cycle of ac output voltage. The equivalent circuit formed by the source, V_{dc} and inductor, L_c during charging of switched-capacitors, C_3 and C_4 is shown in Fig. 5. The equivalent series resistance of the inductor (R_L), ON-state resistance of the switch (R_s), internal resistance (R_c) of the capacitor, forward voltage drop (V_d) of the diode, and internal resistance of the diode (R_d) are examples of parasitic elements that the charging current encounters along its path. If R_{eq} is the equivalent resistance and C_{eq} (=$(C_3C_4)/(C_3+C_4)$) is the equivalent capacitance of C_3 and C_4 of the charging circuit shown in Fig.5(b), the first-order differential equations describing the states of capacitor voltage v_{ceq} and inductor current, i_{Lc} are

$$\begin{aligned} i_{LC} &= C_{eq}\frac{dv_{ceq}}{dt} \\ V_{dc} &= L_c\frac{di_{LC}}{dt} + v_{veq} \end{aligned} \tag{4}$$

From Figs. 2 and 3, it is noted that corresponding to t_3 to t_3', θ_3 to π-θ_3, the capacitors are discharged to the load. Assuming that a resistive load, R_o is connected across the output of the proposed converter, integration of both sides of (4) for the discharging period θ_3 to π-θ_3 gives

$$\begin{aligned} \Delta i_{LC} &= \frac{\omega_r V_{dc}}{\omega R_o}(\theta_2 - \theta_1)\sin(\omega t - \theta_3) \\ \Delta v_{ceq} &= V_{dc} - \frac{\omega_r^2 L_c V_{dc}}{\omega R_o}(\theta_2 - \theta_1)\cos(\omega t - \theta_3) \end{aligned} \tag{5}$$

From (5), the maximum value of ripple present in the charging current, Δi_{LC} is

$$\Delta i_{LC} = \frac{\omega_r V_{dc}}{\omega R_o}(\theta_2 - \theta_1) \tag{6}$$

where, $\omega_r = 1/\sqrt{L_c C_{eq}}$ is the resonant frequency of the equivalent circuit shown in Fig.5(b). Substituting the ω_r in (6) and simplifying, the desired value of L_c required to limit the spikes in source and capacitor current is given by

$$L_c = \left(\frac{V_{dc}}{\omega R_o \Delta I_{LC}\sqrt{C_{eq}}}(\theta_2 - \theta_1)\right)^2 \tag{7}$$

Form (7), it is noted that the magnitude of ripple present in the charging current is inversely proportional to the value of soft charging inductance, L_c. The inclusion of L_c in the proposed converter leads to a reduction in charging current

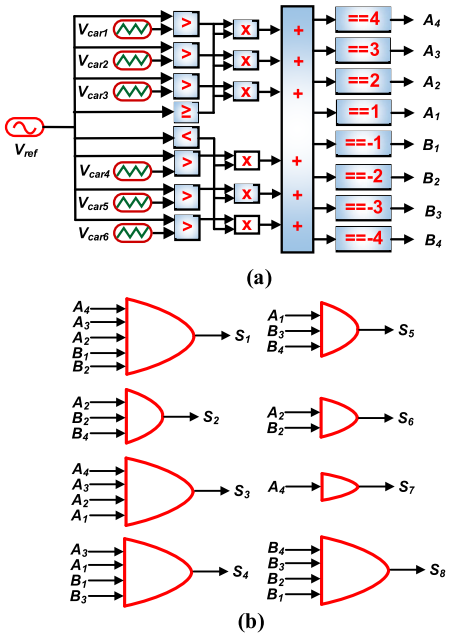


FIGURE 6. (a) Switching scheme of the proposed 7-level inverter. (b) OR logic is used to generate gating pulses to switches.

ripples. The reduction in ΔI_{LC} leads to a reduction in ripple losses occurring in the capacitors.

From the equivalent circuit shown in Fig. 5(b), it is observed that the series combination of elements, L_r, R_{eq} and C_{eq} forms a second-order L-C circuit. For the value of $R_{eq} < 2\sqrt{C_{eq}/L_c}$, the soft switching-based charging circuit behaves as a second-order underdamped circuit. For this underdamped circuit, the value of the damping factor is $\xi = R_{eq}/2\sqrt{C_{eq}/L_c}$. Therefore, in the case of the second-order L-C circuit, the damping factor, ξ is adjusted using the value of inductance, L_c determined from (7).

E. MODULATION TECHNIQUE

To generate a 7-level single-phase ac output voltage, level shifted multicarrier sinusoidal pulse width modulation technique shown in Fig. 6 is used. In this technique, a sinusoidal signal is compared with level shifted triangular carrier signal. In the proposed converter, a sinusoidal signal having a peak amplitude of 3 is compared with six equally level-shifted carrier signals distributed between the peak values of -3 and $+3$. The peak amplitude of each carrier signal is unity. The switching scheme of the converter to generate the various switching states (A_1-A_4, B_1-B_4) is shown in Fig. 6(a). Now these switching states are combined through the OR logic to generate gate pulses required for the switches (S_1-S_8) to generate the 7-level ac output voltage. The gating operation of switching states is shown in Fig. 6(b).

III. LOSS ANALYSIS OF THE CONVERTER

In this section, the losses occurring in the converter are calculated for evaluation of the efficiency of the converter. The losses which occur in a multilevel converter are mainly the conduction losses, P_c, switching losses, P_{sw} and ripple losses, P_r and the total losses in the converter are equal to the algebraic sum of P_c, P_{sw} and P_r.

A. CONDUCTION LOSSES

A multilevel converter's conduction losses are caused by the switch's ON-state resistance, the diodes' internal resistance, and the diode's forward voltage drop. These losses occur in the passive components like switched- capacitors and inductors included in the soft switching circuit due to the equivalent series resistance (ESR) of capacitors and inductors. To evaluate conduction losses in a given converter, the values of charging current and load current are evaluated which is further used to evaluate the instantaneous value of the conduction losses, P_{ci} which occur in the power electronic switches, diodes, inductors and capacitors. The instantaneous values of conduction losses are evaluated for all possible levels of single-phase ac output voltage. The average value of conduction losses happening in various converter components throughout a particular level is calculated using the time ratio factor. The average conduction loss, P_c is

$$P_c = \sum_{i=1}^{n} P_{ci} \tag{8}$$

where the element n refers to the total number of voltage levels.

B. SWITCHING LOSSES

The voltage across the switch and the current flowing through it remains nonzero when the switch turns on and turns off. These nonzero values of switch voltage and currents give rise to nonzero switching losses which occur in the switch during the turn-on and turn-off process. These losses are calculated for the semiconductor switch during turn-on time, t_{on} and turn-off time t_{off}. While evaluating these losses, the variation of switch voltage (v_{sw}) and switch current during turn-on and turn-off periods (I_{on} and I_{off}) is assumed to be linear. The switching loss, E_i occurring in an i^{th} semiconductor switch during a given cycle is

$$E_i = \int_0^{t_{on}} v(t)i(t)dt + \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,i}(I_{on,i}t_{on} + I_{off,i}t_{off}) \tag{9}$$

where, E_i are the switching losses of the i^{th} switch, the element, t_{on} indicates the turn-on time of the switch, $I_{on,i}$ is the current through the switch before turning-on, t_{off} is the switch turn-off time, I_{off} is the switch current flowing before being turning-off, $V_{sw,i}$ is the voltage drop during on-state across the i^{th} switch. The switching loss, $E_{sw,i}$ is given by,

$$\begin{aligned} E_{sw,i} &= N_{on,i}E_{on,i} + N_{off,i}E_{off,i} \\ P_{sw,i} &= \frac{N_{on,i}E_{on,i} + N_{off,i}E_{off,i}}{T} \\ &= \frac{V_{sw,i}(I_{on,i}N_{on,i}t_{on} + I_{off,i}N_{off,i}t_{off})}{6T} \end{aligned} \tag{10}$$

where, the elements, $N_{on,i}$ and $N_{off,I}$ indicates the total number of switch-on and off cycles for an i^{th} switch during a given cycle. Now, the overall switching loss, P_{sw} which occurs in the SC-MLI are

$$P_{sw} = f_s \sum_{i=1}^{13} \frac{V_{sw,i}(I_{on,i}N_{on,i}t_{on} + I_{off,i}N_{off,i}t_{off})}{6T} \quad (11)$$

where the element f_s refers to the switching frequency of the converter.

C. RIPPLE LOSSES

These losses occur mainly in the capacitor during the charging and discharging process of the capacitor. The unequal value of the capacitor across the capacitor during the charging and discharging process gives rise to a voltage ripple appearing across the capacitor voltage. The nonzero magnitude of voltage ripple leads to ripple loss, P_r taking place in switched capacitors. The ripple loss, P_r taking place in a switched capacitor included in SC-MLI is

$$P_r = \frac{1}{2} f_s \sum_{i=1}^{N_k} C_i \Delta v_{ci}{}^2 \quad (12)$$

where N_k is the total number of capacitors' charging cycles. The voltage ripple during the i^{th} charging interval is denoted by ΔV_{ci}. The overall ripple loss, P_r that occurs in the capacitors if total N_c capacitors are going through charging transitions is

$$P_r = \sum_{i=1}^{Nc} (\frac{1}{2} f_s \sum_{i=1}^{N_k} C_i \Delta v_{ci}{}^2) \quad (13)$$

For practical consideration, the magnitude of Δv_c recommended for the selection of switched-capacitor, C_i is in the range of 5-10% of the nominal value of source voltage, V_{dc}.

D. CORE LOSS

The loss occurring in the magnetic material of the core included in the inductor is termed core loss. The core loss included mainly two losses which are hysteresis loss and eddy current loss.

1) HYSTERESIS LOSS

When a magnetic core is subjected to the magnetic field, the losses occurring in the core due to magnetization and demagnetization of the core is termed hysteresis loss and evaluated as

$$P_h = k_h f^{\alpha} B^{\beta} \quad (14)$$

where f is the frequency of flux density, B is the maximum flux density, k_h is a coefficient, α and β are Steinmetz constants.

2) EDDY'S CURRENT LOSS

The loss produced in the magnetic material of the core due to the production of eddy current in the core is attributed as eddy current loss and evaluated as

$$P_e = k_e f^2 B^2 \quad (15)$$

where k_e is a constant. Now from (14) and (15), the core loss occurring in the magnetic material of the inductor is given by

$$P_{ir} = P_h + P_e = k_h f^{\beta} B^{\beta} + k_e f^2 B^2 \quad (16)$$

Relation (16) can also be approximated as

$$P_{ir} = k f^{\beta} B^{\beta} \quad (17)$$

where P is the core loss, which is expressed in watts per volume. For this particular core material, the data sheet provided by the manufacturer gives the values of k, α and β respectively. The relation given by (17) is called the Steinmetz relation to calculate the value of core loss in the inductor. There are various other models used to calculate the core loss in the magnetic material of the inductor. The procedure for core loss measurement in an inductor coil is sufficiently discussed in [30] and [31]. The magnitude of the core loss is very small. Therefore, the core loss is not considered in this study.

Using (8), (11) and (13), the following relation is used to evaluate the efficiency of the proposed converter:

$$\eta = \frac{P_{out}}{P_{out} + P_c + P_{sw} + P_r} \quad (18)$$

To evaluate the efficiency of the converter analytically, the PLECs software is used to evaluate the losses which occur in the switches, diodes, capacitors and inductors included in the soft switching circuit. The software facilitates the thermal modelling of the power semiconductor devices. To show the efficacy of the soft switching circuit on the performance of the converter, the efficiency of the proposed converter is evaluated with and without including the soft switching circuit. Fig. 7 shows the variation of the efficiency of the converter concerning the power supplied to the load for the proposed converter with various values of soft charging inductor. The parameters required to evaluate the efficiency of the proposed converter are listed in Table 3. From these curves, it is observed that with an increase in the value of the soft charging inductor, L_c the effective value of the damping factor, ξ decreases. For the value of L_c increasing from 200μH to 350 μH, the effective value of ξ decreases from 0.57 to 0.40. From (7), the increment in L_c leads to a reduction in the magnitude of spikes present in the source and capacitor charging current which decreases the losses in the switches and capacitors. The reduction in losses takes place due to a reduction in conduction losses in switches and ripples losses in capacitors. This leads to an increment in converter efficiency. From Fig.7, it is observed that for a low value of power demanded by the load, the efficiency of the proposed converter with and without soft charging circuits is nearly

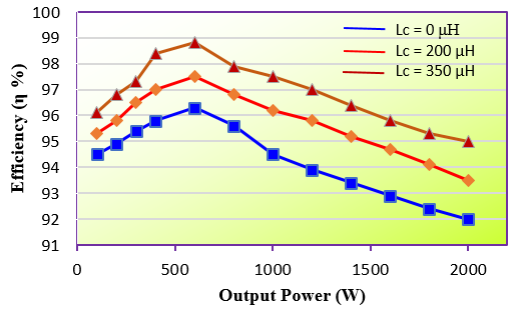


FIGURE 7. Efficiency of the proposed converter with the hard-charging and soft-charging inductor.

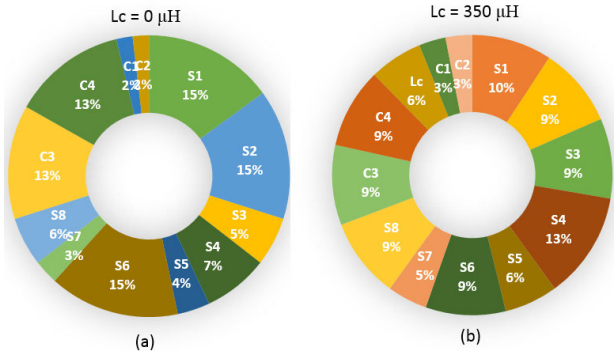


FIGURE 8. Distribution of losses across power semiconductor switches, soft charging inductor and capacitors of the proposed 7-level converter.

equal. However, for the rated load of 1000 W, the efficiency of the converter with $L_c = 0\mu$H is 94.3%, while for $L_c = 200\mu$H, the efficiency of the converter is 96.2% and for $L_c = 350\mu$H, the efficiency of the proposed 7-level converter is evaluated as 97.5%.

Fig. 8 shows the loss distribution on various components included in the proposed 7-level SC-MLI. From Fig. 8(a), it is noted that the losses which occur in the switches, S_1, S_2 and S_6 included in the charging path of the switched capacitors are more as compared to the other switches. However, the losses in switches S_1, S_2 and S_6 are significantly reduced by including a soft charging inductor, $L_c = 350\mu$H in the proposed converter as shown in Fig 8(b).

E. THERMAL ANALYSIS OF THE SWITCHES

The switches connected in the charging loop of the converter are severely affected by the ripples present in the source current. Therefore, the switches connected in the charging path of the proposed converter are considered for thermal analysis. The thermal model of the IGBT switch and diode presented in [32] is taken into consideration for this reason. A thermal investigation is done on the IGBT switch G60N100 IGBT [32] and its antiparallel diode. For accurate modelling of losses taking place in the IGBT and diode, the PLECS software approach is used. Using PLECS, the junction temperature of the IGBT can be measured with and without a soft charging inductor. The initial value of junction

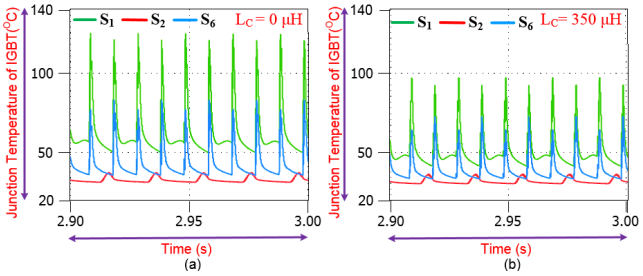


FIGURE 9. Junction temperature profile of IGBT switches S_1, S_2 and S_6 with (a) $L_c = 0\ \mu$H and (b) $L_c = 350\ \mu$H.

temperature across the switches, S_1, S_2 and S_6 is considered to be 25^{O}C. The Fig. 9(a) shows the junction temperature of the switches S_1, S_2 and S_6 for $L_c = 0\mu$H with load power demand of 1kW imposed on the proposed 7-level SC-MLI. The maximum value of junction temperature of switch S_6 is observed which is 127^{o}C. The Fig. 9(b) shows the profile of junction temperature of the switches S_1, S_2 and S_6 for $L_c = 350\mu$H. From Fig. 9(b), it is noted that due to inclusion of soft charging inductor, L_c the junction temperature of switches S_1, S_2 and S_6 decreases. A decrement in junction temperature of switch S_6 is observed from 127^{O}C to 97.5 ^{O}C.

F. SELECTION OF SWITCHED-CAPACITORS AND SOFT CHARGING INDUCTOR

In this subsection, the process of selection of the values of switched capacitors required in the proposed 7-level SC-MLI to generate single-phase ac output voltage is discussed. The relation required to select the values of capacitance C_3 and C_4 are given by (2) and (3) discussed in section II. The peak value of the output voltage of the converter is $V_o = 150$V having a frequency of 50 Hz, and its power rating is 1000W. The value of load current, I_o is 14 A. The voltage appearing across the capacitor, C_3 is $V_{dc}/2 = 50$ V. The maximum permissible value of ΔV_{c3} is taken as 10% of V_{dc}. Using these values, the value of C_1 is

$$C_3 = \frac{I_o \cos\theta_3 \cos\phi}{\pi f_s \Delta v_{c3}} = \frac{9.43 \times \cos 46 \times \cos 22}{\pi \times 50 \times 0.1 \times 100} \approx 3867\mu F \tag{19}$$

To satisfy (14), the value of $C_3 = 3900$uF (ESR, $R_{c3} = 50$mΩ) and voltage rating 450V as supplied by the manufacturer is selected as the desired value of C_3. However, the discharging patterns of capacitors, C_3 and C_4 are identical. Therefore, the value of the capacitor, $C_4 = C_3 = 3900\mu$F.

The systematic procedure for the selection of switched capacitors in the case of multilevel inverter is discussed in detail in [33]. For a given multilevel inverter, the quantities which decide the selection of the capacitor for SC-MLI are the capacitance value and the rated voltage. The selected value of the capacitor should be large enough to block the required voltage level and to limit the ripple voltage magnitude within the defined limit. The capacitor voltage should be

higher than the maximum value of the instantaneous capacitor voltage.

Three types of capacitors are normally used for multi-level inverters which are Aluminum Electrolytic Capacitors (Al-Caps), Metallized Polypropylene Film Capacitors (MPPF Caps) and high capacitance Multi-Layer Ceramic Capacitors (MLC-Caps) [34]. Due to low cost, low heat dissipation, and good stability in various frequency and temperature ranges, MPPF capacitors are considered to be a good choice for MLI [33]. However, in the prototype of the proposed 7-level SC-MLI, Al-Caps are used as C_3 and C_4.

The value of the inductor, L_c to be included in the soft charging circuit is selected using the relation (7). For the value of the input voltage $V_{dc} = 100$ V, load resistance, $R_o = 11.25\Omega$, the peak value of charging current load current, $\Delta I_c = 9.43$A, $\theta_2 = 20.4^o$ and $\theta_1 = 3.6^o$, the desired value of L_c is

$$L_c = \left(\frac{100}{2 \times \pi \times 50 \times 11.25 \times 10 \times \sqrt{1950 \times 10^{-6}}} \times \left(\frac{\pi}{180}\right)(20.4 - 3.6)\right)^2 \approx 350\mu\text{H} \quad (20)$$

To suppress the spikes in the capacitor and source current, the desired value of the soft charging inductor is selected to be 350μH ((ESR, $R_L = 0.11\Omega$). Now for the value of $L_c = 350\mu$H, the value of the damping factor, ξ is

$$\xi = \frac{R_{eq}}{2}\sqrt{\frac{C_{eq}}{L_c}} = \frac{(0.11 + 2 \times 0.05 + 3 \times 0.042)}{2}\sqrt{\frac{1950 \times 10^{-6}}{350 \times 10^{-6}}} \approx 0.4 \quad (21)$$

IV. COMPARATIVE STUDY

In this section, the comparative study of the proposed SC-MLI is carried out with recently reported topologies in reference to parameters such as $\boldsymbol{N_L}$ = Number of levels, $\boldsymbol{G}$ = voltage gain, $\boldsymbol{N_{IS}}$ = the number of input dc sources, $\boldsymbol{N_d}$ = number of diodes in parallel with switches, $\boldsymbol{N_c}$ = the number of capacitors, $\boldsymbol{N_{sw}}$ = Number of switches, $\boldsymbol{N_{ad}}$ = number of auxiliary diodes, $\boldsymbol{N_{gd}}$ = number of the gate driver circuit, $\boldsymbol{PIV}$ = Peak inverse voltage in per unit, $\boldsymbol{VRC}$ = voltage rating of capacitors, $\boldsymbol{TSV_{pu}}$ = Total standing voltage in per unit, η = Efficiency and power density = $\boldsymbol{D}$, $\boldsymbol{SW}$=soft switching circuits and $\boldsymbol{L_c}$ = number of inductors included in the soft charging circuit. The *PIV* appearing across the power semiconductor device is expressed as the normalized value of the dc input voltage source, V_{dc}. The *TSV* is equal to the algebraic sum of the *PIV* of the various power semiconductor devices and represented as the normalized value of the peak of the output voltage, V_o of the proposed converter. These parameters are used to validate the effectiveness of the proposed 7-level topology. The comparison of the proposed converter is carried out concerning 7-level converters with and without requiring soft switching circuits and salient features of the proposed converters are highlighted.

TABLE 1. Switching states for the proposed 7-level architecture.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2	C_3	C_4	V_{out} ($\times V_{dc}$)
1	0	1	0	0	0	1	0	D	-	D	D	+3
1	0	1	1	0	0	0	0	D	-	D	-	+2
1	1	1	0	0	1	0	0	D	-	C	C	+1
0	0	1	1	1	0	0	0	C	C	-	-	0
1	0	0	1	0	0	0	1					
1	1	0	0	0	1	0	1	-	D	C	C	–1
0	0	0	1	1	0	0	1	-	D	-	D	–2
0	1	0	0	1	0	0	1	-	D	D	D	–3

* 1 = ON-state of the switch, 0 = OFF-state of the switch, C= charging, D = discharging of the capacitor.

Based on voltage gains of 7-level converters, the topologies suggested in [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], and [26] can be divided into two categories. The converters which furnish a voltage gain of 1.5 are discussed in [14], [16], [17], [18], [20], [21], [22], and [23] while the converters suggested in [19], [24], and [26] give ac output voltage having a voltage gain of 3. The converters suggested in [13] and [15] give a voltage gain of unity. The converter configurations discussed in [19], [24], and [26] ensure high voltage gain. However, the converter topologies suggested in [24] and [26] require switches having large voltage stress as compared to the converters discussed in [13], [14], [16], [17], and [18]. The converters included in [13], [14], and [15] are less preferred due to two-stage conversion. The converter topologies suggested in [16], [17], [18], [19], [23], and [26] require more switches to produce a 7-level ac output voltage. The converter topologies suggested in [20], [21], [22], and [24] require fewer switches as compared to the converter topologies suggested in [16], [17], [18], [19], [23], and [26]. However, the converter topologies suggested in [20] and [24] require two auxiliary diodes which reduce the efficiency of the converter at a high power rating. The converter suggested in [22] require 8 switches. However, the voltage stress and the TSV across the switch string are more. The converter discussed in [21] requires 9 switches. However, the proposed converter, [P] requires only 8 switches to generate 7-level ac output voltage and does not require any auxiliary diode. Further, the PIV of the switch included in the proposed converter [P] is less as compared to the converter suggested in [21].

From Table 2, it is observed that the converter topologies with soft charging circuits discussed in [19], [25], and [26], [P] offer high efficiency as compared to the converter topologies without soft charging circuits discussed in [13], [14], [15], [16], [17], [18], [20], [21], [22], [23], and [24]. The SC-MLI discussed in [13], [14], [15], [16], [17], [18], [20], [21], [22], [23], and [24] suffers from the limitation that the magnitude of the spikes in source current and charging current of switched capacitors is very high which appears during the charging of the capacitors. There is no arrangement used in these converter topologies to limit the magnitude of spikes appearing in the source current. These spikes may become more pronounced in the case of high-power rating converters. However, a soft charging circuit is used in the

TABLE 2. Comparison of different 7-level SC-MLI topologies with the proposed topology.

Ref.	N_L	G	N_{IS}	N_{SW}	N_{ad}	N_{gd}	N_c	PIV_{pu}	TSV_{pu}	VRC		η (%)	f_s (Hz)	P_o (W)	D	SW	L_c
										$0.5V_{dc}$	V_{dc}						
[13] TS	7	1	2	7	2	7	1	1	9.3	0	1	86-90	400-2500	250	H	No	0
[14]ANTS	7	1.5	1	9	1	9	3	1	10.67	2	1	97	60	200	M	No	0
[15]	7	1	2	8	2	8	4	1.88	5.66	2	2	91	20000	300	M	No	0
[16]	7	1.5	1	10	0	10	3	1	5.3	2	1	91.5	10000	225	L	No	0
[17]ANPC	7	1.5	1	10	0	10	3	1	6	2	1	97.2	50, 2500	1500	L	No	0
[18]ANPC	7	1.5	1	10	0	8	4	1	5.33	4	0	97	50, 5000	150	M	No	0
[19]	7	3	1	12	4	12	4	1	4	0	4	93.5	50	1200	L	Yes	1
[20]	7	1.5	1	7	2	7	2	1.5	5	2	0	96.1	2000	600	H	No	0
[21]ANPC	7	1.5	1	9	0	9	3	1.5	5.3	2	1	96.7	5000	188	M	No	0
[22]	7	1.5	1	8	0	8	1	3	8	0	1	98	80000	1000	H	No	0
[23]ANPC	7	1.5	1	10	0	8	4	2	7.33	4	0	97.4	5000	140	M	No	0
[24]	7	3	1	9	2	9	3	3	4.3	0	3	93.1	50	313	M	No	0
[25]ANPC	5	1	1	12	0	11	4	1.5	14	4	0	97.6	10000	160	L	Yes	2
[26]	7	3	1	11	0	10	4	3	6	0	4	97.4	20000	1000	L	Yes	1
[P]ANPC	7	1.5	1	8	0	8	4	1	5.3	4	0	97.5	5000	1000	M	Yes	1

*N_L= Number of levels, G= voltage gain, N_{IS}= number of input dc sources, N_{sw} = Number of switches, N_d=number of antiparallel diodes with switches, N_{ad}= number of auxiliary diodes, N_{gd}= number of gate drivers, N_c = number of capacitors, VRC = voltage rating of capacitors, PIV = Peak inverse voltage in per unit, TSV_{pu}=Total standing voltage in per unit, f_s = Switching Frequency, η =Efficiency, SW= soft charging, L_c = number of soft charging inductors, D= Power Density, L=Low, M= medium, H= High.

proposed converter [P] and the converters suggested in [19], [25], and [26]. Therefore, for comparison, the emphasis is given to the topologies discussed in [21], [22], and [23] and a detailed comparison of these topologies is carried out concerning the proposed converter [P].

To produce a 5-level single-phase ac output voltage, the converter suggested in [25] requires two inductors each of value 3mH to limit the spikes in the source current. Further, the switch count of the converter is more which increases the value of TSV appearing across the switch string and decreases its power density. The soft charging inductor is reduced to one in [19] and the value of the inductor is 5μH. The switches included in the suggested converter have reduced values of *PIV*. Due to the reduction in *PIV*, the *TSV* across the switch string is reduced. However, the switch count of the suggested converters is more which decreases its power density and increases cost. To reduce switch count, a 7-level converter topology is suggested in [26]. The value of the inductor included in the soft switching circuit is 33μH. A reduction of 50% in the peak value of source current is achieved during the charging of capacitors. However, to produce a 7-level single-phase ac output voltage, the converter suggested in [26] converter still requires 11 switches. To further reduce the switch count, the proposed converter [P] requires only 8 switches to produce a 7-level single-phase ac output voltage. The value of the inductor included in the soft-switching circuit is 350μH, which can achieve a reduction of 60% in the magnitudes of current spikes appearing in the source current.

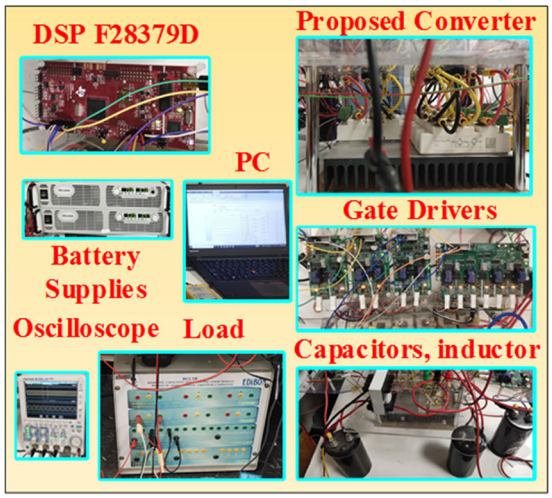
Due to the use of a reduced number of switches, a lower number of gate drivers are required to produce to provide the gate pulses. This signifies an appreciable improvement in the power density of the converter. The proposed converter [P] requires reduced switches as compared to the converter topologies discussed in [19], [25], and [26]. Therefore, the proposed converter has a high power density as compared to converters discussed in [25] and [26].

The validation for the performance of the converters suggested in the literature is carried out with the help of experimental results. The power rating of the converter suggested in [25] is 160W, while almost identical power ratings of converters equal to 1kW are used in [19] and [26] and the proposed converter [P]. The converter discussed in [25] and [26] are operated at a switching frequency of 20kHz and 10kHz while the proposed converter [P] is operated at a switching frequency of 50Hz. The efficiencies of the converter suggested in [19], [25], and [26] and the proposed converter [P] are high as compared to the converters suggested in [13], [14], [15], [16], [17], [18], [20], [21], [22], [23] and [24] due to the use of a soft charging circuit. The converter suggested in [25] offers the highest efficiency of 97.6% at a rated load of 160 W, while the efficiency of the proposed converter [P] is 97.5% at a rated load of 1 kW.

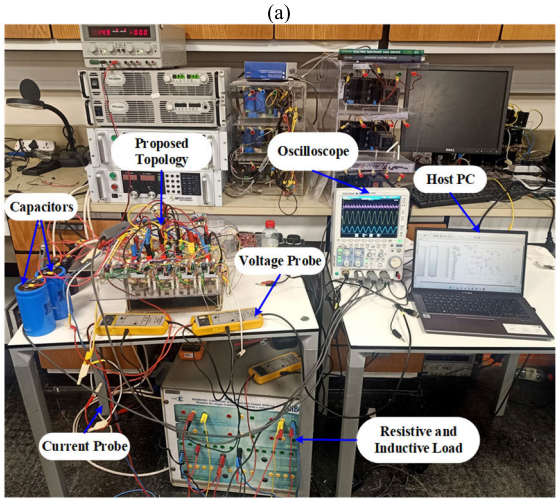
V. EXPERIMENTAL RESULTS

To validate the operation of the proposed 7-level SC-MLI configuration with soft charging operation, a laboratory prototype having a power of 1kW shown in Fig. 10 is used. Fig. 10(a) shows the various elements of the experimental setup while Fig. 10(b) shows the actual view of the experimental setup. The level-shifted PWM technique is used to generate gate pulses required for firing the switches. The digital signal processor (DSP) 28379D Launchpad is used for pulse generation. The switching frequency of the converter is maintained at 5kHz. The parameters of various components of the proposed converter like capacitors, switches and soft charging inductors are included in the experimental setup and are listed in Table 3. To ensure the soft charging of the capacitors included in the proposed 7-level SC-MLI, the waveforms for different conditions are included in the experimental results.

Fig.11 shows the waveforms of the proposed 7-level converter with resistive plus inductive (R-L) load connected at



(a)



(b)

FIGURE 10. Laboratory prototype of the proposed 7-level SC-MLI. (a) Elements of the experimental setup. (b) Actual view of the experimental setup.

TABLE 3. Details of experimental prototype.

Key Components	
Switches	G60N100 IGBT (V_{CE} =1000V, I_C = 60 A, R_S =42mΩ)
Capacitor	B437*3A5398M6 (450V, 3900μF and R_c=50mΩ)
Inductor	L_c= 100μH, R_L=0.11Ω
DSP Controller	TIC 2000 (TMS320F28379)
Gate Driver	GDA-2A4S1
DC Power Supply	TDK Lambda GEN300-11
Resistive + Inductive loads	Two sets of 100Ω-100mH
Input DC Source Voltage	100V
Output Voltage	150 V (peak)
Fundamental/Switching Frequency	50Hz/5kHz

the output of the converter. The effect of the soft charging inductor is not considered i.e. $L_c = 0\mu$H. From this figure, it is observed that for the dc input is 100 V, the measured output voltage is included in seven voltage levels, with the magnitude of each level being equal to 0.5 times the voltage input (100 V). The results are captured for the modulation

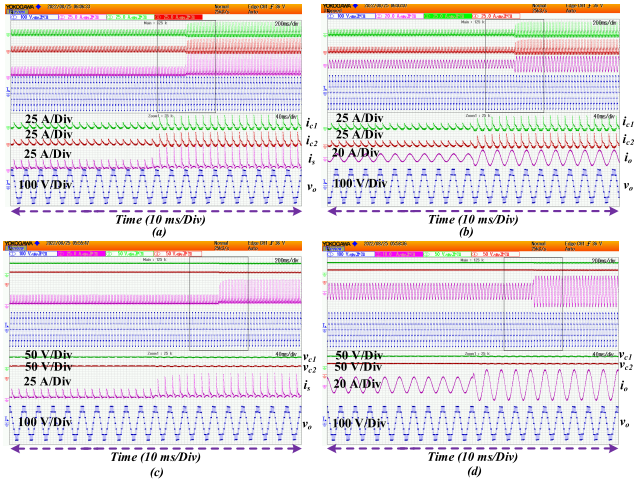


FIGURE 11. Waveforms of (a) Capacitor currents (i_{c1} and i_{c2}), source current (i_s), and load voltage (v_o). (b) Capacitor currents (i_{c1} and i_{c2}), load current (i_o), and load voltage (v_o). (a) Capacitor voltages (v_{c1} and v_{c2}), source current (i_s), and Output voltage (v_o). (a) Capacitor voltages (i_{c1} and i_{c2}), load current (i_s), and Output voltage (v_o) for R-L load with $L_c = 0\mu$H.

index, m = 1. The peak value of the output voltage of the 7-level SC-MLI is 150 V which validates the voltage gain of 1.5.

Fig. 11 also shows the waveforms of capacitor currents (i_{c1} and i_{c2}), capacitor voltages (v_{c1} and v_{c2}), source current (i_s), load current (i_o), and output ac voltage (v_o). These results are captured for R-L load and the effect of the soft charging circuit is not considered. At time instant, t=0s, the *R-L* load connected across the output of the SC-MLI with $R_{Load} = 100\Omega$ and $L_{Load} = 200$mH. The magnitude of current spikes in i_{c1}, i_{c2} and i_s is 15A, 16A and 30A, respectively which can be noted from Fig.11(a). At time instant, t = 0.5, the step variation in power demanded by load takes place and R-L load is changed to $R_{Load} = 50\ \Omega$ and $L_{Load} = 100$ mH. The magnitude of current spikes in i_{c1} and i_{c2} and becomes 26A, 29A and 57A, respectively. Fig. 10(b) shows the waveforms of Capacitor currents (i_{c1} and i_{c2}), load current (i_o), and output ac voltage (v_o). The rms value of load current at time $t = 0$ is 5 A. At time $t = 0.5$ s, the magnitude output current of SC-MLI becomes 10A. Fig. 11(c) shows the waveforms of capacitor voltages, v_{c1} and v_{c2}, output voltage, v_o along with source current, i_s. The maximum voltage appearing across each capacitor, C_3 and C_4 is 50V. Fig. 11(d) shows the waveforms of capacitor voltages, v_{c1} and v_{c2}, output voltage, v_o along with source current, and output current of SC-MLI.

Fig. 12 shows the effect of connecting the soft charging inductor, L_c in the charging path of capacitors, C_3 and C_4. The value of L_c connected in the charging path is $L_c = 200\mu$H. From Fig. 12(a), it is observed that magnitudes of current spikes in i_{c1}, i_{c2} and i_s are 8 A, 9 A and 17 A, respectively. At time instant, $t = 0.5$s, the magnitude of current spikes in i_{c1}, i_{c2} and i_s becomes 13 A, 15 A and 29 A, respectively. The effect of connecting the soft charging inductor, L_c on the waveforms of v_{c1} and v_{c2}, and load current (i_o) is shown in Fig. 12(b), 12(c) and 12(d), respectively.

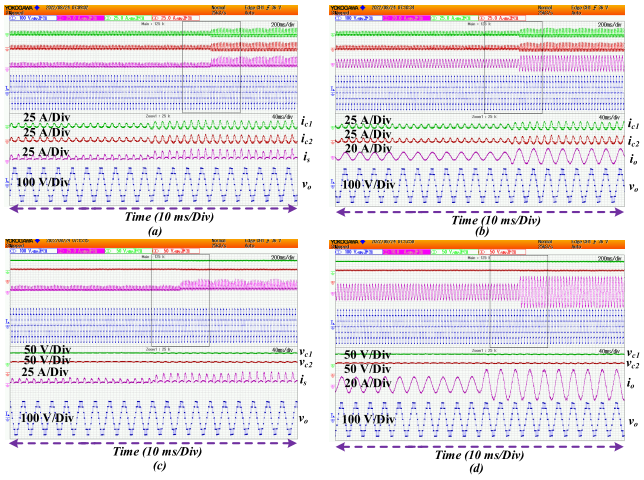


FIGURE 12. Waveforms of (a) Capacitor currents (i_{c1} and i_{c2}), source current (i_s), and load voltage (v_o). (b) Capacitor currents (i_{c1} and i_{c2}), load current (i_o), and load voltage (v_o). (a) Capacitor voltages (v_{c1} and v_{c2}), source current (i_s), and Output voltage (v_o). (a) Capacitor voltages (i_{c1} and i_{c2}), load current (i_s), and Output voltage (v_o) for R-L load including soft charging circuit, $L_c = 200\mu$H.

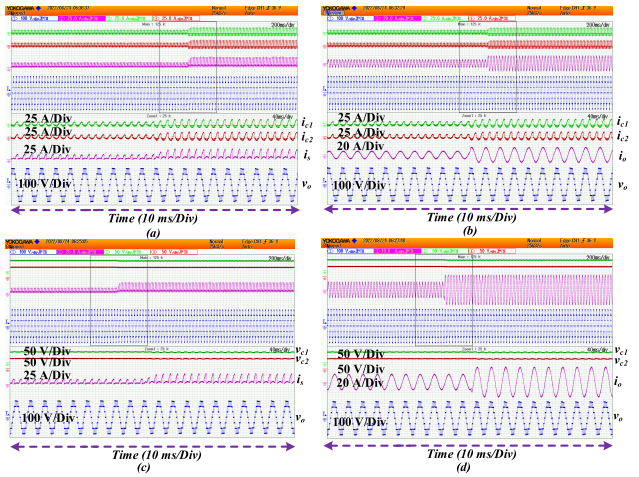


FIGURE 13. Waveforms of (a) Capacitor currents (i_{c1} and i_{c2}), source current (i_s), and load voltage (v_o). (b) Capacitor currents (i_{c1} and i_{c2}), load current (i_o), and load voltage (v_o). (a) Capacitor voltages (v_{c1} and v_{c2}), source current (i_s), and Output voltage (v_o). (a) Capacitor voltages (i_{c1} and i_{c2}), load current (i_s), and Output voltage (v_o) for R-L load including soft charging circuit, $L_c = 350\mu$H.

Fig. 13 shows the effect of connecting the soft charging inductor in the charging path of capacitors, C_3 and C_4. The value of L_c connected in the charging path is $L_c = 350\mu$H. From Fig. 13(a), it is observed that magnitudes of current spikes in i_{c1}, i_{c2} and i_s are 5 A, 6 A and 12 A, respectively. At time instant, t = 0.5s, the magnitude of current spikes in i_{c1}, i_{c2} and i_s becomes 9 A, 10 A and 23 A, respectively. The effect of connecting the soft charging inductor, L_c on the waveforms of v_{c1} and v_{c2}, and load current (i_o) is shown in Fig. 13(b), 13(c) and 13(d), respectively.

From the waveforms shown in Figs. 12 and 13, it is observed that a significant reduction occurs in the magnitudes of spikes appearing in source and capacitor current on the addition of soft charging inductor, L_c. This leads to a reduction of ripple losses appearing in the capacitors.

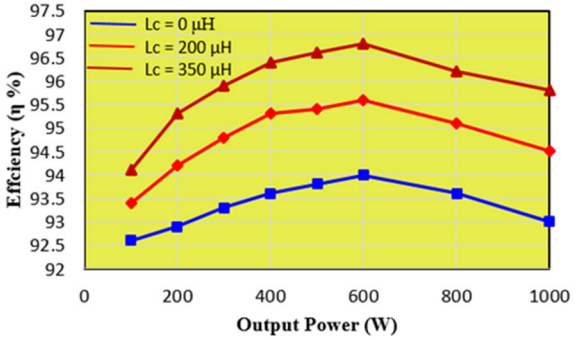


FIGURE 14. Effect of variation in the value of soft charging inductance, L_c on (a) Experimental efficiency.

This overshadows the cost of the addition of a soft charging circuit in the charging path. This feature makes the proposed SC-MLI a viable option to be used in high-power applications compared to the conventional 7-level SC-MLI reported in the literature.

The experimental efficiency of the proposed ANPC-based 7-level SC-MLI is plotted with the help of experimental results. The experimental and theoretical efficiency of the proposed converter with and without a soft charging inductor, L_c is shown in Fig. 14. From Fig.14, it is observed that for the low value of power demanded by the load, the experimental efficiency similar to the efficiency evaluated using simulation approach of the proposed converter with and without soft charging circuits are nearly equal. However, for a rated load of 1000 W, the experimental efficiency of the converter with $L_c = 0\mu$H is 93%, while for $L_c = 200\mu$H, the efficiency of the converter is 94.5% and for $L_c = 350\mu$H, the efficiency of the proposed 7-level converter is evaluated as 95.8%. The experimental efficiency shown in Fig.14 is observed to be slightly lesser than the simulation efficiency shown in Fig.7. This discrepancy in the two efficiencies occurs due to (i) nonideal behaviour of active and passive components, (ii) mismatch in effective internal resistance of semiconductor devices in experimental study. The mismatch in internal resistance occurs due to internal and parasitic components of semiconductor devices.

VI. CONCLUSION

In this paper, an Active-neutral-point-clamped (ANPC) based SC-MLI converter topology is proposed. The proposed converter produces a 7-level single-phase ac output voltage with a voltage gain of 1.5. A detailed comparison of the proposed and the state-of-the-art 7-level SC-MLIs is carried out. From this comparison, it is concluded that the proposed converter requires switches having less value of voltage stresses and the switch count of the proposed converter is less. Further, a soft charging circuit including a parallel combination of inductor and diode is used in the charging path of switched capacitors in the proposed 7-level SC-MLI. This circuit ensures the reduction in magnitudes of spikes appearing in the source and capacitor currents. The effectiveness of the soft charging method is tested on a laboratory prototype having a power rating of 1 kW. For the value of an inductor, $L_c = 200\mu$H, the

magnitude of spikes in the source reduces from 57 A to 29 A (around 50% reduction), while for the value of $L_c = 350\mu$H, the magnitude of current spikes further reduces from 57A to 23A (around 60% reduction). This shows the effectiveness of the soft charging method used in the proposed 7-level SC-MLI. This feature reduces the ripple losses in the capacitors and outweighs the extra cost of a soft charging circuit. For $L_c = 350\mu$H, the efficiency of the converter evaluated at a rated load demand of 1kW is observed to be $\eta = 97.5\%$ while for $L_c = 0\ \mu$H, the efficiency of the converter is $\eta = 94.6\%$.

DECLARATION OF CONFLICT OF INTEREST

The authors declare that they have no conflict of interest that could have appeared to influence the work reported in this paper.

ACKNOWLEDGMENT

This publication, was made possible by NPRP grant # [13S-0108-200028] from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors. The APC for this manuscript is funded by the Qatar National Library, Doha, Qatar.

REFERENCES

[1] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-phase split-source inverter (SSI): Analysis and modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7451–7461, Nov. 2016, doi: 10.1109/TPEL.2015.2513204.

[2] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019, doi: 10.1109/TPEL.2018.2890649.

[3] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage source multilevel inverters with reduced device count: Topological review and novel comparative factors," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2720–2747, Mar. 2021, doi: 10.1109/TPEL.2020.3011908.

[4] S. Kundu, S. Panda, and S. Banerjee, "Fulfillment of some important voltage harmonic standards in a FPGA controlled CHB multilevel inverter utilizing improved SHM-PAM technique," *IEEE Trans. Ind. Appl.*, early access, May 16, 2023, doi: 10.1109/TIA.2023.3276354.

[5] D. Krishnachaitanya and A. Chitra, "Quantitative analysis of asymmetric multilevel inverters with reduced device count from reliability and cost function perspective—A review," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11068–11086, Oct. 2021, doi: 10.1109/TPEL.2021.3071375.

[6] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010, doi: 10.1109/TIE.2010.2043039.

[7] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012.

[8] S. A. Saleh, "Maximum resolution based method for balancing capacitor voltages in 7-level single phase flying-capacitor wavelet modulated inverters," *IEEE Trans. Ind. Appl.*, vol. 59, no. 4, pp. 5019–5031, Aug. 2023, doi: 10.1109/TIA.2023.3258425.

[9] G. Kampitsis, E. I. Batzelis, A. Kolokasis, E. Matioli, and B. C. Pal, "A generalized phase-shift PWM extension for improved natural and active balancing of flying capacitor multilevel inverters," *IEEE Open J. Power Electron.*, vol. 3, pp. 621–634, 2022, doi: 10.1109/OJPEL.2022.3209540.

[10] A. Taghvaie, J. Adabi, and M. Rezanejad, "A multilevel inverter structure based on a combination of switched-capacitors and DC sources," *IEEE Trans. Ind. Informat.*, vol. 13, no. 5, pp. 2162–2171, Oct. 2017, doi: 10.1109/TII.2017.2710265.

[11] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.

[12] B. P. Reddy and S. Keerthipati, "A multilevel inverter configuration for an open-end-winding pole-phase-modulated-multiphase induction motor drive using dual inverter principle," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3035–3044, Apr. 2018, doi: 10.1109/TIE.2017.2750626.

[13] S. R. Raman, K. W. E. Cheng, and Y. Ye, "Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5937–5948, Jul. 2018, doi: 10.1109/TPEL.2017.2742525.

[14] J. Liu, J. Wu, and J. Zeng, "Symmetric/asymmetric hybrid multilevel inverters integrating switched-capacitor techniques," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1616–1626, Sep. 2018, doi: 10.1109/JESTPE.2018.2848675.

[15] P. Manoj, A. Kirubakaran, and V. T. Somasekhar, "An asymmetrical dual quasi-Z-source based 7-level inverter for PV applications," *IEEE Trans. Energy Convers.*, vol. 38, no. 2, pp. 1097–1107, Jun. 2023, doi: 10.1109/TEC.2022.3222498.

[16] J. Liu, X. Zhu, and J. Zeng, "A seven-level inverter with self-balancing and low-voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 685–696, Mar. 2020, doi: 10.1109/JESTPE.2018.2879890.

[17] M. J. Sathik, N. Sandeep, and F. Blaabjerg, "High gain active neutral point clamped seven-level self-voltage balancing inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 11, pp. 2567–2571, Nov. 2020, doi: 10.1109/TCSII.2019.2955318.

[18] S. S. Lee, Y. Bak, S.-M. Kim, A. Joseph, and K.-B. Lee, "New family of boost switched-capacitor seven-level inverters (BSC7LI)," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10471–10479, Nov. 2019, doi: 10.1109/TPEL.2019.2896606.

[19] Y. C. Fong, K. W. E. Cheng, and S. R. Raman, "A modular concept development for resonant soft-charging step-up switched-capacitor multilevel inverter for high-frequency AC distribution and applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5975–5985, Oct. 2021, doi: 10.1109/JESTPE.2020.3043126.

[20] W. Lin, J. Zeng, B. Fu, Z. Yan, and J. Liu, "Switched-capacitor based seven-level boost inverter with reduced devices," *CSEE J. Power Energy Syst.*, early access, Jun. 25, 2021, doi: 10.17775/CSEEJPES.2020.02620.

[21] S. S. Lee, C. S. Lim, Y. P. Siwakoti, and K.-B. Lee, "Hybrid 7-level boost active-neutral-point-clamped (H-7L-BANPC) inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 2044–2048, Oct. 2020, doi: 10.1109/TCSII.2019.2946860.

[22] L. Ren, L. Zhang, L. Wang, and S. Dai, "Capacitor voltage regulation strategy for 7-level single DC source hybrid cascaded inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5773–5784, Oct. 2022, doi: 10.1109/JESTPE.2022.3172146.

[23] S. S. Lee and K.-B. Lee, "Dual-T-type seven-level boost active-neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6031–6035, Jul. 2019, doi: 10.1109/TPEL.2019.2891248.

[24] T. Roy, M. W. Tesfay, B. Nayak, and C. K. Panigrahi, "A 7-level switched capacitor multilevel inverter with reduced switches and voltage stresses," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 12, pp. 3587–3591, Dec. 2021, doi: 10.1109/TCSII.2021.3078903.

[25] S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo, and K.-B. Lee, "Switched-capacitor-based five-level T-type inverter (SC-5TI) with soft-charging and enhanced DC-link voltage utilization," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13958–13967, Dec. 2021, doi: 10.1109/TPEL.2021.3088443.

[26] R. Barzegarkhoo, S. S. Lee, S. A. Khan, Y. P. Siwakoti, and D. D. Lu, "A novel generalized common-ground switched-capacitor multilevel inverter suitable for transformerless grid-connected applications," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10293–10306, Sep. 2021, doi: 10.1109/TPEL.2021.3067347.

[27] S. S. Lee, C. S. Lim, Y. P. Siwakoti, and K.-B. Lee, "Dual-T-type five-level cascaded multilevel inverter with double voltage boosting gain," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9522–9529, Sep. 2020, doi: 10.1109/TPEL.2020.2973666.

[28] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A single DC source cascaded seven-level inverter integrating switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7184–7194, Nov. 2016, doi: 10.1109/TIE.2016.2557317.

[29] V. Anand and V. Singh, "A 13-level switched-capacitor multilevel inverter with single DC source," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 1575–1586, Apr. 2022, doi: 10.1109/JESTPE.2021.3077604.
[30] H. Matsumori, T. Shimizu, X. Wang, and F. Blaabjerg, "A practical core loss model for filter inductors of power electronic converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 29–39, Mar. 2018, doi: 10.1109/JESTPE.2017.2761127.
[31] P. Rasilo, A. Salem, A. Abdallh, F. De Belie, L. Dupré, and J. A. Melkebeek, "Effect of multilevel inverter supply on core losses in magnetic materials and electrical machines," *IEEE Trans. Energy Convers.*, vol. 30, no. 2, pp. 736–744, Jun. 2015, doi: 10.1109/TEC.2014.2372095.
[32] M. Sztykiel, S. Fletcher, P. Norman, S. Galloway, and G. M. Burt, "Electro-thermal analysis of power converter components in low-voltage DC microgrids for optimal protection system design," *IEEE Trans. Smart Grid*, vol. 9, no. 6, pp. 5843–5853, Nov. 2018, doi: 10.1109/TSG.2017.2697686.
[33] Y. Tang, L. Ran, O. Alatise, and P. Mawby, "Capacitor selection for modular multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3279–3293, Jul. 2016, doi: 10.1109/TIA.2016.2533620.
[34] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014, doi: 10.1109/TIA.2014.2308357.

SHIRAZUL ISLAM received the B.E. degree in electrical and the M.Tech. degree in power system and electrical drives from Aligarh Muslim University, Aligarh, India, in 2008 and 2010, respectively, and the Ph.D. degree from the Indian Institute of Technology Kanpur (IIT Kanpur), India, in 2021. Currently, he is a Research Associate with the Department of Electrical Engineering, Qatar University, Doha, Qatar. He was also a Senior Research Fellow with the Department of Electrical Engineering, IIT Kanpur. He was also a Lecturer with the Department of Electrical Engineering, Aligarh Muslim University, in 2010. He was an Assistant Professor with the Department of Electrical and Electronics Engineering, Teerthanker Mahaveer University, India. He has been a topper student in his master's course. He received the Best Renewable Energy Research Project Award from Tarsheed, Qatar, in June 2022. He has published several papers in IEEE TRANSACTIONS, various reputed journals and international conferences. He is a life member of IETE and a member of the System Society of India. His research interests include electric vehicles, multilevel converters, high gain DC/DC converters, the hierarchical control of AC and DC microgrids, sliding mode, and the consensus control of microgrids.

MARIF DAULA SIDDIQUE (Member, IEEE) received the B.Tech. and M.Tech. degrees in electrical engineering from Aligarh Muslim University (AMU), in 2014, and 2016, respectively, and the Ph.D. degree in power electronics from the Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia, in 2021. He was a Research Assistant with the Department of Electrical Engineering, Qatar University, Doha, Qatar. He was a Postdoctoral Researcher with the Energy Harvesting and Mechatronics Research Laboratory, Department of Mechanical Engineering, Virginia Tech, USA, from October 2021 to May 2022. He is currently a Research Fellow with the National University of Singapore, Singapore. He received the Best Paper Award at IEEE GUCON 2020 and ICRP 2020. He is an Early Career Editorial Board (ECEB) Member of *E-Prime and Building and Environment*. He was included in the list of the top 2% highly cited scientists by Stanford University, in 2021 and 2022. He served as a lead editor for a special issue of different journals. He has published more than 80 journals and conference papers. His research interests include power electronics systems for renewable energy, step-up power electronics converters (DC/AC and DC/DC), multilevel inverter topologies and their control, fault detection, diagnosis, and the fault-tolerant operation of power converters.

MD. REYAZ HUSSAN (Student Member, IEEE) received the B.Tech. and M.Tech. degrees in electrical engineering and instrumentation and control from Aligarh Muslim University, Aligarh, India, in 2014 and 2016, respectively. He is currently a Research Scholar with the Department of Electrical Engineering, Aligarh Muslim University. His research interests include multilevel inverters and their control, photovoltaic systems, and multilevel inverter for solar PV applications.

ATIF IQBAL (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in engineering (power system and drives) from Aligarh Muslim University (AMU), Aligarh, India, in 1991 and 1996, respectively, the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2006, and the D.Sc. degree (Habilitation) in control, informatics, and electrical engineering from the Gdańsk University of Technology, in 2019. He is currently a Full Professor with the Department of Electrical Engineering, Qatar University, Doha, Qatar, and a former Full Professor with the Department of Electrical Engineering, AMU. He has been a Lecturer with the Department of Electrical Engineering, AMU, since 1991, where he was a Full Professor, until August 2016. He has published widely in international journals and conferences on his research findings related to power electronics, variable speed drives, and renewable energy sources. He has authored or coauthored more than 500 research articles and four books and several chapters in edited books. He has supervised several large research and development projects worth more than multi-million USD. He is a fellow IET and IE. He was a recipient of the Maulana Tufail Ahmad Gold Medal for standing first at the B.Sc.Engg. (electrical) exams from AMU, in 1991. He was also a recipient of the Outstanding Faculty Merit Award (2014–2015) and the Research Excellence Awards at Qatar University, in 2015 and 2019. He has received several best research papers awards, e.g., IEEE ICIT-2013, IET-SEISCON-2013, SIGMA 2018, IEEE CENCON 2019, IEEE ICIOT 2020, ICSTEESD-20, Springer ICRP 2020, and IEEE GUCON 2021. He has also received the Gold Medal for his B.Sc. degree. He is the Vice-Chair of the IEEE Qatar Section. He is also an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE ACCESS and the Editor-in-Chief of the *Journal of Electrical Engineering* (I'manager). He was a former Associate Editor of the IEEE TRANSACTIONS ON INDUSTRY APPLICATION and a former Guest Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS. His research interests include smart grid, complex energy transition, active distribution networks, electric vehicles drivetrain, sustainable development and energy security, distributed energy generation, and multiphase motor drive systems.