**RESEARCH ARTICLE**

# A Highly Uniform Luminance and Low-Flicker Pixel Circuit and Its Driving Methods for Variable Frame Rate AMOLED Displays

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**ABSTRACT** This paper proposes a 7T2C pixel circuit for active-matrix organic light-emitting diode (AMOLED) displays using low-temperature poly-crystalline silicon (LTPS) thin-film transistors (TFTs) with two key features: high luminance uniformity and low flicker at a wide range of variable frame rates (VFRs). To achieve a high luminance uniformity, the proposed pixel circuit simultaneously compensates for the threshold voltage variation and subthreshold slope variation of the driving TFT with a sufficient compensation time regardless of the frame rate. Furthermore, flicker is reduced by employing a ramping reference voltage and current blocking method, which reduces the effect of the leakage current of TFTs and OLED capacitance, respectively. Therefore, these techniques reduce spatial emission current errors (ECEs) and temporal ECEs, enabling the circuit to be used in the VFR from 15 Hz to 360 Hz. The proposed pixel circuit was verified with unit sub-pixels designed for a 14-inch 3840 × 2160 (4K) AMOLED display. The worst-case spatial ECEs of the proposed 7T2C pixel circuit at the frame rate of 360 Hz were measured as +4.1/−4.2 and +1.2/−1.1 LSB at the 255th and 15th gray levels, respectively. They show better luminance uniformity compared to those of the conventional 7T1C pixel circuit, which were measured as +6.1/−8.9 and +3.6/−3.6 LSB. Furthermore, the worst-case temporal ECEs at the frame rate of 15 Hz that shows flicker performance was measured as −0.3 and −3.2 LSB at the 15th and 255th gray levels, respectively, and they are better than those of the 7T1C pixel circuit, which show 11.2 and 2.41 LSB.

**INDEX TERMS** AMOLED, variable frame rate displays, low-temperature poly-crystalline silicon (LTPS), pixel circuit.

## I. INTRODUCTION

Recently, active-matrix organic light-emitting diode (AMOLED) displays using low-temperature poly-crystalline silicon (LTPS) thin-film transistors (TFTs) have been rapidly growing their market in gaming monitors due to their fast response, low power consumption, and high contrast ratio [1], [2]. In gaming display systems, the graphics processing unit (GPU) produces the display data according to its frame rate and sends them to the display panel. However, when the

The associate editor coordinating the review of this manuscript and approving it for publication was Ludovico Minati [ID].

frame rate of the GPU suddenly changes, the images of the previous and current frames are simultaneously displayed on the monitor, which is known as an image tearing problem. The image tearing becomes severe when a game with much display data to be processed is running, which causes a difference in frame rates between the GPU and display panel. To address this problem, a variable frame rate (VFR) driving method, which synchronizes the frame rates of the GPU and display panel, has been studied [3], [4], [5], [6]. However, although the VFR applications have advantages with the fast response time at high frame rates and low power consumption at low frame rates, those VFR driving methods

have two problems when it is applied to AMOLED display panels using LTPS TFTs: low luminance uniformity and high flicker.

The luminance uniformity issue is derived from the threshold voltage variation ($\Delta V_{th}$) and subthreshold slope variation ($\Delta SS$) of the driving TFT resulting from the randomly formed grain boundaries in an LTPS. Therefore, emission currents of each pixel circuit are different, although the same data voltage is applied, resulting in spatial emission current error (SECEs). Furthermore, since the luminance of OLED is proportional to the emission current of pixel circuits, SECE directly affects the luminance uniformity. The pixel circuits with the voltage programming methods in [7], [8], and [9] compensated for $\Delta V_{th}$ of the driving TFT during the compensation time of the pixel circuit by applying a data voltage to the diode-connected driving TFT. However, as the frame rate of the display panel increases, the compensation time decreases due to the limitation of 1-H time (1-row line time) - consequently, the poor $\Delta V_{th}$ compensation results in increased spatial ECEs that decrease the luminance uniformity. The pixel circuit in [10] secured sufficient compensation time regardless of the frame rate to compensate for $\Delta V_{th}$. However, it does not compensate $\Delta SS$ of the driving TFT, resulting in low luminance uniformity. Another pixel circuit in [11] compensated not only $\Delta V_{th}$ using two parallel capacitors and $\Delta SS$ using the subthreshold current to flow from the source to the gate nodes of the driving TFT. However, its compensation performance is limited by the ratio of the two capacitance values.

Flicker, fluctuation in the pixel circuit's emission current during the emission time is caused by switching TFTs' leakage current ($I_{OFF}$). Moreover, the pixel circuit requires charging the capacitance of the OLED to allow the emission current to flow through the OLED. Emission current fluctuations, especially at low gray levels corresponding to currents lower than 1nA, depend on the charging time of the capacitance of OLED devices. Therefore, the emission current at the start and end point of the emission phase is different, resulting in temporal ECEs (TECEs). Since the human eye perceives the emitted light by integrating it for several tens of milliseconds [12], the TECEs may not be recognized as flickers during the emission phase. However, TECEs become an issue when the frame rate is lower than the integration rate of the human eye. Furthermore, in VFR driving, where frame rates vary significantly, the average (integrated) emission current per frame rate varies significantly, causing severe flicker on display. To solve the flicker problem, pixel circuits in [13] and [14] adopt additional capacitors and switching TFTs at the gate node of the driving TFT to reduce the $I_{OFF}$ of switching TFTs. However, the luminance uniformity degraded because of insufficient compensation time at a high frame rate. Similarly, the pixel circuits using low-temperature poly-crystalline silicon and oxide (LTPO) TFTs use oxide TFTs that have lower $I_{OFF}$s for switching TFTs instead of LTPS TFTs [15], [16]. However, it requires additional fabrication process steps

that increase manufacturing costs [17]. Furthermore, since these pixel circuits do not have any compensation method for the charging time of the OLED, the flicker problem could be severe, especially at low gray levels.

Nevertheless, research still needs to be done on developing the pixel circuits and driving methods to achieve high luminance uniformity and low-flicker performance at a wide range of frame rates in AMOLED displays using LTPS TFTs. This paper proposes the 7T2C pixel with the novel driving method to achieve high luminance uniformity and low flicker at a wide range of VFRs from 15 Hz to 360 Hz. The proposed pixel circuit achieves high luminance uniformity by simultaneously compensating $\Delta V_{th}$ and $\Delta SS$ of the driving TFT with a sufficient compensation time regardless of the frame rate. Furthermore, it achieves low flicker by minimizing the influence of the $I_{OFF}$ in switching TFTs and the OLED capacitance by employing a ramping reference voltage ($V_{REF}$) and current blocking method. The proposed pixel circuit, designed for a 14-inch 4K AMOLED display, was fabricated and verified through the measurement, then analyzed and compared with state-of-the-art works. Sections II and III, respectively, describe the operation principle and implementation of the proposed pixel circuit with the driving methods. Section IV presents the measurement results of the TFT devices and the proposed pixel circuit in the fabricated test bench, and it is compared with the previously reported pixel circuits. Finally, the conclusions are given in Section V.

## II. PROPOSED PIXEL CIRCUIT AND DRIVING METHODS

Fig. 1(a) and (b) respectively show the schematic and timing diagram of the proposed 7T2C pixel circuit located in the n-th row line and the m-th column line of the display panel. The proposed circuit consists of a driving TFT (MD), six switching TFTs (M1-M6), and two capacitors (C1 and C2) and operates in five phases as follows.

In the initial phase (*init*), the *scan[n-1]*, *scan[n]*, and *em[n]* signals are low to turn on M1, M3, M4, M5, and M6, whereas the *em[n-1]* signal is high to turn off M2. Accordingly, node B is initialized to ELVDD voltage ($V_{ELVDD}$), whereas REF voltage ($V_{REF}$) initializes the voltage of node A, node C, and the anode of the OLED.

In the $\Delta V_{th}$ compensation phase (*comp*), the *scan[n-1]* and *scan[n]* signals are low to turn on M1, M3, M5, and M6, whereas the *em[n-1]* and *em[n]* signals are high to turn off M2 and M4, providing $V_{REF}$ to nodes A and C. Since M4 is turned off, the proposed pixel circuit discharges C1 and C2 through MD by lowering the voltage at node B ($V_{node,B}$). There have been studies on compensating for variation in the threshold voltage ($\Delta V_{th}$) of driving TFTs in displays. These studies have the diode-connection method [7], [8], [9] or the source-follower method [10]. They have found that the gate-to-source voltage ($|V_{GS}|$) applied to the driving TFT can reach its $V_{th}$ during the compensation phase. However, in displays with high pixel density, each pixel requires a small amount of current, and MD operates in the sub-threshold current
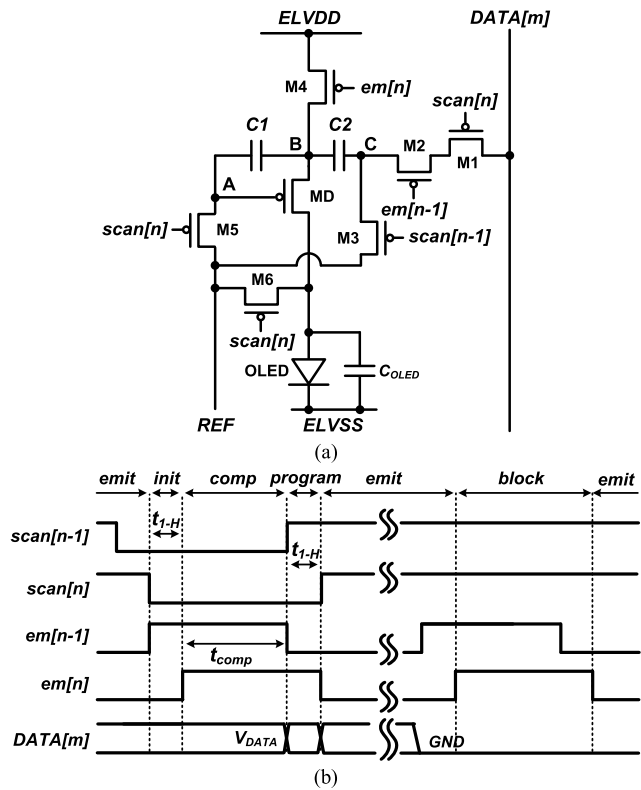
**FIGURE 1.** (a) Schematic diagram and (b) timing diagram of the proposed 7T2C pixel circuit in the n-th row and m-th column of the display panel.
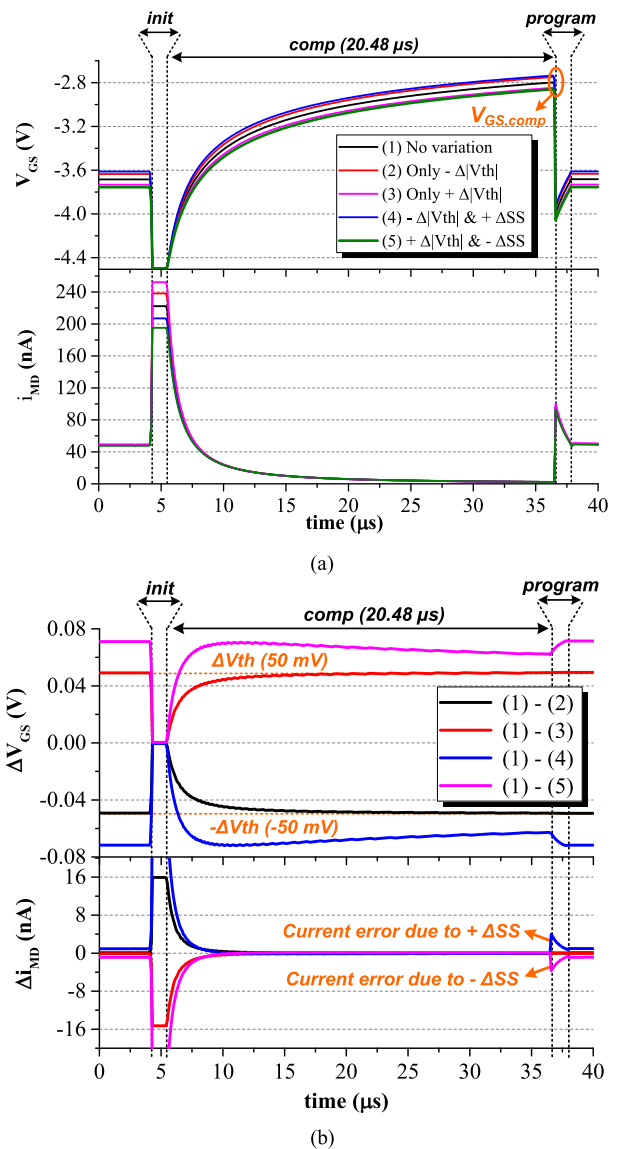


**FIGURE 2.** Transient simulation results of the proposed pixel circuit. (a) $V_{GS}$ and drain current of MD and (b) their deviations. $\Delta V_{th}$ is applied to ±50 mV and $\Delta$SS is applied to ±10mV/dec.

region where TFTs exhibit non-ideal behavior. Accordingly, the $|V_{GS}|$ of MD has to be settled to a much lower voltage than the $|V_{th}|$. Therefore, in the *comp*, $V_{node,B}$ decreases from $V_{ELVDD}$ to $V_{REF} + V_{GS,comp}$, where $V_{GS,comp}$ is the $V_{GS}$ of MD ($V_{GS,MD}$) at the end of the *comp*. In *comp*, the drain current deviations of MD due to $\Delta V_{th}$ and $\Delta$SS at $V_{GS,comp}$ are compensated due to the following equation

$$V_{GS,comp} = \frac{1}{C_1 + C_2} \int_0^{t_{comp}} i_{MD}(t)\,dt, \qquad (1)$$

where $i_{MD}$ is the drain current of MD. If $|V_{th}|$ of MD is smaller or SS of MD is larger than typical values, MD generates a large $i_{MD}$ at the beginning of the *comp*. As a result, $V_{node.B}$ discharged faster than the typical case, further increasing $V_{GS,comp}$. Therefore, by securing a sufficient time in *comp*, the voltage corresponding $\Delta V_{th}$ and $\Delta$SS of MD are stored in $V_{GS,comp}$ to generate the specific amount of current, which is independent of its $\Delta V_{th}$ and $\Delta$SS. Fig. 2 shows the transient simulation result of the proposed pixel circuit. During the *init* phase, since MD generates current according to its $V_{GS}$, which is $V_{ELVDD} - V_{REF}$, there is a large current error due to the $\Delta V_{th}$ and $\Delta$SS. However, during the *comp*, the $V_{GS}$ of MD increases, and the $\Delta V_{GS}$ gradually reaches a voltage corresponding to a point where $i_{MD}$ become same. When MD has only $\Delta V_{th}$ (red and black curves), its $\Delta V_{GS}$ settles to + 50 mV / − 50 mV which are specific amounts of $\Delta V_{th}$.

However, when MD has $\Delta V_{th}$ and $\Delta$SS, its $\Delta V_{GS}$ gradually increases or decreases according to $t_{comp}$. This is because unlike $V_{th}$, which has a specific voltage value, SS requires different voltages according to its $V_{GS}$ to reduce the drain current deviation ($\Delta i_{MD}$).

In the programming phase (*program*), the *scan[n]* and *em[n-1]* signals are low to turn on M1, M2, M5, and M6, whereas the *scan[n-1]* and *em[n]* signals are high to turn off M3 and M4, providing a DATA voltage ($V_{DATA}$) to node C. Since the voltage change from $V_{REF}$ to $V_{DATA}$ at node C is coupled and divided into node B due to a capacitive coupling effect of C1 and C2, the $V_{GS}$ of MD is programmed and can be expressed as

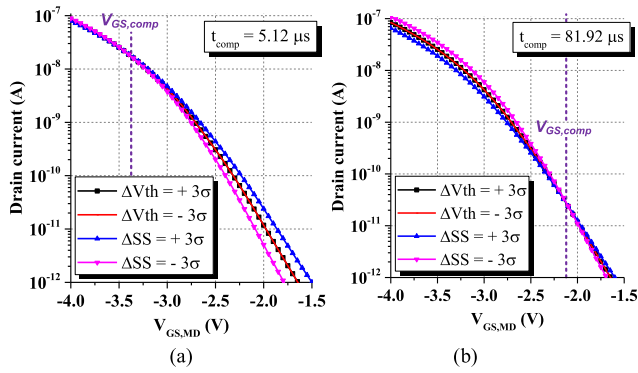$$V_{GS,MD} = V_{GS,comp} + V_{GS,data}, \qquad (2)$$

**FIGURE 3.** Simulated transfer curves of LTPS TFT after the comp phase with (a) $t_{comp}$ =5.12 $\mu$s, and (b) $t_{comp}$ =81.92 $\mu$s.

$$V_{GS,data} = \frac{C_2 \cdot (V_{DATA} - V_{REF})}{C_1 + C_2}, \qquad (3)$$

where $C_1$ and $C_2$ are the capacitance values of C1 and C2, respectively. Therefore, the proposed pixel circuit controls the emission current by adjusting the $V_{GS,MD}$ with $V_{GS,data}$. However, since $V_{GS,MD}$ is changed from $V_{GS,comp}$, $\Delta i_{MD}$ due to $\Delta$SS of MD occurs once again due to the characteristics of SS mentioned in the *comp* phase. Fig. 3(a) and (b) show the simulated transfer curve of MD after the *comp* phase, which illustrates that $\Delta i_{MD}$ increases when $V_{GS,MD}$ moves away from the $V_{GS,comp}$. Therefore, luminance uniformity at a high gray level is well controlled but not at a low gray level when $t_{comp}$ = 5.12 $\mu$s. On the other hand, in the case of $t_{comp}$ = 81.92 $\mu$s, which is a relatively long $t_{comp}$, luminance uniformity at a low gray level is improved at the expense of luminance uniformity at a high gray level. To solve this problem, it is necessary to compensate $i_{MD}$ again when the data voltage is applied. When the data voltage is applied, M6 is turned on, causing $i_{MD}$ to flow from node B to the REF line during 1-row line time ($t_{1-H}$), similar to the *comp* operation. Therefore, $V_{GS,MD}$ is changed from equation (2) to

$$V_{GS,MD} = V_{GS,comp} + V_{GS,data} + V_{GS,comp2}, \qquad (4)$$

$$V_{GS,comp2} = \frac{1}{C_1 + C_2} \cdot \int_0^{t_{1-H}} i_{MD} dt. \qquad (5)$$

Therefore, the error in $i_{MD}$ due to $\Delta$SS is compensated, similar to the operation described in equation (1), except that $t_{comp}$ is changed to $t_{1-H}$. As mentioned above, in Fig. 2(b), $\Delta i_{MD}$ rapidly increases at the beginning of the *program*, and this situation occurs when $\Delta$SS is applied to the driving TFT. However, due to the compensation at the *program* that is compensating for the $\Delta$SS, the $\Delta i_{MD}$ is decreased.

In the emission phase (*emit*), the *em[n-1]* and *em[n]* signals are low to turn on M2 and M4, whereas the *scan[n-1]* and *scan[n]* signals are high to turn off M1, M3, M5, and M6. As M2 is turned on, $V_{node,B}$ becomes

$$V_{node,B} = V_{ELVDD} - \Delta V_{ELVDD}, \qquad (6)$$

where $\Delta V_{ELVDD}$ is the IR-drop voltage on ELVDD. Since the voltage change at node B is coupled into node A due to C1, $\Delta V_{ELVDD}$ is compensated [18]. Therefore, the $V_{GS}$ of MD at *emit* follows the equation (4). As M4 is turned on, the emission current ($I_{OLED}$), which flows from ELVDD to OLED, is equal to the drain current of MD. Thus, $I_{OLED}$, which is in the sub-threshold region, can be expressed as

$$I_{OLED} = \frac{W}{L} C_{ox} K \exp(V_{GS,MD} - |V_{th.MD}|),$$
$$K = \frac{\eta \mu_{p.sub} q}{kT} \exp(\frac{q}{\eta kT})[1 - \exp(-\frac{q V_{DS}}{\eta kT})], \qquad (7)$$

where W/L, $C_{ox}$, $\mu_{p.sub}$, $k$, $T$, $q$, and $\eta$ are the channel width to channel length ratio, oxide capacitance, sub-threshold mobility of MD, Boltzmann constant, absolute temperature, electronic charge, and adjustment parameter, respectively [19]. Since $\Delta V_{th}$, $\Delta$SS, and $\Delta V_{ELVDD}$ are compensated due to the compensating operations, the proposed pixel circuit reduces spatial ECE, achieving high luminance uniformity of the display panel.

In the current blocking phase (*block*), the *scan[n-1]*, *scan[n]*, and *em[n]* signals are high to turn off M1, M3, M4, M5, and M6, blocking $I_{OLED}$ flowing from ELVDD to OLED, and then discharging the charges at the anode of the OLED through the OLED. As a result, the anode voltage of the OLED becomes the threshold voltage of OLED device ($V_{OLED,vth}$). The *block* plays a vital role in restoring the anode voltage of the OLED to be similar to the *init* phase while preventing the current flowing to the OLED, which improves the flicker performance. After the current blocking phase, the emission phase is restarted.

Fig. 4 shows the block and timing diagrams of the VFR display, which illustrate how the proposed 7T2C pixel circuit operates on a VFR display using the proposed ramping $V_{REF}$ and current blocking method. Fig. 4(a) shows all pixel circuits that share the same DATA line for each column to sequentially receive the data voltage from the source driver while receiving $V_{REF}$ generated by the $V_{REF}$ generator. Fig. 4(b) and (c) show the timing diagrams of the VFR display when it operates at the maximum frame rate (MFR) among the VFRs and relatively slower frame rates, respectively. One frame time of the VFR display is the sum of the scan frame time (*scan frame*) for writing display data to the VFR display and the dump frame time (*dump frame*) for skipping display data writing. Therefore, the dump frame time lowers the display panel's frame rate to synchronize the GPU's frame rate. In addition, all the *scan* signals are synchronized at the VFR, whereas all the *em* signals are synchronized at the MFR.

When the VFR display operates at the MFR, as shown in Fig. 4(b), where one frame time is equal to the scan frame time, all the *scan* and *em* signals are activated sequentially during the scan frame time, so all pixel circuits operate in the *init*, *comp*, *program*, and *emit* phases sequentially as shown in Fig. 1(b). Moreover, the source driver simultaneously
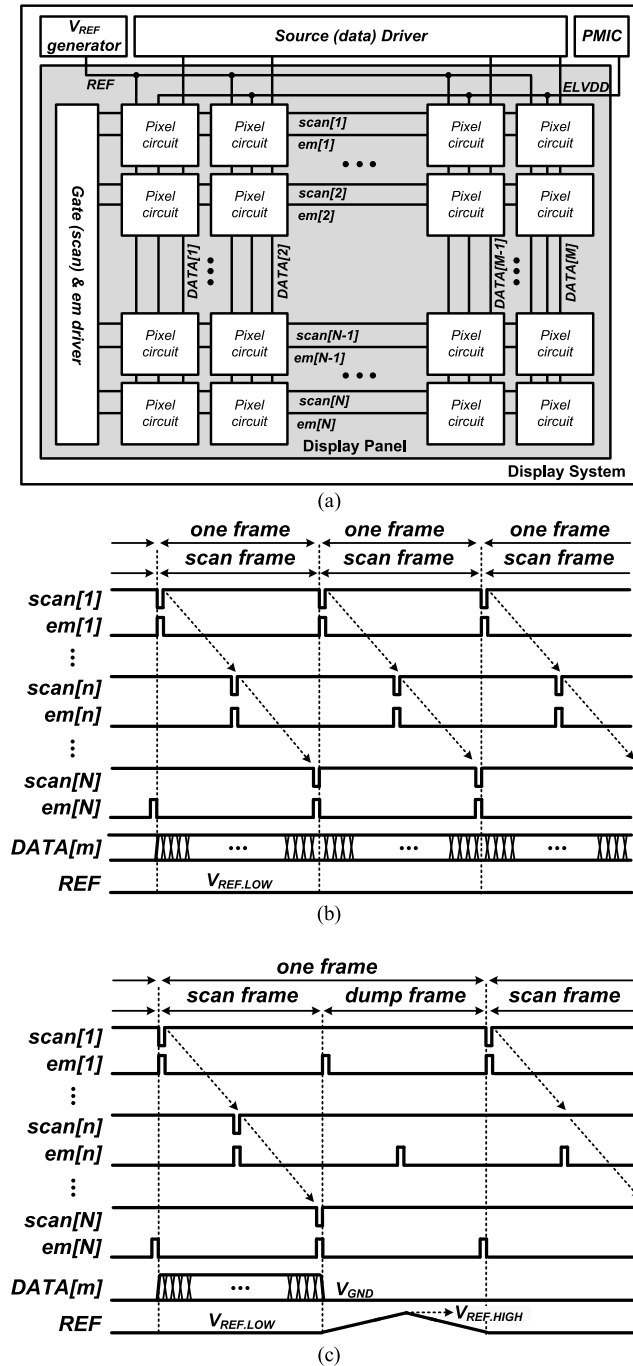
FIGURE 4. (a) Block diagram of the VFR display and its timing diagrams when it operates at (b) the MFR among the VFRs and (c) lower frame rates than the MFR.



FIGURE 5. Transient simulation results of the proposed pixel circuit at 128th gray level (a) with ramping $V_{REF}$ method, (b) without ramping $V_{REF}$ method, 32nd gray level (c) without current blocking method, and (d) with current blocking method.

produces the data voltage to the column data lines while the $V_{REF}$ generator stops ramping and produces a constant voltage through the REF line.

When the VFR display operates at a frame rate lower than the MFR, as shown in Fig. 4(c), it operates in two different frame times; the scan frame time and dump frame times that are added between the scan frame time. All pixel circuits operate the same as at the MFR during the scan
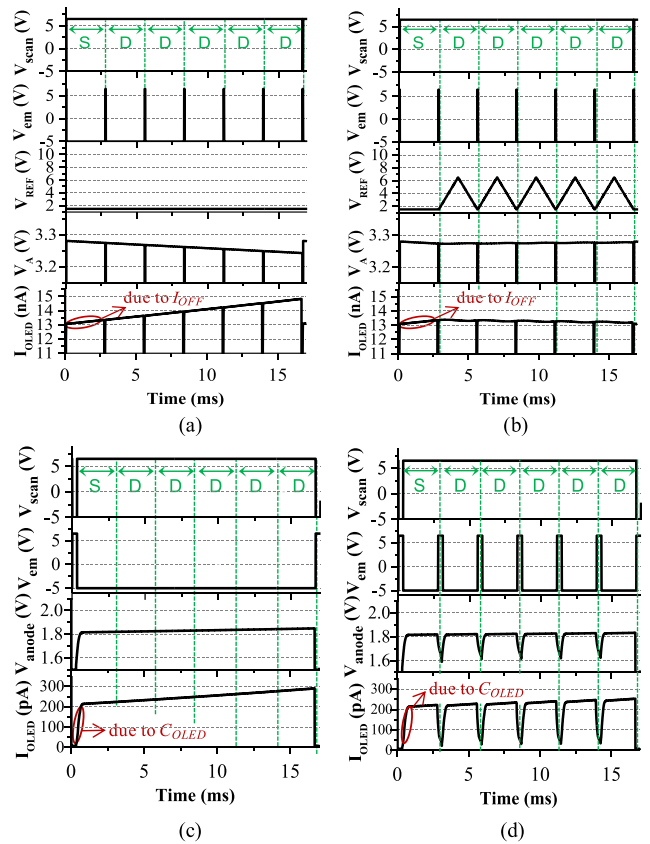
frame time. However, only the *em* signals are activated during the dump frame time without activating the *scan* signals, so all pixel circuits sequentially operate in the *block* and *emit* phases, as shown in Fig. 1(b). Moreover, the source driver does not produce the data voltage, while the $V_{REF}$ generator produces the ramping $V_{REF}$ during the dump frame time.

The proposed pixel circuit reduces the flicker by employing the ramping $V_{REF}$ and current blocking operation during the dump frame time. Fig. 5(a) and (b) show the transient simulation results of the proposed pixel circuit when the frame rate and gray level are 60 Hz and 176th, respectively. To drive the proposed pixel circuit at a frame time of 16.6 ms, we inserted five dump frames (*D*) between scan frames (*S*). When ramping $V_{REF}$ is not employed, the emission current gradually increases (brown circuit) during the emission time because $I_{OFF}$ in M5 lowers the voltage at node A. To reduce this voltage variation at node A ($V_A$), the ramping $V_{REF}$ is employed. It periodically ramps $V_{REF}$ up and down to switch the direction of $I_{OFF}$ during the dump frame time. As a result, the emission current fluctuation due to $I_{OFF}$ in M5 is diminished.

Fig. 5(c) and (d) show the transient simulation results of the proposed pixel circuit when the frame rate and gray level

**TABLE 1.** Target specification of the amoled VFR display.

| Target | Value |
|---|---|
| Panel size | 14-inch |
| Process technology | Low-temperature poly-crystalline silicon (LTPS) p-type thin film transistor (TFT) |
| Resolution | 3840 × 2160 (4K) |
| Unit pixel size | 81 μm × 81 μm |
| Sub-pixel size | 81 μm × 27 μm (RGB stripe type) |
| 1 row line time (1-H time) | 1.28 μs (frame rate = 360 Hz) |

**TABLE 2.** Design parameters of the proposed 7T2C pixel circuit.

| Design parameter | Value |
|---|---|
| $V_{ELVDD}$ | 6.5 V |
| $V_{ELVSS}$ | 0.0 V |
| $V_{REF}$ | 1.5 V |
| Ramping $V_{REF}$ | 1.5 V ~ 6.5 V |
| $C_1, C_2$ | 80 fF, 120 fF |
| $V_{S.HIGH}$ | 6.5 V |
| $V_{S.LOW}$ | -4.0 V |
| $V_{DATA}$ | 0.3 V ~ 3.3 V (red)  0.2 V ~ 3.4 V (green)  0.4 V ~ 3.2 V (blue) |

are 60 Hz and 48th, respectively. At the beginning of the scan frame time, the anode voltage and current of OLED abruptly increase (highlighted circle) due to the capacitance of OLED ($C_{OLED}$), causing fluctuation in emission current. When current blocking operation is not employed, the $C_{OLED}$ has already been charged once in the scan frame time, and the emission current during the dump frame time does not fluctuate. Therefore, the averaged emission current per frame time differs according to VFR, generating the flicker in the display panel. To reduce the flicker, we employed the current blocking operation, which discharges the anode voltage of OLED to $V_{OLED,th}$. Therefore, even if the current blocking operation does not reduce the current fluctuation caused by $C_{OLED}$, it induces current fluctuation during the dump frame time and the scan frame time, resulting in the same averaged emission current per frame time. The emission current increases gradually even after the $C_{OLED}$ is charged is because of the $I_{OFF}$ in M5.

In conclusion, the proposed 7T2C pixel circuit and driving methods compensate both $\Delta V_{th}$ and $\Delta$SS with a sufficient $t_{comp}$. In addition, the ELVDD IR-drop can be reduced by storing $\Delta V_{ELVDD}$ at node A through the capacitive coupling effect of C1. Furthermore, the proposed pixel circuit also reduces the emission current fluctuation due to $I_{OFF}$ in M5 and $C_{OLED}$ by employing the ramping $V_{REF}$ and current blocking operation, respectively. Therefore, the proposed pixel circuit and driving methods achieve high luminance uniformity and low-flicker performance at a wide range of frame rates.

## III. DESIGN AND IMPLEMENTATION OF PROPOSED PIXEL CIRCUIT AND DRIVING METHODS

Table 1, 2 show the target specifications of the VFR display and design parameters of the proposed pixel circuit, respectively. The target specifications come from the requirements of a 14-inch 4K VFR AMOLED display with an LTPS backplane, of which the frame rate varies from 15 Hz to 360 Hz. Here, $t_{1-H}$ is set as 1.28 μs based on the fastest frame rate of 360 Hz and a display resolution of 3840 × 2160.

The driving TFT (MD) has to operate in the saturation region to generate a constant emission current regardless of

a gray level. Considering the anode-to-cathode voltage of the OLED and two $V_{DS}$ of TFTs when flowing a maximum emission current, we set $V_{ELVDD}$ and $V_{ELVSS}$ as 6.5 V and 0 V, respectively. The lowest voltage of the ramping $V_{REF}$ was determined to be 1.5 V to initialize the anode voltage of OLED to $V_{th,OLED}$. The highest voltage of the ramping $V_{REF}$ was determined to be 6.5 V to effectively cancel out the effect of $I_{OFF}$ in M5 for all voltage ranges at node A according to the whole gray level. $V_{S.HIGH}$ and $V_{S.LOW}$, the highest and lowest switching voltages for both the *scan* and *em* switching signals, were determined to turn on and off the switching TFTs, respectively, entirely. The C1 and C2 values were determined by considering several important factors. As the C1 value increases, not only the $V_{DATA}$ range is increased due to the capacitive coupling effect of C1 and C2, but also, the voltage drop due to $I_{OFF}$ in M5 is decreased. However, an increase in the $V_{DATA}$ range leads to an increase in the power consumption of the source driver. Therefore, considering the trade-off between the voltage-holding ratio and the proposed pixel circuit data range, the C1 and C2 values were determined to be 80 fF and 120 fF, respectively. The W/L values of all the switching TFTs and the driving TFT were appropriately determined, minimizing the variations in electrical characteristics of LTPS TFTs within the sub-pixel size. The parasitic capacitances at node A ($C_{para.A}$), such as the gate capacitance of the TFT and the capacitance between the gate and upper metals, were minimized to reduce error in compensated $\Delta V_{th}$, $\Delta$SS, and $\Delta V_{ELVDD}$. In addition, the error on $V_{DATA}$ was caused by the capacitive sharing effect of C1 and $C_{para.A}$ in the emission phase can be minimized as well. The RC delays at the scan, data, and REF line were estimated to be 184 ns (R=4.4 kΩ and C=42 pF) and 59 ns (R=2.5 kΩ and C=24 pF), and 80 ns (R=2.5 kΩ and C=32 pF), respectively. Finally, the prototype of the pixel circuit fabricated on the glass through the LTPS process is shown in Fig. 6.

## IV. VERIFICATION RESULTS & DISCUSSION

Fig. 7 shows the measurement setup of the prototype pixel circuit. The control signals (*scan* and *em*) were generated
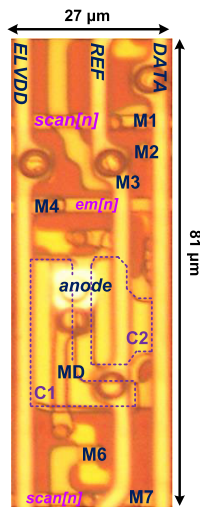
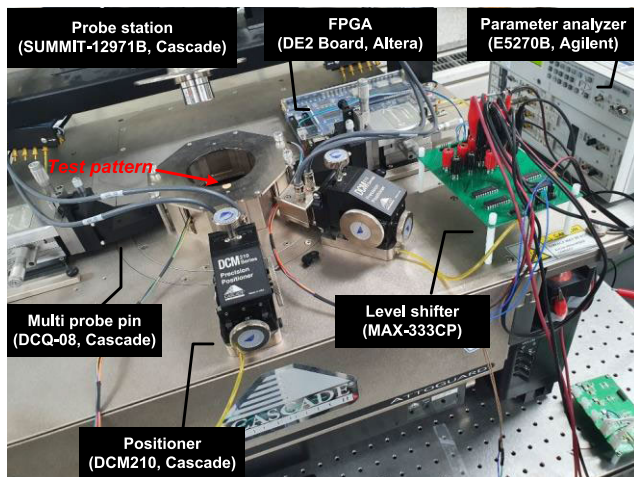**FIGURE 6.** Fabricated prototype of the proposed 7T2C pixel circuit.



**FIGURE 7.** Measurement environment to measure the devices and pixel circuits in the fabricated test pattern.

by an FPGA (DE2-70, Altera) with a clock frequency of 50 MHz, while the amplitudes of the control signals were converted to $V_{S.HIGH}$ and $V_{S.LOW}$ through a level shifter (MAX-333CP, Maxim integrated). The $V_{REF}$ ramping up and down between 2.0 V and 6.5 V was provided using a waveform generator (63318B, Agilent Technologies) and synchronized with the FPGA. The DC voltages, such as $V_{ELVDD}$ and $V_{ELVSS}$, were provided from a parameter analyzer (E5270B, Agilent Technologies). The device under test (DUT) was placed inside the light-blocked probe station to prevent the light-induced leakage current of the TFTs. Each terminal of the TFT devices and the proposed pixel circuits were probed through its connection to the outside of the probe station using the probe pins. The drain current of the TFTs and the emission current of the proposed pixel circuits were sampled and measured by the parameter analyzer.

The electrical characteristics of the driving TFTs and switching TFTs were extracted by measuring the 54 samples of each driving TFT and switching TFT. The $V_{th}$ values of driving TFT were extracted using the $g_m$ max method and the SS values of driving TFT were extracted with the slope, which has the maximum value in the transfer curve. Using these value, the electrical characteristics of LTPS TFT were modeled shown in Fig. 3.

Fig. 8 shows measured SECEs of the proposed pixel circuit according to $t_{comp}$ at the *comp* phase and compensation at the *program* phase to verify its luminance uniformity performance. In order to control the compensation at the *program* phase, M6 was turned on or off during the *program* phase. The emission currents with the 18 samples were measured at a frame rate of 360 Hz and converted to SECE. In Fig. 8(a) and (b), since $t_{comp}$ is insufficient, the compensation point at which SECEs converge zero is out of the target emission current dynamic range, resulting in a large SECE. The worst SECE was measured as ± 9.2 LSB without the compensation at the program and ± 7.2 LSB with the compensation at the program.

In Fig. 8(c)-(f), as explained in Section II, the compensation point appears and moves to a low gray level as $t_{comp}$ increases. In Fig. 8(c) and (e), the worst SECEs are measured to be + 2.0/− 2.2 and + 1.2/− 1.3 in LSB at the 15th gray level, respectively. On the other hand, SECEs at a high gray level, the worst SECEs at the 255th gray level were measured to be ±3.8 LSB and ±6.1 LSB when $t_{comp}$ is 20.48 $\mu$s and 81.92 $\mu$s, respectively. It is in line with our expectation that SECEs at low gray levels are improved as $t_{comp}$ increases but degraded at high gray levels because of $\Delta$SS. Fig. 8(d) and (f) show how much the compensation at the program improves the SECE far from the compensation point. The worst SECEs at the 255th gray level when $t_{comp}$ is 81.92 $\mu$s are measured as + 4.1/− 4.2 LSB, which is + 2.0/− 2.1 LSB improved from the case where the compensation at the program is not applied. Although the sensitivity of the human eye at the high gray level is lower than that of the low gray level in terms of the human visual system, uniformity improvement of a 4.1 LSB can greatly contribute to improving image quality. Similarly, the worst SECEs at the 15th gray level when $t_{comp}$ is 20.48 $\mu$s is measured as + 2.9/− 3.8 LSB, which improved by +0.7 LSB. The uniformity performance of the pixel circuit can be deteriorated by the RC delay of the data line and scan line as well as TFT characteristic variation. However, when the pixel circuit was post-simulated considering the RC delay of the scan and data line estimated in Section III, it was verified that the RC delay negligibly affects the proposed pixel circuit due to the long $t_{comp}$. Therefore, it is verified that the proposed pixel circuit sufficiently compensates for $\Delta V_{th}$ and $\Delta$SS of MD with sufficient $t_{comp}$, thus achieving high luminance uniformity of the display panel.

Fig. 9 shows the measured emission current ($I_{OLED}$) waveform of the proposed 7T2C pixel circuit to illustrate the emission current fluctuation at the high gray level and
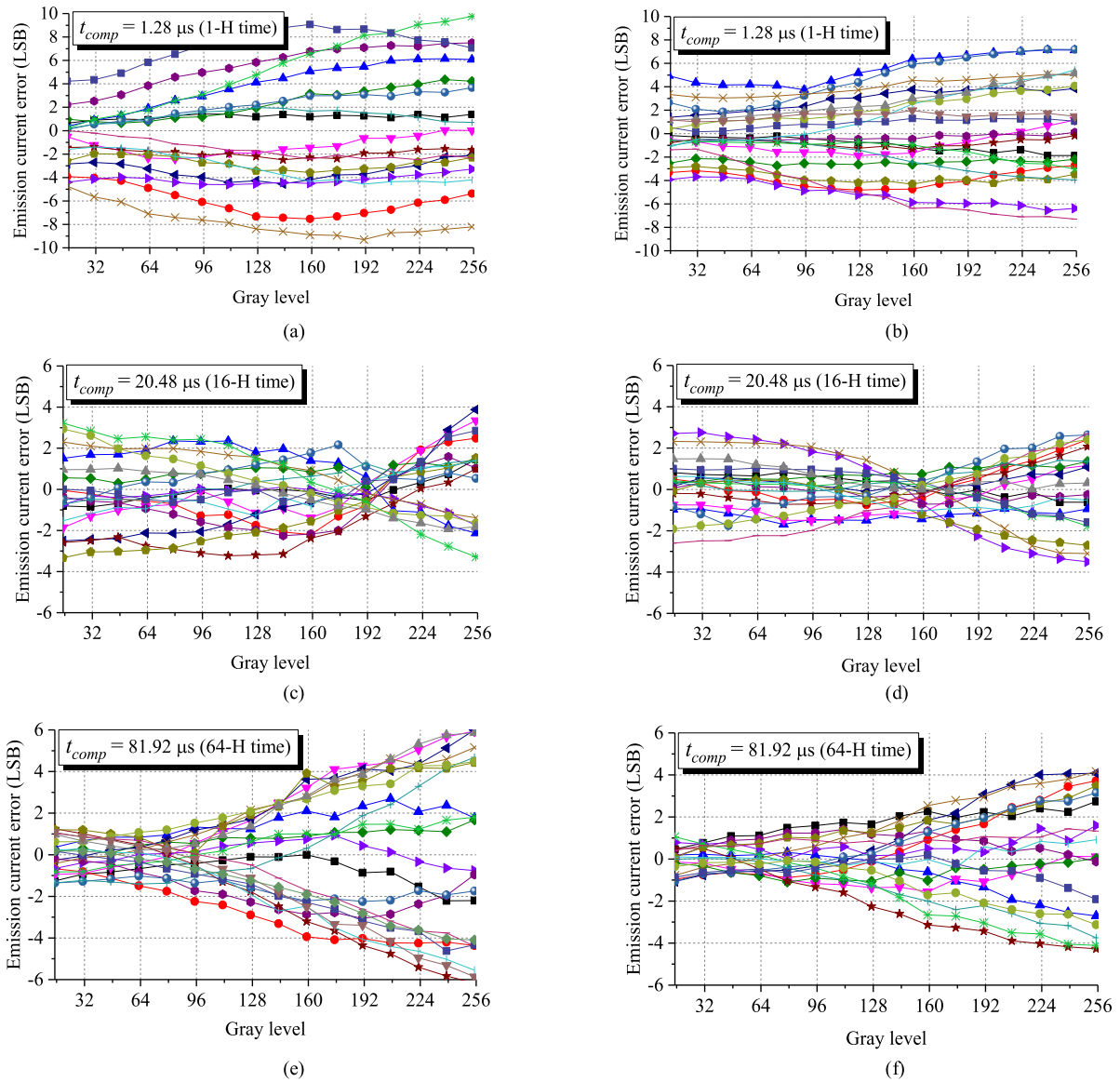
**FIGURE 8.** Measured SECEs of the proposed circuit at (a) $t_{comp}$ = 1.28 $\mu$s, (c) $t_{comp}$ = 20.48 $\mu$s, and (e) $t_{comp}$ = 81.92 $\mu$s without compensation at the program phase. Measured SECEs of the proposed pixel circuit at (b) $t_{comp}$ = 1.28 $\mu$s, (d) $t_{comp}$ = 20.48 $\mu$s, and (f) $t_{comp}$ = 81.92 $\mu$s with compensation at the program phase.

low gray levels without ramping $V_{REF}$ and current blocking method at the frame rate of 15 Hz (1 frame time = 66.7 ms), showing that the emission current is not constant. Since $I_{OFF}$ in M5 flows from the gate node of MD to the REF line, the emission current should increase during the emission time. However, the measured emission current decreased at the high gray level, as shown in Fig. 9(a). This decreasing phenomenon is because the effect of the hysteresis in MD, caused by the trapping of holes that increases $|V_{th}|$ [20], is more dominant than the effect of $I_{OFF}$ in M5. Therefore, it is shown that the emission current of the proposed pixel circuit decreases.

On the other hand, in Fig. 9(b), it is shown that the emission current increases during the emission time. This

increasing phenomenon is because the effect of $I_{OFF}$ in M5 is more dominant than the effect of the hysteresis in MD due to the gate-induced drain leakage effect of M5. Furthermore, at a low gray level, sufficient time is needed to charge the $C_{OLED}$ until the voltage across the $C_{OLED}$ reaches $V_{th,OLED}$. Therefore, the OLED cannot instantaneously flow the emission current and show steep current drops at the beginning of the emit phase. Therefore, it is shown that the emission current of the proposed pixel circuit increases.

Fig. 10 shows the measured TECEs of the proposed pixel circuit according to ramping $V_{REF}$ and current blocking method to verify the flicker performance of the proposed pixel circuit at the different frame rates. Here, the measured
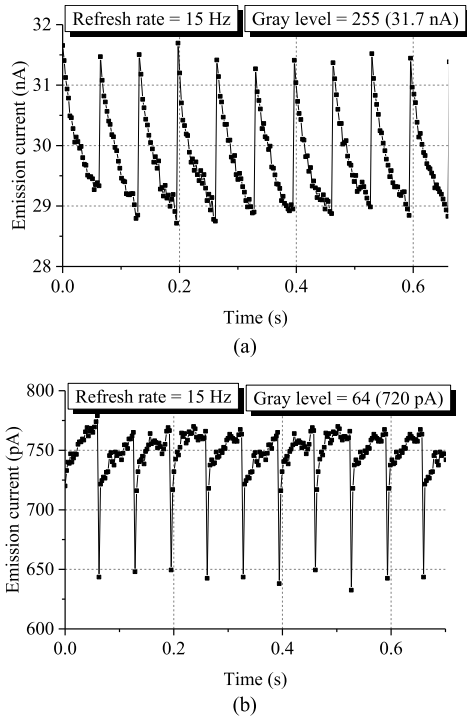
**FIGURE 9.** Measured emission current waveform of the proposed 7T2C pixel circuit without ramping V$_{REF}$ and current blocking method at (a) 255th gray level and (b) 64nd gray level.

emission current is converted to TECEs by subtracting the emission current at the beginning of emission time from the end of emission time. In Fig. 10(a), as analyzed through the measured emission current waveform in Fig. 9, the TECEs of the low gray level have positive values, and TECEs of the high gray level have negative values. Furthermore, since emission time decreases according to the frame rate, the TECEs of the pixel circuit decrease according to the frame rate. The worst TECE of the proposed pixel circuit without any compensation was measured to be +4.6 and −2.7 in LSB at the 15th and 255th gray levels, respectively.

In Fig. 10(b), since the ramping V$_{REF}$ reduces the effect of I$_{OFF}$ in M5, the TECEs at the low gray level, which is highly affected by I$_{OFF}$, are reduced compared to the TECEs in Fig. 10(a). However, since the ramping V$_{REF}$ does not reduce the effect of the C$_{OLED}$, the worst TECE at the 15th gray level was measured to be +3.0 in LSB. Furthermore, since the I$_{OFF}$ in M5 and hysteresis in MD affect the TECEs in opposite polarities at high gray level, the worst TECE at the 255th gray level was measured to be −3.4 in LSB, which are −0.7 in LSB worse compared to the TECE in Fig. 10(a). In Fig. 10(c), since the current blocking method reduces the effect of C$_{OLED}$, the TECEs at the low gray level, which is highly affected by C$_{OLED}$, is reduced compared to the TECEs in Fig. 10(a). However, since the current blocking method does not reduce the effect of the I$_{OFF}$, the worst TECE at the 15th gray levels was measured to be +2.1 in LSB. In Fig. 10 (d), since the effect of I$_{OFF}$ and C$_{OLED}$ at the low gray were reduced, the worst TECE at the 15th gray
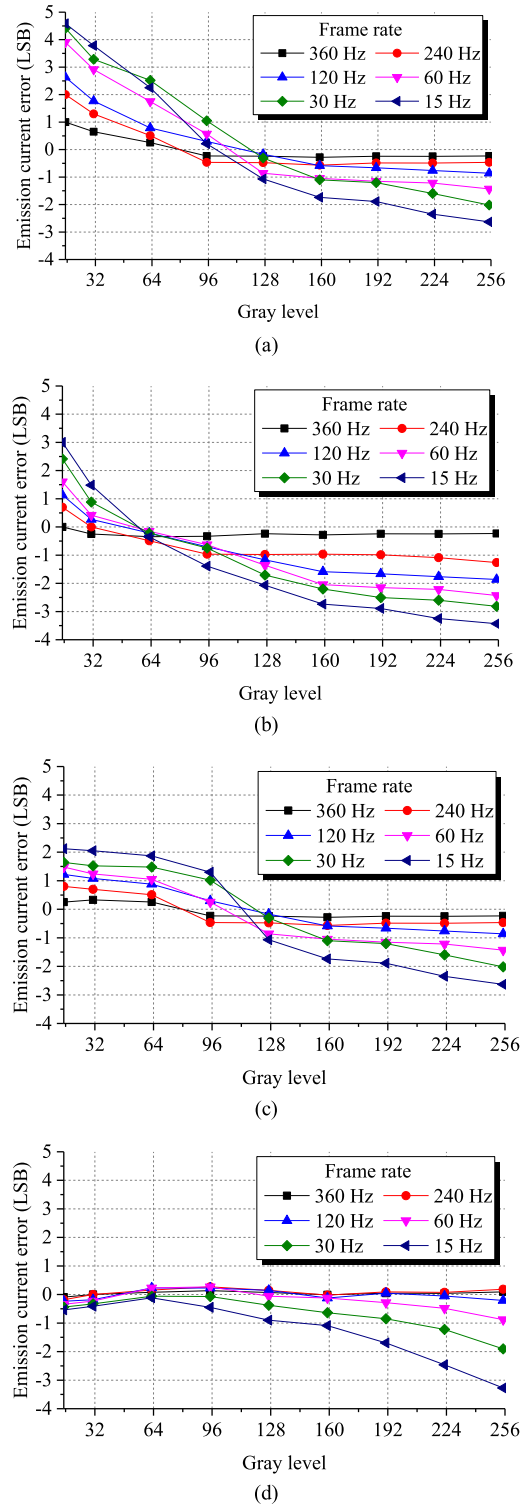


**FIGURE 10.** Measured TECEs of the proposed pixel (a) without ramping V$_{REF}$ and current blocking method, (b) with only ramping V$_{REF}$, (c) with the only current blocking method, and (d) with ramping V$_{REF}$ and current blocking method at different frame rate.

levels was measured to be −1.1 in LSB. Furthermore, the worst ECE at the 255th gray level was 3.1 in LSB, which is -0.4 in LSB worse than compared to the TECE in Fig. 10(a).

**TABLE 3.** Performance comparison of the previous pixel circuits and proposed pixel circuit.

| Index | JSSC [11] | US Patent [9] | This work |
|---|---|---|---|
| Process technology | LTPS | LTPS | LTPS |
| Structure | 6T2C | 7T1C | 7T2C |
| Frame rate | 60 Hz only | 15 ~ 360 Hz | 15 ~ 360 Hz |
| Uniformity performance (SECEs) @ 255th gray level | + 9.2 / - 8.5 | +6.1 / -8.9 | +4.1 / -4.2 |
| Uniformity performance (SECEs) @ 15th gray level | + 2.0 / - 2.0 | +3.6 / -3.6 | +1.2 / -1.1 |
| Flicker performance (TECEs) @ 255th gray level | N/A | +11.2 | -3.2 |
| Flicker performance (TECEs) @ 15th gray level | N/A | +2.41 | -0.8 |

Similar to the uniformity performance of the pixel circuit, the flicker performance can also be deteriorated by the RC delay of the REF line. However, when the pixel circuit was post-simulated considering the RC delay of the REF line estimated in Section III, the ramping time of the REF line (2.78 ms) is much longer than the REF line delay (80 ns), so it does not affect the flicker performance. Therefore, it is verified that the proposed ramping $V_{REF}$ and current blocking method effectively eliminate the effect of $I_{OFF}$ in M5 and $C_{OLED}$.

Table 3 shows the performance comparison of the previously researched pixel circuits and the proposed pixel circuit in this work. In addition, the conventional 7T1C pixel circuit in [9] was also designed and fabricated in the same glass as the prototype and measured to compare the luminance uniformity and flicker performance of the proposed pixel circuit. As a result, regarding both luminance uniformity and flicker performance, the both SECE and TECE of the proposed pixel circuit in this work are the lowest compared to the previously researched pixel circuits in Table 3.

## V. CONCLUSION

This paper proposes a highly uniform and low-flicker 7T2C pixel circuit with novel driving methods for a wide range of VFR AMOLED displays. Regarding luminance uniformity performance, the proposed pixel circuit effectively reduces SECEs by compensating for $\Delta V_{th}$ and $\Delta SS$ of driving TFT with a sufficient $t_{comp}$. Regarding flicker performance, the proposed pixel circuits reduce TECEs by reducing the effect of the $I_{OFF}$ of switching TFT and $C_{OLED}$ by employing a ramping $V_{REF}$ and current blocking method, respectively. The proposed pixel circuit designed for 14-inch 3840 × 2160 (4K) AMOLED displays was verified through the measurement. The verification results demonstrate that the proposed pixel circuit achieved high luminance uniformity and flicker performance. Therefore, the proposed 7T2C pixel

circuit and driving methods suit for a wide range of VFR displays requiring high image quality.

## REFERENCES

[1] A. Nathan, G. R. Chaji, and S. J. Ashtiani, "Driving schemes for a-Si and LTPS AMOLED displays," *J. Display Technol.*, vol. 1, no. 2, pp. 267–277, Dec. 2005.

[2] M. Hack, J. J. Brown, J. K. Mahon, R. C. Kwong, and R. Hewitt, "Performance of high-efficiency AMOLED displays," *J. Soc. Inf. Display*, vol. 9, no. 3, pp. 191–195, Sep. 2001.

[3] G. A. Slavenburg, M. Janssens, L. Lucas, R. J. Schutten, and T. Verbeure, "46–1: Invited paper: Variable refresh rate displays," in *SID Symp. Dig. Tech. Papers*, Sep. 2020, vol. 51, no. 1, pp. 669–672.

[4] B. Yafei, "Variable refresh rate display synchronization," U.S. Patent 10 019 968, Jul. 10, 2018.

[5] M. Emoto, Y. Kusakabe, and M. Sugawara, "High-frame-rate motion picture quality and its independence of viewing distance," *J. Display Technol.*, vol. 10, no. 8, pp. 635–641, Aug. 2014.

[6] J. Kim, H.-J. Chung, and S.-W. Lee, "A low-power pixel circuit comprising low-temperature poly-silicon and oxide TFTs for liquid crystal displays with panel self-refresh technology," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 868–871, Jun. 2020.

[7] C.-L. Lin and Y.-C. Chen, "A novel LTPS-TFT pixel circuit compensating for TFT threshold-voltage shift and OLED degradation for AMOLED," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 129–131, Feb. 2007.

[8] S. M. Choi, O. K. Kwon, and H. K. Chung, "An improved voltage programmed pixel structure for large size and high resolution AM-OLED displays," in *Proc. SID Tech. Dig.*, May 2004, pp. 260–263.

[9] J. S. Lee and S. K. Lee, "Pixel and organic light-emitting diode (OLED) display having the same," U.S Patent 10 170 048, Jan. 1, 2019.

[10] C.-L. Lin, P.-C. Lai, L.-W. Shih, C.-C. Hung, P.-C. Lai, T.-Y. Lin, K.-H. Liu, and T.-H. Wang, "Compensation pixel circuit to improve image quality for mobile AMOLED displays," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 489–500, Feb. 2019.

[11] N.-H. Keum, S.-K. Hong, and O.-K. Kwon, "An AMOLED pixel circuit with a compensating scheme for variations in subthreshold slope and threshold voltage of driving TFTs," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 3087–3096, Nov. 2020.

[12] E. Wells, G. Bernstein, B. Scott, P. Bennett, and J. Mendelson, "Critical flicker frequency responses in visual cortex," *Exp. Brain Res.*, vol. 139, no. 1, pp. 106–110, Jul. 2001.

[13] C.-L. Lin, J.-H. Chang, P.-C. Lai, L.-W. Shih, S.-C. Chen, and M.-H. Cheng, "Pixel circuit with leakage prevention scheme for low-frame-rate AMOLED displays," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 235–240, 2020.

[14] C.-L. Lin, P.-C. Lai, J.-H. Chang, S.-C. Chen, C.-L. Tsai, J.-L. Koa, M.-H. Cheng, L.-W. Shih, and W.-C. Hsu, "Leakage-prevention mechanism to maintain driving capability of compensation pixel circuit for low frame rate AMOLED displays," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2313–2319, May 2021.

[15] T.-K. Chang, C.-W. Lin, and S. Chang, "39–3: Invited paper: LTPO TFT technology for AMOLEDs," in *SID Symp. Dig. Tech. Papers*, May 2019, vol. 50, no. 1, pp. 545–548.

[16] J. Lee, D. Kim, J. Yang, K. Moon, S. Lee, J. Jeon, Y. Kim, S. Choi, U. Chung, K. Park, and K. Park, "Organic light-emitting diode display pixel circuit employing double-gate low-temperature poly-Si thin-film transistor and metal-oxide thin-film transistors," *J. Soc. Inf. Display*, vol. 28, no. 12, pp. 1003–1011, Sep. 2020.

[17] U. J. Chung, S. C. Choi, S. Noh, K. T. Kim, K. J. Moon, J. H. Kim, K. S. Park, H. C. Choi, and I. B. Kang, "15–1: Invited paper: Manufacturing technology of LTPO TFT," *SID Symp. Dig. Tech. Papers.*, Sep. 2020, vol. 51, no. 1, pp. 192–195.

[18] S.-Y. Lee, S.-H. Kuk, S.-M. Song, M.-K. Song, and M.-K. Han, "A novel LTPS TFT pixel circuit for compensating IR drop of large area AMOLED display," *ECS Trans.*, vol. 50, no. 8, pp. 269–275, Mar. 2013.

[19] M. Estrada, A. Cerdeira, A. Ortiz-Conde, F. J. G. Sanchez, and B. Iñiguez, "Extraction method for polycrystalline TFT above and below threshold model parameters," *Solid-State Electron.*, vol. 46, no. 12, pp. 2295–2300, Dec. 2002.

[20] H.-C. Lin, C.-H. Hung, W.-C. Chen, Z.-M. Lin, H.-H. Hsu, and T.-Y. Hunag, "Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors," *J. Appl. Phys.*, vol. 105, no. 5, Mar. 2009, Art. no. 054502.

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