RESEARCH ARTICLE

A Fully-Integrated CMOS Dual-Band RF Energy Harvesting Front-End Employing Adaptive Frequency Selection

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ABSTRACT This paper proposes a fully-integrated dual-band CMOS RF energy harvesting (RFEH) front-end with an adaptive frequency selector that can select between two harvesting frequencies of 1.9 GHz and 2.4 GHz. The RFEH front end includes two pairs of on-chip LC networks and rectifiers that convert the harvested RF power into a usable DC voltage. An internal control logic circuit, powered by an auxiliary path, selects the input harvesting frequency band with a higher power output to the load. The proposed dual-band adaptive frequency selection RFEH system achieves a peak PCE of 40% and 32% at 1.9 GHz and 2.4 GHz, respectively.

INDEX TERMS RF energy harvesting (RFEH), multiband, dual-band, Dickson, adaptive frequency selection, impedance matching network (IMN), CMOS.

I. INTRODUCTION

Radio frequency (RF) is identified as one of the most promising energy harvesting sources due to fewer placement constraints for the harvester and the abundance of available RF energy as compared to kinetic or thermal energy [1]. While solar and vibration have a higher power density than RF, they are limited as energy sources due to irregularity and strong dependence on weather conditions [2]. RF Energy Harvesting (RFEH) is now being employed in medical implants,

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biomedical applications [3], and the Internet of Things (IoT) wireless sensor nodes (WSN). However, the effectiveness of RF energy harvesting largely depends on the nature of the ambient RF sources. Obstructions have prevented the widespread adoption of RFEH as a power source, despite the availability of RF energy in the environment. Non-uniform deployment of RF frequencies [4], geographical fluctuations of RF energy, and high RF spreading loss have impeded the performance of RFEH systems. Additionally, fluctuations in the power and frequency of the RF energy source can negatively impact the efficiency of the RF Energy Harvesting (RFEH) system [1].

While the conventional RFEH system can only harvest from a single band, this approach may be limited in situations where the designated band is unavailable or experiences fading from the harvesting path. As such, investigating multiband RFEH [5], [6], [7], [8], [9], [10] is a viable option to enhance the practicality and productivity of the harvesting system [9]. In previous multiband RFEH systems, the dc power from each harvesting frequency branch was summed [11]. However, if one of the frequency branches lacks power, the overall system performance would be adversely affected [12]. Therefore, the adaptiveness of harvesting the frequency selection in RFEH systems provides a valuable advantage in boosting system performance by overcoming varying RF energy due to external environmental factors.

The field survey findings emphasize the significance of various operating bands, including DTV, GSM850/900, GSM1800/PCS1900, UMTS2100, 3G, WiFi, and LTE, as crucial ambient wireless energy harvesting sources in urban areas [13], [14], [15]. Notably, the LTE band stands out as a widely deployed frequency band, making a substantial contribution to the RF available power extracted by the RFEH node [14]. LTE, built upon the GSM and UMTS technology, represents a standard for high-speed wireless communication for mobile devices and data terminals [16]. This technology encompasses an extensive range of ultra-high-frequency bands, spanning from 0.609 GHz to 5.925 GHz [16]. Moreover, the GSM1800 band is considered a highly reliable frequency band for energy harvesting due to its higher average power density in the ambient [17]. Additionally, the rise of the Internet of Things (IoT) has led to a proliferation of wireless communication systems through Wi-Fi devices operating at the 2.4 GHz ISM band [18]. This proliferation is expected to result in a corresponding increase in ambient RF power density at 2.4 GHz [19]. Furthermore, research by [19] has demonstrated that GSM1800 and Wi-Fi exhibit relatively higher maximum power density at uplink ports than GSM900. As a result, this work targets the RF harvesting frequency bands of GSM1800, LTE, PCS1900 and 2.4 GHz Wi-Fi. Furthermore, as CMOS RFEH systems offer better flexibility, scalability, and portability for large deployment of IoT devices [17], a fully integrated system with an on-chip Impedance Matching Network (IMN) and CMOS rectifier can increase the reliability of the RFEH and motivated by the form factor miniaturization trend in IoT applications [20], [21].
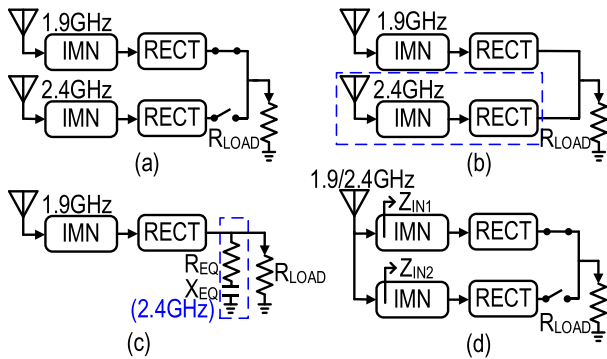
This work presents a novel CMOS RFEH circuit architecture capable of harvesting energy from 1.9 GHz and 2.4 GHz with an adaptive frequency selection feature. The proposed solution harvests from dual RF sources and selects the path with a higher power density using an internal adaptive path selection without the need for any external power source. To maintain a consistent comparison of the input RF power at 1.9 GHz and 2.4 GHz frequencies, two auxiliary rectifiers are employed. The auxiliary rectifiers are optimized with a relatively smaller size to consume lesser power than the main rectifier. This optimization prevents unnecessary energy waste while facilitating continuous comparison. Additionally, these internal auxiliary rectifiers also serve the purpose of powering the logic control unit responsible for adaptive selection. This optimizes the harvesting system performance across the harvesting environment. The path with lower power is automatically turned off by utilizing adaptive frequency selection. This prevents the reverse current flow and consequent drop in the output power when experiencing a significant variation of power density between two paths. In this paper, we first review prior-art on-chip multiband RFEHs in Section II, followed by the description of the principle of operation and implementation of the proposed circuit in Section III. The experimental results are presented in Section IV, while Section V concludes the paper.
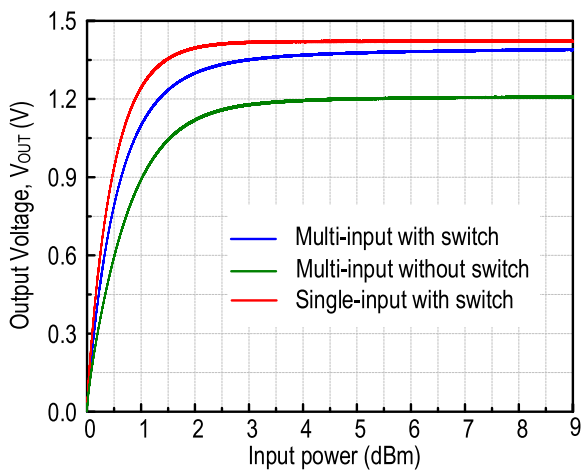
II. PRIOR-ART MULTI-BAND RFEH SYSTEMS

We can classify the multiband RFEH system into fully integrated [6], off-chip IMN [8], [10], [22], [23], [24], or antenna co-design [5], [7], [9] systems. The typical design of the multiband off-chip IMNs of the RFEH system involves a printed circuit board (PCB) using T-network [8] or a transmission line [10], [22], [24]. Although the off-chip IMN-based RFEH system achieves a high peak power conversion efficiency (PCE) and sensitivity performance due to better quality (Q)-factor of the passive components, it is not suitable for deployment in IoT applications such as wearables and biomedical implants where the physical size of the devices is critical [25]. Besides, a large form factor contradicts the miniaturization of design for system-on-chip (SoC) applications. Alternatively, an antenna co-design system would need customization of the antenna, hence limiting the application due to the lack of design flexibility. A favorable RFEH system should have complete integration. However, prior-art fully integrated on-chip RFEH systems are single-band harvesting systems [26], [27], [28], [29]. Single-band harvesting system limits the harvesting frequency to maximize PCE.

Efforts to achieve a fully integrated multiband RFEH system have been made, including using an integrated passive device (IPD) in standard CMOS technology as proposed in [6]. However, this method still requires supplementary technology and results in a significant consumption of area. Another proposed architecture for a dual-band RFEH system, presented in [10] and [19], uses a resistance compression network and a dual-band IMN on an FR4 substrate, with an on-chip RF limiter and a differential drive [10]. Several approaches have been proposed to achieve multiband harvesting, utilizing multiband antennas, multiband IMNs, and multiband rectifiers [22], [23], [24]. While these approaches offer the advantage of using fewer components compared to combining individual single-band antennas, IMNs, and rectifier branches into a multiband system [5], [10], they often rely on transmission lines and resistance compression networks for multiband implementation. The physical form factor of the IMN still poses limitations for SoC integration. Additionally, when employing a dual-band antenna implementation,
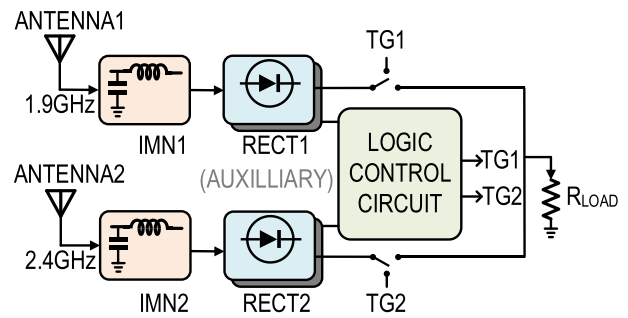
FIGURE 1. Multiband RFEH system configurations: (a) Multi-input (multi single-band antennas) with path selection. (b) Multi-input without switching. (c) Equivalent loading effect of multi-input without switching. (d) Single-input (dual-band antenna) with path selection.

FIGURE 2. Simulated output voltage of multiband RFEH system configurations, in relative to Figure 1.

FIGURE 3. Top architecture of the proposed adaptive frequency selection RFEH system.

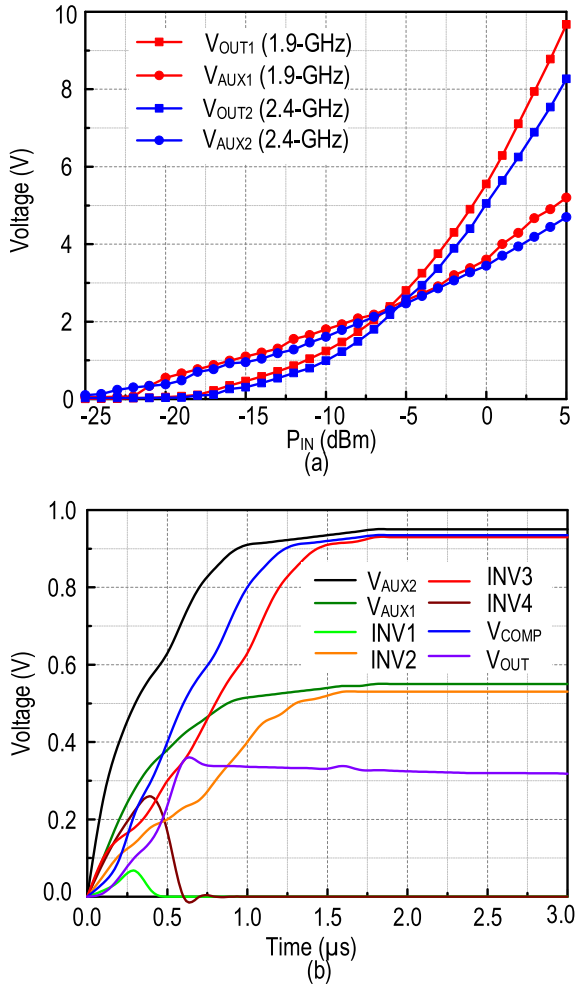capacitor biasing networks are still required to realize the system.

The absence of a controller or switch in the system [6], [8], [9] may compromise the PCE as the output may generate a reverse power flow from the harvesting frequency with a higher power to the frequency branch of lower power. When one branch receives a high input power, it harvests a high output voltage, and the output of the high-power branch flows to the low-power branch. The adjacent low-power branch will be considered as load and increase the parasitic capacitance of the system [12]. This, in turn, allows some power from the high-power branch to leak into the low-power branch [12]. To maintain the PCE performance, turning off the harvesting path is necessary if the input RF power from the subsequent frequency is insufficient. In [5] and [7], the schemes did not combine the harvested power from the two frequency branches but instead generated two separate DC outputs from their respective harvesting branches.

III. PROPOSED ON-CHIP FREQUENCY SELECTIVE RECTIFIER

A. INVESTIGATION OF MULTIBAND CONFIGURATIONS
The different configurations of the multiband RFEH system are shown in Fig. 1, along with their corresponding simulation results in Fig. 2. The simulations are conducted to represent practical scenarios in outdoor and suburban areas, where power density varies due to geographical fluctuations [17]. Considering the differences in input power density, with -10 dBm at 1.9 GHz and -25 dBm at 2.4 GHz, Fig. 1(a) demonstrates the highest output voltage at the load when one of the input powers is very low. In contrast, Fig. 1(b) exhibits a lower output voltage as the path with the lower input power acts as a load [12], [32], as shown in Fig. 1(c). A considerable stream of current will flow through the equivalent resistor in parallel (R_{EQ}) instead of flowing only to the R_{LOAD}.

As demonstrated in [12], the PCE is lower when harvesting from frequencies with different input power compared to harvesting from two paths with the same frequencies. This highlights the necessity of a control logic unit to regulate the output of the multiband RFEH system, as evident from the comparison between Fig. 1(a) and (b). Traditional output

electromagnetic crosstalk between the adjacent path antennas operating at different frequencies can occur [30]. Ensuring high gain and performance of the antenna requires the use of isolation techniques. Previous works have explored the use of two discrete external antennas along with a power combiner before the IMN to merge the RF signals and enhance the total received power [31]. However, given our focus on developing a plug-and-play RFEH system for IoT applications, the design of a high-performance dual-band antenna is not within the scope of this study.

In [7] and [9], the authors designed a bow-tie antenna and a wideband circularly polarized antenna to directly connect the antenna to the rectifier. This approach eliminates the need for the IMN block by matching and specifically tuning the antenna impedance to the rectifier. However, this limits the flexibility of the RFEH system to harvest using a standard 50Ω antenna. This limitation hinders the easy integration of the system into IoT applications and the widespread adoption of WSNs. In [5], a non-standard antenna with an on-chip LC network was employed. However, off-chip resistor and

FIGURE 4. (a) The output of main and auxiliary rectifiers for both paths at different input power range. (b) Time-domain output when input power for path 1 is -20 dBm and path 2 is -15 dBm at 80 kΩ.
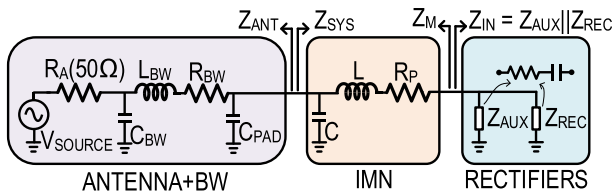
FIGURE 5. Modelling of our RFEH system for impedance matching network.

summation methods involve the use of output combiners that often rely on external clocks, occupy a large area due to the inclusion of inductors [33], [34], and consume power ranging from 40.5uW to 3.33mW [35]. Furthermore, these combiners impose limitations on the required input voltage and output voltage range. Considering that RF input power in ambient environments is typically low and fluctuating, incorporating additional components for output control becomes impractical.

Moreover, Fig. 1(d), which represents a multiband antenna proposed in [22], [23], and [24], supplying input power to the IMN and rectifier paths, exhibits a lower output voltage compared to the proposed circuit. This difference arises due to the inherent variations in input RF power between the two frequencies. When two distinct RF powers are combined within a single source, superposition and interference effects occur. Applying two different frequencies to the circuit results in the waveform being the algebraic sum of the individual waveforms at 1.9 GHz and 2.4 GHz. This summation can lead to constructive or destructive interference, thereby affecting the input voltage and reducing the peak PCE.

Furthermore, when introducing a dual-band system antenna with two IMNs and rectifiers [22], [23], [24] for harvesting two frequencies, it becomes necessary to design different IMNs for each frequency. Instead of designing two separate single-band IMNs for each frequency, the impedances of the IMNs and rectifiers from each path ($Z_{IN1,IN2}$) now interact in parallel, as depicted in Fig. 1(d). This interaction between the blocks affects their respective matching properties and leads to power splitting. Consequently, optimizing energy harvesting at either 1.9 GHz or 2.4 GHz becomes intertwined, posing additional challenges in achieving optimal performance.

B. OPERATION PRINCIPLE

The block diagram in Fig. 3 outlines the top architecture of the proposed RFEH system. As most of the on-chip RFEH systems can harvest only from a single frequency band, the harvesting process will be interrupted without the individual frequency. The proposed circuit overcomes this limitation by enabling simultaneous harvesting from 1.9 GHz and 2.4 GHz frequency bands, and adaptively selecting the higher power path to be connected to the load. Consequently, the proposed system can harvest energy even when one of the frequency bands is absent.

The proposed RFEH system comprises two harvesting paths, each consisting of an antenna, IMN, rectifier, auxiliary rectifier, and transmission gate, as shown in Fig. 3. IMN1 and IMN2 utilize on-chip L-networks to match the impedance of the rectifier to a 50Ω antenna at 1.9 GHz and 2.4 GHz, respectively. The rectifiers convert the harvested RF power to DC power for use at the output. To achieve adaptive frequency selection, a logic control circuit compares the output of the two paths by switching on/off transmission gate 1 (TG1) and transmission gate 2 (TG2). If the RF power density at 1.9 GHz in the environment is higher than at 2.4 GHz, TG1 will be turned on while TG2 will be turned off. In this scenario, the DC output from the rectifier of path 1 will be transmitted to a load, while path 2 will be an open circuit.

The proposed RFEH system is intended for low-power IoT, biomedical implants, or other SoC applications that aim to eliminate the need for batteries [36]. Therefore, an external power source for the control circuit is redundant. The system includes two harvesting paths, each with a main and auxiliary
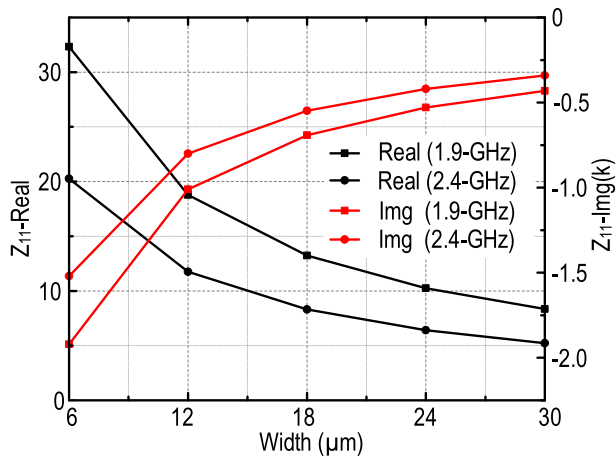
FIGURE 6. Behavior of the impedances across the width of the transistor, under different frequency variation.

rectifier, which are used to effectively compare and switch the transmission gates. The main rectifier converts the matched RF power into usable DC power and sends it to the load. The auxiliary rectifier serves as an input and supply for the logic control circuit. The logic control circuit contains a common gate comparator and inverters. The comparator compares the output from the auxiliary rectifiers from paths 1 and 2, while the inverters trigger TG1 and TG2 to turn off the lower output path. The main and auxiliary rectifiers are designed identically for path 1 and path 2, resulting in similar output with the same input power, but with slight degradation at 2.4 GHz due to larger parasitic effects [5], as shown in Fig. 4(a). Fig. 4(b) presents a time-domain simulation in which V_{AUX2} is higher than V_{AUX1} in the configuration, resulting in V_{COMP} being HIGH. At a steady state, V_{COMP} follows V_{AUX2}, with a slight voltage loss contributed by the transistors. Since V_{AUX1} is lower, path 1 will be turned off by TG1. The V_{OUT} is 0.32V at a steady state, which follows the output of path 2 at -15 dBm, as shown in Fig. 4(a).

C. CIRCUIT IMPLEMENTATION
The rectifier modeled as resistor and capacitor in series (Z_{AUX} and Z_{REC}) [37] with the input matching is shown in Fig. 5. In each frequency path, an LC network is adopted for impedance matching. The analysis of the IMN considers C_{PAD} as the bond pad parasitic and L_{BW}, R_{BW}, and C_{BW} as the equivalent parasitic of the bond wire. L and C represent the matching reactance, and R_P is parasitic of the matching inductor. The transformation ratio of IMN is denoted by k=Re(Z_{SYS})/Re(Z_{ANT}) [27], which reveals how the performance of the IMN is affected by the inductor and the passive amplification contributed by IMN [27]. Passive amplification is the optimal voltage gain when maximum power transfer occurs, which enhances the sensitivity of the system at the matched desired frequency. To achieve the matching, the impedance of the antenna and IMN needs to be in complex conjugate with rectifiers' impedance [38], where
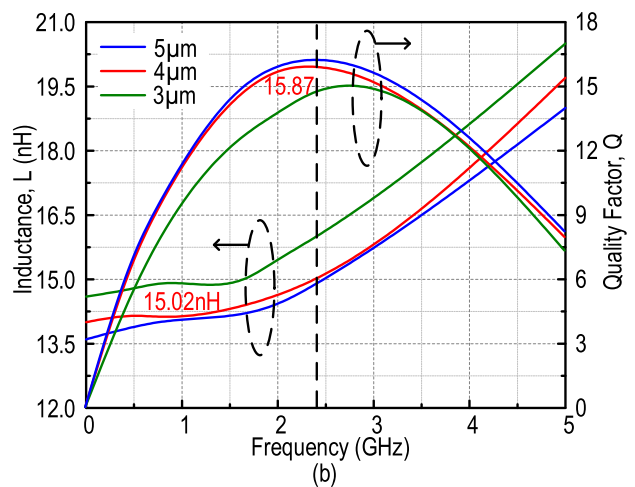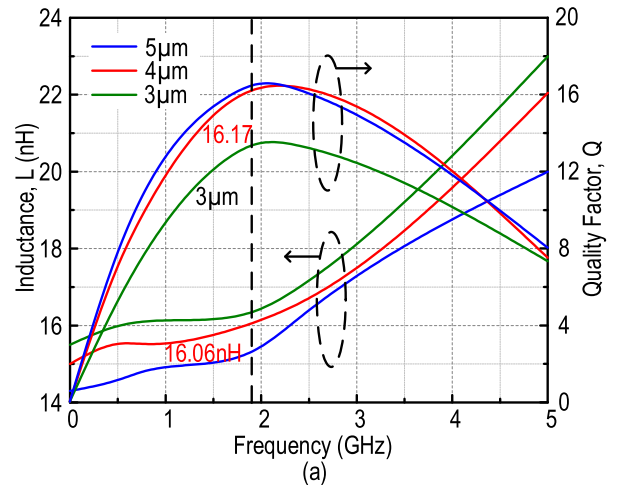

FIGURE 7. Properties of inductors with spiral width of 3 μm, 4 μm and 5 μm, designed for (a) L_{match1}. (b) L_{match2}.

Re(Z_M) = Re(Z_{IN}), while Img (Z_M) = *Img(Z_{IN}). The parasitic of the inductors can be modeled as a resistor placed in series with the equivalent bonding inductance/ matching inductor [39]. The relationship between the inductors' Q-factor and the parasitic is shown in (1). At the matching condition, equations (2) to (4) are satisfied, while equations (5) and (6) show the transformation ratio and passive amplification of the matching network when considering the parasitic.

$$Q = \frac{j\omega L_{BW}}{R_{BW}}; \frac{j\omega L}{R_P} \tag{1}$$

$$Z_{ANT} = \frac{1}{j\omega C_{PAD}} || [j\omega L_{BW} + R_{BW} + (\frac{1}{j\omega C_{BW}} || R_A)] \tag{2}$$

$$Re[Z_M] = Re[j\omega L + R_P + (\frac{1}{j\omega C} || Z_{ANT})]$$
$$= Re[Z_{IN}] \tag{3}$$

$$Img[Z_M] = Img[j\omega L + R_P + (\frac{1}{j\omega C} || Z_{ANT})]$$
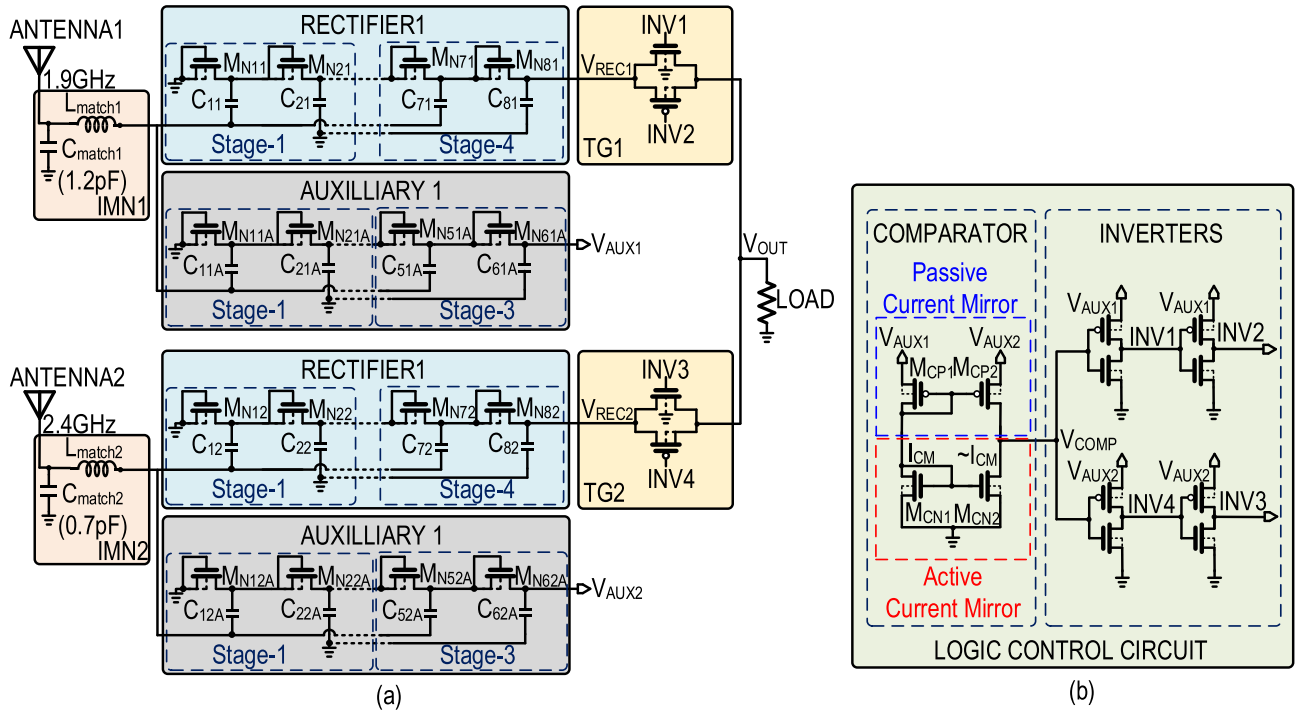$$= *Img[Z_{IN}] \tag{4}$$

FIGURE 8. (a) Two harvesting paths. (b) Logic control circuit for the harvesting paths.

$$k = \frac{Re[\frac{1}{j\omega C}||(j\omega L + R_P) + Z_{IN}]}{Re(Z_{ANT})} \quad (5)$$

$$A_{gain} = \frac{1}{2}\sqrt{\frac{Re[\frac{1}{j\omega C}||(j\omega L + R_P + Z_{IN})]}{Re(Z_{ANT})}}$$

$$= \frac{1}{2}\sqrt{\frac{Re(Z_{SYS})}{Re(Z_{ANT})}} \quad (6)$$

The illustration of Z_{ANT} is presented in equation (2). As indicated by equations (3) and (4), an increase in Z_{ANT} leads to a corresponding increase in Z_M. A higher value of Z_{ANT} can lead to a reduction in matching inductance, thereby improving area efficiency. It is worth noting that Z_{ANT}, which encompasses both bonding wires and bond pad, can also affect IMN transformation and contribute to antenna-rectifier matching [29]. Notably, Q_{BW} is the dominant factor that influences Z_{ANT}, where a higher Q_{BW} results in a larger Z_{ANT}. Consequently, Q_{BW} plays a crucial role in matching. Minimizing the length of the bonding wire is crucial in reducing parasitic [40]. A shorter bonding wire leads to a lower equivalent resistance, R_{BW}, and, consequently, higher Q_{BW}.

Fig. 5 shows Z_{AUX} is placed in parallel with Z_{REC} to reduce $Re(Z_{IN})$ [41], thereby degrading the required transformation and reducing the inductance of the IMN [41] necessary for matching the antenna and rectifier. The lower the $Re(Z_{IN})$, the lower the inductance required for matching. Additionally, the parasitic can be represented by R_P or Q of the inductor, as described in equation (1). The higher the parasitic, the greater the losses, and the lower the Q becomes. As Q dominates the transformation [27], higher Q increases

the value of k along with the passive amplification described in [41] (6).

Fig. 6 shows the equivalent capacitance and resistance of the rectifier decrease as the frequency increases under different matching frequency conditions. Referring to Fig. 6 and (3), a smaller rectifier size can increase the matching frequency when the same matching inductor is used. Additionally, if the rectifier sizes are fixed, a smaller inductor can increase the matching frequency as ω varies. In the proposed design, the rectifier transistor size is smaller for 2.4 GHz, with a smaller inductor size compared to the 1.9 GHz rectifier.

Designing on-chip inductors poses several challenges due to limitations in size, high parasitic resistance, and close coupling between turns. These factors contribute to a narrow range of self-resonant frequencies for on-chip inductors. The Q-factor increases with higher inductance until the self-resonant frequency is reached, after which the Q-factor starts to decrease [27]. The self-resonant frequency can vary by approximately 0.25 GHz for a difference of around 2nH [27]. Therefore, designing an on-chip inductor with high inductance, high Q-factor, and an inductive behavior within the desired frequency range of 1.9 GHz to 2.4 GHz, while ensuring operation below the self-resonant frequency, presents a significant challenge. Figs. 7(a) and (b) depict the inductors specifically designed for the two harvesting paths at 1.9 GHz and 2.4 GHz, respectively.

To ensure optimal performance, careful design consideration and optimization are necessary when selecting on-chip inductors due to their inherent limitations. Various parameters such as inner radius, spiral width, number of turns, and metal
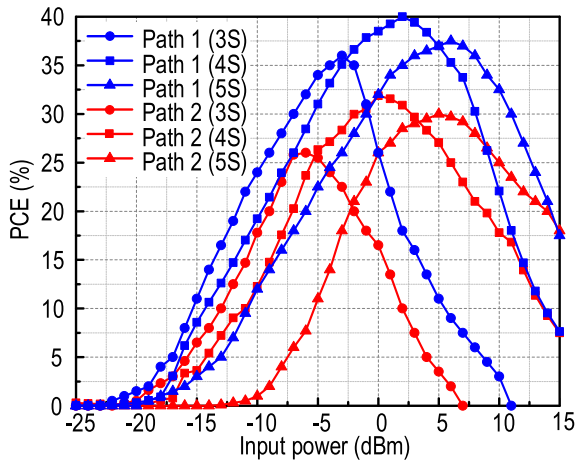
FIGURE 9. PCE of the RFEH system evaluated for different configurations of the main rectifiers, namely 3-stages (3S), 4-stages (4S), and 5-stages (5S).

TABLE 1. Rectifiers' transistors sizing.

| Transistors	Width (μm)
$M_{N11,21,31,41,51,61,71,81}$	30
$M_{N12,22,32,42,52,62,72,82}$	12
$M_{N11A,12A,21A,22A,31A,32A,41A,42A,51A,52A,61A,62A}$	0.6

TABLE 2. Truth table of the switching signals.

Net Voltage	Path1>Path2	Path2>Path1
V_{COMP}	LOW	HIGH
INV1	HIGH	LOW
INV2	LOW	HIGH
INV3	LOW	HIGH
INV4	HIGH	LOW

layer must be taken into account. In this design, Metal 9, known for its high conductivity, is chosen for the inductor fabrication. Based on calculations derived from equations (2) and (3), the required inductance values are determined to be a minimum of 16nH for 1.9 GHz and 15nH for 2.4 GHz. Guided by equations (3) and (4), specific inductors with a fixed number of turns (11 turns) are designed. The performance of these inductors, designed for matching at 1.9 GHz and 2.4 GHz, is depicted in Figs. 7(a) and (b) respectively. In line with insights from [27], it is observed that the self-resonant frequency of an inductor is influenced by its inner radius, with a larger radius resulting in lower resonant frequencies, higher Q and inductance. To optimize the design, an inner radius of 70μm is chosen for the 1.9 GHz matching inductor, while the 2.4 GHz matching inductor is set to have an inner radius of 65μm. In the process of optimization, different spiral widths of 3μm, 4μm, and 5μm are evaluated and compared to achieve the IMN with the highest gain and lowest losses. Ultimately, the inductors with a width of 4μm are chosen as they exhibit the optimal Q factor, while their inductance values meet the requirements for both 1.9 GHz (>16nH) and 2.4 GHz (>15nH), within the self-resonant frequency range of the respective inductors. By selecting appropriate matching inductors, the matching network can achieve optimal gain and reduce parasitic losses, resulting in improved sensitivity.

Figs. 8(a) and (b) show the schematic of the proposed circuit architecture. All MOSFETs in the system are low-threshold voltage transistors to increase the conduction capability. Several added advantages are foreseen by incorporating an auxiliary rectifier into the system. These include the reduction of impedance at the rectifier block, providing an input signal for the comparator without affecting V_{OUT}, and acting as the supply voltage for the transmission gate. It alleviates the demand for an external power supply for the control logic circuit. The auxiliary rectifier ensures the

continuous comparison of the two frequencies. As V_{AUX1} and V_{AUX2} change according to the direct input RF power, the high or low of V_{OUT} does not affect the comparator; hence the comparison is constantly accurate. Moreover, there is no power loss for V_{OUT} after the comparator and transmission gate are included. This is because the inverter signals are controlled by V_{AUX1} and V_{AUX2} instead of V_{OUT}. It is observed that the main and auxiliary rectifiers are isolated, yet the auxiliary assists in adaptive frequency selection to prevent output loss at the main rectifier. For area efficiency, the auxiliary rectifier is designed in a smaller size than the main rectifier, with sufficient output for the control logic unit.

Extensive design simulations and optimizations were conducted to develop a high-performance RF-DC rectifier within the RFEH system. To maximize conductivity and achieve a lower threshold voltage, low-threshold (LVT) transistors were chosen for integration. The rectifier design exploration involved comparing 3 to 5 stages of the Dickson topology main rectifier while keeping the auxiliary rectifier sizing and stages fixed. Fig. 9 illustrates the results of the PCE at different stages of the main rectifier for the 1.9 GHz and 2.4 GHz harvesting paths. In the 3-stage configuration, the peak PCE was observed at a lower input power, followed by the 4-stages and 5-stages configurations. It is noteworthy that the 3-stages configuration exhibited the lowest peak PCE and power dynamic range (PDR) for both harvesting paths. In contrast, the PDR for the 4 and 5-stage configurations remained the same, but the 4-stage configuration demonstrated a higher peak PCE. Therefore, a 4-stage Dickson topology forms both paths' main rectifiers, while the auxiliary rectifiers are constructed with a 3-stage Dickson topology, with the rectifiers' nMOS sizing shown in Table 1.

Based on Fig. 8(b), the logic control circuit consists of a common-gate comparator and inverters. The comparator takes V_{AUX1} and V_{AUX2} as inputs to be compared. When V_{AUX1} is higher than V_{AUX2}, V_{COMP} will be LOW, and vice versa. Two sets of inverters are used for both paths. The first inverter set (INV1 and INV4) inverts the signal from V_{COMP}. Since transmission gates are used to switch the harvesting paths, it requires two inverting signals to operate the transmission gates. V_{OUT} will have a higher loss if V_{COMP} is used
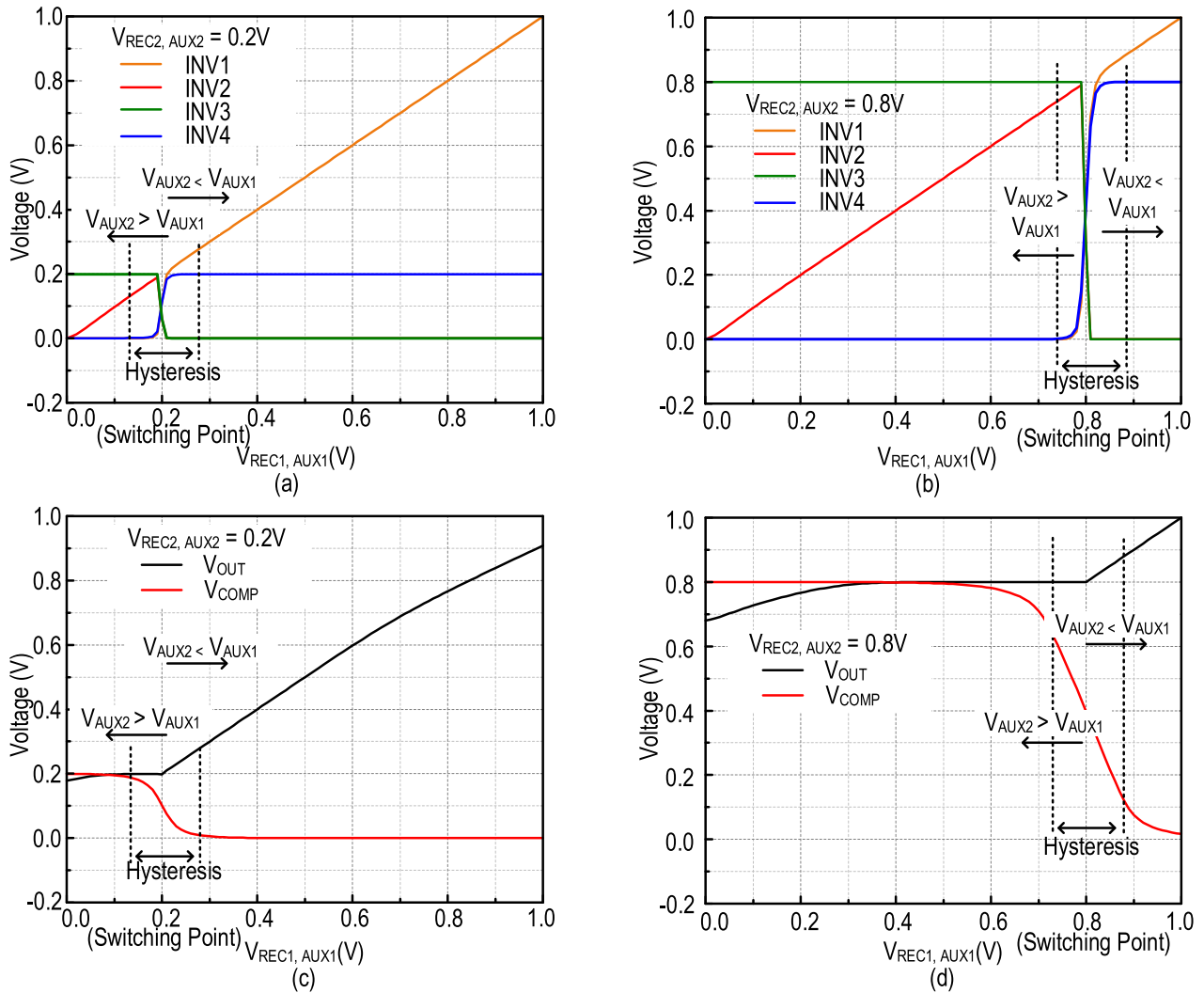
FIGURE 10. Illustration of control logic circuit operations, when $V_{REC1,AUX1}$ sweep from 0 to 1V: (a) INV1-4 when $V_{REC2,AUX2}$ = 0.2V (b) INV1-4 when $V_{REC2,AUX2}$ = 0.8V (c)$V_{OUT,COMP}$ when $V_{REC2,AUX2}$ = 0.2V (d) $V_{OUT,COMP}$ when $V_{REC2,AUX2}$ = 0.8V.

to control the transmission gates. This is due to the sharing and splitting of the V_{COMP} signal for both transmission gates at paths 1 and 2. Therefore, the second inverter set is implemented to flip the signal of the first inverter set. Table 2 summarizes the logic switching of the output logic state of the transmission gate at different described conditions.

To illustrate the working principle of the logic control circuit, ideal signals representing $V_{REC1,2}$ and $V_{AUX1,2}$ in Fig. 8(a) are fed into the control logic circuit and TGs. $V_{REC1,2}$ represents the output from the two main rectifiers that direct to the TGs, and $V_{AUX1,2}$ are the outputs of the auxiliary rectifiers. Based on Fig. 10(a) and (b), the HIGH of INV1 and INV2 follows V_{AUX1}, and the LOW is 0. Consequently, the HIGH and LOW for INV3 and INV4 follow V_{AUX2} and 0, respectively. When both received signals are relatively close to each other, hysteresis occurs in the comparator due to the change of region in the comparator circuit transistors.

The common-gate comparator is formed by a cascode passive and active current mirror, as shown in Fig. 7(b). The input voltages at M_{CP1} (V_{AUX1}) and M_{CP2} (V_{AUX2}) are compared and provide the compared result between M_{CP2} and M_{CN2}. The passive current mirror (M_{CP1} and M_{CP2}) mirrors the current from M_{CP1} to M_{CP2} based on the voltage difference between M_{CP1} and M_{CP2}. Subsequently, the active current mirror generates a reference current based on the gate voltage of M_{CN1} and mirrors it to M_{CN2}. The mirrored current from the passive current mirror is then compared to the reference current generated by the active current mirror. The comparator output is determined by the relative current difference between M_{CP1} and M_{CP2}.

The V_{COMP} waveform is illustrated in Fig. 10(c) and (d). When V_{AUX1} is smaller than V_{AUX2}(the relative difference between V_{AUX1} and V_{AUX2} is significant), the $M_{CN1,CN2}$, and M_{CP1} receive a small signal, and hence they are in the deep triode region. The M_{CN2} carries zero current, therefore,
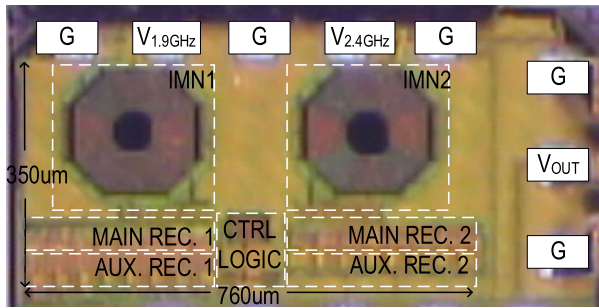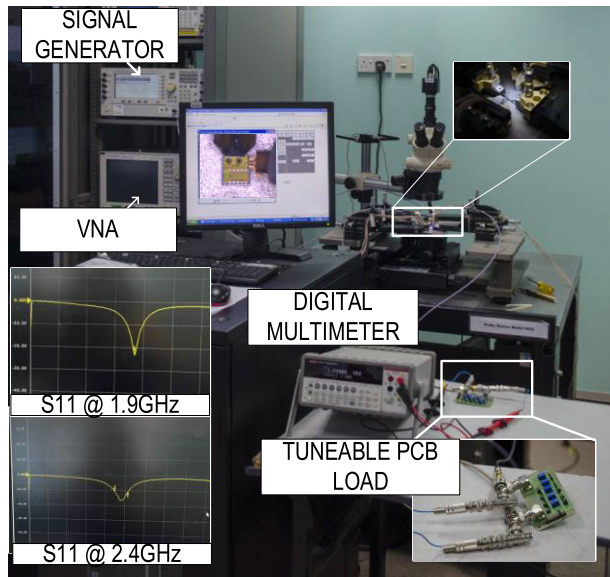
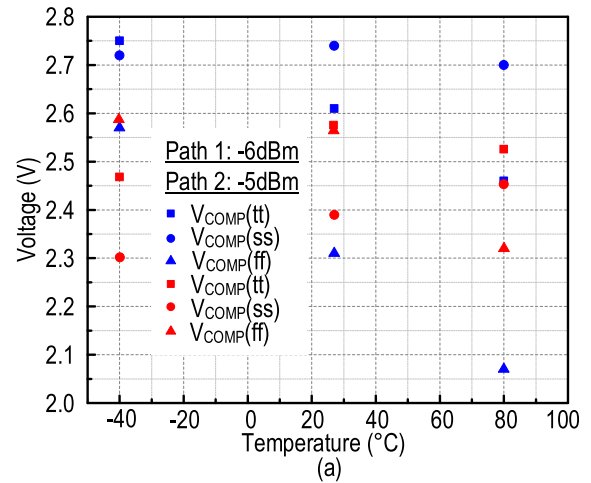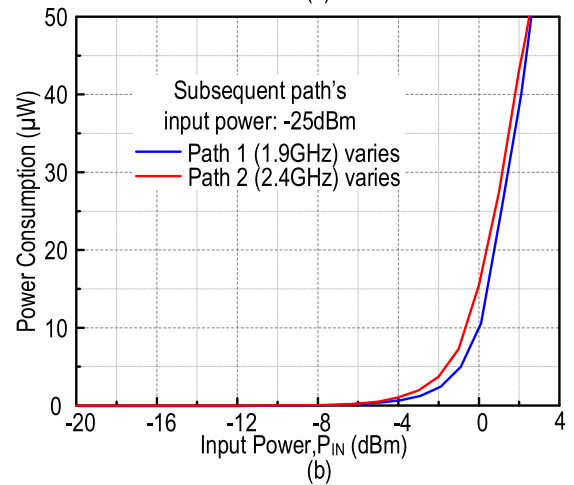**FIGURE 11.** Verification of the proposed design: (a) Chip photo of the presented fabricated RFEH system. (b) Measurement set-up.

FIGURE 12. (a) Post-layout PVT simulation of V_{OUT} and V_{COMP} at 80 kΩ, at typical-typical (tt), slow-slow (ss) and fast-fast (ff) processes. (b) Power consumption of the control logic unit varies when one path is fixed at -25dBm, and the input power of the other path is swept at different levels.

V_{COMP} equals V_{AUX2}. As V_{AUX1} approaches V_{AUX2} (the relative difference is low) or when both inputs are equal, the $M_{CN1,CN2}$, and M_{CP1} are driven into the triode region, and hysteresis arises as the change of region occurs in the transistors. When the MOSFETs are driven into the triode region, the mirrored current is no longer solely determined by the input current and the mirror ratio. Instead, it becomes dependent on the drain-source voltage (V_{DS}) and the transistor's characteristics in the triode region. This can introduce deviations from the desired mirroring behavior, leading to inaccuracies and inconsistencies in the mirrored current. As a result, there will be a mismatch between the V_{DS} of M_{CN1} and M_{CN2}. However, the hysteresis of the designed comparator is low due to the cascode configuration and the differential operation of $M_{CP1,CP2,CN1,andCN2}$. The discussion on the hysteresis will be presented in the subsequent paragraph.

When V_{AUX1} is greater than V_{AUX2}, the $M_{CN1,CN2}$, and M_{CP1} are driven into the saturation region. In this case, a large current will be drawn into M_{CN2}, and $V_{COMP} = 0$. The current flowing at the node V_{COMP} can be expressed as (7) [42] when $V_{AUX1/2}$ is low. Here, δ is the subthreshold slope factor, and V_T is the thermal voltage. When $V_{AUX1} < V_{AUX2}$, I_{COMP}

will be positive, and V_{COMP} is HIGH. The current flowing in M_{CP2} is larger than I_{CM}. In contrast, when $V_{AUX1} > V_{AUX2}$, I_{COMP} will be negative, and V_{COMP} is LOW, with the current of M_{CP2} lower than I_{CM}. Based on the operation of the common-gate comparator, it is shown that the comparison can work in subthreshold, hence providing an accurate comparison for both harvesting paths.

$$I_{COMP} = I_{M_{CP2}} - I_{CM}$$
$$= I_{CM} \left\{ \exp\left(\frac{V_{AUX2} - V_{AUX1}}{\delta V_T} \right) - 1 \right\} \quad (7)$$

The hysteresis causes the inverter signal to be half of the average of the signal. As shown in Fig. 10(a) and (b), the inverter has an output of 0.1V and 0.4V when both input signals are 0.2V and 0.8V. In this case, both the TGs are partially ON, forming a parallel configuration for both path 1 and path 2. Hence, the V_{OUT} will be the average of both paths' output. The V_{OUT} when both paths are at 0.2V and 0.8V are 0.2V and 0.8V, respectively. When V_{AUX1} is low (<0.2V), the
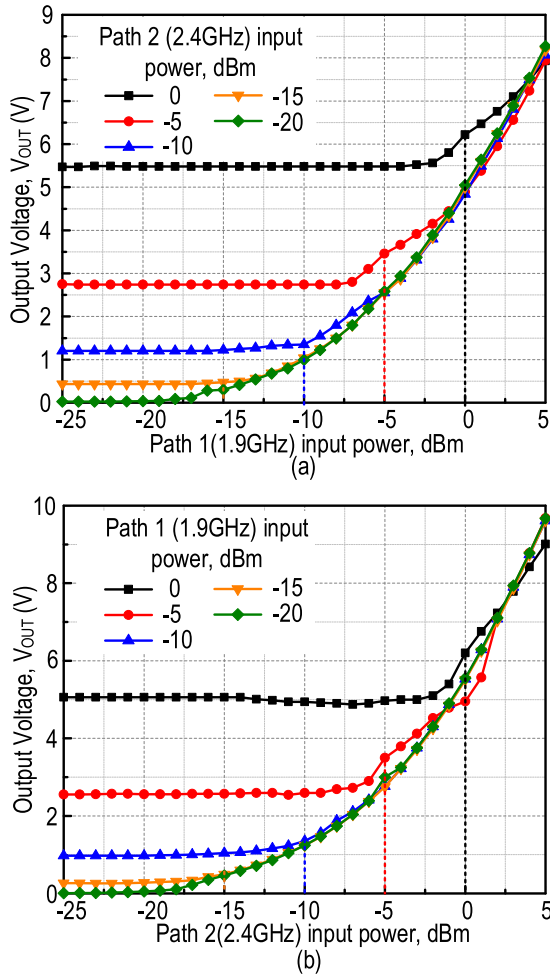
FIGURE 13. Experimental results of the RFEH system: (a) V_{OUT} when path 2 input is set with increment of 5dBm, (b) V_{OUT} when path 1 input is set with increment of 5 dBm.

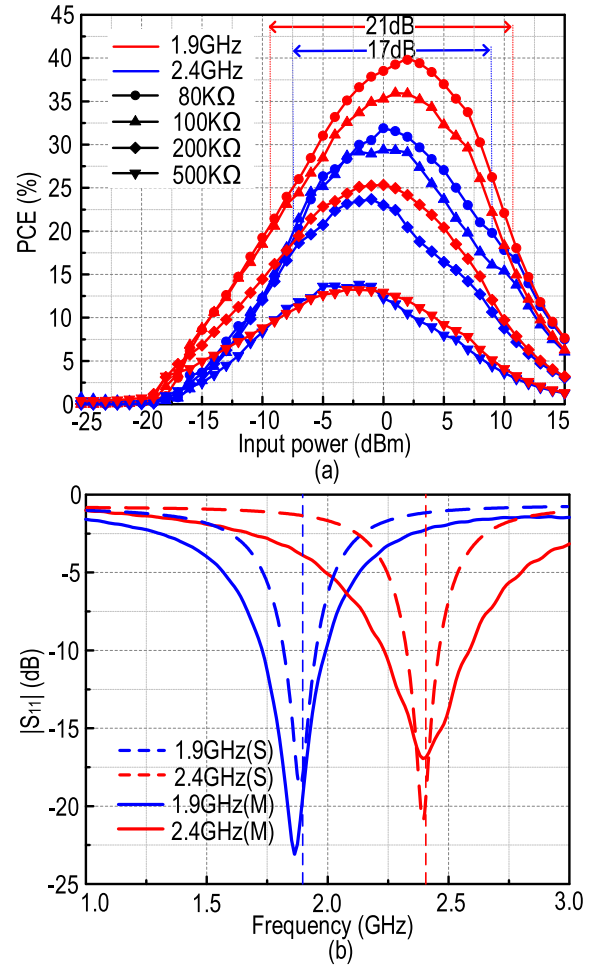**FIGURE 14.** (a) PCE of each path when the relative path is fixed at -25 dBm, and (b) Post-layout simulation (S) and measured (M) reflection coefficient, ($|S_{11}|$).

V_{OUT} is lower, as shown in Fig. 10(c) and (d). It is due to the low turn-on voltage provided by INV2 as it follows V_{AUX1}. Also, if V_{AUX2} is low (<0.2V), and V_{AUX1} is high, the V_{OUT} will drop slightly, as shown in Fig. 10(c). The pMOS in the TG2 receives a low voltage (INV3), causing it to be partially on. Therefore, there is a reverse leakage from the output to path 2. If both inputs are high, the output follows the higher output path as the pMOS in TG2 is properly turned off by a high voltage.

IV. EXPERIMENTAL RESULTS

Fig. 11(a) depicts the chip photo of the fully integrated RFEH system in 65-nm CMOS technology. On-wafer probing was adopted in the chip assessment, with the measurement setup shown in Fig. 11(b). To accommodate the two harvesting paths, two bond pads were used to receive input power for each path. As shown in Fig. 11(a), each path comprises a matching network, a main rectifier, an auxiliary rectifier, and a control logic circuit that compares both paths. The output voltage, V_{OUT} measurement is performed using the right bond pad. The chip size, excluding bond pads, is 350 μm × 760 μm. In measurement, two signal generators

were employed to represent the 1.9 GHz and 2.4 GHz input power. Various combinations of input power were examined to demonstrate the control logic circuit's switching behavior. Connected to the rectifier, a variable printed circuit board (PCB) resistive load is used to measure the output of the system with load variation. The reflection coefficient of each path was measured using a vector network analyzer (VNA).

A post-layout simulation was conducted on PVT variations, and the results are presented in Fig. 12(a) for V_{COMP} and V_{OUT}. When path 1 and path 2 are individually measured at a typical-typical process (-6 dBm for path 1 and -5 dBm for path 2) and 27°C, V_{AUX1} is 2.36V, and V_{AUX2} is 2.61V. Since V_{AUX2} is greater than V_{AUX1}, V_{COMP} is set to HIGH, following the value of V_{AUX2}, and V_{OUT} follows the output of path 2. The variation of V_{COMP} due to PVT stays within a range of 0.3V for all temperature and process variations, except for a lower value at fast-fast process and 80°C. The selector works correctly under all conditions, as shown in Fig. 12(a). The maximum variation of V_{COMP} due to PVT is 0.3V.

In the proposed RFEH system, the control logic unit consumes low power. It draws power from the auxiliary rectifier,

TABLE 3. Performance summary and comparison with prior arts.

	Process (nm)	Operating Frequency (GHz)	Peak PCE (%)	Load at Peak PCE	Sensitivity at 1V(dBm)	Rectifier Scheme	IMN	Chip Area (mm x mm)
This Work	65	1.9, 2.4	40, 32 (2dBm, 0dBm)	80kΩ	-14.2, -13.2 (@500kΩ)	Dickson with Adaptive Path Selection	On-chip LC	0.35 x 0.76
[5]	130	0.9, 1.9	9.1, 8.9 (-19.3dBm, -19dBm)	1.5MΩ, 1MΩ	-19.3*, -19** (@1.5MΩ, 1MΩ)	Dickson with Off-chip Resistor and Capacitor Biasing Network	On-chip LC	2 x 2
[6]	180+IPD	0.93, 2.36	22.5, 23.3 (-1dBm, -1dBm)	500kΩ	-15.4, -15.4 (@500kΩ)	Native NMOS Dickson	IPD Band Pass/Stop Filter	2.9 x 4
[26]	180	0.915	25 (0dBm)	1MΩ	-14.8 (@1MΩ)	Reconfigurable Dickson	On-chip LC	0.756 x 0.624
[27]	65	0.9	19.1 (-10dBm)	200kΩ	-18.8 (@1MΩ)	High PCE CCDD	On-chip Transformer	0.546 x 0.462
[28]	130	1.3	<1 (-11dBm)	10MΩ	-4 (@10MΩ)#	Dickson	On-chip Transformer	0.2 x 0.25
[29]	90	0.915	11.2# (-14dBm)	500kΩ	-22.4 (@10MΩ)	Threshold Compensated Dickson	On-chip LL with bond wire inductance	1.51 x 1.03
[41]	180	2.4	21.15 (0dBm)	3.3kΩ	-14.1	3 x 3 CCDD Rectifier with Charge Pump	On-chip LC	1 x 0.7
[44]	180	0.915, 2.45	24.9, 24.4 (2dBm, 1dBm)	7kΩ	-1,-3# (@7kΩ)	Dickson	On-chip Dual-band LC	N/A
[45]	130	0.9, 1.9	15.44, 26.33 (-4dBm, -4dBm)	147kΩ	-14 (@147kΩ)	Reconfigurable CCDD	Manually Tuned Dual-Band LC	N/A

*At 1.15V **At 1.05V #Estimated from graph

which is isolated from the main rectifier. The power consumption of the control logic unit, including the comparator and inverters, is shown in Fig. 12(b). At peak PCE, assuming the 2.4 GHz path has a low power level of -25 dBm and the 1.9 GHz path has a power level of 2 dBm (with 40% PCE), the maximum power consumption is only 40 μW, while the output power from the rectifier is 632 μW. Similarly, assuming the 1.9 GHz path has a low power level of -25 dBm and the 2.4 GHz path has a peak PCE of 32% at 0 dBm, the power consumption of the control logic circuit is 15.8 μW, with output power from the main rectifier of 400 μW.

Fig. 13(a) and (b) show the measured V_{OUT} of the system. In the first setup, the input for 1.9 GHz is swept from -25 dBm to 0 dBm, while gradually increasing the input for 2.4 GHz from -20 dBm with an increment of 5 dBm. As depicted in Fig. 13(a), when the input for 2.4 GHz is higher than that for 1.9 GHz, the V_{OUT} follows the output for path 2 (2.4 GHz), then continues with path 1 (1.9 GHz) when 1.9 GHz is higher than 2.4 GHz. For example, when the input for 2.4 GHz is -5 dBm, and 1.9 GHz is increasing from -25 dBm, the V_{OUT} remains at 2.8V until it reaches -5 dBm. When both 1.9 GHz and 2.4 GHz have an input power of -5 dBm, the V_{OUT} of path 1 is slightly higher than that of path 2, and hence the switch for path 2 is turned off, selecting path 1 to be connected to the output. As the input power of -5 dBm is reached for 1.9 GHz, the V_{OUT} continues to rise along with the higher

input power, following the output from path 1. The second setup is similar, where the input power for 2.4 GHz is swept from -25 dBm to 5 dBm with an increment of 5 dBm for 1.9 GHz. Figs. 13(a) and 13(b) establish the functioning of the harvesting path switching. The proposed RFEH system achieves a high peak PCE of 40% at 1.9 GHz and 32% at 2.4 GHz, as shown in Fig. 14(a). It also scores a PCE dynamic range (>20%) of 21 dB at 1.9 GHz and 17 dB at 2.4 GHz at 80 kΩ. This is measured by fixing one of the paths to low power (-25 dBm) and sweeping the output of the other harvesting path. Only one input path is included at one time; hence, the PCE is denoted by $P_{OUT}/P_{HIGHERPOWER}$.

To mitigate performance variations caused by on-chip component layout placement, post-layout simulation and tuning were conducted in response to frequency shifts resulting from fabrication processes. By using the VNA, the input reflection coefficient ($|S_{11}|$) is measured and shown in Fig. 14(b), concerning the post-layout result. The measured $|S_{11}|$ for both paths are conducted separately, in which the matching is achieved with -19.8 dB and -16.9 dB at 1.9 GHz and 2.4 GHz, respectively. There is only a slight variation between the post-layout and measured $|S_{11}|$, with a slight frequency shift to the left. The fabricated chip exhibits a larger bandwidth, primarily due to the increased parasitic effects introduced during the fabrication process. This observation aligns with the relationship between bandwidth and quality

factor, where a higher parasitic contribution leads to a lower quality factor and, consequently, a wider bandwidth [5]. Furthermore, the system has demonstrated a matched condition (below -10dB) in the frequency range of 1.7 GHz to 2 GHz and 2.25 GHz to 2.6 GHz. It effectively maintains a high level of efficiency within these frequencies, aligning with the targeted harvesting frequency bands of GSM1800, PCS1900, LTE, and WiFi. Several fabricated chips were measured, and the results varied within an acceptable range of 2%, which verified a stable result for the proposed fabricated chip.

Table 3 summarizes the state-of-the-art RFEH systems, including the IMN and rectifier. Since there are limited fully-integrated multiband RFEH systems available, we include [10] and [43] for comparison in terms of multi-band capability. While [10] and [43] achieved a slightly higher PCE compared to the proposed work, the use of a transmission line as an IMN resulted in a larger form factor, contradicting the miniaturization requirements for IoT applications. Since on-chip solutions are preferred in current IoT applications and large-scale WSN deployments, the use of an off-chip transmission line is not practical. Additionally, [10] and [43] achieved only slightly higher peak PCE due to PCB packaging parasitics and the lack of reconfiguration in the harvesting scheme. Consequently, the proposed adaptive frequency-selective RFEH system achieves better PCE compared to all other on-chip solutions. Compared with the proposed work, [6] has a lower peak PCE and a large form factor due to the integration of IPD technology for the matching network. Furthermore, although [5] attained a higher sensitivity, it has a tradeoff of low PCE. The co-antenna design of [5] alters the antenna impedance to realize the on-chip LC network, yet it hinders reliability as it cannot be implemented with a standard 50Ω antenna. Reference [44] implemented a dual-band LC network, but it has low sensitivity, and it was not fabricated to prove the designed dual-band on-chip LC network in terms of frequency shifting due to fabrication processes. The reconfigurable dual-band LC proposed by [46] has lower peak PCE and sensitivity compared to our work, and it requires manual tuning of the dual-band LC network. This manual tuning limits the system from automatically harvesting from the desired bands based on the ambient input RF power. Subsequently, [27] has a similar sensitivity, yet the peak PCE is lower. It can only harvest from 915 MHz, while the proposed work increases the harvesting capability by harvesting from 1.9 GHz and 2.4 GHz. Besides, [29] has a high sensitivity by implementing the high Q wire bonding parasitic as an inductance [46] to match the impedances. The high Q wire bond provides high gain, yet the use of the LL network occupies a large chip area. With a larger form factor, [29] harvests only from a single band, limiting the harvesting frequency and obtaining a lower peak PCE. Although [27], [28], and [32] report a miniaturized form factor, they are harvesting only at a single-band frequency. Hence, the harvesting fails if the frequency is absent. With dual-band harvesting for the RFEH system, the proposed system retains a high PCE and a small die area.

As a fully on-chip design solution, the dual-band adaptive frequency selection approach is preferred for an RFEH system as bulky components bottleneck the IoT application. Future work can explore triple or multi-band harvesting, along with the integration of a power management unit, to cater to a variety of applications that depend on the ambient RF power density.

V. CONCLUSION

This paper presents a fully integrated RFEH system with dual-band capabilities and adaptive frequency selection. The system can harvest energy from the path with higher input power density, between 1.9 GHz and 2.4 GHz, using LC-network IMNs, main rectifiers, and auxiliary rectifiers in each harvesting path. The control logic circuit can compare the output of the auxiliary rectifiers and controls the path-switching mechanism. With this architecture, we eliminated the need for external sources and utilized an auxiliary rectifier to supply the logic control circuit and transmission gates. The proposed system can harvest energy from multiple frequency options, allowing it to operate even if one frequency is absent. Compared to other multiband systems, the proposed system achieves a higher peak PCE of 40% at 1.9 GHz and 32% at 2.4 GHz, respectively, while consuming a smaller die area.

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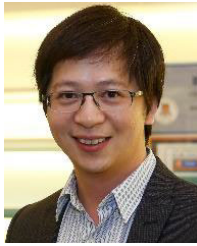
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