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RESEARCH ARTICLE

Evaluation of the A&S and the Advanced EMI Detectors Based on Modeling Frameworks With Appropriate Condition Assessment

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ABSTRACT Electromagnetic interference can cause disruptions to the functional signal on a wired communication channel. Detecting whether the transmitted data has been affected by electromagnetic interference is an important challenge that needs to be addressed. This paper describes an advanced design of an electromagnetic interference detector to detect electromagnetic interference in a wired communication channel, and compares it with the previously proposed adder and subtractor based A&S electromagnetic interference detector. The performance of both EMI detectors is evaluated in light of recently proposed electromagnetic interference condition monitoring definitions. These definitions categorize the received signal based on the impact of electromagnetic disturbance on the transmitted data and its detection by the EMI detector, which helps to determine if the overall detection is contributing towards enhancing safety and/or availability. An in-depth numerical analysis of both electromagnetic interference detectors is performed using a mathematical model. The mathematical model considers different scenarios for the electromagnetic disturbance that is present at the location of the electromagnetic interference detector. These scenarios include varying amplitude, frequency, and phase as well as varying phase differences of the voltages induced by the electromagnetic disturbance in each of the data transmission lines. In addition, the performance of both electromagnetic interference detectors is analyzed in semi-reverberant environments using a Monte-Carlo simulation framework. This research concludes that the Advanced electromagnetic interference detector addresses the inadequacies of the A&S electromagnetic interference detector and can be effectively used for enhancing the safety of wired communication channels.

INDEX TERMS EMI, EMC, electromagnetic resilience, risk management, bit error detection.

I. INTRODUCTION

In the recent past, the usage of Electrical/Electronic and Programmable Electronic (E/E/PE) devices has increased drastically. These devices encompass a wide range of technologies, including mobile phones, smartwatches, and systems that perform sophisticated safety-critical functions. [1]. However, the ongoing trend of miniaturization and the need for more energy-efficient products make the internal signals in E/E/PE devices smaller. As the electromagnetic noise level remains the same or even increases, E/E/PE devices inevitably become more vulnerable to electromagnetic disturbances (EMDs) [2]. EMI risk reduction techniques are generally employed for mitigating the impact of EMDs on E/E/PE devices. However, these techniques may not provide a comprehensive solution for all possible scenarios, especially as new technologies emerge and electromagnetic noise levels continue to increase.

Not surprisingly, new ways to adequately manage risks with regards to EMDs have received significant attention

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over the last years for safety- critical E/E/PE devices. A key milestone in this field is the establishment of the IET code of practice on EM Resilience, which has been the basis for the recent IEEE Standard 1848-2020 [3]. IEEE Std 1848-2020 focuses on the development of systems that are resilient for EMDs. It mentions various techniques and measures that can help to achieve this goal [3].

The reliability of internal communication channels is crucial for sophisticated applications such as Industry 4.0, autonomous vehicles, and the Internet of Things (IoT). These applications heavily rely on complex E/E/PE devices. To reduce the potential risk of bit-errors caused by EMDs in such communication channels, IEEE Standard 1848-2020 provides recommendations for various hardware- and software-based techniques [4], [5]. Hardware-based techniques most often rely on the application of redundancy in the communication channel, followed by a voting system. However, a particular challenge is that the redundancy should have EM-diversity. This means that an EMD should not disturb all redundant paths in the same way, as that would mislead the voting system. Several diversity principles have been proposed and studied in the recent past, including spatial [6], frequency [7], and time diversity [8]. The software-based techniques proposed in IEEE Std 1848-2020 include, but are not limited to, Error Detection Codes (EDCs) and Error Correction Codes (ECCs) [9], [10]. Recent research has demonstrated that these hardware and software techniques can be highly effective. However, certain cases have also been identified where their performance may not be sufficient for safety- and mission- critical applications. Hence, in addition to the techniques and measures already described, other techniques must be investigated in order to reduce risks further [11].

Due to the aforementioned factors, a sensor capable of identifying the presence of an EMD as well as its impact on the data being transferred through the communication channel is definitely needed. Regardless of how an EMD affects the system, current electromagnetic interference (EMI) sensors can only infer its presence. Some of the existing sensors include field strength probes to determine the EM field strength [12], intentional EMI detectors [13], [14], and an antenna-based Ultrawideband EMD detector [15]. Whereas merely identifying EMDs can be challenging for mission- and safety-critical systems that require high availability. This is because situations can arise where an EMD is present and detected but is not actually causing electromagnetic interference (EMI) in the communication channel, resulting in data false positives (DFPs). In fact, identifying an EMD can shift the system to a minimum-risk or safe state, which frequently involves shutting down the system to prevent fatal errors. The availability of the system is significantly decreased if this occurs too frequently and unnecessarily. Therefore, the goal is to detect when an EMD is really interfering with the transmitted data in the communication channel.

Generally, EDCs are employed to identify bit errors in transmitted data caused by EMI. Nonetheless, they need the transmission of redundant data and additional processing at the receiver end. Moreover, EDCs need data blocks to identify bit errors, adding substantial latency. In [16], a first comparator-based detector was presented for identifying bit-wise errors due to EMI. This design employs a simple comparator to identify EMI caused by a sinusoidal EMD, whereas it needs inverted-pair data transmission lines (DTLs) for the data transfer. Unfortunately, thorough research concluded that the comparator-based EMI detector was unable to identify cases when data was inverted in both DTLs due to EMI. Hence, in [11] a novel design of an adder and subtractor-based EMI detector (A&S EMI detector) was proposed. The A&S EMI detector also requires inverted-pair DTLs, but it adds and subtracts the received signal for a number of samples per bit. It was observed that the A&S EMI detector outperformed the comparator-based design. However, in certain cases, the A&S EMI detector also fails to identify bit errors caused by EMI. To solve this issue, an analysis was performed to integrate the A&S EMI detector and field strength probes in [17]. The results of the new design were very promising. However, it is challenging to properly position these field strength probes over the communication channel, especially when the length of the communication channel is very long. An EMD can disturb the transmitted data throughout the DTLs, and field probes may be impractical to install everywhere and therefore have not been considered further. Furthermore, the Advanced design of the EMI detector along with its preliminary analysis is presented in [18]. The Advanced EMI detector is designed by using the Adder-part from the A&S EMI detector along with an additional phase shifter to shift the phase of the added signal, which attempts to successfully identify bit errors due to EMI in all cases for closely spaced DTLs.

In previous studies, such as [11] and [20], the A&S EMI detector was evaluated using classical performance assessment definitions. However, these definitions do not provide a comprehensive evaluation of the performance effectiveness. This paper employs the novel condition assessment definitions proposed in [19] to classify the performance. The practical application of these definitions in this paper provides better insight into the performance of the EMI detectors and offers the ability to identify areas for future research. The primary focus of the research leading to this paper is to minimize the occurrence of Channel False Negatives (CFNs), which refer to bit errors caused by EMI but not identified by the detector. It is crucial to avoid such CFNs, particularly for safety-critical systems.

This paper comprehensively discusses the design of the A&S and the Advanced EMI detectors and assesses their performance and limitations. The benefit of adding a phase shift to the added signal from both DTLs is also investigated in this paper. Furthermore, a mathematical model is developed to thoroughly investigate both the A&S and

the Advanced EMI detectors. This mathematical model uses a continuous-wave EMD-induced voltage with varying amplitude, frequency, incoming phase, and phase difference between the EMD-induced voltages in both DTLs. These are the primary parameters of the induced voltage caused by a continuous wave EMD; the remaining parameters are dependent upon these or the channel. Performing analyses using the mathematical model enables the designer to evaluate the performance limitations for each parameter and gain the necessary insights to model an EMI detector tailored to a specific electromagnetic environment. By utilizing the mathematical model, it is possible to evaluate performance in an efficient and reliable way without the need to add continuous EMD-induced voltage on randomly transmitted data, as previously used to evaluate the A&S EMI detector in [11]. To compare the performance of both EMI detectors, simulations are also performed in a real-like semi-reverberant environment by the Monte-Carlo-based simulation framework. This simulation framework was previously used in [6], [7], [8], and [16].

The remainder of this paper is structured as follows. Section II discusses the theoretical principles behind the design of the A&S EMI detector. Furthermore, it introduces the mathematical model to assess the performance of the A&S EMI detector. Section II also explains the new condition assessment definitions for analysing an EMI detector and assesses the performance of the A&S EMI detector. At the end of Section II, the performance of the A&S EMI detector is analysed. Section III elaborates on the working principle of the Advanced EMI detector. Moreover, it proposes the mathematical model of the Advanced EMI Detector. In addition, a thorough analysis is performed in Section III to compare the performance of both EMI detectors. Lastly, Section IV draws concluding remarks.

II. THE A&S EMI DETECTOR

A. DESIGN AND WORKING PRINCIPLE

The A&S EMI detector (shown in Fig. 1) needs to be installed at the receiver end of the DTLs. For this design to function, data must be sent over inverted-pair DTLs. To detect EMI, the A&S EMI detector processes the signal twice using the Adder and the Subtractor and attempts to raise a warning when an EMD disturbs the data transmitted over the communication channel. The detector takes multiple samples of each bit to detect EMI. It then processes each sample and uses the worst-case one to determine if a warning should be triggered. This approach helps to ensure that the detector can accurately detect EMI even when strong EMD-induced voltage is not present in all of the samples.

For the A&S EMI detector to function, signals must be transmitted through two DTLs, with one (the data line) carrying the actual signal and the other (the inverted data line) carrying its inverted counterpart. The signal that is transmitted in the data line and the inverted data line can be characterized as $V_{\mathrm{BIT}}^{\mathrm{DL}}$ and $V_{\mathrm{BIT}}^{\mathrm{IDL}}$, respectively, where "DL" refers to the data line and "IDL" refers to the inverted data

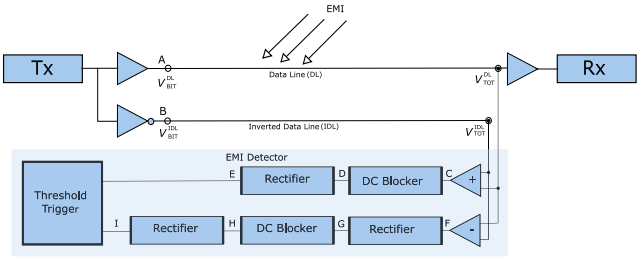

FIGURE 1. The A&S EMI Detector - block diagram.

line. In the presence of an EMD, the voltages at the receiver end $V_{\mathrm{TOT}}^{\mathrm{DL}}$ and $V_{\mathrm{TOT}}^{\mathrm{IDL}}$ are given by:

$$V_{\mathrm{TOT}}^{\mathrm{DL}}(t) = V_{\mathrm{BIT}}^{\mathrm{DL}}(t) + V_{\mathrm{EMD}}^{\mathrm{DL}}(t) \tag{1}$$

$$V_{\mathrm{TOT}}^{\mathrm{IDL}}(t) = V_{\mathrm{BIT}}^{\mathrm{IDL}}(t) + V_{\mathrm{EMD}}^{\mathrm{IDL}}(t) \tag{2}$$

$V_{\mathrm{EMD}}^{\mathrm{DL}}$ and $V_{\mathrm{EMD}}^{\mathrm{IDL}}$ are the EMD-induced voltages in each line. Assuming a single frequency continuous wave EMD, these can also be represented as

$$V_{\mathrm{EMD}}^{\mathrm{DL}}(t) = A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta) \tag{3}$$

$$V_{\mathrm{EMD}}^{\mathrm{IDL}}(t) = A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta + \phi) \tag{4}$$

Equations (3) and (4) depict the amplitude of the EMD-induced voltage as A, the frequency as f_{EMD} and the phase as θ. Additionally, these equations illustrate the phase difference, represented by ϕ, of the EMD-induced voltages between two closely situated DTLs. Due to the close proximity of the DTLs, the amplitude of the EMD-induced voltage is assumed to be the same in the mathematical evaluation.

The Adder of the A&S EMI detector adds the voltage from both DTLs. The sum will remain constant equal to V_{DC}, if both DTLs transmit an inverted signal and there is no EMD-induced voltage:

$$V_{\mathrm{DC}}(t) = V_{\mathrm{BIT}}^{\mathrm{DL}}(t) + V_{\mathrm{BIT}}^{\mathrm{IDL}}(t) \tag{5}$$

In this research, a binary "1" is represented by 1 V and a binary "0" by 0 V using the unipolar Non-Return-to-Zero-Level (NRZ-L) encoding. A fixed frequency f_{BIT} is used by both DTLs for the transfer of data. Unlike the A&S EMI detector, the receiver Rx does not oversample. It samples the received bit from the center and decodes the received voltage of more than or equal to 0.66 V as "1" and less than or equal to 0.33 V as "0." In our analysis (worst-case analysis), a voltage between 0.33 V and 0.66 V is classified as a bit-error.

The sum of the signals from both DTLs when an EMD is not present in our case is 1 V i.e., V_{DC}. Indeed, if $V_{\mathrm{BIT}}^{\mathrm{DL}}$ is 0 V, then $V_{\mathrm{BIT}}^{\mathrm{IDL}}$ is 1 V or vice versa. Equations (6)-(14) are derived for points C to I in Fig. 1. The voltage at point C is defined as:

$$V_{\mathrm{C}}(t) = V_{\mathrm{TOT}}^{\mathrm{DL}}(t) + V_{\mathrm{TOT}}^{\mathrm{IDL}}(t) \tag{6}$$

Using equations (1) and (2), equation (6) can be re-written as

$$V_C(t) = V_{DC}(t) + V_{EMD}^{DL}(t) + V_{EMD}^{IDL}(t) \quad (7)$$

The constant DC voltage V_{DC} is eliminated by the DC blocker. Afterwards, the voltage only comprises the sum of the EMD-induced voltages in both DTLs. Hence, the voltage at point D equals:

$$V_D(t) = V_{EMD}^{DL}(t) + V_{EMD}^{IDL}(t) \quad (8)$$

After the rectifier (point E) the voltage is given by:

$$V_E(t) = |V_{EMD}^{DL}(t) + V_{EMD}^{IDL}(t)| \quad (9)$$

Similarly, the Subtractor finds the difference between the EMD-induced voltages in both DTLs. This voltage at point F equals:

$$V_F(t) = V_{TOT}^{DL}(t) - V_{TOT}^{IDL}(t) \quad (10)$$

$$V_F(t) = \pm V_{DC}(t) + V_{EMD}^{DL}(t) - V_{EMD}^{IDL}(t) \quad (11)$$

After the rectifier (point G), the voltage can be written as:

$$V_G(t) = |\pm V_{DC}(t) + V_{EMD}^{DL}(t) - V_{EMD}^{IDL}(t)| \quad (12)$$

The DC blocker is used to remove the DC component from equation (12), and the resulting voltage at point H is:

$$V_H(t) = |\pm V_{DC}(t) + V_{EMD(t)}^{DL} - V_{EMD}^{IDL}(t)| - V_{DC}(t) \quad (13)$$

Lastly, the signal is rectified once more at point I:

$$V_I(t) = ||\pm V_{DC}(t) + V_{EMD}^{DL}(t) - V_{EMD}^{IDL}(t)| - V_{DC}(t)| \quad (14)$$

The A&S EMI detector will generate a warning when the output of equations (9) and/or (14) is more than the pre-defined threshold voltage V_{thresh}^{det} for any sample of a bit. The phase difference of the EMD-induced voltage is dependent on the distance between the DTLs and the frequency of the EMD. The induced voltage due to an EMD in both DTLs will be similar if they are placed very close to each other, and the phase difference ϕ of the induced voltage between both DTLs is almost zero. In these instances, the Adder can detect an EMD in an effective manner.

Unfortunately, it is not always possible to have closely placed DTLs. and, also because of higher frequencies, the induced voltages between two transmission DTLs will always have a phase difference. The EMD-induced voltages will not be equal because of the phase difference, and if the phase difference becomes too large, the Adder may not be able to detect EMI. The Subtractor tries to solve this by finding the difference of the EMD-induced voltage in both DTLs. The A&S EMI detector raises a warning when either the Adder or the Subtractor have been triggered.

As stated above, at the receiver end, the A&S EMI detector uses oversampling and samples the signal an integer multiple times per bit, i.e., three times. Although we did investigate the use of more samples per bit, this analysis revealed that the impact of adding more samples was not significant enough to warrant the additional cost, both related to hardware and signal processing, that comes along with a higher oversampling.

TABLE 1. Defined conditions for analysing the response of an EMI Detector.

Output determined by Data: $A < V_{thresh}^{BIT}$ Channel: $A > V_{thresh}^{BIT}$	Detector Warning True: Correct False: Wrong	Received Bit Positive: Correct Negative: Wrong	Abbreviation
Data	True	Positive	DTP
Data	True	Negative	DTN
Data	False	Positive	DFP
Data	False	Negative	DFN
Channel	True	Positive	CTP
Channel	True	Negative	CTN
Channel	False	Positive	CFP
Channel	False	Negative	CFN

B. PERFORMANCE ASSESSMENT DEFINITIONS

The new condition assessment definitions presented in [19] are utilized to evaluate the EMI detector's performance. These definitions are used to categorize the incoming signal based on its effect on the system and the channel's health. As proposed in [19] the definitions are based on three different queries. The first query determines if the communication channel is controlled by the data or by the ''channel'', i.e. here the EMD. In this paper, the threshold voltage V_{thresh}^{BIT} is defined as the minimum voltage required to cause a bit error. The channel is in control when the amplitude A of the induced voltage (3) or (4) is larger than the V_{thresh}^{BIT}. When it is smaller, the disturbance can never cause a bit error. Hence, the data is in control. The second query states whether the output of the receiver is either correct or wrong. The response of the query is then either positive or negative, respectively. The last query determines that if the detector correctly detected a bit error, the response is true, otherwise false. The colours used in Table 1 are also used in the remainder of the paper to indicate a particular case.

C. MATHEMATICAL EVALUATION MODEL

In this section, a mathematical evaluation model is presented. The main goal of this model is to evaluate the cases when bit errors occur, but the EMI detector can not detect them, i.e., the occurrence of CFNs. Nonetheless, this model can also help in the evaluation of other cases.

1) BIT ERROR

To disturb the data transmitted through a communication channel, the induced voltage by an EMD should be large

enough to flip a bit, i.e. the induced voltage is greater than a defined threshold voltage. Mathematically this can be written as follows for the case when the data line is transmitting a '1'

$$V_{\mathrm{EMD}}^{\mathrm{DL}}\left(t_{\mathrm{s}}=\frac{T_{\mathrm{BIT}}}{2}\right)=A\cdot\sin(2\pi f_{\mathrm{EMD}}t_{\mathrm{s}}+\theta)<-V_{\mathrm{thresh}}^{\mathrm{BIT}} \tag{15}$$

and as follows for the case when the data line is transmitting a '0'

$$V_{\mathrm{EMD}}^{\mathrm{DL}}\left(t_{\mathrm{s}}=\frac{T_{\mathrm{BIT}}}{2}\right)=A\cdot\sin(2\pi f_{\mathrm{EMD}}t_{\mathrm{s}}+\theta)>V_{\mathrm{thresh}}^{\mathrm{BIT}} \tag{16}$$

In what follows, we assume that in the data, the likelihood of a '1' and '0' are the same:

$$P\left[1_{\mathrm{Sent}}\right]=P\left[0_{\mathrm{Sent}}\right]=0.5 \tag{17}$$

2) ADDER

The A&S EMI Detector samples a bit multiple times. More specifically, an oversampling of 3 is used here, i.e. three equally divided time intervals of a bit are used. The Adder adds up the signals from both DTLs for each of these samples and is followed by a rectifier and DC blocker. The Adder in the A&S EMI detector will raise a warning if the voltage in point C is larger than the defined threshold $V_{\mathrm{thresh}}^{\mathrm{det}}$:

$$|V_{\mathrm{TOT},k}^{\mathrm{DL}}+V_{\mathrm{TOT},k}^{\mathrm{IDL}}-V_{\mathrm{DC}}|>V_{\mathrm{thresh}}^{\mathrm{det}} \tag{18}$$

In equation (18), k=1,2 or 3, is used to show the sample number. The samples are taken at the time t_k, which can be written as

$$t_k=\frac{(2k-1)T_{\mathrm{BIT}}}{6}=\frac{2k-1}{6f_{\mathrm{BIT}}} \tag{19}$$

In (19), T_{BIT} is the total length of a single bit and f_{BIT} represents the bit frequency. This equation may be changed if the sampling points or number of samples vary. Despite the fact that the signal is sampled after it has been processed by all blocks of the EMI detector, equations for the total voltage for each sample point may be developed. The total voltage at the DTLs for each sample can be defined as the sum of the signal and the voltage induced by the continuous-wave EMD. This can be mathematically represented as

$$V_{\mathrm{TOT},k}^{\mathrm{DL}}=V_{\mathrm{BIT}}^{\mathrm{DL}}+A\cdot\sin(2\pi f_{\mathrm{EMD}}t_k+\theta) \tag{20a}$$

$$V_{\mathrm{TOT},k}^{\mathrm{IDL}}=V_{\mathrm{BIT}}^{\mathrm{IDL}}+A\cdot\sin(2\pi f_{\mathrm{EMD}}t_k+\theta+\phi) \tag{20b}$$

To simplify further equations, a frequency ratio is used, which is defined as

$$f_{\mathrm{ratio}}=\frac{f_{\mathrm{EMD}}}{f_{\mathrm{BIT}}}. \tag{21}$$

Using the definition of t_k from (19) in (20) leads to

$$V_{\mathrm{TOT},k}^{\mathrm{DL}}=V_{\mathrm{BIT}}^{\mathrm{DL}}+A\cdot\sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3}+\theta\right) \tag{22a}$$

$$V_{\mathrm{TOT},k}^{\mathrm{IDL}}=V_{\mathrm{BIT}}^{\mathrm{IDL}}+A\cdot\sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3}+\theta+\phi\right) \tag{22b}$$

Employing (22) in (18) leads to the condition that should be valid for the Adder to generate a warning.

$$\left|A\cdot\sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3}+\theta\right)+A\cdot\sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3}+\theta+\phi\right)\right|>V_{\mathrm{thresh}}^{\mathrm{det}} \tag{23}$$

3) SUBTRACTOR

Similarly, the Subtractor calculates the difference between the EMD-induced voltages in both DTLs. Afterwards, it eliminates the constant DC voltage and recalculates the absolute value. It generates a warning when this value exceeds the $V_{\mathrm{thresh}}^{\mathrm{det}}$ at any sample point, and this can be mathematically given as

$$||V_{\mathrm{TOT},k}^{\mathrm{DL}}-V_{\mathrm{TOT},k}^{\mathrm{IDL}}|-V_{\mathrm{DC}}|>V_{\mathrm{thresh}}^{\mathrm{det}} \tag{24}$$

The DTLs transmit logical '1's or '0's. Subtracting voltages of both DTLs leads to a $\pm V_{\mathrm{DC}}$ along with the difference of the EMD-induced voltage. Again using equations (22) in equation (24) leads to

$$\left|\left|\pm V_{\mathrm{DC}}+A\cdot\sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3}+\theta\right)-A\cdot\sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3}+\theta+\phi\right)\right|-V_{\mathrm{DC}}\right|>V_{\mathrm{thresh}}^{\mathrm{det}} \tag{25}$$

The A&S EMI detector will raise a warning if an EMD interferes with the transmitted data, and the equations (23) or (25) are valid. A CFN occurs when equations (15) or (16) are valid but the EMI detector does not generate a warning, i.e. (23) or (25) are invalid.

The proposed mathematical model makes it possible to assess the performance of an EMI detector for given levels of EMD-induced voltage, frequency, phase, and phase difference between DTLs. This approach offers an advantage over previous analyses by eliminating the need to transmit random data and adding the induced voltage to analyze performance for each case. Moreover, it facilitates a speedy evaluation for future design, in which sample points or numbers of samples are varied. Lastly, this model equips designers with a tool that will enable them to adjust EMI detector settings so they are optimized for operating within particular environmental settings.

D. PERFORMANCE EVALUATION

In order to analyse the performance of the A&S EMI detector, the mathematical model is implemented using MATLAB. Furthermore, the design is tested using Monte-Carlo based simulation framework as used in [6], [7], [8], and [16].

The voltages utilized for data transmission will always determine how the EMD-induced voltage will affect the transmitted data. As a result, the response of the EMI detector is examined utilizing a Signal-to-Interference Ratio (SIR).

It is defined as

$$\text{SIR} = 20 \cdot \log_{10}\left(\frac{V_{\text{BIT}}^{\text{RMS}}}{V_{\text{EMD}}^{\text{RMS}}}\right) \tag{26}$$

1) THEORETICAL SIMULATIONS

Several simulations have been performed to analyse the performance of the A&S EMI detector using the mathematical model. The EMD-induced voltage is added to the transmitted signal with varying amplitude, incoming phase, and phase difference between DTLs. The phase of the incoming EMD-induced voltage is varied from 0° to 359° with 10000 steps, the SIR from -50dB to 25dB with 1000 steps and, ϕ is kept at 10 degrees, and $V_{\text{thresh}}^{\text{det}}$ is fixed at one-third of the received voltage. The response of the A&S EMI detector is evaluated separately for the data line transmitting '1' and '0'. The overall probability of each condition given in Table 1 is calculated by:

$$\begin{aligned} P[\text{Condition}] = {} & P[\text{Condition}|1_{\text{Sent}}] * P[1_{\text{Sent}}] \\ & + P[\text{Condition}|0_{\text{Sent}}] * P[0_{\text{Sent}}] \end{aligned} \tag{27}$$

a: RESULTS

This subsection shows the performance of the A&S EMI detector assessed using the mathematical model. In the figures, the x-axis represents the SIR. The colors in the figure illustrate different conditions for assessing the performance of the EMI detector. When the interference is significantly weaker than the signal, the DTLs transmit data correctly, and the detector does not raise a warning. These cases are classified as data true positives (DTPs) and indicated by the green region in the figures. However, when the strength of the EMD-induced voltage increases, the EMI detector starts generating warnings even though data is being correctly transmitted. Ideally, these cases should not occur, as they compromise availability. They are shown using a yellow region as data false positives (DFPs). Furthermore, the cases when the EMD-induced voltage is significantly high and the EMI detector correctly detects bit errors due to EMI are shown by the salmon region as channel true positives (CTPs). In the presence of high EMD-induced voltage, the received bit can be correct, pure by luck. For example, if "one" is being transmitted and an EMD adds positive voltage to the signal, a voltage greater than two-thirds of the V_{BIT} is classified as high at the receiver end, and, hence, the received signal will appear correct even though a strong EMD is present. This category is shown in the results by the orange region indicating channel false positives (CFPs). Moreover, channel false negatives (CFNs), which should never happen, occur when the EMI detector fails to raise a warning while transmitted data is corrupted by EMI.

Results shown in the Figs. 2-5 are the average percentage of all possible cases of θ. Fig. 2 shows the response of the A&S EMI detector for $f_{\text{ratio}} = 1$. This figure clearly shows that the detector can detect EMI in all considered scenarios. The response also shows that the A&S EMI detector does not generate a warning when the SIR is high, i.e. DTPs. As the SIR decreases, DFPs followed by CFPs and CTNs are visible. The findings demonstrate that the detector can be used effectively to detect EMI in the DTLs for $f_{\text{ratio}} = 1$.

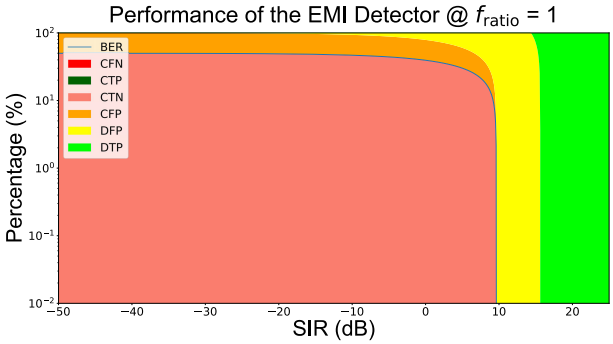

FIGURE 2. Evaluation of the A&S EMI Detector at $f_{\text{ratio}} = 1$.

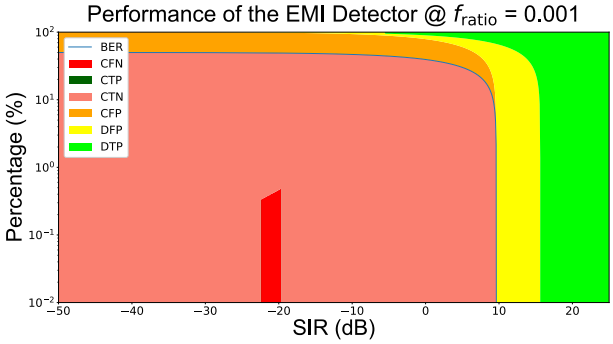

FIGURE 3. Evaluation of the A&S EMI Detector at $f_{\text{ratio}} = 0.001$.

In addition, an analysis was carried out to examine the performance of the EMI detector at a very low frequency ratio using $f_{\text{ratio}} = 0.001$, as shown in Fig. 3. The outcome of the analysis demonstrates that the EMI detector is not able to detect EMI at low values of f_{ratio} for the small range of SIR.

Furthermore, a frequency sweep is performed to identify a f_{ratio}, where the A&S EMI detector is not able to detect an EMD. Simulations are performed to analyse the response of the A&S EMI detector by varying the f_{ratio}. The f_{ratio} is varied from 0 to 7, while the SIR is kept at -20dB as shown in Fig. 4. The results of the frequency sweep show that the A&S EMI detector can effectively detect EMI in most cases. However, it generates CFNs when the frequency ratio is almost an integer multiple of the sampling rate.

Subsequent analysis is performed to investigate the response of the A&S EMI detector at a f_{ratio} multiple of the sampling rate. In the simulations, the f_{ratio} is kept constant while the SIR is varied. Fig. 5 shows the response of the A&S EMI detector when the f_{ratio}=3. The results demonstrate that the EMI detector can detect EMI in the majority of cases for the f_{ratio}=3, but there are some CFNs for a narrow range of the SIR.

2) FULL-WAVE SIMULATIONS

An in-house developed Monte Carlo based simulation framework is utilized to analyze the performance of the

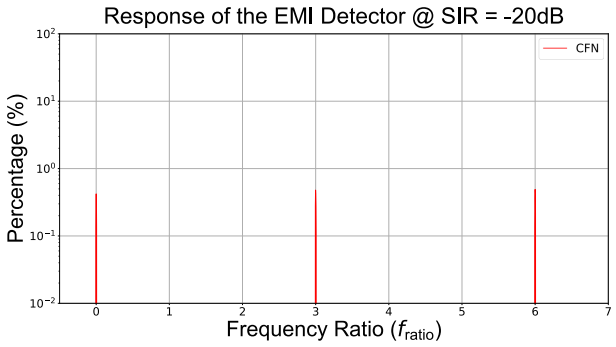

FIGURE 4. Evaluation of the A&S EMI Detector at frequency sweep from $f_{ratio} = 0$ to 7 and SIR = −20dB.

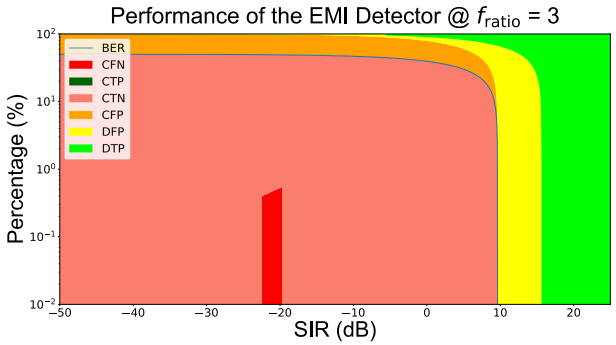

FIGURE 5. Evaluation of the A&S EMI Detector at $f_{ratio} = 3$.

EMI detector in a semi-reverberant environment that closely mimics real-world conditions. The applied EM disturbance in the simulation framework incorporates numerous occurring reflections, similar to those found in a reverberation room. In this study, Keysight Technologies' PathWave finite difference time domain (FDTD) solver is used to perform the full-wave simulations.

a: GEOMETRY UNDER STUDY

The performance of the EMI detector is investigated using a communication channel with a well-defined geometry (see Fig. 6). This communication channel is used in the simulation framework to transmit data and absorb an EMD. A single PCB with the dimensions of 10 cm x 16 cm and a thickness of 1.6 mm is used to model the communication channel. The FR4 substrate is employed to design the PCB, and the bottom layer of the PCB has a complete ground plane. The two DTLs are designed with a 3 mm width and a characteristic impedance of 50 ohms. However, the approach outlined is more generic and may be used with other types of wired communication channels than the one presented.

b: SIMULATIONS

The simulation framework, used for the analysis, takes into account all aspects of the reverberant environment and geometry, including the signal integrity and the EMD-induced voltages caused by an incoming EMD in the DTLs. It also takes into account the S-parameters of the DTLs' transmitter and receiver. To evaluate the accurate response of the signal, it takes into account resonances, characteristic

FIGURE 6. Geometry of the PCB Design.

TABLE 2. Angles of incidence: Statistical distribution.

Variable	Symbol	Distribution
Polar angle	θ_{inc}	$\cos^{-1} U(-1, 1)$
Azimuth angle	ϕ_{inc}	$U(0, 2\pi)$
Polarization angle	ψ_{inc}	$U(0, \pi)$
Phase angle	β	$U(0, 2\pi)$

impedance, mutual coupling, and time delay from transmitter to receiver [21].

In this analysis, a reverberating environment is simulated by using N=200 superimposed plane waves with random polar, azimuth, polarization, and phase angles. Specific statistical distributions of each angle are given in Table 2. To ensure the normalization of the superimposed waves, they are normalized by $E_N = E_0/\sqrt{N}$. To take into account the fluctuating characteristics of a reverberating environment, the simulation process is repeated M=10000 times, each time using a distinct set of plane waves. 100 random bits are transmitted over the DTLs for each analysis, and the behavior of the transferred data is evaluated.

In the simulation framework, the SIR is determined by using the average RMS EMD-induced voltage for a given incident field strength. First, the RMS EMD-induced voltage is computed for each reverb waveform, and then an average is taken over M waveforms to evaluate the final value.

The results in Fig. 7 show the performance of the A&S EMI detector in a semi-reverberant environment for a $f_{ratio} = 1$. Bits are transmitted at a bit frequency of 500 MHz, and the EMD frequency is also 500 MHz. The results show that the A&S EMI detector detects EMI in all circumstances for this analysis.

Fig. 8 shows the EMI detector's response for $f_{ratio} = 3$. In this analysis, a bit frequency of 166.666 MHz is used, and bits are transmitted at 500 MHz. The result indicate that the A&S EMI detector fails to detect EMI for a small range of SIRs. The response is analogous to the analysis shown in Fig. 5 for the A&S EMI detector.

Furthermore, analysis is performed to evaluate the response of the A&S EMI detector for EMDs of multiple frequencies. First, the analysis is performed for EMDs at two distinct frequencies: 400 MHz and 500 MHz, as shown in Fig. 9. Notably, one of these EMD frequencies is purposefully chosen to be non-multiple of the EMI detector's

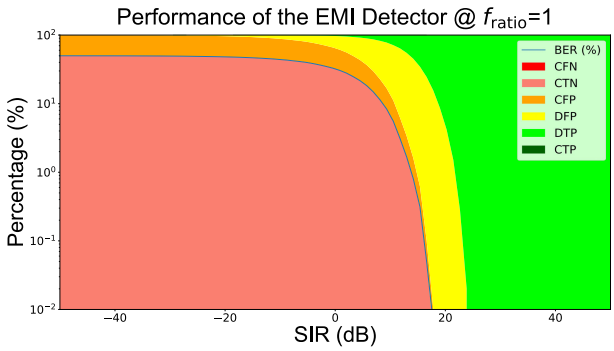

FIGURE 7. Evaluation of the A&S EMI Detector at f_{EMD} = 500 MHz and f_{BIT} = 500 MHz, line to line distance = 10 mm.

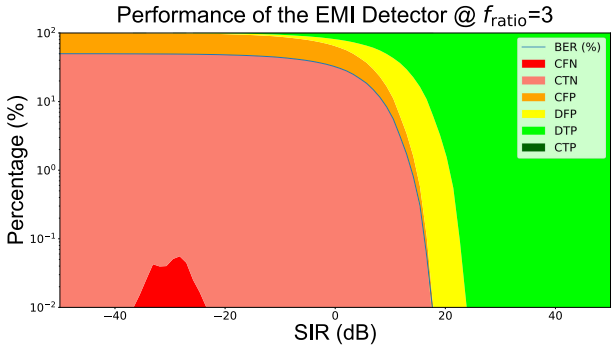

FIGURE 8. Evaluation of the A&S EMI Detector at f_{EMD} = 500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

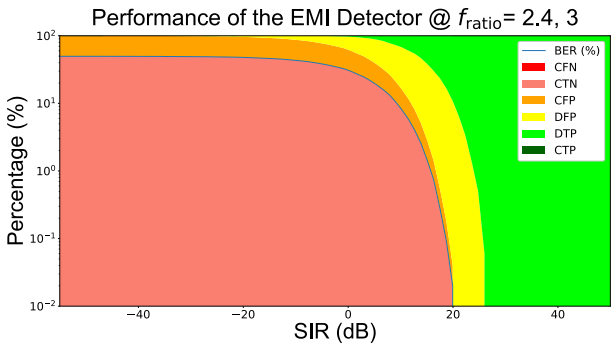

FIGURE 9. Evaluation of the A&S EMI Detector at Multiple EMDs of f_{EMD} = 400 MHz, 500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

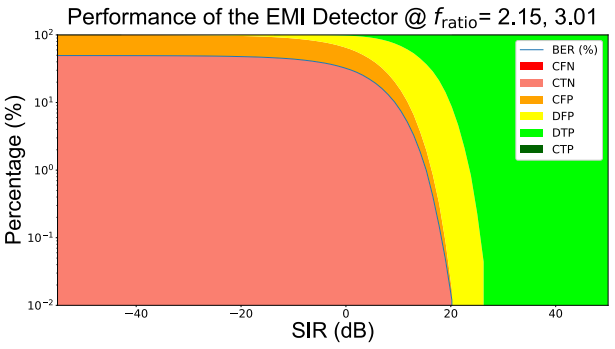

FIGURE 10. Evaluation of the A&S EMI Detector at Multiple EMDs of f_{EMD} = 359 MHz, 503 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

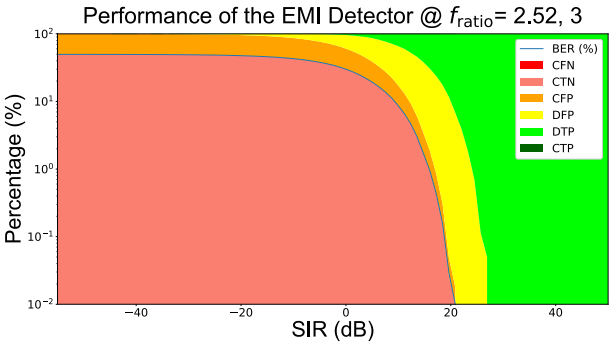

FIGURE 11. Evaluation of the A&S EMI Detector at Multiple EMDs of f_{EMD} = 421 MHz, 500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

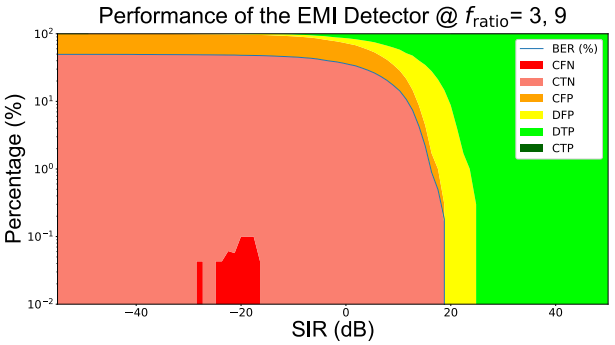

FIGURE 12. Evaluation of the A&S EMI Detector at Multiple EMDs of f_{EMD} = 500 MHz, 1500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

sampling rate. Results indicate that the A&S EMI detector can effectively detect bit errors in this case. For the all forthcoming analysis pertaining to the A&S EMI detector, M is set at 1000.

In addition, an analysis is performed to assess the performance of the A&S EMI detector for EMDs at frequencies of 359 MHz and 503 MHz, as shown in Fig. 10. Results reveal that the A&S EMI detector successfully detects bit errors due to EMDs and upholds its robust performance.

Further analysis is performed to evaluate the performance of the A&S EMI detector when the DTLs are exposed to EMDs with frequencies of 421 MHz and 500 MHz, as depicted in Fig. 11. As demonstrated in the analysis, the A&S EMI detector continues to show a strong ability to detect bit errors due to EMI.

Lastly, an analysis is performed to explore the response of the A&S EMI detector to EMDs at frequencies of 500 MHz and 1500 MHz, both multiples of the detector's sampling rate. The findings, as depicted in Fig. 12, reveal that the A&S EMI detector struggles to effectively detect bit errors under these specific conditions and generates CFNs. This observation highlights the previously identified limitation of the A&S detector: it fails to detect bit errors due to EMI when EMD frequencies align closely with or are integer multiples of its sampling rate. However, it's worth noting that the A&S EMI detector performs effectively when at least one frequency of the EMD is not a multiple of the sampling rate, showing its strong potential for deployment in complex electromagnetic environments.

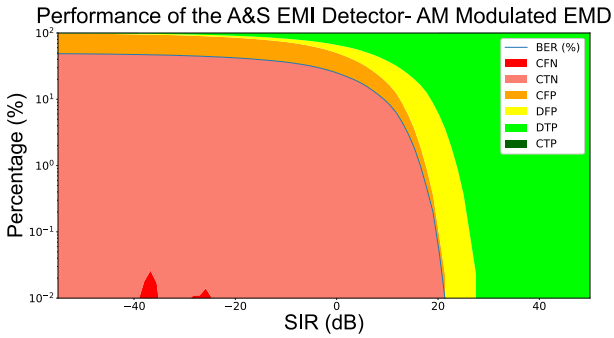

FIGURE 13. Evaluation of the A&S EMI Detector for AM Modulated EMD, f_{BIT} = 166.666 MHz and line to line distance = 10 mm.

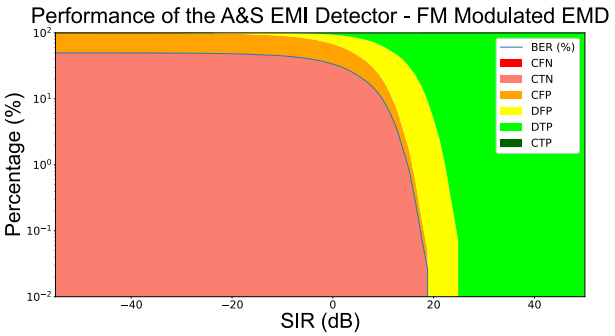

FIGURE 14. Evaluation of the A&S EMI Detector for FM Modulated EMD, f_{BIT} = 166.666 MHz and line to line distance = 10 mm.

AM and FM signals manifest a time-variant behavior; using them as sources of EMDs can add an added layer of complexity to the considered EM environment. This time dependence enables a more accurate depiction of the dynamism inherent in real-world EMI scenarios. An EMD induced voltage due to an AM modulated signal is defined as $V_{\text{EMD}} = (1 + \mu \cdot m(t)) \cdot A_c \sin(2\pi f_c t)$, where μ stands for the modulation index, which in this particular context equals 1. The signal at the baseband is symbolized by $m(t)$. A_c represents the carrier signal's amplitude, its frequency is $f_c = 500$ MHz, and t is the time.

In this analysis, the baseband frequency for AM signals is intentionally set at 20 kHz, with the carrier signal positioned at 500 MHz. This frequency allocation mirrors practical communication systems where the modulating (baseband) signal resides in the audio frequency range, such as 20 kHz, while the carrier signal is much higher, for instance, 500 MHz. Fig. 12 shows that the A&S EMI detector fails to detect bit errors in some cases. This is due to the fact that, despite the AM modulation, the carrier signal frequency is a multiple of the sampling rate, where the A&S EMI detector fails to work effectively, as shown earlier.

On the other hand, an EMD due to an FM modulated signal is characterized by the equation $V_{\text{EMD}} = A_c \cdot \cos\left(2\pi f_c t + \phi + \beta \int_0^t m(\tau)\, d\tau\right)$, depicting the temporal variability of the carrier frequency. In this equation, β is is defined as the ratio of the frequency deviation to the frequency of the modulating signal. For the purpose of this analysis, β is set to 1. In our analysis of FM modulation, we have selected a baseband frequency of 25 MHz, which falls within the frequency range typically utilized by wireless microphones. The carrier frequency has been consistently set at 500 MHz. Fig. 14 shows that the A&S EMI detector effectively identifies bit errors due to FM modulated EMI.

III. ADVANCED DESIGN OF THE EMI DETECTOR

A. DESIGN AND WORKING PRINCIPLE

The results of the preceding chapter show that CFNs emerge in certain cases for the A&S EMI detector. To evaluate the circumstances under which CFNs occur, we have undertaken a time domain analysis for both the Adder and Subtractor, as shown in Fig. 15. The vertical lines in Fig. 15 show the

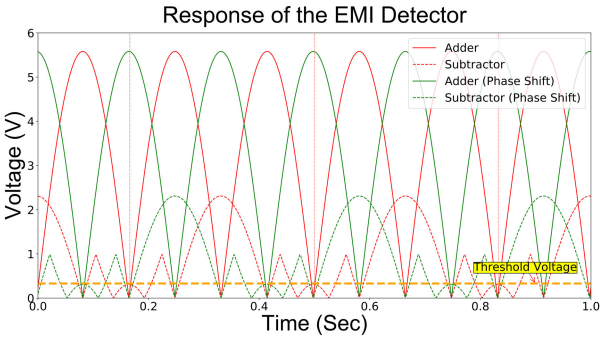

FIGURE 15. Induced voltage due to an EMD for the Adder and the Subtractor, with and without phase-shift.

sample points. It is observed by the analysis that when an EMD frequency is a multiple of the sampling rate, the sum and difference of the induced voltages on both DTLs can be less than the predefined threshold voltage $V_{\text{thresh}}^{\text{det}}$ for all sample points of a bit. Therefore, the A&S EMI detector fails to detect EMI, and CFNs occur. This happens when phase mismatch of the EMD-induced voltages in the DTLs induces voltages with opposite polarity in both DTLs.

It can also be observed in Fig. 15, shifting the phase of the added signal can make it detectable. The response also shows that the Subtractor is not beneficial in detecting EMI after adding a phase shift. Therefore, a new design of an EMI detector (Advanced EMI detector) is proposed in which the Subtractor is removed and the added signal is phase shifted using a phase shifter. Since the EMD's frequencies are often unknown, a phase shifter for the unknown frequency range can be designed utilizing the principles of a frequency-independent phase shifter described in [22], [23], [24], and [25].

Overall, the signal is processed twice by the Advanced EMI detector, with and without a phase-shift. The Advanced EMI detector aims to issue a warning whenever the EMD-induced voltage, with or without phase-shift, exceeds the pre-defined voltage threshold. The 90° phase-shift is selected for the analysis performed in this research as it can shift zeros of the added signal to a maxima. Fig. 15 also shows that the sum of an EMD-induced voltage that was undetectable by the A&S EMI detector, can be detected by utilizing a phase-shift of 90°. Nevertheless, if the phase difference is significantly

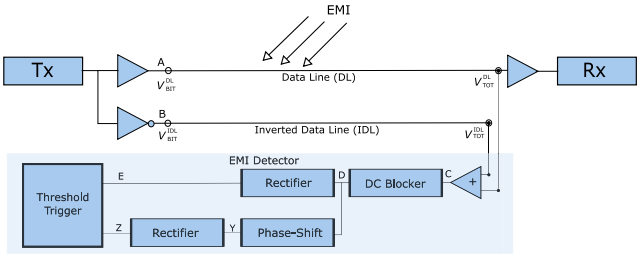

FIGURE 16. The Advanced EMI Detector - block diagram.

big, i.e., greater than 90°, the added voltages from the DTLs may stay below the specified threshold voltage, and the detector may fail to raise a warning.

B. MATHEMATICAL EVALUATION

For the Advanced EMI detector, additional equations for a phase shift block are defined, and equations for the Subtractor are removed. The equations below refer to the points given in Fig. 16. Equation (9) at point E for the Adder remains unchanged. However, for the phase shift block additional equations are added. The voltage at point D in the presence of an EMD can be written as

$$V_{\mathrm{D}} = A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta) + A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta + \phi) \tag{28}$$

The voltage at point Y after a ψ phase shift can be written as

$$V_{\mathrm{Y}} = A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta + \psi) + A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta + \phi + \psi) \tag{29}$$

The rectifier converts equation (29) to the absolute value. The voltage at point Z can be given as

$$V_{\mathrm{Z}} = |A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta + \psi) + A \cdot \sin(2\pi f_{\mathrm{EMD}} t + \theta + \phi + \psi)| \tag{30}$$

where ψ is dependent upon the introduced phase shift. In the proposed Advanced EMI detector ψ is equal to

$$\psi = \frac{\pi}{2} \tag{31}$$

To evaluate the EMD-induced voltage at each sample point with a 90° phase shift, t_k in equation (19) changes to

$$t_k = \frac{(2k-1)T_{\mathrm{BIT}}}{6} + \frac{T_{\mathrm{EMD}}}{4} = \frac{2k-1}{6f_{\mathrm{BIT}}} + \frac{1}{4f_{\mathrm{EMD}}} \tag{32}$$

Using equation (32), the EMD-induced voltage taken at the sample points of data and inverted data line can be written as

$$V^{\mathrm{DL}}_{\mathrm{EMI},k} = A \cdot \sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3} + \frac{1}{4f_{\mathrm{EMD}}} + \theta\right) \tag{33a}$$

$$V^{\mathrm{IDL}}_{\mathrm{EMI},k} = A \cdot \sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3} + \frac{1}{4f_{\mathrm{EMD}}} + \theta + \phi\right) \tag{33b}$$

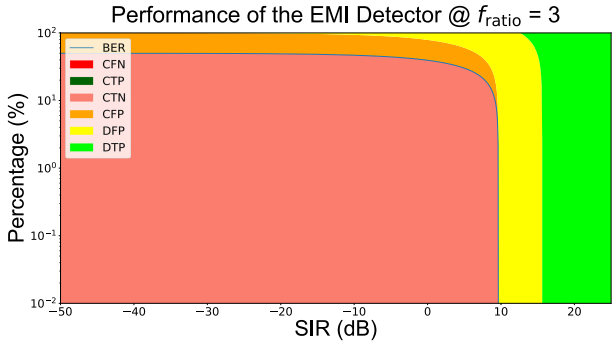

FIGURE 17. Evaluation of the Advanced EMI Detector at $f_{\mathrm{ratio}} = 3$.

The Advanced EMI detector will issue a warning when V_{E} or V_{Z} is more than $V^{\mathrm{det}}_{\mathrm{thresh}}$. The condition for V_{Z} to generate a warning can be written as

$$\left| A \cdot \sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3} + \frac{1}{4f_{\mathrm{EMD}}} + \theta\right) + A \cdot \sin\left(\frac{(2k-1)\pi f_{\mathrm{ratio}}}{3} + \frac{1}{4f_{\mathrm{EMD}}} + \theta + \phi\right) \right| > V^{\mathrm{det}}_{\mathrm{thresh}} \tag{34}$$

In the mathematical model of the Advanced EMI detector, the equations in (34) will be used instead of (25) to identify when the Advanced EMI detector can not detect an EMD. This is in addition to parallel detection of the EMI without a phase shift. The overall mathematical model of the Advanced EMI detector will not issue a warning when equations (23) or (34) are valid. The remaining conditions for a bit error and overall probability of CFNs stays the same as mentioned in equations (15), (16) and (27).

C. PERFORMANCE EVALUATION

To compare the performance of the Advanced EMI detector with that of the A&S EMI detector, an analysis is performed in a similar setup, utilizing the modified mathematical model and the Monte-Carlo based simulation framework.

1) THEORETICAL SIMULATIONS

The performance of the Advanced EMI detector is evaluated by using the same setup as for the A&S EMI detector but with an updated mathematical model. In this design, the phase of the added signal is shifted by 90°. Fig. 17 shows the performance of the detector when the f_{ratio} is 3 and the phase difference of the EMD-induced voltages in both lines is 10°. The result illustrates that the Advanced EMI detector can identify bit error for a $f_{\mathrm{ratio}} = 3$, at which the A&S EMI detector was not able to do so for the complete range of SIR analysed.

The Advanced EMI detector is also analysed at very low values of f_{ratio}. Previously, the A&S EMI detector was unable to identify EMI at low values of f_{ratio}. The response in Fig. 18 shows that the Advanced EMI detector can also recognize EMI at $f_{\mathrm{ratio}} = 0.001$.

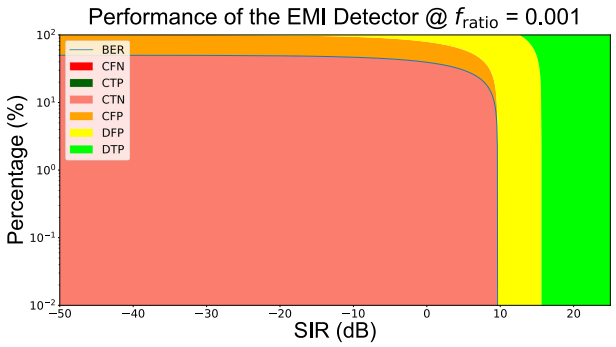

FIGURE 18. Evaluation of the Advanced EMI Detector. $f_{ratio} = 0.001$.

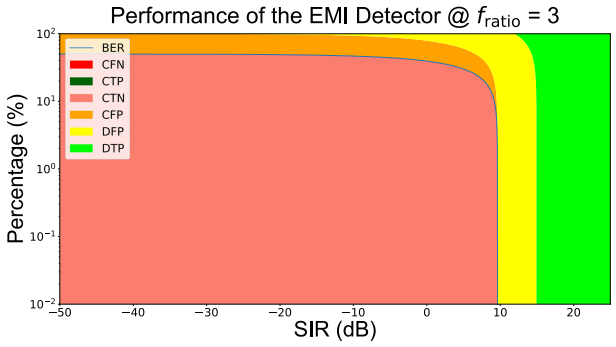

FIGURE 19. Evaluation of the Advanced EMI Detector at $f_{ratio} = 3$, and $\phi = 45°$.

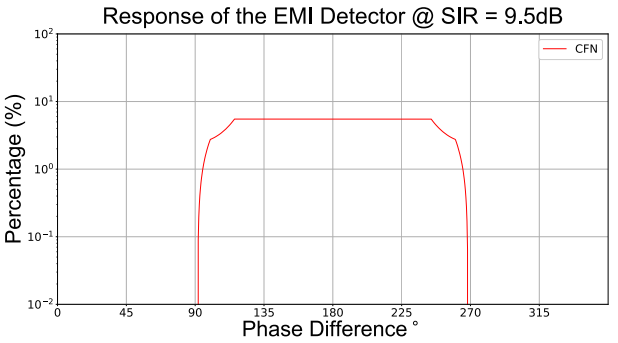

FIGURE 20. Evaluation of the Advanced EMI Detector to phase difference ϕ between DTLs @ SIR = 9.5dB.

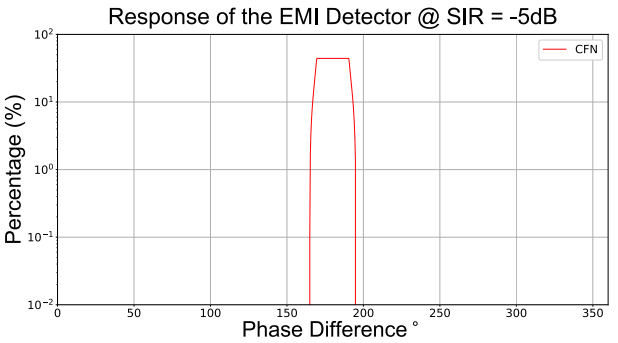

FIGURE 21. Evaluation of the Advanced EMI Detector to phase difference ϕ between DTLs @ SIR = -5dB.

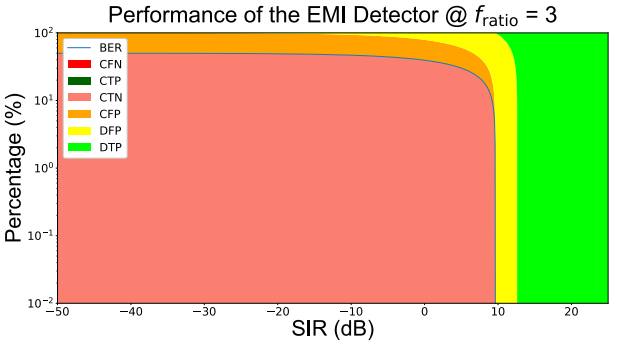

FIGURE 22. Evaluation of the Advanced EMI Detector to phase difference ϕ of the EMD-induced voltage between DTLs = 90°.

To analyse another vital aspect of the Advanced EMI detector, the phase difference ϕ of the EMD-induced voltage between the DTLs is increased from 10° to 45°. The phase difference ϕ is directly related to the EMD frequency and distance between both DTLs. Increasing the ϕ increases the difference of the EMD-induced voltage between the DTLs. Results in Fig. 19 illustrate that the Advanced EMI detector can also detect EMDs with significantly large values of ϕ.

In addition, a phase difference sweep is performed to examine the performance of the Advanced EMI detector to the phase difference of the EMD-induced voltage between the DTLs. As the EMI detector fails to detect bit errors due to EMI for a narrow range of SIR values, the values of SIR are carefully examined, and a 9.5 dB SIR is selected for this analysis. This value is selected with the aim of observing the maximum range of phase differences where CFNs occur. All parameters are kept constant in this analysis, while the phase difference of the induced voltage is increased from 0° to 360°. Fig. 20 shows the response of the Advanced EMI detector to varying phase differences between DTLs for a $f_{ratio} = 3$. The results show that the detector can effectively detect EMI when a phase difference of EMD-induced voltage between DTLs is greater than 90 degrees (the phase-shift added by the Advanced EMI detector).

Furthermore, the impact of the phase difference of the EMD-induced voltages between the DTLs is investigated by decreasing the SIR to -5 dB. Results in Fig. 21 illustrate that the range of the phase difference of the EMD-induced voltage decreases while the percentage of CFNs increases. However, the EMI detector works effectively for a larger phase difference of the EMD-induced voltage in this case. Nevertheless, it may fail to detect EMI if an EMD induces a voltage with a significant phase difference between DTLs.

The response of the EMI detector is further investigated when the phase difference of the EMD-induced voltage is 90°, i.e., equal to the phase-shift given by the Advanced EMI detector to the added signal. Analysis is performed at a $f_{ratio} = 3$, and the results in Fig. 22 demonstrate that the EMI detector performs effectively in all considered cases.

In addition, the performance of the EMI detector is assessed when the phase difference of the EMD-induced voltage is greater than the phase shift given by the Advanced EMI detector. For this analysis, the EMD-induced voltage is set to 100°. The analysis is again performed at a $f_{ratio} = 3$. The results in Fig. 23 demonstrate that the EMI detector starts generating CFNs for a small range of SIR around 9.5 dB.

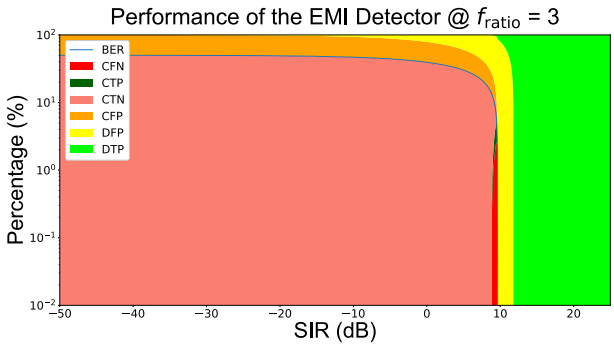

FIGURE 23. Evaluation of the Advanced EMI Detector to phase difference ϕ of the EMD-induced voltage between DTLs = 100°.

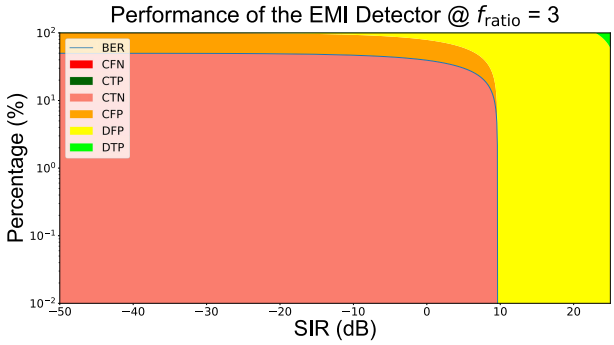

FIGURE 24. Evaluation of the Advanced EMI Detector at $f_{ratio} = 3$, and $V_{thresh}^{det} = 0.1$V.

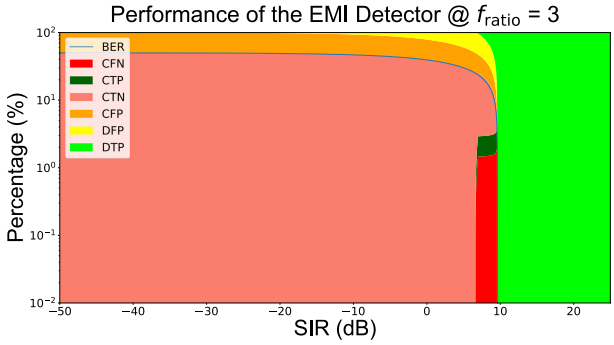

FIGURE 25. Evaluation of the Advanced EMI Detector at $f_{ratio} = 3$ and $V_{thresh}^{det} = 0.66$V.

In order to analyse the effect of change in V_{thresh}^{det}, the design is tested by using different values of V_{thresh}^{det}. Simulations are performed by using a V_{thresh}^{det} of 0.1V and 0.66V, shown in Fig. 24 and Fig. 25. The response of the Advanced EMI detector shows that decreasing V_{thresh}^{det} increases EMI detection, reduces DTPs and increases DFPs. On the other hand, increasing the V_{thresh}^{det} can decrease detection and lead to the occurrence of CFNs.

The overall analysis shows that the Advanced EMI detector works effectively in all analysed cases when the phase difference is not very large, i.e., not greater than the phase shift given by the detector. The phase difference of the induced voltage between DTLs is dependent on distance and frequency. Therefore, at very high frequencies, even at a small distance, an EMD may induce a voltage with a substantial

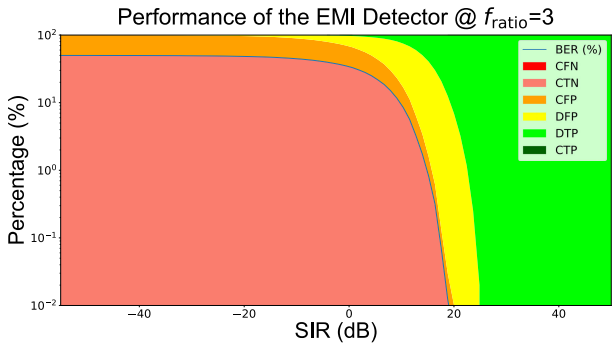

FIGURE 26. Evaluation of the Advanced EMI Detector at f_{EMD} = 500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 20 mm.

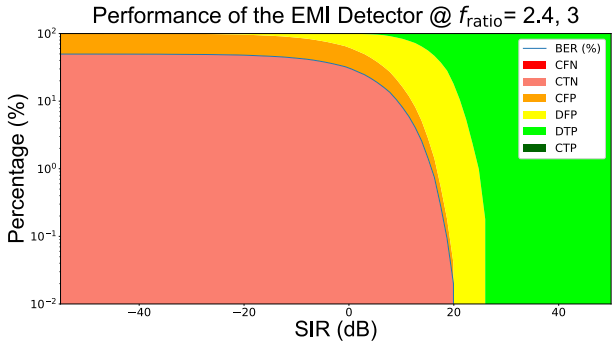

FIGURE 27. Evaluation of the Advanced EMI Detector at multiple EMDs of f_{EMD} = 400 MHz, 500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

phase difference between DTLs, which the detector may not detect.

2) FULL-WAVE SIMULATIONS

The Monte-Carlo simulation framework is also used to examine the performance of Advanced EMI detector in a semi-reverberant environment. The simulation framework's fundamental architecture is the same as that of the A&S EMI detector. Nevertheless, in order to assess the phase shift in the simulation framework, each bit is sampled 360 times. The samples are delayed according to the EMD frequency to achieve a 90-degree phase shift for the EMD-induced voltage.

The evaluation of the Advanced EMI detector to the EMD frequency of 166MHz and the bit frequency of 500MHz is shown in Fig. 26, indicating $f_{ratio} = 3$. The analysis is performed using the same frequencies as shown in Fig. 8 for the A&S EMI detector, but the distance between DTLs is doubled. It can be observed that even with greater distances between DTLs, the Advanced EMI detector detects EMI for the whole range of SIR.

Furthermore, the performance of the Advanced EMI detector is analysed when DTLs were subjected to a multi-frequency EMDs. This is done to evaluate its effectiveness in complex electromagnetic environment. In the forthcoming analysis, the phase shift is given by using the Hilbert transform, as used in [26] and [27]. Fig. 27 showcases the detector's efficacy in identifying bit errors associated with

TABLE 3. Comparison of existing techniques for detecting bit errors due to EMI.

	Error Detection Codes (EDCs) [28]	Field strength probes [12]/ Antenna-based ultrawideband EMD detector [15]	Comparator based EMI Detector [16]	A&S EMI Detector [11]	Advanced EMI Detector [18]
Requirements	• Data blocks transmission • Redundant data transmission • Post processing	• Extra hardware	• Pair of DTLs • Extra hardware	• Pair of DTLs • Extra hardware	• Pair of DTLs • Extra hardware
Limitations	• Different EDCs fail for various data types [28], [29] • Latency	• Large number of Data False Positives (DFPs) • Challenging placement for lengthy communication channel	• Fails when EMI inverts data in both DTLs	• Fails for frequencies multiple to the detector sampling rate	• Works effectively when DTLs are closer to each other, which is generally the case

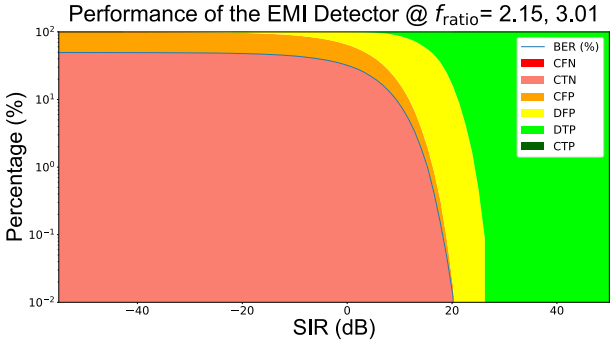

FIGURE 28. Evaluation of the Advanced EMI Detector at multiple EMDs of f_{EMD} = 359 MHz, 503 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

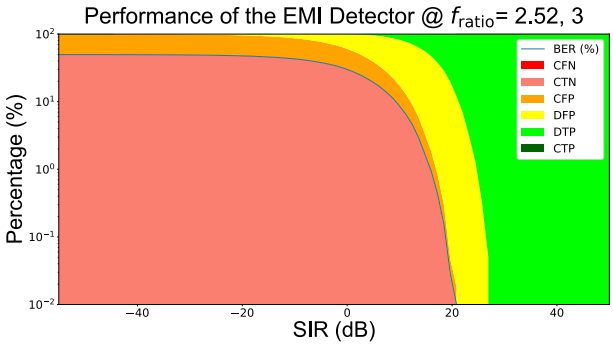

FIGURE 29. Evaluation of the Advanced EMI Detector at multiple EMDs of f_{EMD} = 421 MHz, 500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

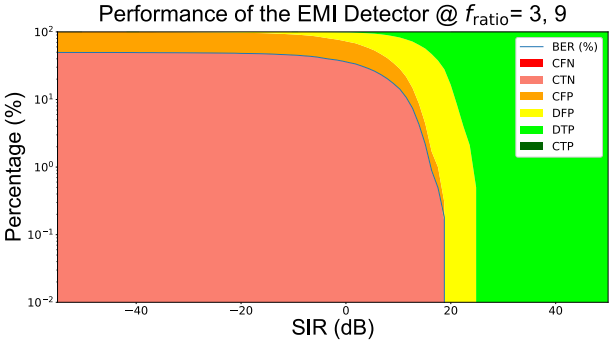

FIGURE 30. Evaluation of the Advanced EMI Detector at multiple EMDs of f_{EMD} = 500 MHz, 1500 MHz and f_{BIT} = 166.666 MHz, line to line distance = 10 mm.

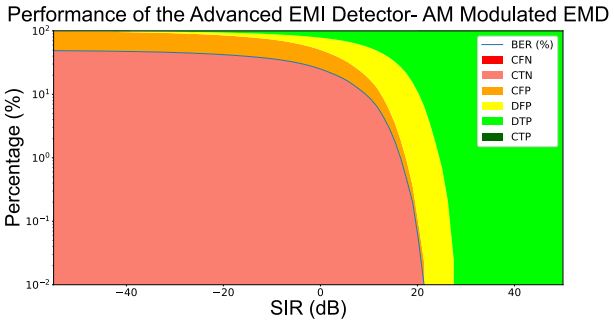

FIGURE 31. Evaluation of the Advanced EMI Detector for AM Modulated EMD, f_{BIT} = 166.666 MHz and line to line distance = 10 mm.

EMDs with frequencies of 400 MHz and 500 MHz. M=1000 for all subsequent analyses.

Broadening the scope, the performance of the advanced EMI detector was examined for EMDs at frequencies of 359 MHz and 503 MHz, both of which are not multiples of each other. Fig. 28 shows the response of the Advanced EMI detector, and it can be observed that it is capable of detecting bit errors at these EMD frequencies.

In the analysis demonstrated in Fig. 29, the DTLs are subjected to EMDs at frequencies of 421 MHz and 500 MHz. Results show that the Advanced EMI detector once again validates its ability to successfully detect bit errors due to EMI.

The Advanced EMI detector is further analyzed for EMDs at frequencies of 500 MHz and 1500 MHz, both integer multiples of the detector's sampling rate. This additional level of analysis sheds light on its performance in comparison to the limitations of the A&S EMI detector. The Advanced EMI detector adeptly identifies bit errors, overcoming the shortcomings observed in its A&S EMI detector, as illustrated in Fig. 30.

Further evaluations are also carried out to understand the detector's behavior under AM and FM modulated EMDs. The Advanced EMI detector maintains its effectiveness under these modulated conditions. For the AM-modulated EMDs, the carrier frequency was fixed at 500 MHz, and the baseband signal was set at 20 kHz. Other parameters are also aligned with the parameters used in the A&S EMI detector analysis. The Advanced detector successfully identifies bit errors for AM modulated EMD, as presented in Fig. 31.

Moreover, the performance of the Advanced EMI detector is analyzed when DTLs are subjected to FM modulated EMDs. In this instance, the baseband frequency is 25 MHz, the same as used in the analysis of the A&S EMI detector, and the carrier frequency is 500 MHz. Results in Fig. 32 show that the Advanced EMI detector effectively detects bit errors in all considered cases.

These combined results underline the Advanced EMI detector's capabilities and versatility in addressing a diverse

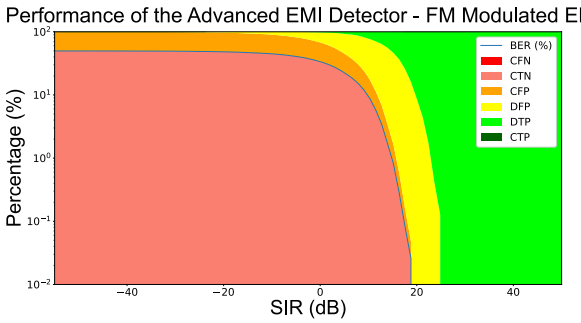

FIGURE 32. Evaluation of the Advanced EMI Detector for FM Modulated EMD, f_{BIT} = 166.666 MHz and line to line distance = 10 mm.

and dynamic range of EM scenarios. The detector's ability to handle multiple frequencies and AM and FM modulated EMI, underscores its value in complex, real-world EM environments.

IV. CONCLUSION

A comprehensive study is conducted to analyse the performance of the A&S and the Advanced EMI detector in the light of the novel EMI condition assessment definitions. This analysis is carried out by using the designed mathematical model for each EMI detector and a Monte-Carlo based simulation framework which depicts a real-like semi-reverberant environment. The research concludes that the Advanced EMI detector outperforms the A&S EMI detector by detecting EMI in all considered cases when the DTLs are relatively close to each other. However, research also shows that when an EMD-induces a voltage with a large phase difference between the DTLs, the Advanced EMI detector may fail to detect EMI. The focus of this article was on radiated EMD, but it is anticipated that the detectors will also function the same way for conducted EMD. The comparison of the A&S and the Advanced EMI detectors to existing technologies along with their requirements and limitations is provided in Table 3, and it can be observed that the Advanced EMI detector is comprehensively better than the existing technologies.

The mathematical model presented in this paper can be effectively used to evaluate the limitations of an EMI detector, and it can equip modeling of the design for a specific electromagnetic environment, e.g., for a specific phase-difference between EMD-induced voltage in a particular frequency range. The proposed model takes into consideration crucial parameters that can impact transmitted data over a wired communication channel. Validation with simulations demonstrates the proposed model is effective for evaluating the performance of the EMI detectors, and it can be used for future research in this field. Future work should focus on the hardware design of the Advanced EMI detector. Studies are also needed to reduce the associated cost and hardware requirements of the EMI detector. In addition, future research is required to evaluate the performance of both EMI detectors for other kinds of noise, including pulsed, broadband or random noise. Attention is also needed to design an EMI detector for a wired communication channel with higher availability.

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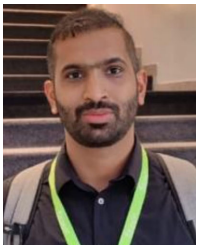

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