IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 9 June 2023, accepted 7 July 2023, date of publication 13 July 2023, date of current version 20 July 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3294995

RESEARCH ARTICLE

Model Predictive Control Algorithm for Prolonging Lifetime of Three-Phase Voltage Source Converters

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This work was supported in part by the National Research Foundation of Korea (NRF) Grant funded by the Korea Government, Ministry of Science and ICT (MSIT), under Grant 2020R1A2C1013413; and in part by the Technology Development Program to Solve Climate Changes through NRF funded by MSIT under Grant 2021M1A2A2060313.

ABSTRACT One of the key goals of power electronics is to reduce losses in three-phase converters in order to increase efficiency and reduce thermal stress, which can lengthen the lifetime of devices. However, the aforementioned studies do not account for the fact that the phase legs of the converter can experience various aging conditions, which reduces the expected lifetime of converter. This paper proposes a minimum loss per-phase method based on predictive control for voltage source inverter, which aims at particularly reducing loss of specific phase leg to increase the lifetime of the entire converter. The output currents will be controlled using predicted reference voltages and predictive zero-sequence voltage injection in the proposed technique. The particular phase leg, which is the most aged leg, will be clamped to the positive and negative dc-link to generate a non-switching region. This will result in the reduction of switching frequency and switching loss of the most aged phase leg in the voltage source inverter, which prolongs the lifetime of the particular phase leg and entire converter. The results of simulation and experimentation are used to confirm the validity of the proposed method and effectiveness in increasing lifetime of converter, where the switching loss of the most aged leg is reduced by up to 85%, and corresponding lifetime increases by about four times compared to the conventional model predictive control method.

INDEX TERMS Switching loss, model predictive control, per-phase, thermal reduction, lifetime.

I. INTRODUCTION

The two-level three-phase voltage source inverter (VSI) is a well-liked power converter that has a wide range of applications, including uninterruptible power supply, back-to-back converters in wind turbine systems, and electric drive systems [1], [2], [3], [4]. This converter topology is widely recognized, trustworthy, and relatively easy to control. The most vulnerable parts of a power converter are the dc-link capacitor accounting for 30%, whereas power semiconductors are 21% of components. The main source of stress in power semiconductors is a high temperature, which is caused by power semiconductor losses [5], [6], [7], [8]. One of the main reasons for power module failure, according to research, is thermal stress. Thermal stress, which is caused by power loss, speeds up the deterioration of semiconductor devices and reduces the system's dependability. From several previous studies and data surveys, the deterioration of the power converter's components, particularly the power modules, is mostly caused by thermal stress, which ultimately leads to the power converter's failure. One of the most susceptible parts of the power converter is the power circuit, which is constructed using a number of semiconductor devices. The thermal stress indicated previously is the main root of

The associate editor coordinating the review of this manuscript and approving it for publication was Sze Sing Lee.

failure [5], [9], [10]. During the operation, the semiconductor devices conduct and switch at high current, which causes a substantial power loss. At the chip junction, a significant quantity of heat is stored as a result of this loss accumulation. The junction temperature rapidly increases in this manner. Bond cables, soldering layers, and direct-bond copper, among other materials inside the power module, repeatedly undergo temperature rises and falls and endure mechanical changes at various coefficients of thermal expansion. The interface may experience crack and void problems that grow until an unanticipated separation is created. Different failure modes are specified based on the location of this separation, such as bond-wire liftoff and solder joint fatigue [5]. Conduction losses, leakage current losses, and switching losses all raise the temperature of the switching components. Static losses that are dependent on device technology include conduction losses and leakage current losses. Alternatively, altering the switching frequency might affect switching losses in addition to other variables. Therefore, reducing switching losses to keep the thermal stress as small as possible is a crucial target, which leads to an increased lifetime of the converter [11], [12].

The three main methods for reducing switching losses are decreasing the voltage or current of switches during commutation [13], [14], [15], adjusting the switching time interval [16], [17], [18], [19], or changing the number of commutations in the fundamental period [20], [21], [22], [23], [24], [25]. System reliability is decreased by the additional hardware, complexity, and control that soft-switching and advanced gate drivers demand [26]. Nevertheless, modulation strategies and switching frequency variation might be improved to reduce thermal stress, which do not need to use additional hardware. The simplest approach to achieve thermal control is to adjust the switching frequency as it has a direct influence on the power switching losses without notably affecting the operating point of the application when adjusted within system constraints. The method in [20] and [21] conducts a hysteresis controller using calculated junction temperature variation to reduce switching frequency to its lowest level when the junction temperature variation of switching devices is higher than a certain level. The reduction of switching frequency lowers corresponding switching loss of the entire converter. In [22], the switching sequence with the least number of commutation is selected to reduce the switching loss of the thermal overloading power device. The alternative approaches based on using discontinuous pulse-width modulation (DPWM) are widely used for reducing switching frequency [23]. The fundamental concept behind DPWM is to clamp the voltage reference of the converter output to either the upper or lower dc-link potential within a specific interval. This ensures that the corresponding power device remains in its current state without switching, leading to a decrease in switching losses within that interval. The switching frequency and corresponding switching loss can be decreased by about 33% and 50%, respectively. The use of DPWM can also be applied to cascaded/paralleled converter system as in [24] and [25].

In the three-phase converter, each phase leg could have a different aging condition or an expected lifetime, which may be caused by uneven stress during operation or by the failure of a switch and the consequent replacement. Additionally, manufacturing methods have been identified as a potential source of failure for power semiconductor devices. To increase the reliability of the entire VSI, however, the aforementioned active thermal control approaches do not account for the fact that the phase legs of the converter can experience various aging conditions. As indicated earlier, the soft-switching and advanced gate driver techniques require additional hardware, control, and complexity though they can particularly reduce the power loss of specific switches.

Model predictive control (MPC), a nonlinear control technique, has recently been increasingly used in power electronics control as a result of advancements in microprocessors [27], [28]. A converter topology with a specific level has a finite number of switching states; thus, MPC heuristically chooses the best switching state from among the possibilities by minimizing the objective function. According to authors in [29], a linear low-pass filter can be added to the cost function as a way to reduce power loss when employing MPC. The filter excludes predicted switching states consuming more power to lower thermal stress. Nevertheless, this linear filter, which is very dependent on the problem formulation of MPC, might be incorrect by nonlinear constraints. Therefore, it is not advised to include nonlinear constraints in the objective function. The ability of MPC to simultaneously handle numerous targets is a key benefit [27], [28]. In the conventional MPC method aiming at reducing switching loss, the additional cost function corresponding to the number of switching transitions will be added in addition to other control variables such as output currents, power, etc. [30]. In [31], the authors include various constraints corresponding to thermal stress as device junction temperature spread, power losses, maximum device temperature, etc., in a predicted cost function to control thermal of electric drive converters. However, it leads to the requirement of tuning the weighting factor for each term of cost function, increasing complexity of the method, and the added cost function might decrease the output performance of converter.

In this article, a minimum loss per-phase method based predictive control for VSI is introduced to particularly reduce the loss of a specific phase leg, which leads to increases of VSI's lifetime and reliability. Different from conventional MPC, the proposed minimum loss per-phase method based predictive control method uses modified predicted reference voltages to regulate the output current and achieve switching loss reduction in a particular phase leg. A predictive zero-sequence voltage is generated and injected to the predictive reference voltage of desired phase leg, which clamps the corresponding phase leg to either positive or negative dc-link rails. It is possible to create a non-switching region without any switching

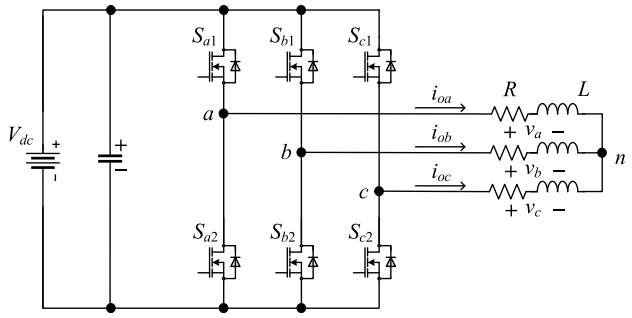


FIGURE 1. Typical configuration of two-level three-phase VSI.

activity by injecting the predictive zero-sequence voltage, which prevents the required phase leg from being switched at any instant. The remainder of this article's information is arranged as follows. In Section II, the conventional MPC used in two-level three-phase VSIs is investigated. For the switching loss reduction strategy, the proposed minimum loss per-phase method-based predictive control is described in Section III. Simulation and experimental results are presented and analyzed in Section IV. Section V evaluates the impact of proposed method on lifetime extension. Finally, Section VI concludes this article.

II. MODEL PREDICTIVE VOLTAGE CONTROL FOR VOLTAGE SOURCE INVERTER

Fig. 1 depicts the typical circuit of a two-level, three-phase VSI. This system contains a dc-source, a two-level three-phase converter, and a $R-L$ load. i_{ox} $(x = a, b, c)$ is phase output current, and v_x $(x = a, b, c)$ is the converter voltage. S_{x1} and S_{x2} $(x = a, b, c)$ stand for the upper and lower switching states of the converter leg, respectively.

Applying Kirchhoff's law to the VSI circuit, the equations for the load current dynamic can be written as

$$v_x = Ri_{ox} + L\frac{di_{ox}}{dt} \quad (x = a, b, c) \tag{1}$$

The predictive model is a basic element of predictive current control, which is used to predict the system's future output according to previous information about the object. Hence, to realize the current control strategy, the forward Euler algorithm is applied to (1), and the discrete-time expression of (1) is acquired as

$$i_{ox}(k+1) = \left(1 - \frac{RT_{sp}}{L}\right) i_{ox}(k) + \frac{T_{sp}}{L} v_x(k) \quad (x = a, b, c) \tag{2}$$

where T_{sp} is the sampling time. In accordance with (2), the converter voltage and current at time instant k, indicated by $v_x(k)$ and $i_x(k)$ $(x = a, b, c)$, respectively, determine the current at time instant $k+1$, $i_x(k+1)$ $(x = a, b, c)$. Since the converter generates a total of eight switching states, the converter voltage $v_x(k)$ can be any one of the eight voltage vectors listed in Table 1. As a result, any one of the eight

TABLE 1. Available switching states and converter phase voltage of three-phase VSI.

Voltage vectors	Switching state			Converter voltage		
	S_a	S_b	S_c	v_a	v_b	v_c
V_0	0	0	0	0	0	0
V_1	0	0	1	$-V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$
V_2	0	1	0	$-V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$
V_3	0	1	1	$-2V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$
V_4	1	0	0	$2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$
V_5	1	0	1	$V_{dc}/3$	$-2V_{dc}/3$	$V_{dc}/3$
V_6	1	1	0	$V_{dc}/3$	$V_{dc}/3$	$-2V_{dc}/3$
V_7	1	1	1	0	0	0

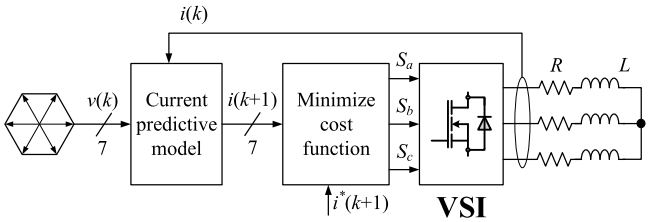


FIGURE 2. Control diagram of MPCC.

current vectors derived using (2) may be predicted to represent the current at time instant $k+1$, $i_x(k+1)$ $(x = a, b, c)$. A cost function is consequently needed in order to assess the predictions and is defined as follows:

$$g_i = \left|i_x^*(k+1) - i_x(k+1)\right| \tag{3}$$

where the reference current for time instant $k+1$ is represented by $i_x^*(k+1)$. Determining the switching state that will minimize the cost function specified in (3) and applying it to the converter is how MPCC is implemented. Fig. 2 depicts the control diagram corresponding to MPCC.

In traditional MPCC, the goal is to choose a voltage vector that will bring the predicted current $i_x(k+1)$ as closely as possible to its reference $i_x^*(k+1)$. One may determine predicted reference voltage $v_x^*(k)$ by taking into account the projected current in (2) and then using the following formula. Equation (2) may be changed by substituting $i_x(k+1)$ with $i_x^*(k+1)$, and after rearranging the equation, (4) can be yielded as

$$v_x^*(k) = \frac{1}{T_{sp}}\left\{Li_{ox}^*(k+1) + \left(RT_{sp} - L\right) i_{ox}(k)\right\} \tag{4}$$

As stated in Eq. (4), if the converter voltage acting at time instant k can be adjusted to be the same as v_x^*, then the current $i_x(k+1)$ will be precisely identical to its reference $i_x^*(k+1)$. Table 1 shows available switching states and corresponding converter voltage vectors. Given the cost function below, the current predictive control must thus choose one voltage from a set of eight voltage vectors that satisfies the requirement:

$$g_v = \left|v_x^*(k) - v_x(k)\right| \quad (x = a, b, c) \tag{5}$$

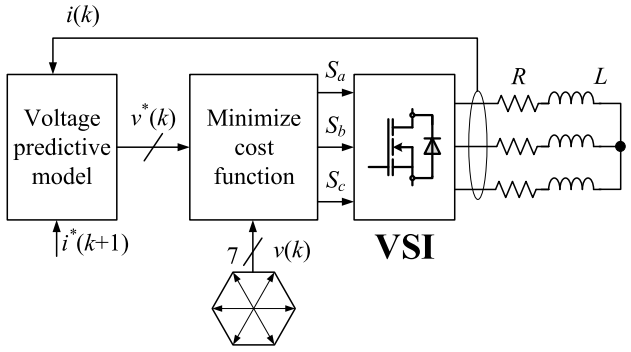


FIGURE 3. Control diagram of MPC using predicted reference voltage.

By calculating which voltage vector is closest to the "required voltage vector" $v_x^*(k)$, it is possible to determine the switching state that should be applied to the power converter at time instant k. Fig. 3 illustrates the control diagram of MPVC.

III. PROPOSED MINIMUM LOSS PER-PHASE METHOD BASED PREDICTIVE CONTROL

As for the aforementioned analysis, the phase legs of the power converter might have different aging conditions due to the manufacturing process, uneven thermal stress distribution, and earlier replacement. This leads to the difference in the remaining useful lifetime among phase legs. Because the converter will stop working if one phase leg is broken, it is necessary to increase the remaining useful lifetime of the most aged leg. A basic idea of an increased lifetime of most aged devices is decreasing their specific operating frequency, which results in reducing switching loss. However, the output performance of VSIs might decline with a decrease in switching frequency. Additionally, inappropriately reducing the switching frequency of one phase leg in VSI will deteriorate the output currents. Theoretically, a straightforward strategy is to include a term in the cost function that measures the number of switches that alter when the switching state $S_x\,(k)\,(x = a, b, c)$ changes in order to directly assess the decrease in the number of switching actions. The switching states at time instant k is applied with respect to the previously switching state $S_x\,(k-1)\,(x = a, b, c)$. The generated cost function can be described as [26]

$$g = \left|i_x^*\,(k+1) - i_x\,(k+1)\right| + \lambda_n \times n \tag{6}$$

where n is the number of switching actions that change when the switching state $S_x\,(k)\,(x = a, b, c)$ is applied and λ_n is a weighting factor. The difference of the number of switching actions from time instant $k-1$ to time instant k, n, is

$$n = \sum_{x=a,b,c} |S_x\,(k) - S_x\,(k-1)| \tag{7}$$

The reduction of switching frequency will increase along with the rise of weighting factor λ_n value. However, the output current might deteriorate, and the minimum switching loss for a particular phase leg cannot be achieved.

To achieve the reduction of switching loss in a particular phase leg of converter without using the additional cost function term corresponding to switching frequency, in this study, the simplified MPC using predicted reference voltage in (4) is modified by adding a predictive zero-sequence voltage. The predictive zero-sequence voltage is produced in such a way that the particular phase converter reference voltage in (4) with predictive zero-sequence voltage injection connects the corresponding phase to the upper or lower dc-link rail to create the non-switching region. First, the three-phase predicted reference voltages acquired by the voltage model in (4), i.e., $v_a^*\,(k)$, $v_b^*\,(k)$, and $v_c^*\,(k)$, are normalized by dividing them by the peak value. It is possible to acquire the normalization's peak value via

$$V_{peak}\,(k) = \sqrt{\left(v_\alpha^*\,(k)\right)^2 + \left(v_\beta^*\,(k)\right)^2} \tag{8}$$

where $v_\alpha^*\,(k)$ and $v_\beta^*\,(k)$ are the α and β components obtained by the abc-to-$\alpha\beta$ transformation. The filtered normalized reference voltages, calculated in (4), are shown in Fig. 4. In this study, phase a leg is considered the most aged. The available non-switching region and switching region can be selected on the basis of the instantaneous magnitude of the corresponding phase leg. It can be seen that the available non-switching region corresponds to the interval that the normalized reference voltage of phase $av_{na}^*\,(k)$ is $v_{max}^*(k)$ or $v_{min}^*(k)$, where the switching state can be forced to stop changing. Meanwhile, at the available switching region, which relates to the medium voltage $v_{mid}^*(k)$, the phase leg of VSI should be prevented from being clamped to guarantee that VSI operates precisely in the linear modulation range. As shown in the previous studies, adding the same zero-sequence voltage signal to three-phase reference voltages does not change the line-to-line voltage per carrier cycle average value. Therefore, to reduce the switching frequency of phase a without deteriorating the output current performance, the predictive zero-sequence voltage $v_{ZSV}\,(k)$ will be calculated differently following the available non-switching and switching regions of the assumed most aged phase a leg as follow:

$$\begin{cases} v_{ZSV}\,(k) = 1 - v_{max}^*\,(k) & if\ v_{max}^*\,(k) = v_{na}^*\,(k) \\ v_{ZSV}\,(k) = -1 - v_{min}^*\,(k) & if\ v_{min}^*\,(k) = v_{na}^*\,(k) \\ v_{ZSV}\,(k) = -\dfrac{v_{max}^*\,(k) + v_{min}^*\,(k)}{2} & other\ cases \end{cases} \tag{9}$$

It can be seen from Fig. 4 the maximum angle of the available non-switching region is 120° in each positive or negative dc-link rail. Using (9), the waveforms of filtered reference voltages, the predictive zero-sequence voltage, and corresponding modified reference voltages after adding the predictive zero-sequence voltage are illustrated in Fig. 5. In this case, it should be noted that phase a is considered the most aged leg, which needs to reduce its switching frequency to extend the lifetime of phase leg a and the entire VSI. Following (9), the generated predictive zero-sequence voltage

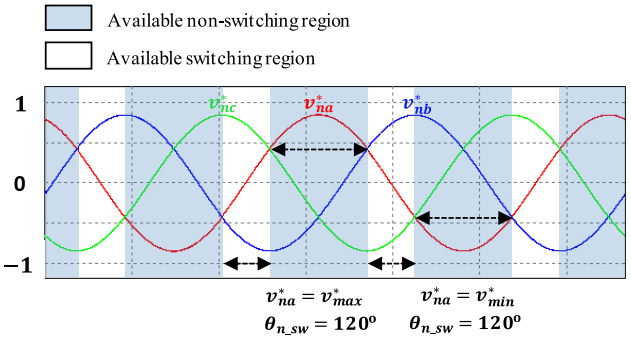


FIGURE 4. Filtered normalized reference voltage of VSI.

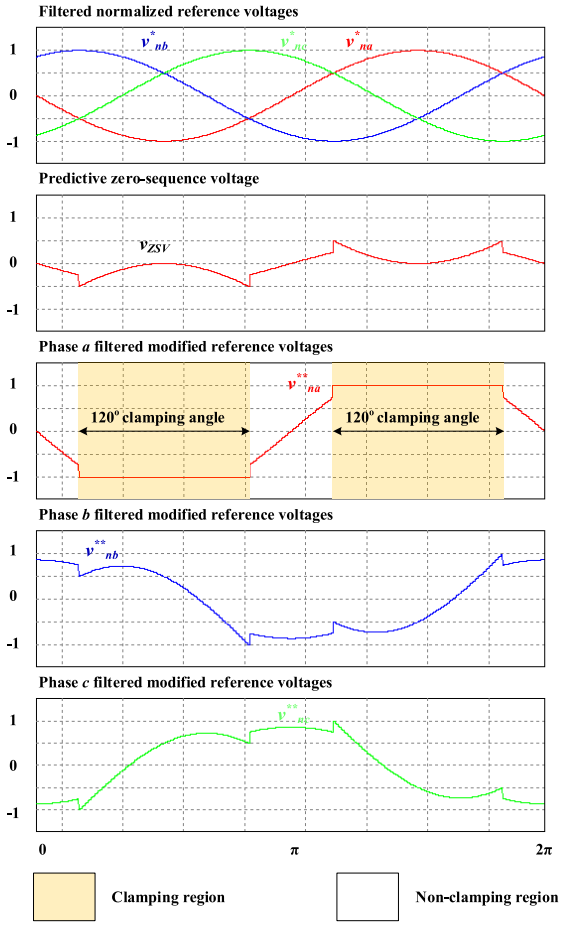


FIGURE 5. Filtered normalized reference voltages, predictive zero-sequence voltage, and filter modified reference voltages obtained from (9).

will be added to three-phase reference voltages. Thus, phase a modified reference voltage contains the clamping region of 120° in both positive and negative dc-link rail. Meanwhile, phases b and c do not contain clamping regions.

The different non-switching regions can be realized by modifying (9) by using upper and lower limits for the magnitude of reference phase voltage, as shown in (10). The non-switching region $\theta_{n_{sw}}$ will range from 0° to 120°. If $\theta_{n_{sw}} = 120°$, (10) will be the same as (9).

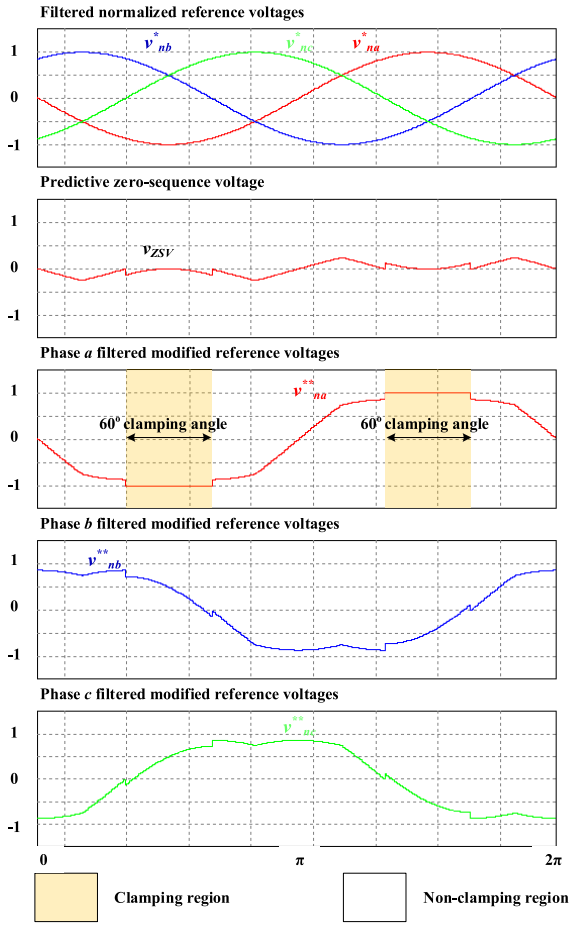


FIGURE 6. Filtered normalized reference voltages, predictive zero-sequence voltage, and filter modified reference voltages obtained from (10) by setting the non-switching region $\theta_{n_{SW}} = 60°$.

Fig. 6 depicts the waveforms of filtered reference voltages, the predictive zero-sequence voltage, and corresponding modified reference voltages after adding the predictive zero-sequence voltage obtained from (10) by setting the non-switching region $\theta_{n_{sw}} = 60°$. In this case, phase a is also considered the most aged leg, which needs to reduce its switching frequency to extend the lifetime of phase leg a and the entire VSI. Following (10), the generated predictive zero-sequence voltage $v_{ZSV}(k)$ will be added to three-phase reference voltages. Thus, phase a modified reference voltage contains the clamping region of 60° in both positive and negative dc-link rail. Meanwhile, phases b and c do not contain clamping regions.

$$\begin{cases} v_{ZSV}(k) = 1 - v^*_{max}(k) & if\ v^*_{na}(k) \geq \cos\left(\theta_{n_{sw}}/2\right) \\ v_{ZSV}(k) = -1 - v^*_{min}(k) & if\ v^*_{na}(k) \leq -\cos\left(\theta_{n_{sw}}/2\right) \\ v_{ZSV}(k) = -\dfrac{v^*_{max}(k) + v^*_{min}(k)}{2} & other\ cases \end{cases} \tag{10}$$

Fig. 7 shows the flowchart for the generating of a predictive zero-sequence voltage. The normalized modified predicted

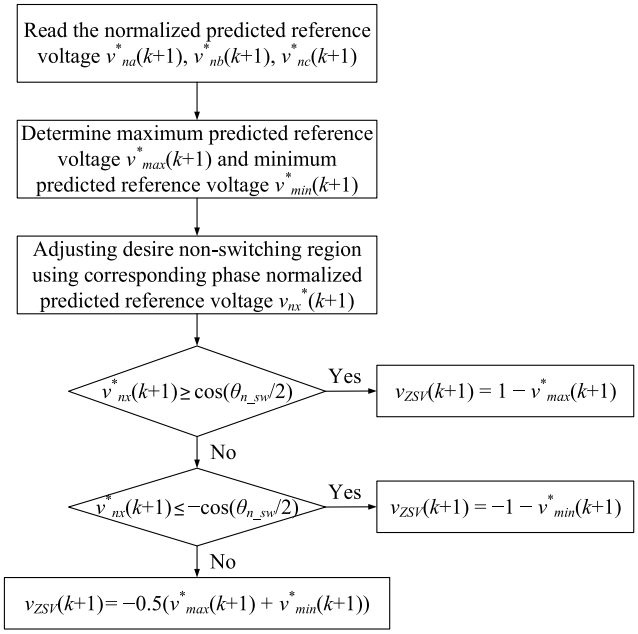


FIGURE 7. Flowchart of the predictive zero-sequence voltage generation in the proposed minimum loss per-phase method based predictive control.

reference voltage $v^{**}_{nx}(k)$ with predictive zero-sequence voltage injection will be calculated as:

$$v^{**}_{nx}(k) = v^*_{nx}(k) + v_{ZSV}(k) \quad (x = a, b, c) \tag{11}$$

The normalized term $v^{**}_{nx}(k)\,(x = a, b, c)$ will be multiplied by a normalization factor to obtain the desired modified predicted reference voltage $v^{**}_{x}(k)\,(x = a, b, c)$. The modified predicted reference voltage $v^{**}_{x}(k)\,(x = a, b, c)$ with predictive zero-sequence voltage injection is assessed using a cost function that is specified as

$$g_v = \left|v^{**}_x(k) - v_x(k)\right| \quad (x = a, b, c) \tag{12}$$

To reduce negative impact on control and operation of proposed approach, the controller's delay is taken into account, and the voltage model in (4) is implemented one step forward. Then the predicted reference voltage at $(k+1)$ th instant is acquired as

$$v^*_x(k+1) = \frac{1}{T_{sp}}\left\{Li^*_x(k+2) + \left(RT_{sp} - L\right) i_x(k+1)\right\} \tag{13}$$

To obtain the one-step predicted output current $i_x(k+1)$ $(x = a, b, c)$ required in (13), the measured output current $i_x(k)$ and the VSI voltage $v_x(k)$ from (4), are used. Furthermore, the one-step and two-step predicted reference currents, $i^*_x(k+1)$ and $i^*_x(k+2)\,(x = a, b, c)$, can be determined using the Lagrange extrapolation as in [26], which can be expressed as follows

$$i^*_x(k+1) = 3i^*_x(k) - 3i^*_x(k-1) + i^*_x(k-2) \tag{14}$$

$$i^*_x(k+2) = 3i^*_x(k+1) - 3i^*_x(k) + i^*_x(k-1) \tag{15}$$

Finally, the modified predicted reference voltage with predictive zero-sequence voltage injection is, assessed by a cost function specified as

$$g_v = \left|v^{**}_x(k+1) - v_x(k+1)\right| \quad (x = a, b, c) \tag{16}$$

The available switching states and the corresponding converter voltages are shown in Table 1 previously. Following [32], the use of the cost function in (16) cannot guarantee the precise selection of switching states corresponding to zero voltage vector. The improper selection of zero voltage vector may result in unwanted switching operations, increasing the switching loss. As a result, the polarity of the predictive zero-sequence voltage is taken into consideration while choosing the zero voltage vectors. As in [32], zero voltage vectors V_0 and V_7 are employed when the predictive zero-sequence voltage v_{ZSV} is negative and positive, respectively. Fig. 8 displays the overall block drawing of the proposed minimum loss per-phase method based predictive control method. As can be seen in Fig. 8, the three-phase predicted reference voltages achieved by the inverse dynamic model in (13), i.e., $v^*_a(k+1)$, $v^*_b(k+1)$ and $v^*_c(k+1)$, are normalized by dividing them with the peak value to limit their magnitude within ± 1. The three-phase normalized predicted reference voltages $v^*_{na}(k+1)$, $v^*_{nb}(k+1)$ and $v^*_{nc}(k+1)$ will be used to calculate the predictive zero sequence voltage $v_{ZSV}(k+1)$ corresponding to the most aged leg. The three-phase normalized modified reference voltage $v^{**}_{na}(k+1)$, $v^{**}_{nb}(k+1)$ and $v^{**}_{nc}(k+1)$, generated after adding $v_{ZSV}(k+1)$ as in (11), are multiplied by a normalization factor to produce three-phase modified predicted reference voltages $v^*_a(k+1)$, $v^*_b(k+1)$ and $v^*_c(k+1)$. These modified predicted reference voltages are assessed by the cost function in (16) to generate optimal switching pattern for two-level three-phase VSI.

By comparing the block diagram of the conventional MPC method and proposed minimum loss per-phase method based predictive control technique, the difference between the conventional and proposed MPC methods is only the predicted zero-sequence voltage generation part. This part is added to modify the predicted reference voltages for control purpose of reducing switching loss and thermal stress of the most aged leg. It also becomes evident that the proposed minimum loss per-phase method based predictive control technique with offset voltage injection can be implemented without requiring any additional components. Also, it does not need extra information about the load power factor since the algorithm uses the known sampled values of the reference voltage to determine the appropriate switch to clamp for every sampling period. With this proposed MPC strategy, the VSI with the most aged leg can operate with minimum switching losses at any operating point, irrespective of the steady-state or transient conditions.

The proposed minimum loss per-phase method based predictive control that uses the cost function selects the optimal switching state, which can generate the optimal output voltage state closest to the modified predicted reference volt-

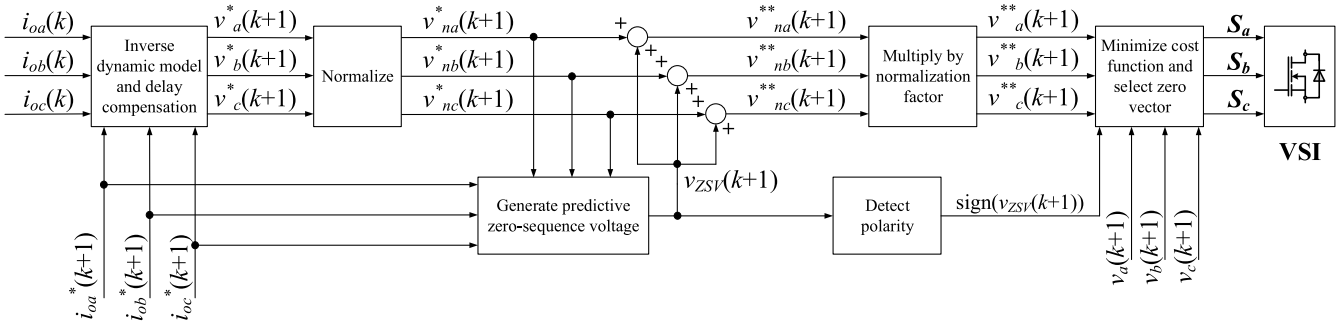


FIGURE 8. Block diagram of the proposed minimum loss per-phase method based predictive control with predictive zero-sequence voltage generation.

TABLE 2. Parameter of two-level three-phase VSI.

Parameters	Value
DC-link voltage V_{dc} (V)	200
DC-link capacitance (μF)	680
Load resistance R (Ω)	10
Load inductance L_f (mH)	10
Load angle (degree)	20
Sampling frequency (kHz)	20
Fundamental frequency (Hz)	60
Reference current (A)	5

age. The predicted reference voltage is modified to ensure clamping of the most aged leg to decrease the corresponding switching loss and guarantee satisfactory output current performance.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The developed minimum loss per-phase MPC method was simulated using the PSIM program for a three-phase VSI. Table 2 displays the two-level three-phase VSI parameter.

Fig. 9 presents the phase output currents and switching patterns waveforms using the conventional MPCC and the proposed minimum loss per-phase method based predictive control with $\theta_{n\_sw} = 0°$. It can be observed that the noticeable difference between the two control schemes is the switching pattern. In Fig. 9(a), the conventional MPCC method implemented in this study uses the zero-voltage vector V_0 to generate a corresponding zero switching state. When using the traditional MPCC approach, the x-phase ($x = a, b, c$) clamps to the negative dc-link without switching operations. This results in switching pulse patterns with spontaneous clamping periods. It should be observed that when the conventional MPCC technique uses the zero state V_7, the x-phase ($x = a, b, c$) clamps to the positive dc-link with the same interval. However, in Fig 9(b), due to the zero-voltage vector is selected following the polarity of predictive zero-sequence voltage v_{ZSV}, the resulting switching pattern of the proposed minimum loss per-phase method based predictive control is different from that of the conventional MPCC. Regarding the output performance, the proposed minimum loss per-phase method based predictive control with $\theta_{n\_sw} = 0°$ produces the sinusoidal and correct phase output currents as the conventional MPCC. The output current correctly follows the corresponding reference current. The total harmonic distortion (THD) findings from the two algorithms are similar to one another, coming in at roughly 3.83%.

Fig. 10 shows the simulation results of the proposed minimum loss per-phase predictive method at different clamping angles where phase a is considered the most aged phase leg. It can be seen that in both four cases of clamping angle, the output currents are sinusoidal and correct in terms of phase and magnitude. The filtered modified reference voltage of phase a and the predictive zero-sequence voltage are presented for clarity. The proposed minimum loss per-phase method based predictive control stops switch S_{a1} of the VSI from switching following the non-switching region generated by the modified predicted reference voltage.

Fig. 11 displays the performance of the proposed minimum loss per-phase method based predictive control after changing the clamping angle. Fig. 11(a) illustrates the change of output current THD along with the rise of the clamping angle. The clamping angle $\theta_{n\_sw} = 30°$ has the lowest output current THD compared to other clamping angles. However, the difference in output current THD at various clamping angles is negligible. The insignificant change in terms of output current THD can be explained from (4), where it expresses that the output current $i_x(k+1)$ and its reference $i^*_x(k+1)$ will be correctly identical if the converter voltage vector acting at time instant k can be managed to the same as the predicted reference voltage v^*_x. However, it leads to an increase in switching loss in the two remaining phase legs. It can be noticed by observing Fig. 11(a) and 11(b), the switching frequency of phase a is significantly decreased thanks to the non-switching region, where the reduction of switching frequency is about 75%. Meanwhile, the switching frequency of the two remaining phases increases by about 50%. Fig. 11(c) shows the change of phase a conduction loss and switching loss following the change of clamping angle. When the clamping angle is lower than 60°, the switching loss of phase a decreases along with the increase of clamping angle. The

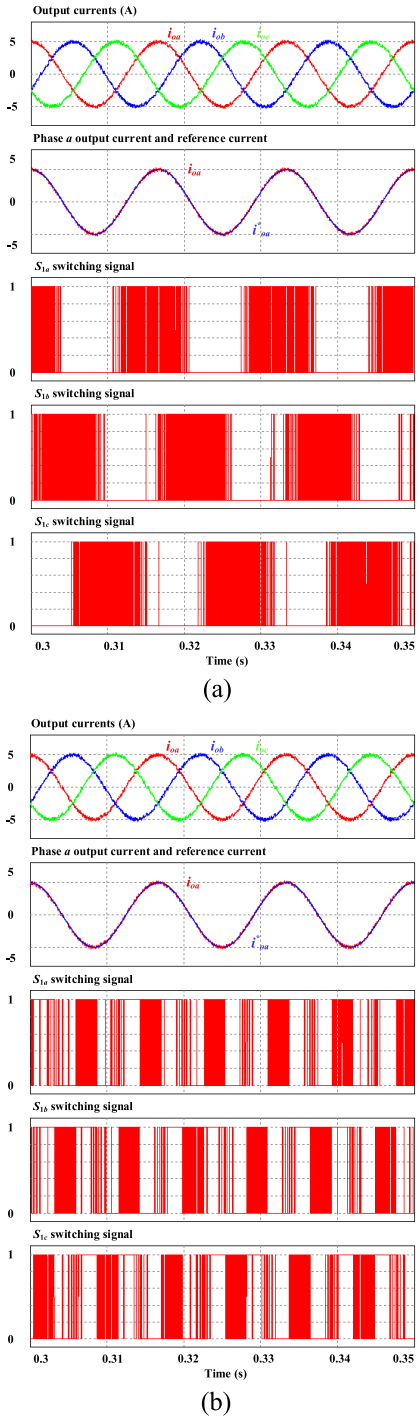


FIGURE 9. Output currents and switching patterns waveforms acquired by (a) conventional MPCC, (b) proposed method with $\theta_{n\_sw} = 0°$.

switching loss does not decrease anymore when the clamping angle is higher than 60°. Additionally, the conduction loss has a minor increase due to the reduction of switching loss. Although the switching loss of phase a reduces significantly, the total loss of VSI following the change of clamping angle varies slightly due to the increase of loss in two remaining phase legs.

Fig. 12 shows the performance comparison in terms of loss between two control schemes, including conventional MPCC and the proposed method. The proposed method with the clamping angle $\theta_{n\_sw} = 120°$ is used for comparison. It is seen that the proposed method can decrease the switching loss of a particular phase by 85% compared to the conventional MPCC approach. The conduction loss of the proposed method slightly increases compared to the conventional method. In terms of VSI total loss, the difference between the two control schemes is negligible. Thus, the proposed method can achieve the minimum loss for a particular phase leg.

B. EXPERIMENTAL RESULTS

The VSI prototype is built for experimental verification, as shown in Fig. 13. The common IGBTs are used as bidirectional switches. The conventional MPCC and proposed approaches are implemented on Texas Instruments Digital Signal Processor TMS320F28335. The ac power supply is the dc source from Keysights. The parameters and conditions are the same as in the simulation model, as given in the previous section.

Fig. 14 presents the waveforms of phase a output current, switching pattern, and filtered reference voltage acquired by conventional method in experimental implementation. It can be noticed that the experiment waveforms are the same as the simulation waveforms. As shown in Fig. 14, because of the uses of the zero-voltage vector V_0 to generate a corresponding zero switching state, the conventional MPCC method generates the switching patterns with spontaneous clamping periods, where the x-phase ($x = a, b, c$) clamps to the negative dc-link without continuous switching operations. Phase a output current is sinusoidal and correct in terms of phase and magnitude.

Fig. 15 shows the waveforms of phase a output current, switching pattern, and filtered reference voltage acquired by proposed method with clamping angle $\theta_{n\_sw} = 60°$ in experimental implementation. The simulated waveforms of Fig. 10(b) and the experimental results of Fig. 15 are matching. The output current is sinusoidal and correct in terms of phase and magnitude. The filtered reference voltage of phase a contains 60° clamping region in both positive and negative side. The corresponding switching pattern of phase a has non-switching region also.

Fig. 16 presents the waveforms of phase a output current, switching pattern, and filtered reference voltage acquired by the proposed method with clamping angle $\theta_{n\_sw} = 120°$ in experimental implementation. It should be indicated that this is the maximum clamping angle that one phase leg can achieve in the proposed method. The experimental waveforms of Fig. 16 are similar to the simulation results of Fig. 10(d). The output current is sinusoidal and correct in terms of phase and magnitude. The filtered reference voltage of phase a contains 120° clamping region in both positive and negative side. The corresponding switching pattern of phase

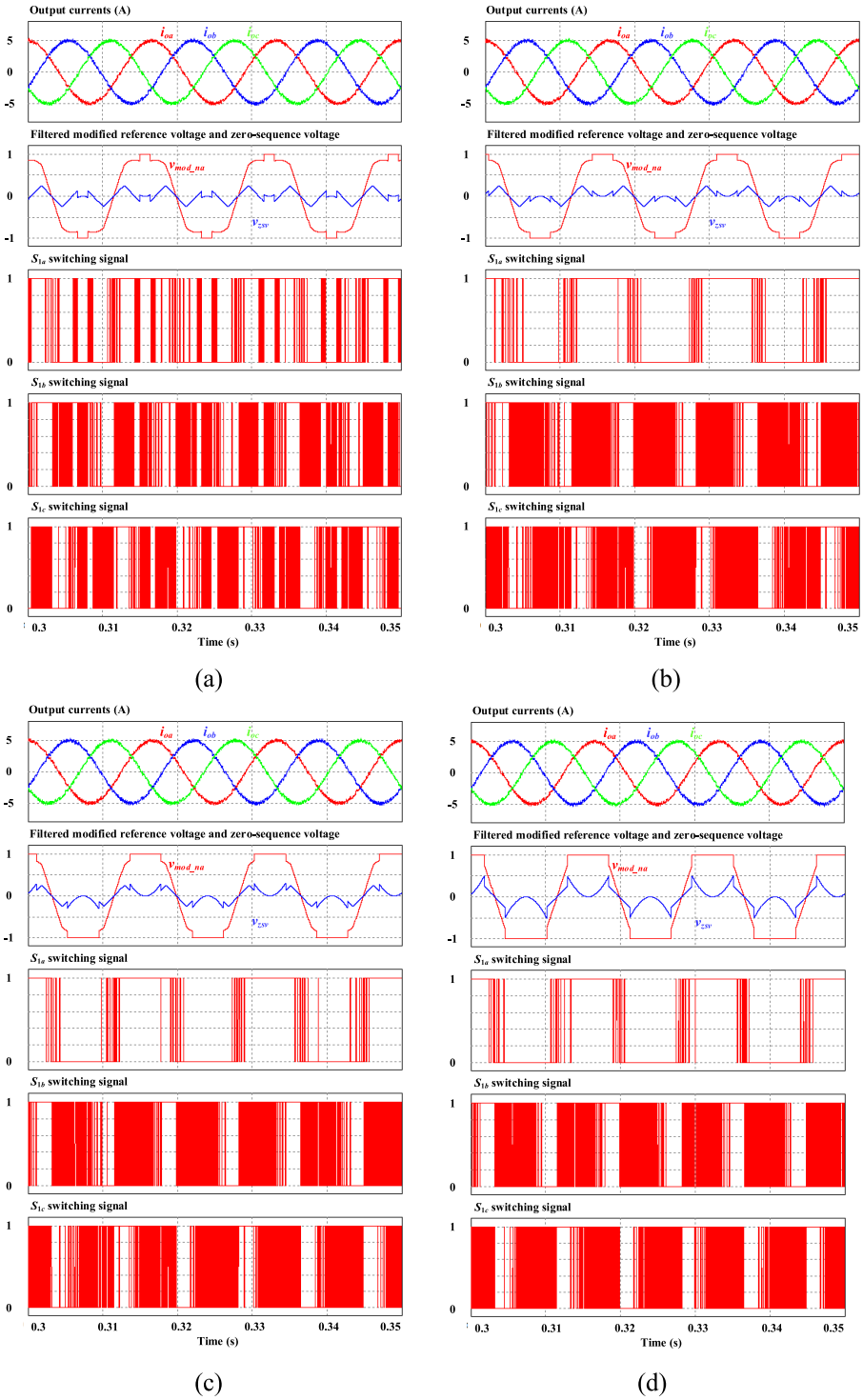


FIGURE 10. Output currents and switching patterns waveforms acquired by proposed method with (a) $\theta_{n\_sw} = 30°$, (a) $\theta_{n\_sw} = 60°$, (a) $\theta_{n\_sw} = 90°$, (a) $\theta_{n\_sw} = 120°$.

a has a non-switching region also. The switching pattern of phase an in Figs. 15 and 16 show that the switching frequency has been reduced in comparison to the traditional approach. Additionally, this also verifies the accuracy of the proposed method.

The experimental waveforms show an identical result to the simulation waveforms. Additionally, they verify the ability of reducing switching frequency and switching loss for a particular phase by using the proposed method.

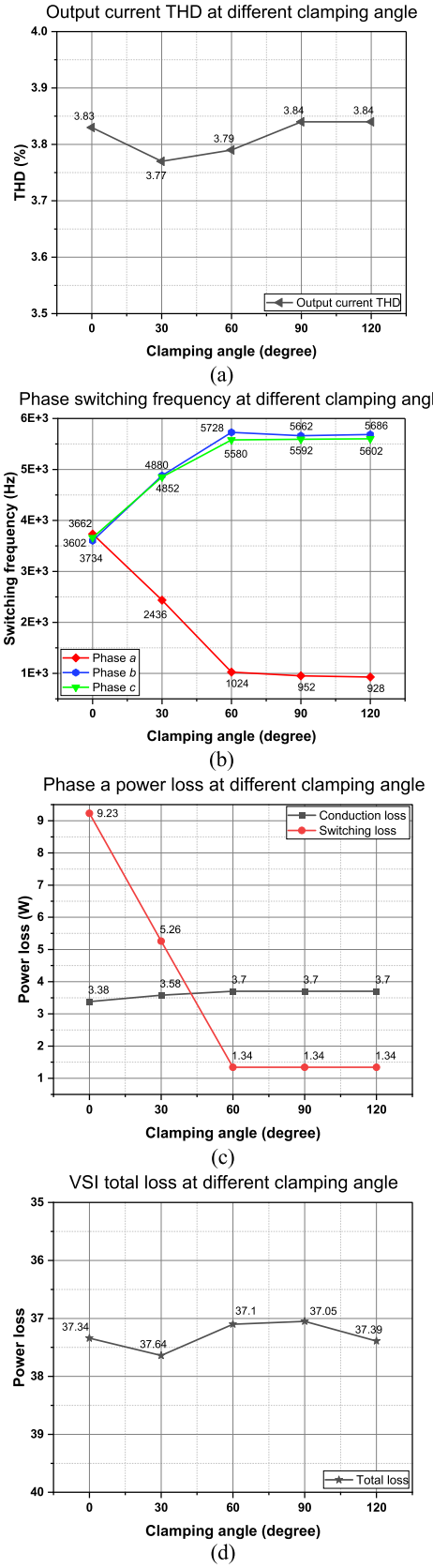


FIGURE 11. Comparison results of the proposed predictive method at different clamping angle in terms of (a) output current THD, (b) phase switching frequency, (c) phase *a* conduction loss and switching loss, (d) VSI total loss.

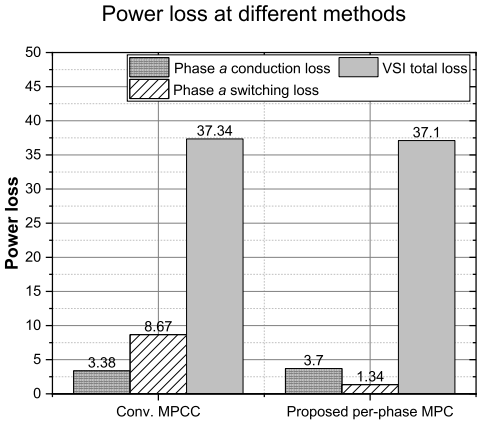


FIGURE 12. Power loss comparison among conventional MPCC and proposed MPC methods.

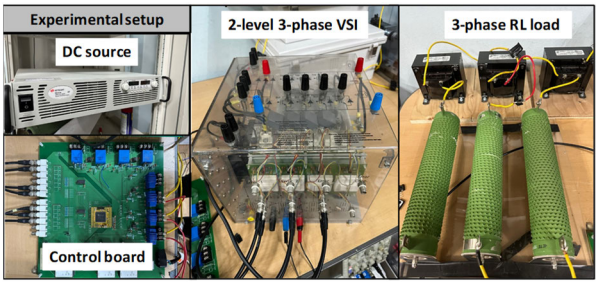


FIGURE 13. Experimental setup of the two-level three-phase VSI.

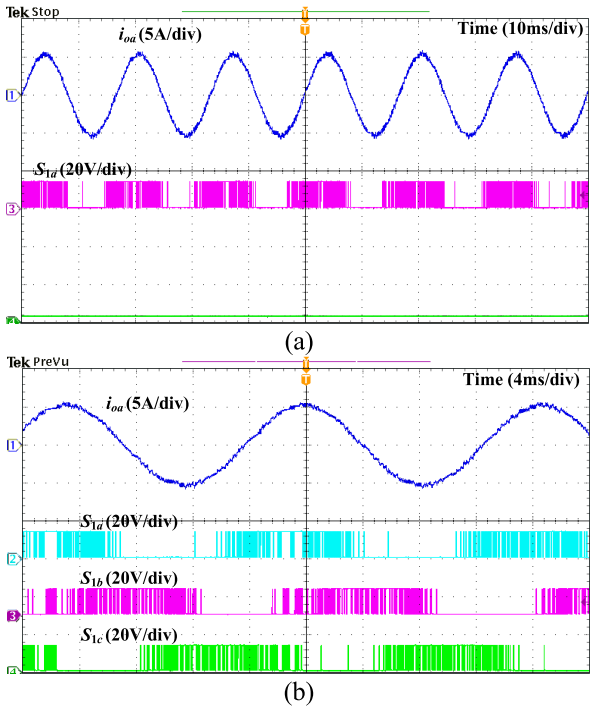


FIGURE 14. Experimental waveforms of phase *a* output current, switching pattern, and filtered reference voltage acquired by conventional MPCC.

C. PERFORMANCE COMPARISON

To enhance the clarity regarding the performance of proposed minimum loss per-phase method based predictive control, a comparison between conventional MPC and proposed MPC

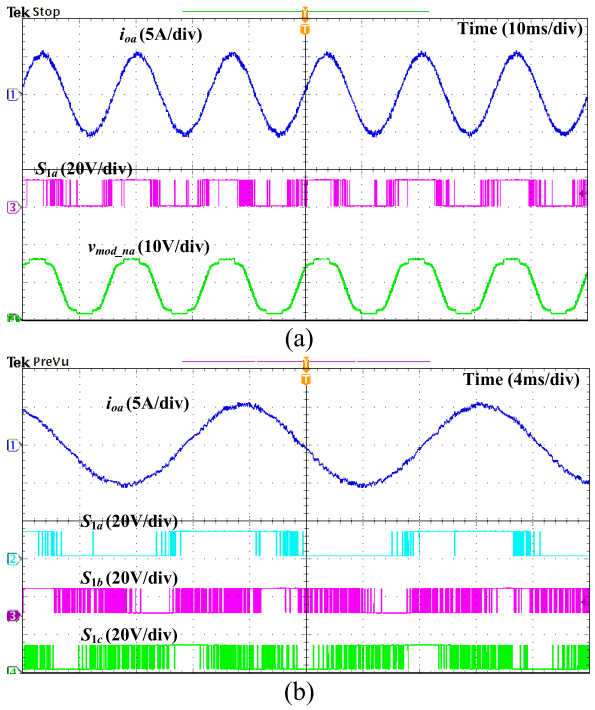


FIGURE 15. Experimental waveforms of phase *a* output current, switching pattern, and filtered reference voltage acquired by proposed method with $\theta_{n\_sw} = 60°$.

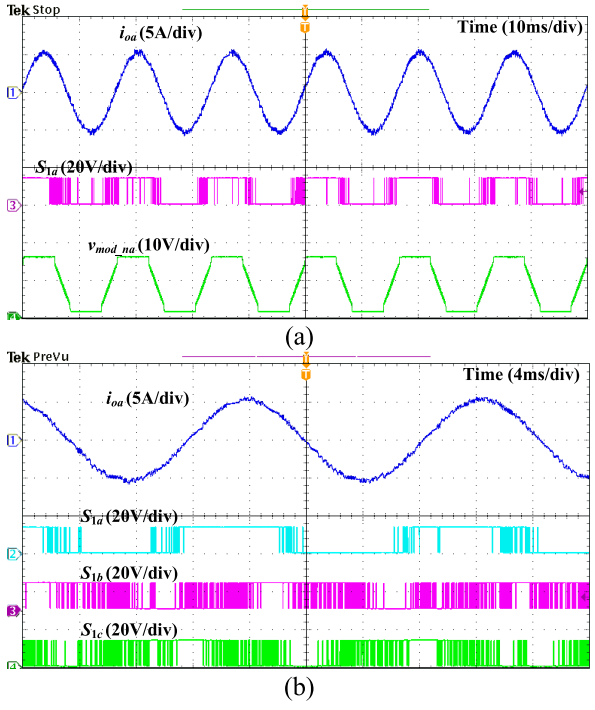


FIGURE 16. Experimental waveforms of phase *a* output current, switching pattern, and filtered reference voltage acquired by proposed method with $\theta_{n\_sw} = 120°$.

methods under various condition including the change of carrier frequency, output power and load condition is conducted.

Fig. 17 presents the phase and average output current THD obtained by two approaches versus the change of sampling frequency. Increasing the sampling frequency leads to the reduction of the output current THD value. Because the proposed MPC method aims at reducing the switching frequency of phase *a*, the corresponding phase *a* output current THD is slightly higher than that of conventional MPC. Meanwhile, the average output current THD between the two control schemes is similar.

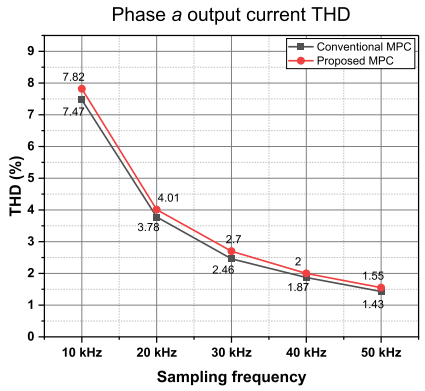
Phase switching frequency comparison of the conventional MPC and proposed MPC methods under different sampling frequencies are shown in Fig. 18. Following the increase of sampling frequency, the phase switching frequency of conventional MPC increases significantly. The proposed MPC method reduces switching frequency of only phase *a* by about 67% compared to the conventional MPC scheme in every sampling frequency condition, whereas the switching frequency of phase *b* and *c* increase by about 40% and 20%, respectively. Regarding the average switching frequency, the average switching frequency of proposed MPC is similar to the conventional MPC with a negligible difference.

In terms of switching loss in Fig. 19, the proposed MPC method reduces the switching loss of phase *a* by about 78% at every sampling frequency condition compared to conventional MPC. The switching loss of phase *b* obtained by the proposed MPC method is higher than that of conventional MPC by about 60% at every sampling frequency condition, whereas the switching loss of phase *c* obtained by two control schemes is similar. Thus, the total switching loss of the proposed MPC is similar to the conventional MPC under different conditions of sampling frequency.

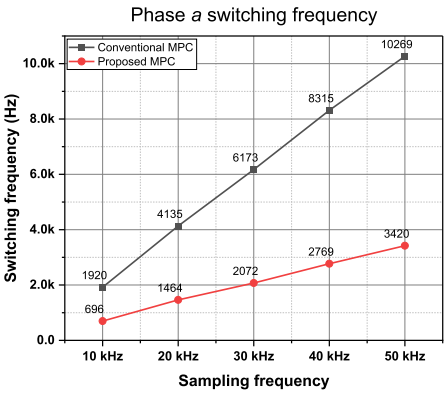
Fig. 20 presents the obtained total loss and corresponding efficiency of conventional MPC and proposed MPC method under different sampling frequency conditions. It can be seen that the total loss obtained by the two control schemes are similar, but at high sampling frequency conditions, the total loss obtained by the proposed method is slightly lower than that of conventional MPC. Therefore, the efficiency of VSI obtained by conducting the two control schemes is similar.

Fig. 21 presents the phase and average output current THD obtained by two approaches versus the change of output power. Under different conditions of output power, the proposed MPC method has the same behavior as in different conditions of sampling frequency. Because the proposed MPC aims at reducing the switching frequency of phase *a*, the corresponding phase *a* output current THD is slightly higher than that of conventional MPC. Meanwhile, the average output current THD between the two control schemes is similar under different conditions of output power.

Phase switching frequency comparison of the conventional MPC and proposed MPC methods under different output powers is shown in Fig. 22. The proposed MPC method reduces switching frequency of only phase *a* up to about 80% compared to the conventional MPC scheme at small output power. When the output power increases, the reduction of switching frequency in phase *a* reduces to about 65%. Regarding the average switching frequency, the average switching frequency of proposed per-phase MPC is a little



(a)



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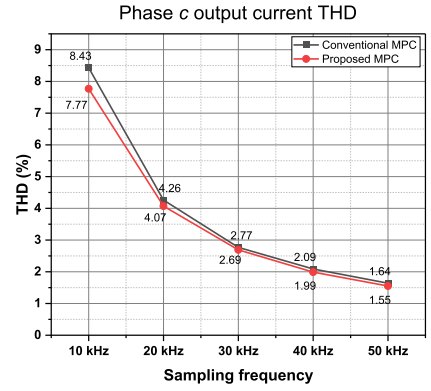
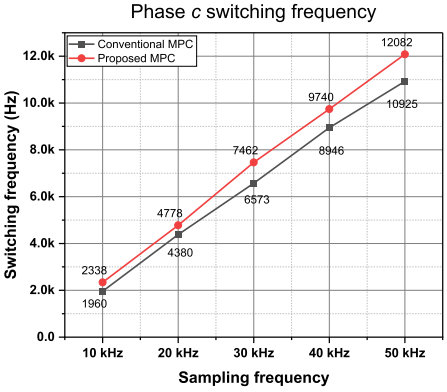


(c)



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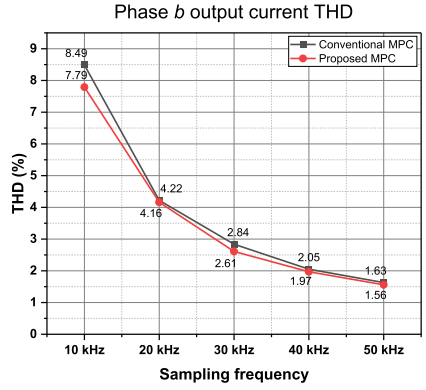
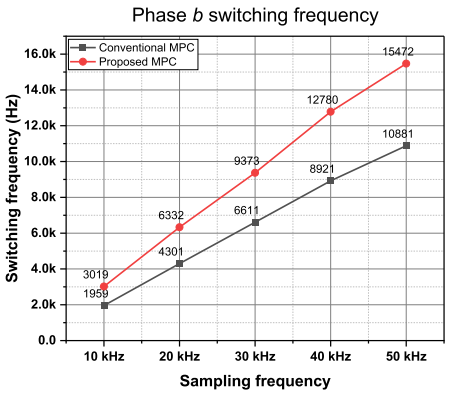


(b)



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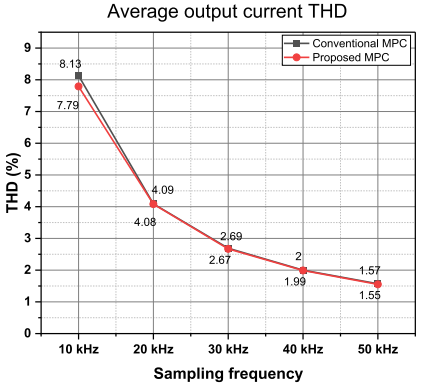

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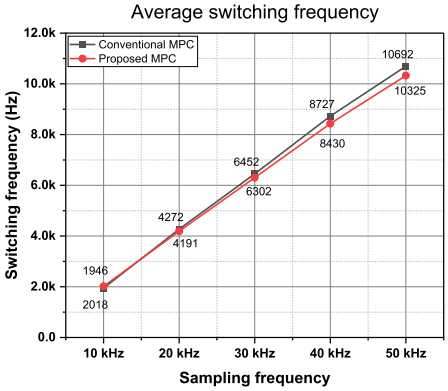


(d)

FIGURE 17. Comparison results between conventional MPC and proposed MPC methods versus the change of sampling frequency in terms of phase output current THD (V_{dc} = 200 V, load angle $\theta = 20°$ and P_{out} = 1 kW).

FIGURE 18. Comparison results between conventional MPC and proposed MPC methods versus the change of sampling frequency in terms of phase switching frequency (V_{dc} = 200 V, load angle $\theta = 20°$ and P_{out} = 1 kW).

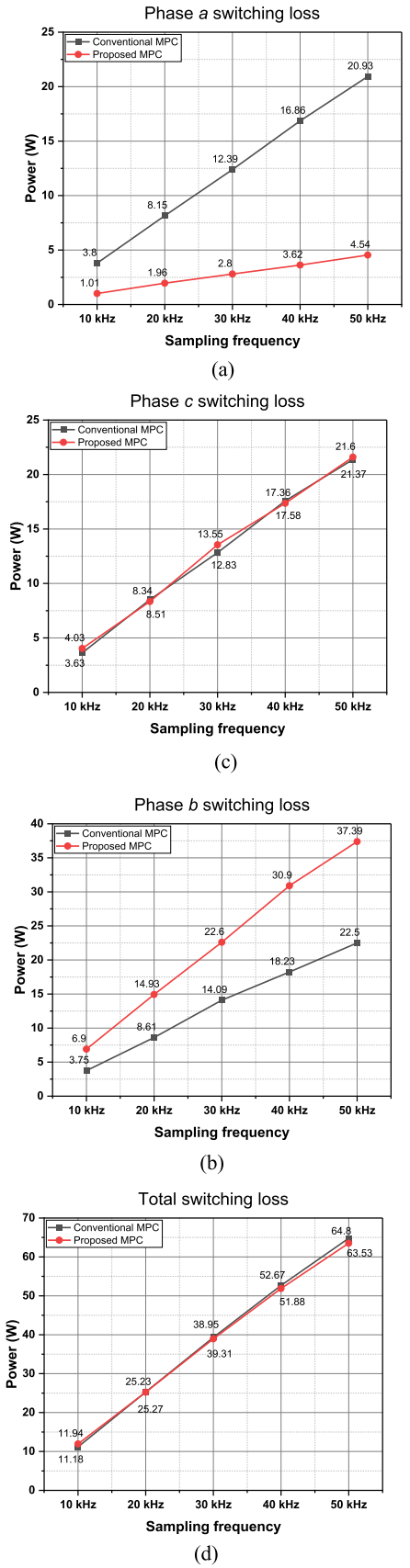


FIGURE 19. Comparison results between conventional MPC and proposed MPC methods versus the change of sampling frequency in terms of phase switching loss (V_{dc} = 200 V, load angle $\theta = 20°$ and P_{out} = 1 kW).

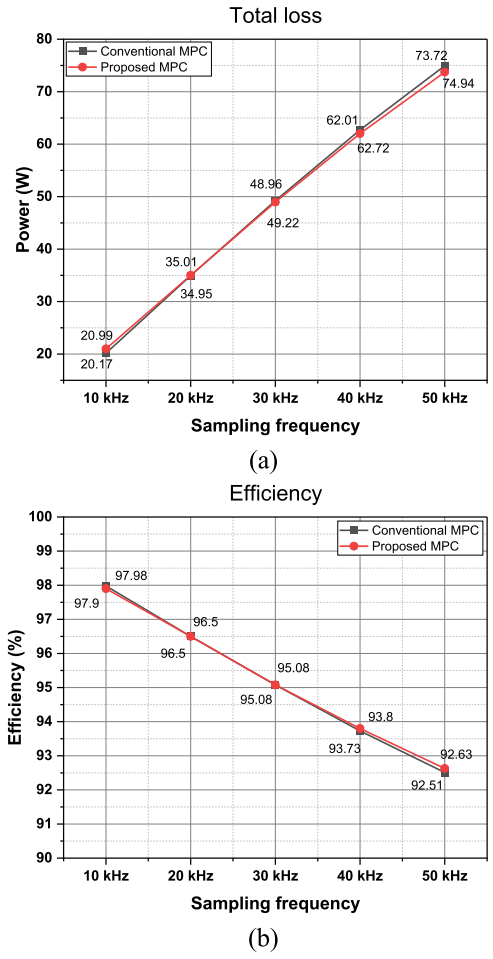
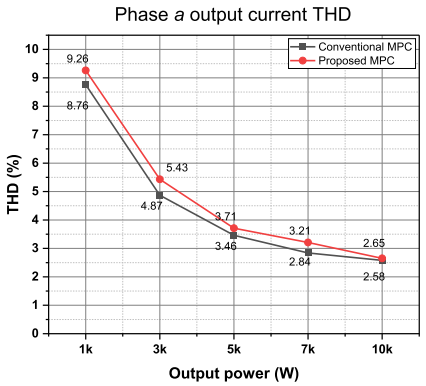


FIGURE 20. Comparison results between conventional MPC and proposed MPC methods versus the change of sampling frequency in terms of total loss and efficiency (V_{dc} = 200 V, load angle $\theta = 20°$ and P_{out} = 1 kW).

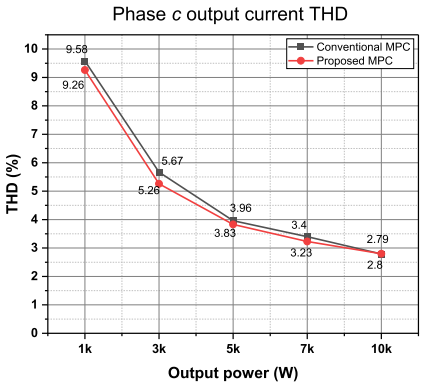
bit lower than the conventional MPC under different output power conditions.

In terms of switching loss in Fig. 23, the proposed per-phase MPC method reduces the switching loss of phase *a* up to about 85% at small output power condition compared to conventional MPC and about 70% at high output power condition. The switching loss of phase *b* obtained by the proposed MPC method is higher than that of conventional MPC by about 56% at every output power condition, whereas the switching loss of phase *c* obtained by two control schemes is similar. Thus, the total switching loss of the proposed MPC is similar to the conventional MPC under different output power conditions.

Fig. 24 presents the obtained total loss and corresponding efficiency of conventional MPC and proposed MPC method under different output power. It can be seen that the total loss obtained by the two control schemes are similar, but at high sampling frequency conditions, the total loss obtained by the proposed method is slightly lower than that of conventional MPC. Therefore, the efficiency of VSI obtained by conducting the two control schemes is similar.



(a)



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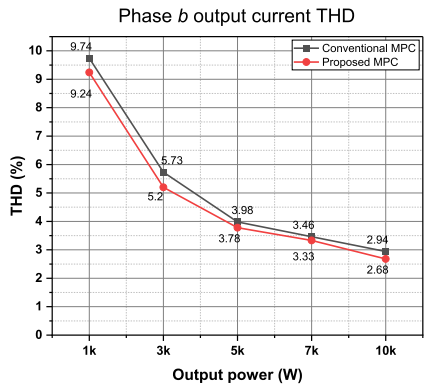

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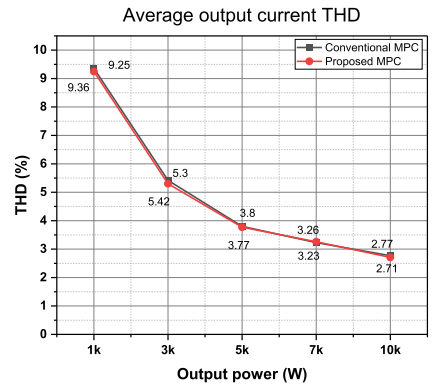
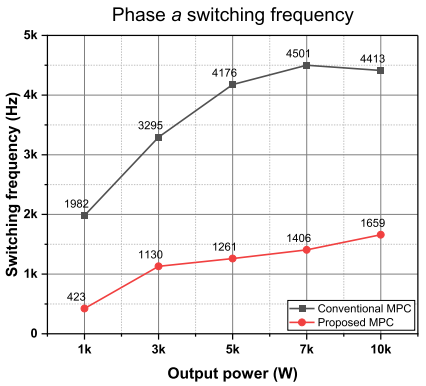
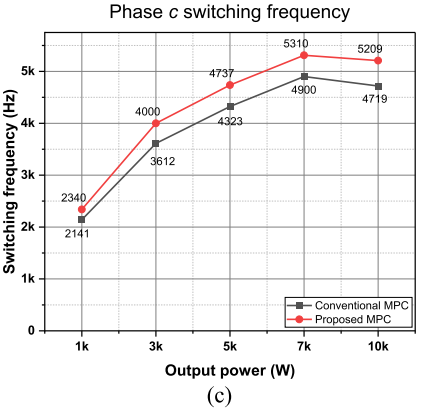


(d)

FIGURE 21. Comparison results between conventional MPC and proposed MPC methods versus the change of output power in terms of phase output current THD (V_{dc} = 720 V, load angle $\theta = 20°$ and sampling frequency f_{sp} = 20 kHz).



(a)



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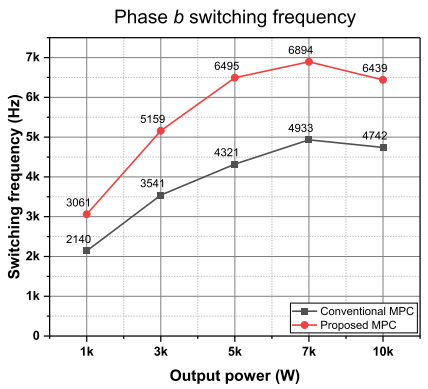

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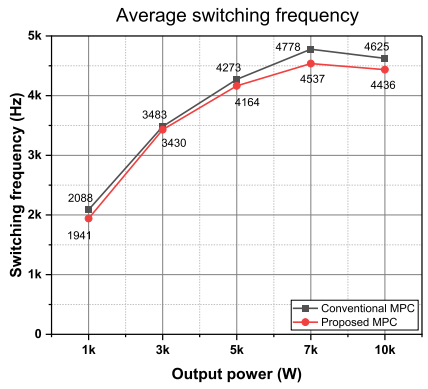


(d)

FIGURE 22. Comparison results between conventional MPC and proposed MPC methods versus the change of output power in terms of phase switching frequency (V_{dc} = 720 V, load angle $\theta = 20°$ and sampling frequency f_{sp} = 20 kHz).

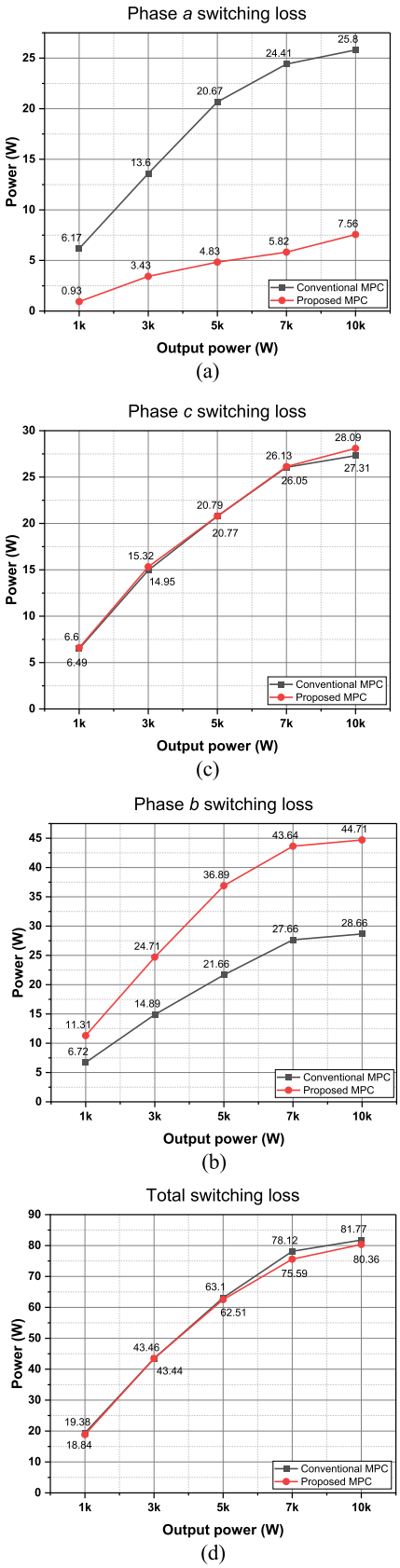


FIGURE 23. Comparison results between conventional MPC and proposed MPC methods versus the change of output power in terms of phase switching loss ($V_{dc} = 720$ V, load angle $\theta = 20°$ and sampling frequency $f_{sp} = 20$ kHz).

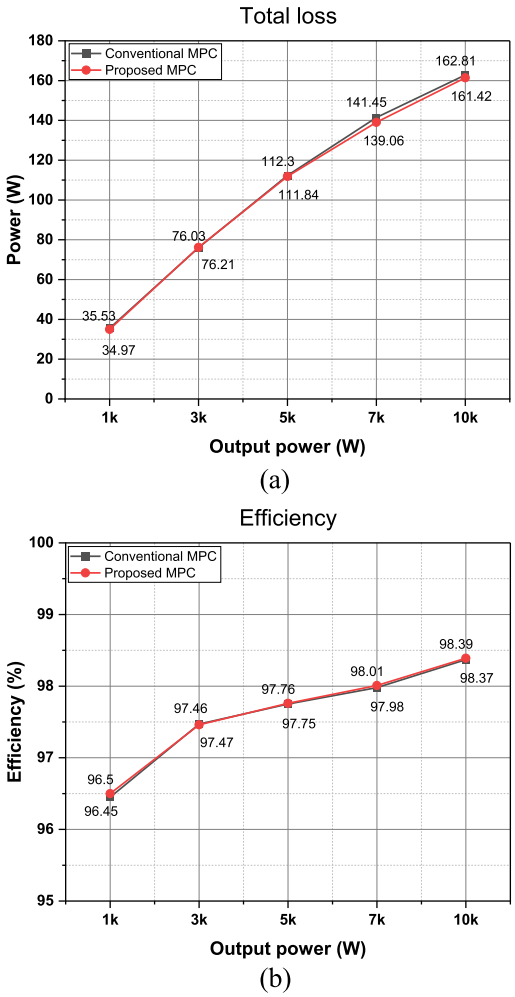
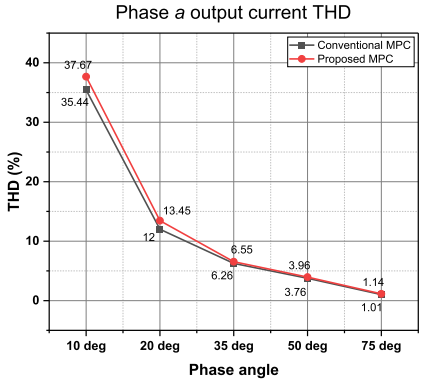


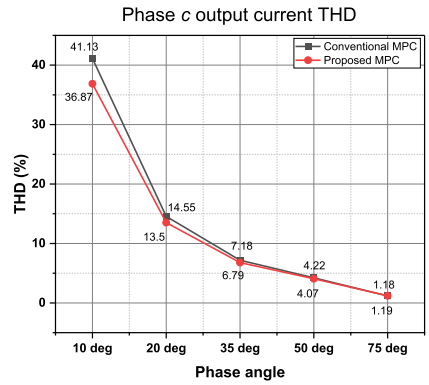
FIGURE 24. Comparison results between conventional MPC and proposed MPC methods versus the change of output power in terms of total loss and efficiency ($V_{dc} = 720$ V, load angle $\theta = 20°$ and sampling frequency $f_{sp} = 20$ kHz).

Fig. 25 presents the phase and average output current THD obtained by two approaches versus the change of load conditions where the load induction is increased to change the load phase angle. Apparently, the output current THD decreases thanks to the increase of load phase angle. As can be seen in Fig. 25 the phase and average output current THD obtained by the conventional MPC and proposed MPC method is similar under different phase angles.

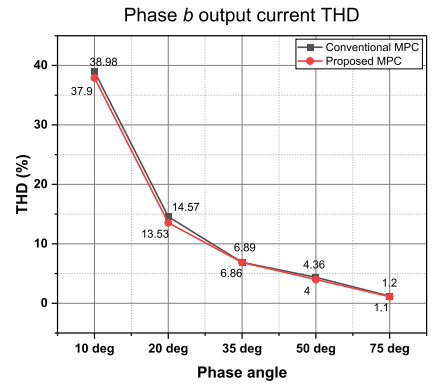
Phase switching frequency comparison of the conventional MPC and proposed MPC methods under different load conditions is shown in Fig. 26. The proposed MPC method reduces switching frequency of only phase *a* up to about 85% compared to conventional MPC scheme with small load phase angle. When the load phase angle increases, the reduction of switching frequency in phase *a* reduces to about 70%. Regarding the average switching frequency, the average switching frequency of the proposed MPC is slightly lower than the conventional MPC under different load phase angles.



(a)



(c)



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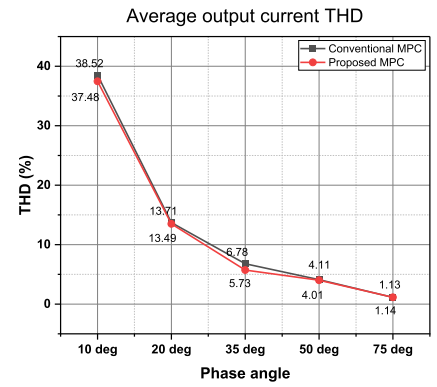
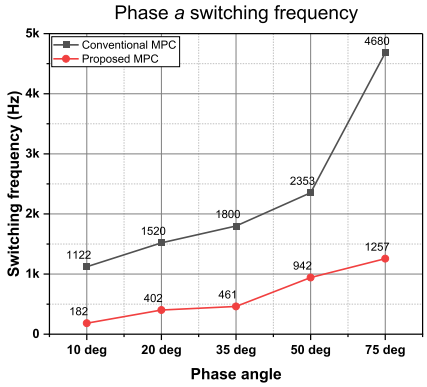
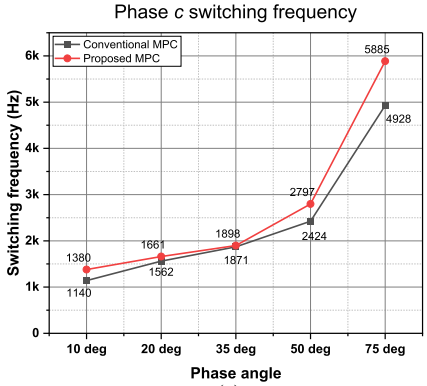


(d)

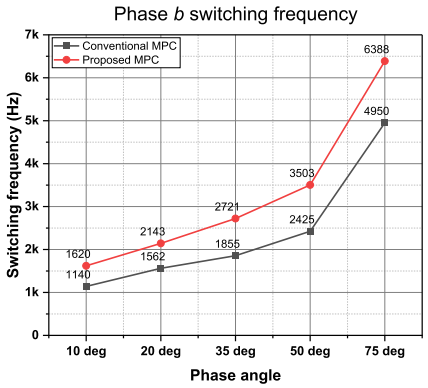
FIGURE 25. Comparison results between conventional MPC and proposed MPC methods versus the change of load condition in terms of phase output current THD (V_{dc} = 720 V, P_{out} = 1 kW and sampling frequency f_{sp} = 20 kHz).



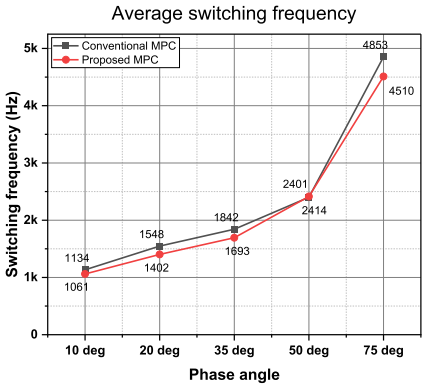
(a)



(c)



(b)



(d)

FIGURE 26. Comparison results between conventional MPC and proposed MPC methods versus the change of load condition in terms of phase switching frequency (V_{dc} = 720 V, P_{out} = 1 kW and sampling frequency f_{sp} = 20 kHz).

In terms of switching loss in Fig. 27, the proposed MPC method reduces the switching loss of phase a up to about 90% at small load phase angle compared to conventional MPC and about 70% at large load phase angle. The increase of switching loss of phase b obtained by the proposed MPC method compared to conventional MPC ranges from 20% to 60% depending on load condition, whereas the switching loss of phase c obtained by two control schemes are similar. The total switching loss obtained by the proposed MPC method is lower than that of conventional MPC when the load phase angle increases.

Fig. 28 presents the obtained total loss and corresponding efficiency of conventional MPC and proposed MPC method under different load conditions. It can be seen that the total loss obtained by the proposed MPC method is lower than that of conventional MPC, especially at high sampling frequency conditions. The efficiency of VSI obtained by conducting the two control schemes decreases following the rise of phase angle, but the efficiency of proposed MPC method is slightly higher than that of conventional MPC.

Fig. 29 presents the output current and phase a switching pattern obtained by proposed MPC method under unbalanced load conditions. Phase a is considered as the most aged leg. In Fig. 29(a), the simulation is conducted under unbalanced conditions where $R_a = 0.5R$, $R_b = R_c = R$. It can be seen that the output currents are regulated correctly in terms of phase and magnitude. The output currents are balanced with similar peak values. Additionally, the switching pattern of phase a correctly contains non-switching region of 120° as expected in Fig 29(a). However, at the unbalanced load condition where $R_a = 1.5R$, $R_b = R_c = R$, the capability of switching frequency reduction is degraded, as shown in Fig. 29(b) though the output currents are regulated correctly.

Fig. 30 presents the performance comparison in terms of output current THD, switching frequency, power loss, and %error of output current under different unbalanced load conditions. As can be seen in Fig. 30(a), the phase a and average output current THD slightly change following the change of unbalanced conditions. However, when the unbalanced condition of increasing R_a by 50% ($\Delta R = 50$), the capability of switching frequency reduction of the proposed MPC method is significantly degraded. It can be seen that the phase a switching frequency and switching loss at this unbalanced condition increase by about 2.7 and 4.3 times respectively compared to balanced condition ($\Delta R = 0$), as shown in Fig. 30(b) and (c). The effect of unbalanced load on error of load current is shown in Fig. 30(d). The error of load current increases when the load of phase a increase.

Fig. 31 presents the output current and phase a switching pattern obtained by proposed MPC method under unbalanced load conditions. Phase a is considered as the most aged leg. In this case, the unbalanced condition is at load of phase c. In Fig. 31(a), the simulation is conducted under unbalanced conditions where $R_a = R_b = R$, $R_c = 0.5R$. It can be seen that the output currents are regulated correctly in terms of phase and magnitude. The output currents are balanced with

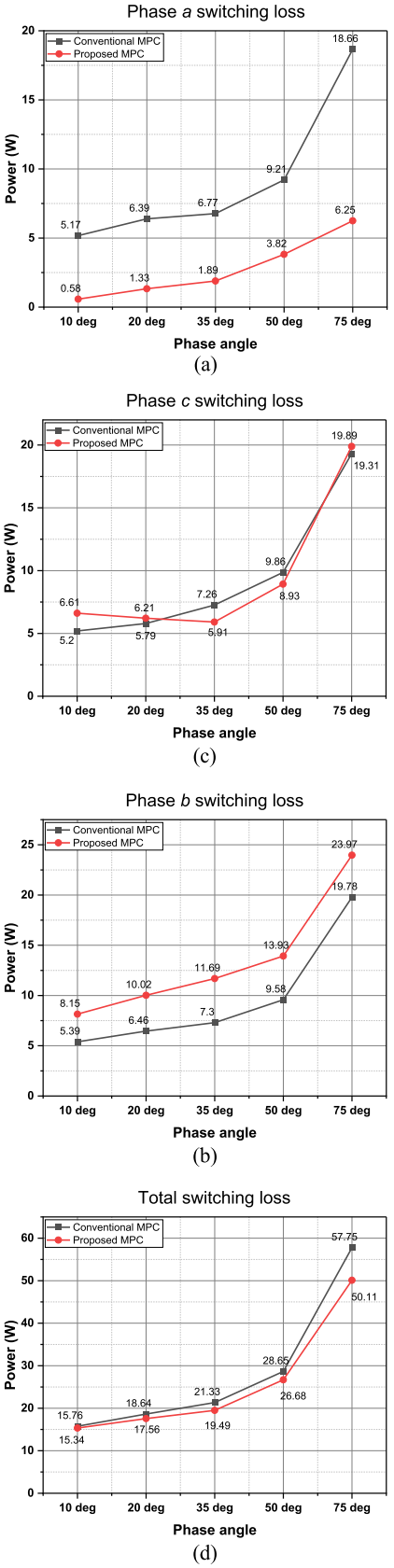


FIGURE 27. Comparison results between conventional MPC and proposed MPC methods versus the change of load condition in terms of phase switching loss (V_{dc} = 720 V, P_{out} = 1 kW and sampling frequency f_{sp} = 20 kHz).

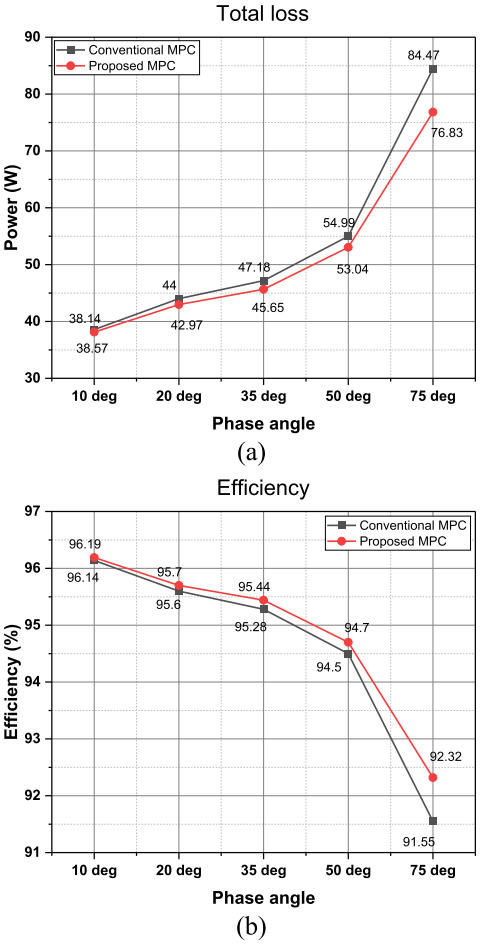


FIGURE 28. Comparison results between conventional MPC and proposed MPC methods versus the change of load condition in terms of total loss and efficiency (V_{dc} = 720 V, P_{out} = 1 kW and sampling frequency f_{sp} = 20 kHz).

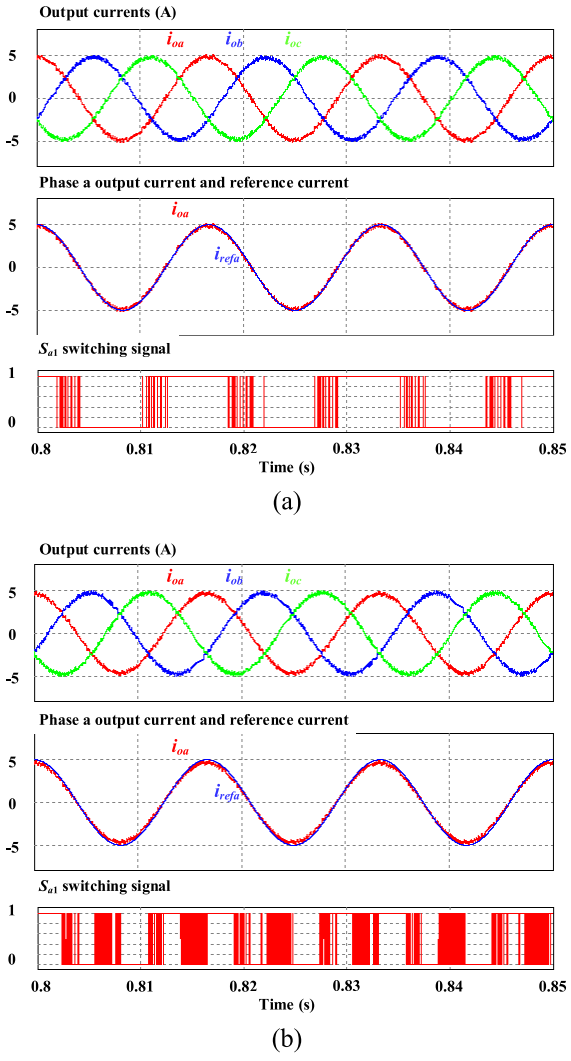


FIGURE 29. Output currents waveforms obtained by proposed MPC method under unbalanced load (a) $R_a = 0.5R$, $R_b = R_c = R$, (b) $R_a = 1.5R$, $R_b = R_c = R$.

similar peak values. Additionally, the switching pattern of phase a correctly contains non-switching region of 120° as expected in Fig. 31(a). However, at the unbalanced load condition where $R_a = R_b = R$, $R_b = R_c = 1.5R$, the capability of switching frequency reduction is degraded, as shown in Fig. 31(b) though the output currents are regulated correctly.

Fig. 32 presents the performance comparison in terms of output current THD, switching frequency, power loss, and %error of output current under different unbalanced load conditions. As can be seen in Fig. 32(a), the phase a and average output current THD slightly change following the change of unbalanced conditions. However, when the unbalanced condition of increasing R_c by 50% ($\Delta R = 50$), the capability of switching frequency reduction of the proposed MPC method is significantly degraded. It can be seen that the phase a switching frequency and switching loss at this unbalanced condition increase by about 1.8 and 2.3 times respectively compared to balanced condition ($\Delta R = 0$), as shown in Fig. 32(b) and (c). The effect of unbalanced load on error of load current is shown in Fig. 32(d). The error of load current increases when the load of phase a increase.

It can conclude that the proposed MPC can correctly regulate output currents under unbalanced load conditions. However, the capability of switching frequency reduction is degraded when the load resistance is higher than the equivalent value, especially the unbalanced load at the most aged leg.

Following simulation, experiment, and various comparison results, it can be noticed that the proposed MPC method can significantly reduce the switching loss of the most aged leg without deteriorating the output performance and efficiency of the converter. Although the switching loss in the two remaining phase leg increases, it does not exert negative impact on the two-level three-phase VSI when the most aged leg still can be prolonged its lifetime and delayed its failure until the next maintenance. Additionally, the increase of switching frequency in the two remaining phase leg will lead to the balance of aging condition between three phase legs. The proposed MPC method uses only a single cost

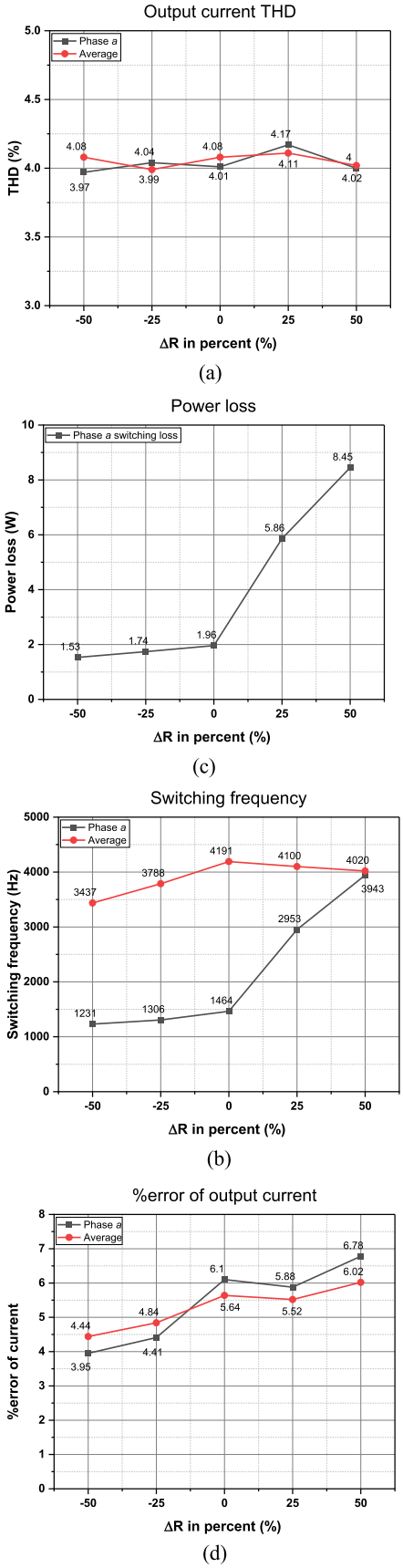


FIGURE 30. Comparison performance under the unbalanced degree of load in phase *a*.

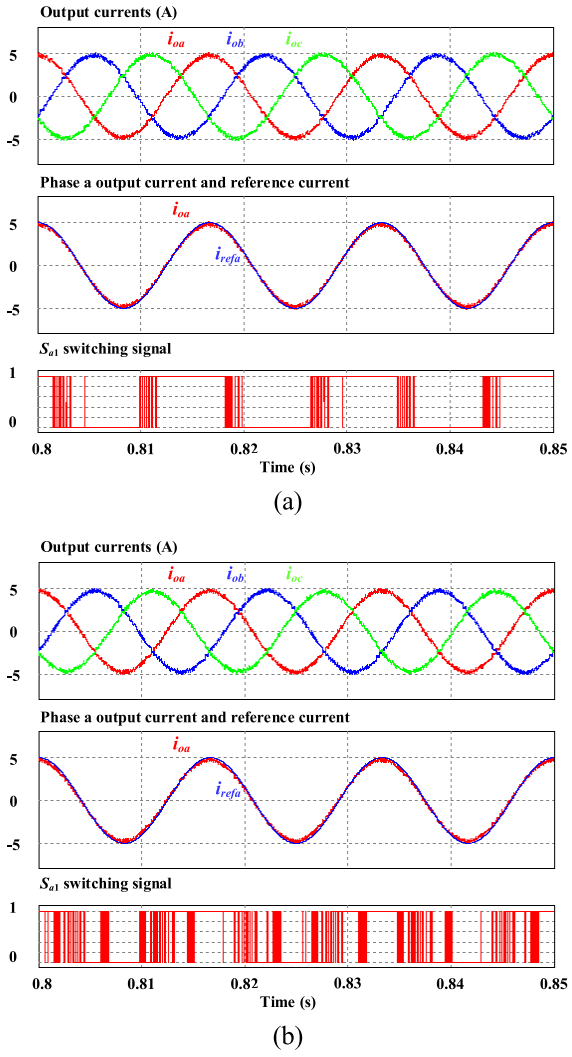
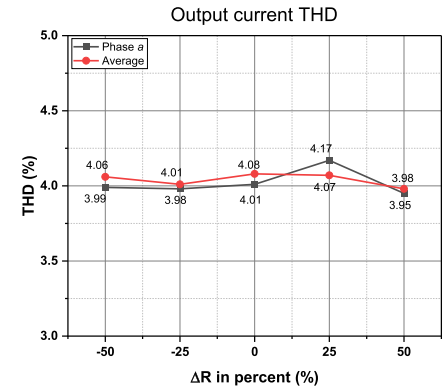


FIGURE 31. Output currents waveforms obtained by proposed MPC method under unbalanced load (a) $R_a = R_b = R$, $R_c = 0.5R$, (b) $R_a = R_b = R$, $R_b = R_c = 1.5R$.

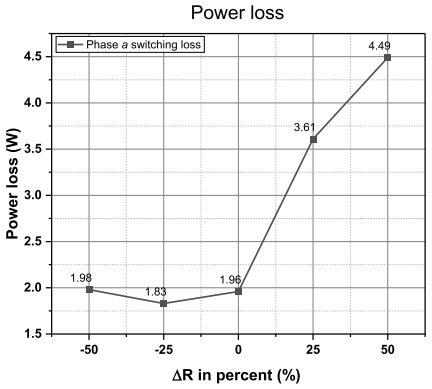
function corresponding to reference voltages, so the proposed method is straightforward to implement and does not need the weighting factor tuning procedure and additional hardware.

V. IMPACT OF THE PROPOSED METHOD ON LIFETIME

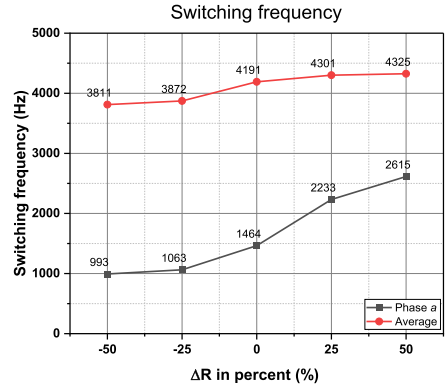
As indicated earlier, the primary cause of failure of the power semiconductor devices is thermal stress, which reduces the lifetime of corresponding devices and entire converter. Hence, this section is introduced to determine how the application of the proposed MPC method is affecting the lifetime consumption of the power semiconductor devices. To calculate the lifetime of switching devices, analytical models, which are well-known to describe the dependence of the number of cycles to failure N_f on the parameters of temperature cycles, will be used. In this study, Bayerer's model (CIPS 2008 model) [33] is used, which is the most comprehensive analytical model. It includes the influence of the various parameters as temperature variation ΔT_j, the minimum junc-



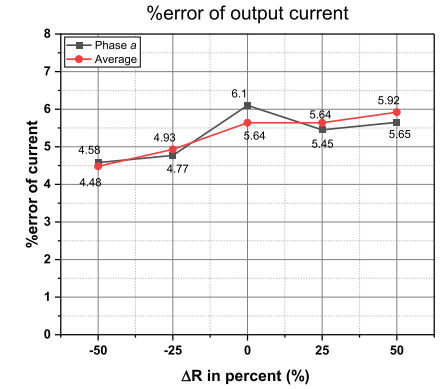
(a)



(c)



(b)



(d)

FIGURE 32. Comparison performance under the unbalanced degree of load in phase c.

TABLE 3. Parameter for Bayerer's model (CIPS 2008 model).

Parameter	Value	Coefficient	Value
A	2.03e14		
ΔT_j	Variable	β_1	−4.416
$T_{j,min}$	Variable	β_2	1285
t_{on}	1.66 s	β_3	−0.463
i_B	10 A	β_4	−0.716
V_C	6.5 V	β_5	−0.761
d_b	400 µm	β_6	−0.5

TABLE 4. Parameters for the foster-type thermal network.

i	1	2	3
R_{thi}	0.3031	0.1333	0.2038
τ_i	0.117123062	0.659264816	0.017939156

TABLE 5. Lifetime estimation for predefined mission profile.

	$T_{j,\text{high}}$	$T_{j,\text{low}}$	ΔT_j	Est. Lifetime
Conventional MPC	83 °C	59 °C	24 °C	4.5 yr
Proposed MPC	76.7 °C	59.2 °C	17.5 °C	18.3 yr

tion temperature $T_{j,min}$, the pulse duration t_{on}, the current per bond foot i_B, the voltage class V_C, and the diameter of the bond wire d_b. Table 3 summarizes the parameters of (17) used in this paper.

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot exp\left(\frac{\beta_2}{T_{j,min}}\right) \cdot t_{on}^{\beta_3} \cdot i_B^{\beta_4} \cdot V_C^{\beta_5} \cdot d_b^{\beta_6}. \quad (17)$$

It can be seen that the lifetime model in (17) requires information of junction temperature. The junction temperature of power semiconductor devices can be calculated by thermal models using calculated power loss. Thus, the junction temperature of power semiconductor devices in VSI is calculated using a Foster-type thermal network as implemented in [34], as presented in Fig. 33. Here, T_j and T_c are the junction temperature and the case temperature, respectively. In this study, T_c is assumed to be 50°C. R_{th} is the thermal resistance, whereas τ is the thermal time constant. The thermal network parameters of a three layers Foster-type network are shown in Table 4.

For lifetime estimation, a periodical mission profile is used with changing of the output power between 9kW to 3kW. Fig. 18 shows the calculated junction temperature and three-phase output currents following the change of output power in the mission profile. For comparison, the simulation is operated by conventional MPCC method and the proposed MPC scheme. In normal operation, the conventional MPCC method is employed to regulate the load current in accordance with the reference current, as shown in Fig. 34(a). A temperature variation ΔT_j amplitude of 24°C obtained by

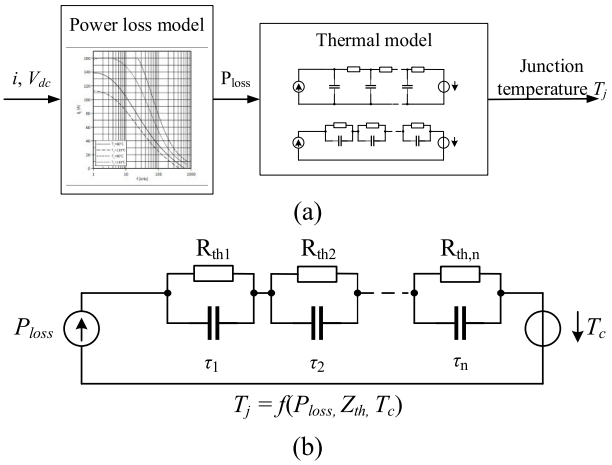


FIGURE 33. (a) Junction temperature calculation model using power loss, (b) Foster-type thermal network.

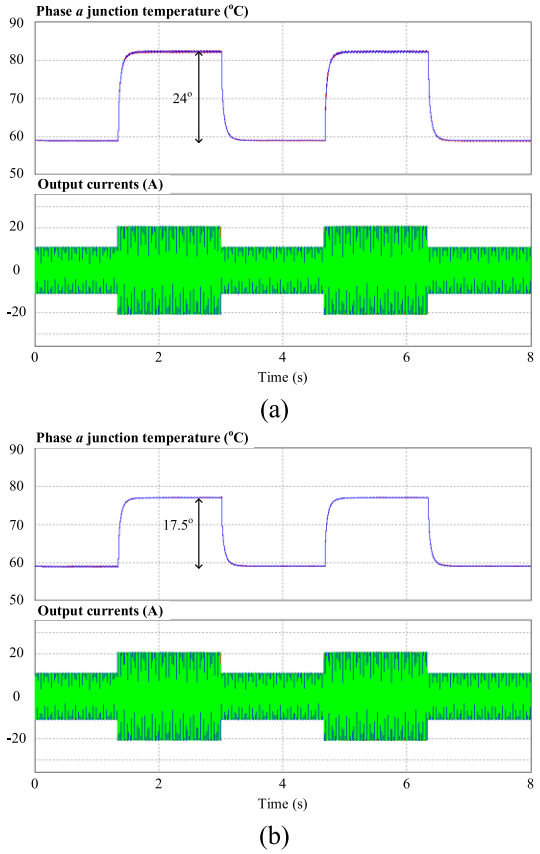


FIGURE 34. Calculated junction temperature of transistor in phase *a* and output currents waveforms following predefined mission profile (a) conventional MPCC, (b) proposed method.

the conventional MPCC method is acquired. The proposed per-phase MPC method is employed with the assumption that phase *a* is the most aged leg in the second simulation. The effect of this proposed per-phase MPC method is the reduction of the temperature variation in phase *a* to 17.5°C at the same boundary conditions, as shown in Fig. 34(b). Using Bayerer's model (CIPS 2008 model) in (17), the number of cycles to failure of the established mission profile can be calculated. Table 4 presents the estimated lifetime. As a result, the reduction of the temperature variation obtained by the proposed per-phase MPC method results in an increase in the estimated lifetime by four times in this investigation. It can be concluded that the proposed per-phase MPC method can effectively reduce thermal variation to increase the corresponding lifetime of VSI.

VI. CONCLUSION

A minimum loss per-phase method based predictive control is introduced to decrease the loss of specific phase legs and ease thermal stress in most aged power devices, resulting in the increase of converter lifetime. By injecting the predictive zero-sequence voltage, the modified predicted reference voltages generate a non-switching region in the desired phase leg, which results in reducing the switching frequency and switching loss. The proposed method is compared to the conventional MPC, concluding that it can reduce switching loss of particular phase leg and achieve quite the same THD for output current. With this method, the lifetime of the most aged phase leg will be extended by reducing the corresponding switching loss. Switching losses can be cut by up to 85% with the proposed technique. The consequent decrease in switching loss lowers the heat generated by switches, reducing thermal stress and lengthening the lifetime of VSI.

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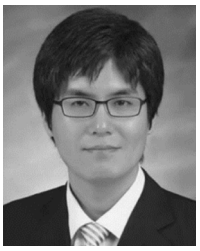

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