RESEARCH ARTICLE

A Multi-Finger GHz Frequency Doubler Based on Amorphous Indium Gallium Zinc Oxide Thin Film Transistors

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ABSTRACT This paper presents a multi-finger doubler based on amorphous-indium gallium zinc oxide (a-IGZO) thin film transistors (TFT) operating at GHz frequency. The doubler and the TFTs have been fabricated in-house with chromium (Cr) gate electrodes. We have used the Rensselaer Polytechnic Institute amorphous silicon (RPI-a) TFT DC model and a Null-Bias method extracted AC model for simulation. The device output power, the threshold voltage mismatch, and breakdown characteristics are explained with the help of the model. The device yield reduces as the number of fingers in the TFTs increase. The model helps explain the doubler's non-idealities and compensate for these transistors' low yield. The peak second harmonic conversion gain of the doubler is measured to be -32 dB at a gate overdrive voltage of around 2.8 V for a 500 MHz input signal. This second harmonic output frequency exceeds the TFT's transit and maximum oscillation frequencies.

INDEX TERMS Radio frequency, TFT, a-IGZO, S-parameters, Y-parameters, f_T, f_{max}, frequency doubler, conversion gain.

I. INTRODUCTION

Metal-oxide thin film transistors (TFT)s have been recently popular in ongoing research for high-frequency circuit design. Compared to Si-based technologies, metal oxide semiconductors are cost-effective and can be fabricated at room temperature. As such, there have been attempts to make RF circuits from TFTs using different semiconductor devices. A frequency doubler was presented in [1] showing a conversion loss of around 44 dB for an input of 100 MHz. The same device was used as a detector to detect signals up to 1 GHz with an equivalent noise power of $30\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$. Most recently, Mehlman et al. demonstrated a ZnO-based cross-coupled LC oscillator that operates at 1.25 GHz [2]. The speed of metal oxide TFTs has consistently improved over the past decade. ZnO, as well as a-IGZO TFTs, now

demonstrate transit frequency (f_T) and maximum oscillation frequency (f_{max}) above 1 GHz [3], [4].

However, the power capability of a-IGZO decreases as frequency increases. A frequency doubler can relax the output power versus the frequency trade-off of an a-IGZO-based signal source.

Frequency doublers operating between a few hundred MHz to GHz is nonexistent in the literature. An accurate TFT model is required to simulate amplification, mixing, and impedance matching for GHz circuit design and simulation. Although a SPICE level $= 3$ model is typically sufficient for fundamental AC analysis and simulation, the discontinuity in the level $= 3$ models leads to convergence issues for RF design involving non-linear analysis and simulation. Therefore, a model more suitable for amorphous TFTs, namely the RPI-a model, is adopted [5]. Created initially for amorphous Silicon [5], the model has been applied successfully in the MHz frequency range for a-IGZO

The associate editor coordinating the review of this manuscript and approving it for publication was Nagendra Prasad Pathak.

transistors in [6]. Their procedure, however, has been applied to a minimum channel length of 3 μm. The RPI-a model is yet to be applied to the submicron length channel for GHz application. A combined DC and high-frequency model is necessary to simulate the power output and impedance matching for GHz frequency circuit design.

In this paper, we have used a combination of the continuous charge-based RPI-a TFT model and high-frequency elements to address the parasitic components of the TFT. The algorithm presented by [7] has been used to extract the DC model parameters. Moreover, we have used the null-bias method from [8] to extract the parasitic elements. In the same spirit, we have fabricated a four-finger common-gate (CG) doubler in-house, as described in [1] and [4]. A higher number of fingers can increase RF power handling capabilities of TFTs. We measured the CG frequency doubler and compared the measurements and the simulations to show the model's efficacy in RF circuit design. The model is derived from the DC and S-parameter measurements and implemented as a Verilog-A code. In that case, one can extensively reduce the cost and time required for modeling and simulation.

Moreover, the shorter length of the a-IGZO channel leads to poor device yield [9]. The yield worsens if the number of fingers increases since the probability of device failure will be higher. The model can substitute the low-yield device, helping us learn about circuit behaviors.

This paper is organized as follows: section II comments on device fabrication; in section III, we present the DC and AC models, their extraction procedure, implementation, and verification. The theoretical background of the CG doubler is presented in section IV; section V shows the measurement results and discussion for the doubler, and section VII concludes this paper.

II. DEVICE FABRICATION
The fabrication steps outlined in section II of [4] are used to ensure consistency and comparability of the channel material. This work presents chromium as the gate electrode instead of the composite Ti/Au/Ti used in [4].

It was shown in the literature that water that adsorbs on the surface of the channel material can substantially affect the characteristics of metal-oxide TFTs, such as hysteresis [10]. Thus, an ALD grown Al_2O_3 encapsulation layer, which is an excellent barrier against the diffusion of water molecules [11], is used to protect the TFTs in our lab environment (24°C, 60%).

As mentioned in [4], the on current and off current for a single 100 μm/0.8 μm TFT are around 5.46×10^{-12} A and 1.06×10^{-3} A respectively, resulting in an on/off ratio of around 10^8. For a ten-finger TFT, the on current increases to 8.3×10^{-3} A, while the off current stays in the same order, around 7.36×10^{-12} A. Thus the on/off ratio for a ten-finger TFT is around 10^9.

III. MODELING OF TFTs
The single-finger, ten-finger, and doubler were designed on the same substrate. The model of the TFT was developed

simultaneously with the measured data. First, the single-finger TFT was measured for both DC and S-parameters, and the model was extracted. Next, the model was used to simulate the TFT in Cadence, and the simulated data were compared with the measured data. Next, the ten-finger TFT was measured, and the model was verified for multi-finger transistors. The doubler performance was also measured, and the model was then used to simulate, verify and analyze the output results obtained.

A. DC MODEL PARAMETER EXTRACTION
The drain current equation for a TFT of channel width W and length L according to the RPI-a TFT model [7] is given as

$$I_d = \frac{\frac{W}{L}C_g\mu_{FE}(V_{gs}-V_{th})V_{ds}}{1+(R_s+R_d)\left[\frac{W}{L}C_g\mu_{FE}(V_{gs}-V_{th})\right]}$$
$$\times \frac{(1+\lambda V_{ds})}{\left[1+\left(\frac{V_{ds}}{\alpha_{sat}(V_{gs}-V_{th})}\right)^m\right]^{1/m}}, \quad (1)$$

where, V_{ds} is the sum of DC and AC drain voltages, V_{DS} and v_{ds} respectively, V_{gs} is the sum of DC and AC gate voltages, V_{GS} and v_{gs}, and the other variables signify the properties as mentioned in Table 1. The mobility μ_{FE} defines the channel mobility under the influence of gate-source voltage as

$$\mu_{FE} = \mu_0 \left(\frac{V_{gs}-V_{th}}{VAA}\right)^{\gamma}, \quad (2)$$

where VAA is a fitting parameter describing the characteristic voltage of field effect mobility.

The two most popular methods in the literature for DC parameters extraction are the 'integral function method' [12] and the integrated non-saturating and self-heating effect-based extraction procedure in [7]. The latter is more suitable for our TFTs as the drain current does not saturate in the short-channel devices. The modeling steps mentioned in [7] have been applied here.

The extracted parameter values are presented in Table 1. The model has been implemented as a Verilog-A code.

Fig. 1 shows the resultant simulated versus the measured output and transfer behaviors. The simulated output characteristic agrees closely with the measurement, as shown in Fig. 1a. The simulated drain current is underestimated at low V_{GS}, as shown in Fig. 1b. The model incorporates a fixed V_{th}. However, the threshold voltage decreases as V_{DS} increases, leading to this fitting error. The normalized root mean square error (NRMSE) is calculated as NRMSE = RMSE/$(I_{D,max}-I_{D,min})$ and presented in Table 2. As gate voltage increases, the value of NRMSE decreases, leading to around 1% error at $V_{GS} = 2$ V.

B. RF MODEL PARAMETER EXTRACTION
One of the most critical parameters in an RF circuit is the gate resistance R_G that defines the maximum oscillation frequency f_{max}. The value of f_{max} additionally depends on the transit frequency f_T of the transistor. The transconductance and parasitic capacitances play a significant role in determining f_T.

TABLE 1. Extracted RPI-a parameters and RF element values for a single-finger TFT.

| Parameter	Unit	Description	Extracted Value
W	μm	Channel width	100
L	μm	Channel length	0.8
α_{sat}	-	Saturation modulation parameter	0.906
ϵ_i	-	Relative permitivitty of the insulator	8.5
γ	-	Power law mobility parameter	1.014
λ	1/V	Output conductance parameter	0.101
m	-	Knee shape parameter	1.3698
μ_0	m^2/Vs	Conduction band mobility	0.001
R_d	m	Drain contact resistance	160.077
R_s	m	Source contact resistance	160.077
T_{nom}	°C	Nominal temperature	24
t_{ox}	m	Oxide (Al_2O_3) thickness	5e-8
VAA	V	Characteristic voltages for field effect mobility	1.902
V_{th}	V	Zero bias threshold voltage	-0.948
R_{G1}	Ω	First part of gate electrode resistance	385
R_{G2}	Ω	Second part of gate electrode resistance	1078
R_{DSE}	Ω	Drain-source electrode resistance	10
C_{PG}	fF	Gate pad capacitance	36.5
C_{PD}	fF	Drain pad capacitance	17
C_{OV}	fF	Gate-drain or gate-source overlap capacitance	57
r_{gd}	Ω	Distributed gate-drain channel resistance	0
r_{gs}	Ω	Distributed gate-source channel resistance	650
τ	ps	Channel transit delay	150
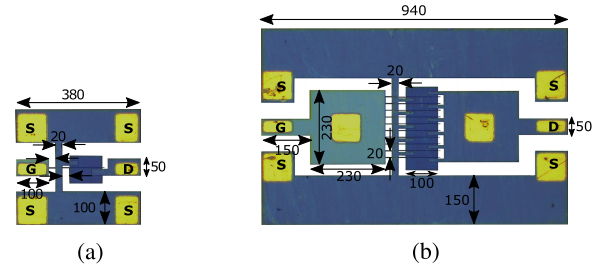
FIGURE 2. Photos (background edited) of the top views of (a) a single-finger and (b) a ten-finger TFTs with dimensions in μm.
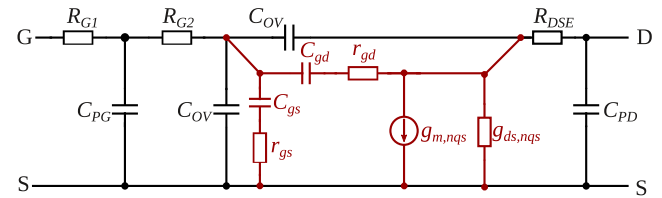

FIGURE 3. Two lumped embedded model (red represents the intrinsic parameters).
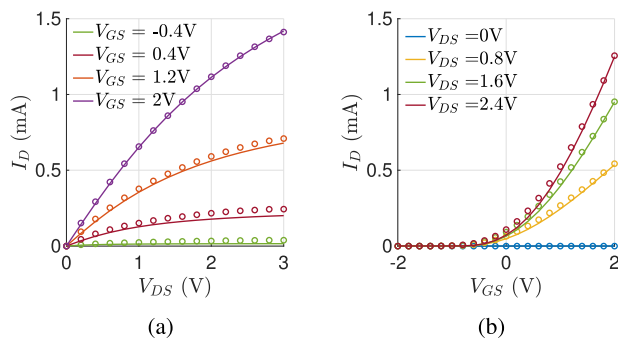

FIGURE 1. Simulated versus measured (a) output and (b) transfer characteristics (solid lines - simulation and circular markers - measurement) for a single-finger TFT.

TABLE 2. Normalized root mean square error in the DC output characteristics simulation.

V_{GS} (V)	-1.2	-0.4	0.4	1.2	2
RMSE (mA)	0.003	0.056	0.118	0.096	0.015
$I_{D,max} - I_{D,min}$ (mA)	0.002	0.039	0.244	0.710	1.41
NRMSE	1.5	1.438	0.484	0.136	0.011

These device parameters depend on the material, geometry, and fabrication technique.

The top view of the layout of a 100 μm/0.8 μm single-finger TFT is shown in Fig. 2a. The source terminal is large and spans both sides of the channel to facilitate the multi-finger architecture, as shown in the photos in Fig. 2b. Compared to the single-finger TFT, a multi-finger architecture provides a lower gate resistance, resulting in low reflected power at the input.

For high-frequency modeling of the TFT, one must separate the intrinsic and extrinsic components of the devices, as shown in Fig. 3. Here, C_{PG} and C_{PD} represent the gate and drain pad capacitance, respectively. C_{OV} is gate-drain and gate-source overlap capacitance. R_{G1} and R_{G2} are two parts of the gate resistance separated by C_{PG}. R_{DSE} represents the combined drain and source electrode resistance. The elements highlighted in red represent the intrinsic components. $g_{m,nqs}$ and $g_{ds,nqs}$ are the non-quasi-static (NQS) transconductance, and channel conductance, respectively [13].

The extrinsic components are derived at null-bias condition at $V_{DS} = 0$ V and $V_{GS} = -2$ V [8]. The gate resistance has two components, namely R_{G1} and R_{G2}. An initial calculation of the ratio $r = R_{G2}/R_{G1}$ is first done according to formula

$$r = \frac{\#\text{squares beyond } C_{PG}}{3 \cdot \#\text{squares before } C_{PG}} = \frac{110/0.8 + 20/1.1}{3 \cdot (2 + 20/1.1)} = 2.57.$$

(3)

A factor of 3 in the denominator is used, as the gate electrode will follow the RC ladder rule beyond C_{PG} [14]. However, due to the non-uniformity of the gate electrode above the source and drain (see Fig. 2a), we must adjust the value of r slightly. First, an estimation of $R_{G1} = 400 \, \Omega$ is done from the sheet resistance of the chromium electrode, which is around $20 \, \Omega/\square$ [4]. Then fitting is used until the input admittance Y_{11} is identical for both measurement and simulation. Thus, the value of r is determined to be 2.8, while the value of R_{G1} is 385 Ω.

Next, R_{G1} is subtracted from the null-biased Z-parameters and then converted to Y-parameters, from which the values of the pad capacitance C_{PG}, C_{PD}, and the overlap capacitance
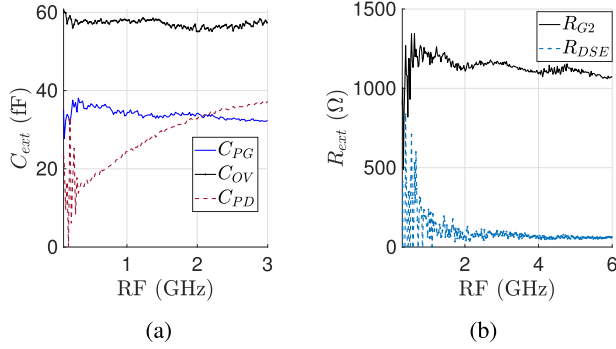
FIGURE 4. Extracted (a) extrinsic capacitances after de-embedding of R_{G1} and (b) R_{G2} and R_{DSE} over frequency.

FIGURE 5. Extracted (a) r_{gs} and (b) τ over frequency.

C_{OV} are extracted. Fig. 4a shows the extrinsic capacitances over frequency. The values at a lower frequency give the correct approximation of the capacitive elements. At higher frequencies, the extrinsic capacitances show dispersion due to the presence of R_{G2} and R_{DSE}.

Then, the extracted pad capacitances are de-embedded, and R_{G2} and R_{DSE} are extracted from the de-embedded Z-parameters, as shown in Fig. 4b. The values at higher frequencies are taken for the resistance estimation [15]. The extracted values are not constant and vary over frequency. Hence, fitting around the average extracted values is done in Cadence Spectre to match the extrinsic Y-parameters. The resultant extrinsic resistances for the single-finger TFT are $R_{G2} = 1078\,\Omega$ and $R_{DSE} = 10\,\Omega$.

C. INTRINSIC EXTRACTION AND MODELING

The intrinsic model for NQS extraction has been adopted from [13], as shown in Fig. 3. Here, r_{gs} and r_{gd} represent the distributed channel resistance corresponding to capacitances C_{gs} and C_{gd}, respectively. NQS signifies the inertia of the channel to a change in gate-source voltage. This phenomenon occurs at frequencies beyond f_T. The NQS effect has been represented by a transit delay τ in the literature. The delay appears both on the transconductance and channel conductance. The first-order representation of $g_{m,nqs}$ and $g_{ds,nqs}$ are given by [16],

$$g_{m,nqs} = \frac{g_m}{1 + j\omega\tau}, \tag{4}$$

$$g_{ds,nqs} = \frac{g_d s}{1 + j\omega\tau}. \tag{5}$$

The intrinsic Y-parameters in the strong inversion are given by the following equations [13]:

$$
\begin{aligned}
Y_{11,i} &= \omega^2(R_{gd}C_{gd}^2) + j\omega(C_{gd} + C_{gs}), \\
Y_{12,i} &= -\omega^2 R_{gd}C_{gd}^2 - j\omega C_{gd}, \\
Y_{21,i} &= g_m - \omega^2 R_{gd}C_{gd}^2 - j\omega(C_{gd} + g_m\tau), \\
Y_{22,i} &= g_{ds} + \omega^2 R_{gd}C_{gd}^2 + j\omega(C_{gd} - \tau g_{ds}).
\end{aligned}
\tag{6}
$$

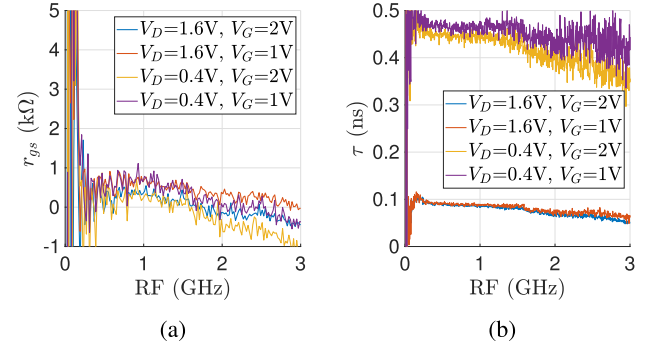The intrinsic capacitances, distributed resistances and transit delay are extracted from the above equations. The

resistances r_{gs} and r_{gd} are extracted for different gate-source voltages while keeping the drain-source voltage zero. It is observed that applying this method results in negative r_{gd} for all bias points, which means that r_{gd} is practically zero. The maximum $r_{gs} \approx 650\,\Omega$ is obtained for $V_{GS} = 0.4\,\text{V}$, as shown in Fig. 5a.

The channel delay τ obtained from Y_{21} is shown in Fig. 5b for different bias points. The channel delay decreases as V_{DS} increases. The lowering of channel delay between the source and drain signifies an increased carrier speed with an increasing electric field between the source and drain.

D. IMPLEMENTATION OF THE MODEL

The extrinsic components are implemented as constants in the Verilog-A model of the TFT.

The voltage dependency of C_{GD} and C_{GS} are implemented using the Meyer capacitance distribution of the total oxide capacitance of 90 fF. For a-IGZO TFTs, the validity of the Meyer model has already been proved for intrinsic capacitance in literature [17] and [18]. The total capacitance and the transconductance g_m determine f_T of the TFT.

The derived DC RPI-a model parameters control the low-frequency values of g_m and g_{ds}.

The NQS effect, i.e. the effect of τ on g_m, is modeled in the charge calculation with the help of the "laplace_nd" function in VerilogA. In the RPI-a model, there is no simple equation for g_m. So τ is introduced in the channel charge concentration (n_s) of the RPI-a model.

$$n_s = \frac{\epsilon_i \epsilon_0}{q t_{ox} \text{VAA}^\gamma} \frac{(V_{gs} - V_{th})^{\gamma+1}}{1 + \omega\tau} \tag{7}$$

The same function is used for g_{ds}, which can be given by

$$g_{ds} = \frac{g_{chi}}{1 + g_{chi}\frac{(R_D + R_S)}{N_{\text{finger}}}} \frac{1}{1 + \omega\tau}, \tag{8}$$

where g_{chi} is the intrinsic channel conductance of the RPI-a model and N_{finger} is the number of fingers in a TFT [5]. After repeated fitting, a constant value of the channel delay $\tau = 150\,\text{ps}$ is taken for our modeling purpose.
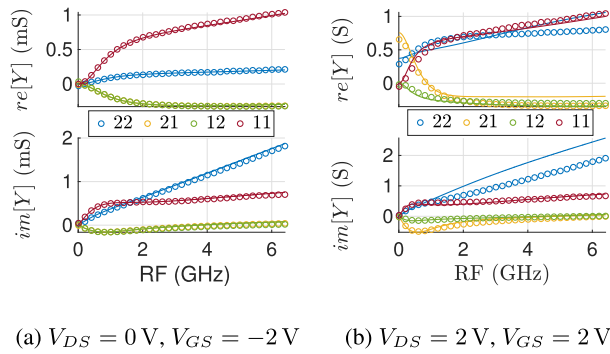
(a) $V_{DS} = 0\,\mathrm{V}$, $V_{GS} = -2\,\mathrm{V}$ (b) $V_{DS} = 2\,\mathrm{V}$, $V_{GS} = 2\,\mathrm{V}$

FIGURE 6. Simulated versus measured Y-parameters (solid lines - simulation and circular markers - measurement) of a single-finger TFT for different bias conditions. Legend (11,12,21 and 22) represents the subscripts of the Y-parameters.

E. SINGLE-FINGER TFT VERIFICATION OF THE MODEL

For the single-finger TFT, we get an almost perfect fit for all Y-parameters in the null-bias condition, as seen in Fig. 6a. When bias voltages are applied, as shown in Fig. 6b, $re[Y_{21}]$ and $re[Y_{22}]$ deviate from the measured values, especially as the frequency increases. Since the transconductance and the channel conductance are derived from the DC model, the values at higher frequencies are not estimated accurately. However, we get a good fit for Y_{21} up to around 1.0 GHz; the simulated $re[Y_{21}]$ become higher than measured data for $RF \geq 2$ GHz. The imaginary parts of Y-parameters give a good fit up to around 1.0 GHz, which also indicates the validity of the Meyer capacitance model.

F. MULTI-FINGER TFT VERIFICATION OF THE MODEL

To verify the derived model's scalability, a ten-finger ($N_{\mathrm{finger}} = 10$) was simulated for DC behavior using Cadence Spectre. It has been observed that V_{th} decreases as the number of fingers increases. For the measured multi-finger device, at $V_{DS} = 0.4$ V, a threshold voltage $V_{th} = -1.38$ V has been extracted using the integration method presented in [7].

The electric and magnetic field couplings between the fingers are ignored during the modeling. Due to a high separation of 20 µm between the adjacent fingers, their isolation is very high. The high isolation is verified by simulating the gate multi-finger architecture in Ansys HFSS, shown in Fig. 7a. The pad in the gate electrode is removed to simulate only the reactive coupling between the fingers. The reflection coefficient for the center finger (suffixed 'C') and its isolations with the adjacent left (suffixed 'L') and right (suffixed 'R') fingers are shown in Fig. 7b. The couplings are lower than −40 dB for frequencies up to 6 GHz. Hence the coupling can be ignored.

The simulated versus measured output and transfer characteristics are plotted in Fig. 8a and 8b, respectively. As seen in Fig. 8a, the simulated current (solid lines) matches the measurements (circular markers) better at high V_{GS}, whereas from Fig. 8b, the simulated transfer curve matches the measurement better at low V_{DS}.
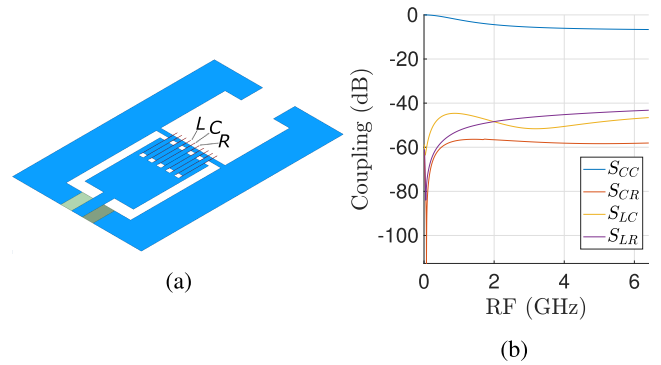

(a)

(b)

FIGURE 7. Reactive coupling simulation (a) setup and (b) results for the ten-finger TFT. The suffixes 'C', 'L' and 'R' indicate central, left and right fingers, respectively.

(a)

(b)
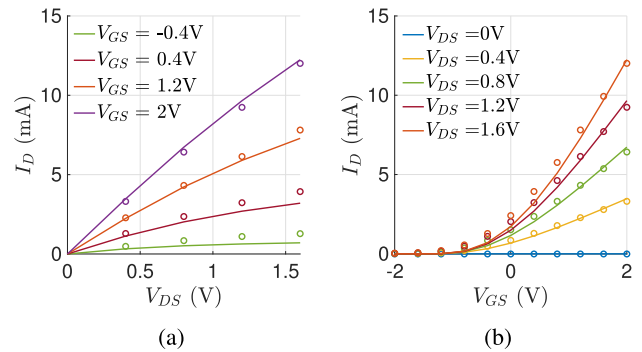
FIGURE 8. Simulated versus measured (a) output and (b) transfer characteristics (solid lines - simulation and circular markers - measurement) for a ten-finger TFT.

The Y-parameters are also compared for the ten-finger TFT. The extrinsic drain-source resistance is kept at $R_{DSE} = 10\,\Omega$ since it gives the best fitting. The simulated Y-parameters agree with the measured data in the null-bias condition, as shown in Fig. 9a.

The simulated Y-parameters under biasing show higher deviations, as depicted in Fig. 9b. The simulated $re[Y_{22}]$ deviates over a large frequency range.

G. TRANSISTOR SPEED AND AMPLIFICATION

The measured versus simulated short circuit current gain H_{21} and the maximum available power gain G_{max} are extracted from the S-parameter. The frequencies at which H_{21} and G_{max} reach unity are f_T and f_{max}, respectively.

The relation between f_{max} and f_T is given by [4]

$$f_{max} = \frac{1}{2}\frac{f_T}{\sqrt{2\pi f_T C_{gd} R_G + g_{ds} R_G}}, \qquad (9)$$

where $f_T = g_m/(2\pi(C_{gs} + C_{gd}))$.

Fig. 10a and 10b show f_T and f_{max} for the single and ten-finger TFTs, respectively. The bias points in both figures correspond to equal gate overdrive voltage and equal drain voltage for both TFTs.

The top halves of both the figures show f_T. The measured f_T values for the single and ten-finger TFTs are identical. Increasing the number of fingers scales the transconductance
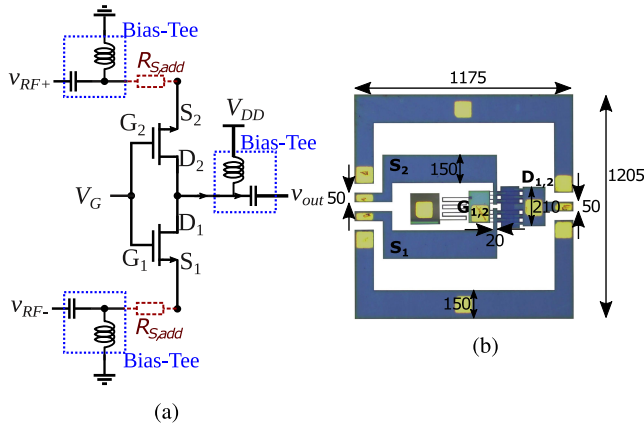
(a) $V_{DS} = 0$ V, $V_{GS} = -2$ V   (b) $V_{DS} = 2$ V, $V_{GS} = 1.6$ V

FIGURE 9. Simulated versus measured Y-parameters (solid lines - simulation and circular markers - measurement) of a multi-finger TFT for different bias conditions. Legend (11,12,21 and 22) represents the subscripts of the Y-parameters.

(a)   (b)

FIGURE 10. Simulated (solid lines) versus measured (circular markers) f_T and f_{max} of (a) single-finger and (b) ten-finger TFTs.

and the gate capacitances proportionately. Hence, f_T remains independent of the number of fingers.

There is a good agreement between the measured and simulated H_{21} for the single-finger and ten-finger TFTs ($<$ 5% error) at higher gate voltages. We can conclude that the Meyer capacitance model approximates the intrinsic oxide capacitances with a low error rate for higher gate voltage. However, at a low gate voltage of $V_G = 0.4$ V, the simulated f_T is underestimated. The higher measured f_T value could be due to additional traps due to impurities or uneven electric field distribution across the oxide that reduces the gate capacitance in reality.

The bottom halves of the figures depict f_{max} of the TFTs. There is a decrease in the multi-finger f_{max} compared with the single-finger TFT. This reduction in the oscillation frequency is due to the additional gate electrode material from the probe tip to the channel (see Fig. 2b), which increases the gate resistance.

For the bias points where f_Ts are in good agreement, we achieved a good agreement between the simulated and the measured f_{max} ($<$ 20% error), thereby proving a reasonable estimation of the gate resistances.

H. TRANSFER FUNCTION

Comparisons of the small signal transfer function between the simulation and measurement are shown in Fig. 11a and 11b for V_{DS} of 0.4 V and 2 V, respectively.

(a) $V_{DS} = 0.4$ V   (b) $V_{DS} = 2$ V

FIGURE 11. Transfer function S_{21} of the TFT for (a) $V_{DS} = 0.4$ V and (b) $V_{DS} = 2$ V.

TABLE 3. Root mean square error in the simulated transfer function.

V_{GS} (V)	-0.8	0.4	1.6	2
region	Weak	Moderate	Strong	Strong
RMSE $V_{DD} = 0.4$ V	0.08	0.067	0.086	0.088
RMSE $V_{DD} = 2.0$ V	0.129	0.264	0.360	0.365

Table 3 presents the root mean square error between the measured and simulated S_{21}. As seen here, the weak inversion presents a lower error than the strong inversion region. Moreover, the error is higher at higher V_{DS}.

The reason for this error is the fitted value of τ, which is higher than the value extracted for high V_{DS}, as seen in Fig. 5b. The RMS error increases above 1 GHz. Thus the frequency limit of the model for different bias points is around 1 GHz, which is the frequency of operation.

IV. THEORY OF a-IGZO TFT BASED FREQUENCY DOUBLERS

The schematic of the common-gate (CG) differential frequency doubler is shown in Fig. 12a. The device can be simulated and explained with the extracted behavioral model. The CG architecture helps avoid Miller capacitance. The differential architecture provides AC ground at the gate and the drain terminals when the doubler is symmetric [1]. If the two TFTs are symmetric, it helps eliminate the fundamental harmonic signal from the output.

A. NUMBER OF FINGERS VERSUS OUTPUT

The extracted model simulates the doubler for output power and conversion gain. A drain voltage of $V_{DS} = 2$ V and an input power P_{in} of 12.3 dBm are taken. The nominal V_{th} of the TFT is -0.95 V, as extracted from the single-finger TFT data (see Table 1).

First, the simulated P_{2f} is plotted over V_{GS} for different numbers of fingers $N_{fingers}$ in Fig. 13a. The variation of peak P_{2f} from the graph over $N_{fingers}$ is shown in Fig. 13b. As $N_{fingers}$ increases, the peak P_{2f} also increases.

However, the fabrication-yield scales inversely with the number of gate fingers. Moreover, a higher $N_{fingers}$ also increases the process mismatch. Hence, we chose a differential doubler with four fingers in each TFT.

FIGURE 12. (a) Schematic and (b) photo (background edited) of the top-view of a common-gate frequency doubler with dimensions in μm.
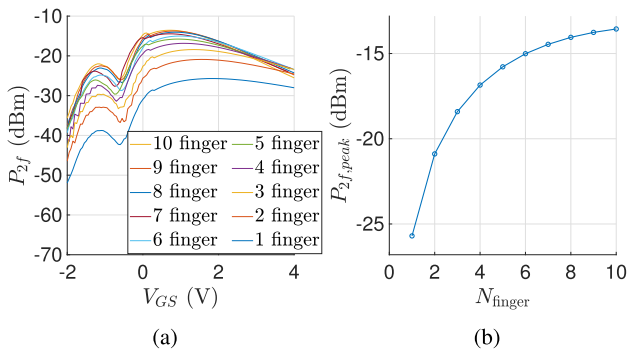

FIGURE 13. Simulated (a) P_{2f} over V_{GS} for different fingers, and (b) peak achievable P_{2f} over the number of fingers, given $V_{DS} = 2$ V, $V_{th} = -0.95$ V and $P_{in} = 12.3$ dBm.
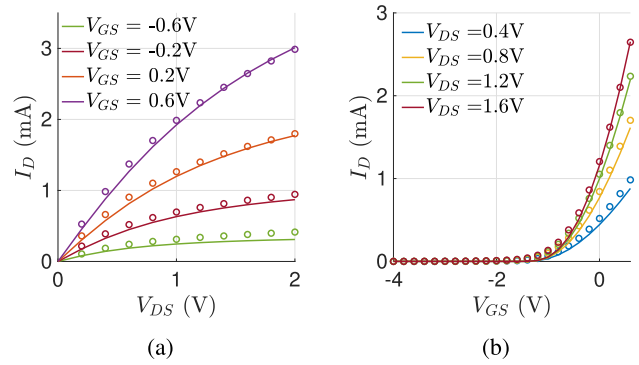

FIGURE 14. Initially measured (a) output and (b) transfer I-V characteristics of the doubler.
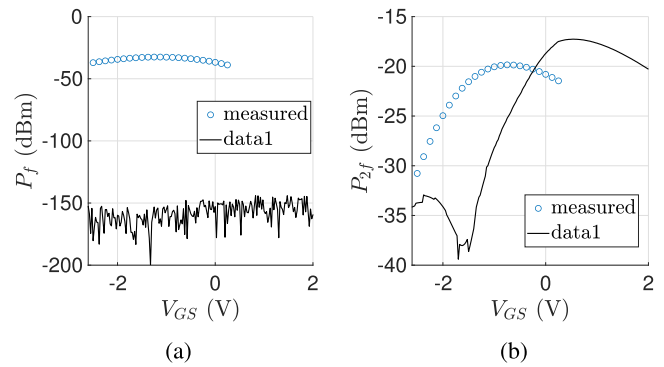
FIGURE 15. Measured versus simulated (a) P_f for and (b) P_{2f} for $V_{th} = -1.475$ V and $\Delta V_{th} = 0$ V.

V. RESULTS, SIMULATIONS AND DISCUSSIONS

The photo of the fabricated CG doubler is shown in Fig. 12b. The TFTs are susceptible to breakdown. Hence V_{DS} is limited up to 2 V during characterization.

The measurement setup for the doubler consists of an Agilent frequency synthesizer followed by an HP 3304C 20 dB attenuator and a Mini-Circuits ZHL 3010+ power amplifier. The overall gain provided by the attenuator and amplifier chain is around 16 dB. The output from the amplifier is then fed into a Mini-Circuits ZFSCJ-2-4-S+ 180° hybrid. The differential output from the hybrid is then applied to a Picoprobe 40A-GSSG-150-P ground-signal-signal-ground probe in combination with a Mini-Circuits bias tee ZX85-12G-S+. On the output of the doubler, a Mini-Circuits bias tee ZFBT-6G+ reads the output power and provides the drain bias.

The input power is calculated after de-embedding the attenuator and power amplifier chain gain of 16 dB, the hybrid loss of 1.1 dB [19], the GSSG probe loss of 1.6 dB [20] and the total connector loss of 0.5 dB from the available power of −1 dBm of the spectrum analyzer. Moreover, the common ground paths of the doubler, composed of Molybdenum, also attenuate the input power. The resistivity of the 90 nm molybdenum source terminal is taken to be around 5.6 ×

10^{-6} Ωcm [21]. Hence, an additional source path resistance $R_{S,add}$ of around 15 Ω is added to the inputs of each TFT.

A. DC SIMULATION

As mentioned in subsection III-F, the TFTs' V_{th} varies as the number of fingers increases. The initial measured DC characteristics of the doubler are shown in Fig. 14a and 14b with the circular markers. The best fit for the simulated current (solid lines) is achieved by fitting V_{th} to −1.475 V. A perfect estimation of V_{th} is impossible due to device asymmetry and process variation among the fingers.

B. GATE VOLTAGE VERSUS OUTPUT POWER

Since the breakdown voltage of the TFTs is unknown, a very low supply voltage $V_{DD} = 500$ mV is taken first for characterization. At an input power of around 12 dBm, the gate voltage is swept from −4 V to 0.25 V. Initially, both the first harmonic power P_f and second harmonic power P_{2f} increase as V_{GS} increases, as shown in Fig. 15a and Fig. 15b, respectively. The maximum values are obtained at around $V_{GS} = -0.725$ V, then both output powers decrease.

The simulated P_{2f} does not match the measurement in terms of the V_{GS} corresponding to the peak. The simulated peak P_{2f} is observed at $V_{GS} = 0.5$ V, i.e. at a value of 1.5 V higher than the measured peak location. Moreover, for the same 12.3 dBm of input power as in the measurement, the
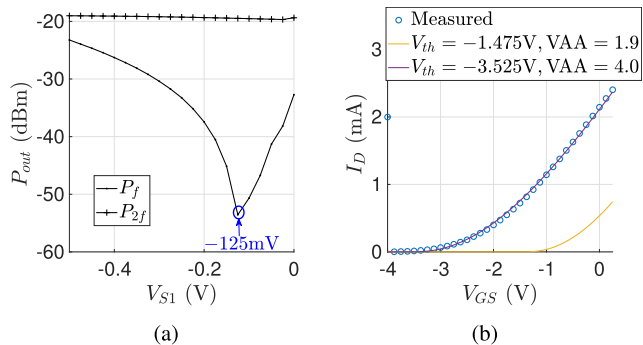
FIGURE 16. (a) Measured P_f and P_{2f} over V_{S1} and (b) measured versus simulated I_D during RF measurement.

peak simulated P_{2f} is -18 dBm. This value is 2 dB higher than the measured P_{2f}.

C. SPECTRAL IMPURITY

The doubler also shows a high first harmonic output P_f. The spectral impurity in doublers occurs from device asymmetry. Hence, the source voltage of one of the TFTs is swept to find V_{th}-mismatch while keeping the gate voltage $V_G = -725$ mV and drain voltage $V_D = 0.5$ V. The lowest P_f is obtained at $V_{S1} \approx -125$ mV (see Fig. 16a). The change in ΔV_{th} does not affect P_{2f}.

D. BIAS STRESS

As applied bias and P_{in} increase, the TFT V_{th} decreases. We can confirm this shift in V_{th} from the measurements and fitting of the model. The drain current is measured simultaneously as a V_{GS} sweep for RF is performed. Fig. 16b shows the measured I_D with circular markers. By keeping the same $V_{th} = -1.475$ V (from Fig. 14), we cannot achieve the same simulated current values for the same V_{GS}. Hence, we sweep V_{th} and the fitting parameter VAA in Cadence Spectre to arrive at the same current. The best fitting is achieved at values $V_{th1} = -3.525$ V, $V_{th2} = -3.65$ V and VAA $= 4.0$. This change implies that V_{th} has moved to a more negative value under the influence of the RF signal. The adjustment in VAA indicates a change in mobility as well.

The negative shift in V_{th} is assumed to be caused by the long exposure of the TFT to bias and heat generated by the RF input, as suggested in [22]. Moreover, the presence of water molecules and hydrogen atoms in the oxide can also cause a negative V_{th} shift [22], [23].

The RF output behavior is also simulated with the final chosen values $\gamma = 1.014$, $V_{th1} = -3.525$ V, $V_{th2} = -3.65$ V and VAA $= 4.0$. The input power is kept at 12.3 dBm. As shown in Fig. 17a, the simulated fundamental harmonic output power has a lower deviation (≈ 3 dB) from the measured values.

The simulated second harmonic output P_{2f} agrees better with the measured result, as shown in Fig. 17b. One must note that an accurate simulation result is impossible to obtain as there are four fingers in each transistor. There may be
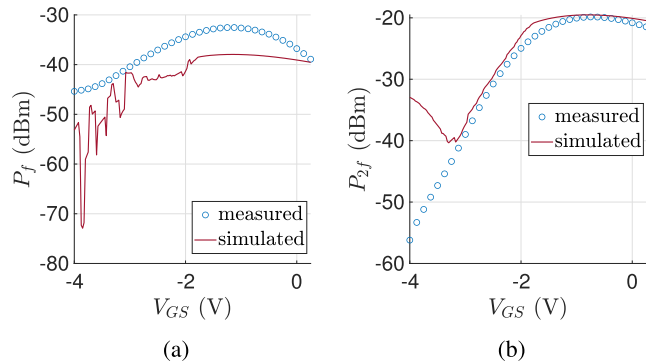

FIGURE 17. Measured (circular markers) versus simulated (solid lines) (a) P_f and (b) P_{2f} for $\gamma = 1.014$, $V_{th1} = -3.525$ V, $V_{th2} = -3.65$ V and VAA $= 4.0$ at $P_{in} = 12.3$ dBm.
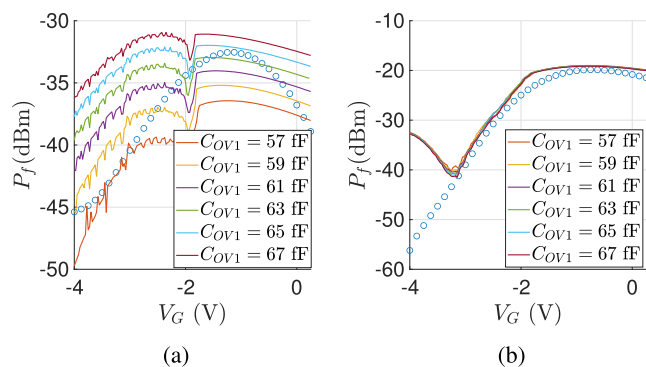

FIGURE 18. Measured versus simulated (a) P_f for and (b) P_{2f} for different values of the overlap capacitance per finger C_{OV1} of TFT 1 while keeping C_{OV2} of TFT 2 constant.

mismatches in the process parameters among all the fingers. However, the peak simulated P_{2f} is the same as the measured peak.

E. MISMATCH IN OVERLAP

The multi-finger layout is susceptible to alignment issues since low-resolution PET foil is used for UV exposure. This misalignment could cause a mismatch between the overlap lengths between the two TFTs. As a result, the overlap capacitances between the two TFTs can be different. The mismatch can also result in higher spectral impurity in addition to the threshold and mobility mismatch. The effect of overlap capacitance C_{OV} per finger mismatch on P_f and P_{2f} are shown in Fig. 18a and 18b, respectively. The TFT with the lower $V_{th1} = -3.525$ V and higher $C_{OV1} = 63$ fF per finger shows a better fit between the simulated and the measured measured P_f. The change in the overlap capacitance does not affect P_{2f}.

However, the effect of C_{OV} mismatch can only be speculated. The mismatch in intrinsic capacitance could also lead to a similar effect in P_f and spectral purity.

F. RF VERSUS BREAKDOWN

One of the most important characteristics of a frequency doubler is compression. It is the condition at which P_{2f}
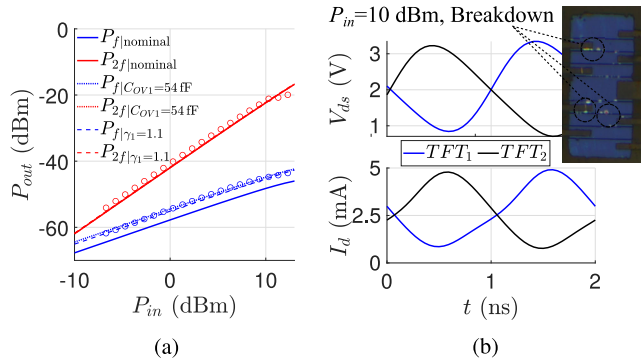
FIGURE 19. (a) Measured (circular markers) versus simulated (solid lines) P_{out} over P_{in} with the breakdown (inset - doubler after breakdown) (b) simulated V_{ds} and V_{gs} for $\gamma = 1.014$, $V_{th1} = -3.525$ V, $V_{th2} = -3.65$ V and VAA = 4.0 at $P_{in} = 10$ dBm; the inset shows a photo of the channels' breakdown.

becomes saturated. The doubler output power normally increases when V_{DS} increases. Here the input power is swept for a $V_{DS} = 2$ V, $V_{GS} = -0.775$ V, and $V_{S1} = -125$ mV to compensate for a $V_{th1} - V_{th2} = -125$ mV. The simulation is also done with the same biasing conditions. As shown in Fig. 19, the nominal simulation using the parameters from Table 1 agrees with the measured value in terms of the slope. The simulated $P_{2f|nominal}$ is underestimated by around 1 dB.

However, the measured $P_{f|nominal}$ is underestimated in the simulation by around 3 dB. The simulation shows that P_f can be matched to the measured data if the total gate capacitance C_{GG1} of TFT 1 is lowered by 3 fF. The same effect is also observed if the power law mobility parameter of the TFT 1 can be increased from its nominal value (1.0144) to 1.1. Further investigation is required to pinpoint the exact source of the spectral impurity.

The measured power starts reducing at $P_{in} = 10$ dBm. The inset in Fig. 19b shows that the device breaks down beyond this point. Not all the fingers break down simultaneously, indicating that the heat generation is not uniform across the fingers. The simulated V_{ds} and I_d over time of the two TFTs at the input power of $P_{in} = 10$ dBm. The root-mean-square (rms) V_{DS} is only around 0.84 V at this point, while the rms drain current per TFT is 1.35 mA. Ideally, a 47 nm thick Al_2O_3 dielectric layer should easily sustain this value. We assume that the presence of impurities such as water or hydrogen in the oxide layer reduced the breakdown voltage of the dielectric.

G. COMPARISON WITH THE STATE OF THE ART
The application of a-IGZO in RF is a relatively new field; hence, there are only a few publications. The presented frequency doubler is a record in terms of the frequency of operation. The previous work in [1] showed frequency doubling for an input frequency of 100 MHz. Table 4 shows some TFT technology and its performance in a frequency doubler.

TABLE 4. Comparison of doubler with the state of the art.

Ref	W/L (µm/µm)	RF (MHz)	Gain (dB)
a-IGZO TFT [1]	500/3	100 × 2	−44
Graphene Ambipolar [24]	4/6	11 × 2	−17.7
This work	4× 100/0.8	500 × 2	−32

VI. LIMITATION OF THE MODEL
The model adopted suffers from the following limitations, and further investigations are required:
- The channel transit delay τ is considered constant in the model, while this is a function of the drain-source voltage, as described in subsection III-C. The effect of velocity saturation is not included in the model.
- The simulated transfer function S_{21} deviates substantially from measured values as V_{DD} and RF increase.
- The modeling of the capacitor is done with Meyer's model, which is ideal for frequency below f_T [25]. Applying an input signal beyond f_T will cause the transistor capacitances to charge and discharge slowly compared to the input signal. The dispersive behavior of capacitance is not considered in the model.
- The error in the output admittance is high, as shown in Fig. 6b and 9b. The drain-source capacitance is included in the pad capacitance and is considered constant. Any effect of the drain-induced barrier lowering is not included.
- Temperature dependencies of model parameters are not considered.
- Hot carrier effect and trapping and de-trapping of charge carriers in the oxide cannot be simulated by the model.

VII. CONCLUSION
This paper presents the efficacy of the RPI-a model in conjunction with small-signal modeling for the simulation of GHz TFT circuits based on a-IGZO. We verified the small-signal model parameters for a single-finger and a ten-finger TFT. An excellent agreement is achieved between measurement and simulation for the obtained DC and RF parameters. The agreement between most Y-parameters makes the model suitable for basic RF circuit simulation. However, the DC output conductance is underestimated at GHz frequencies for higher bias points.

A four-finger TFT-based doubler is characterized and also evaluated with the derived model. The doubler shows a conversion gain of -32 dB for an input signal of 500 MHz without impedance matching. It is the first doubler in literature with GHz output frequency. Owing to the non-linear relation between V_{gs} and I_d, we could achieve the frequency doubling beyond transistor f_T and f_{max}. The second harmonic frequency is a new record in terms of conversion gain of a-IGZO doubler. Our previous work presented a 100 MHz to

200 MHz doubler with only a -44 dB conversion gain [1]. The application of impedance matching can further improve the conversion gain in the future.

Applying the RF input power, a significant V_{th} shift is observed. This shift is hypothesized to be due to impurities in the dielectric. Since the TFT is handled in a laboratory atmosphere, the dielectric-semiconductor and the semiconductor-encapsulation interfaces have water molecules that reduce the lifetime of the transistor.

We can feed the shift in the threshold voltage to the model to replicate its effect on the second harmonic output. The model can also simulate the spectral impurity of the doubler based on the threshold voltage mismatch.

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