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RESEARCH ARTICLE

Accurate Layout-Dependent Effect Model in 10 nm-Class DRAM Process Using Area-Efficient Array Test Circuits

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ABSTRACT This study presents an accurate model for non-monotonic layout-dependent effects (LDEs) measured using 10nm-class dynamic random access memory technology. To collect the LDE measurement data, a test module with an individually addressable array of 240 transistors has been developed. The proposed test module occupies a small area of 0.1 square millimeters with a density 15 times higher than that of typical scribe-line circuits. The proposed model employs a novel empirical function to precisely describe the non-monotonic dependence on each pair of geometrical parameters, such as the diffusion lengths, lateral/vertical spacings to the adjacent shallow trench isolations, and gate-to-contact distances. Additionally, this model can be easily realized as a sub-circuit model in standard circuit simulators, requiring only two additional tuning parameters for the core transistor. The fitted model demonstrates excellent agreement with the measured values obtained from test modules (802 transistors in total), achieving mean absolute errors of 0.7% for the drain current in the saturation region and 4.7 mV for the threshold voltage.

INDEX TERMS Addressable array circuit, layout-dependent effects, dynamic random-access memory, scribe lines, shallow trench isolation.

I. INTRODUCTION

Layout-dependent effects (LDEs) refer to the change in the electrical performance of a transistor caused by the layout of the surrounding structures in an integrated circuit (IC) [1]. LDEs result in unintended failures in ICs unless they are properly accounted for during circuit simulations [2], [3]. Thus, it is crucial to characterize their behavior depending on technologies to achieve the desired power and performance of ICs [4]. For example, one primary cause of LDEs is the stress on the transistor channel imposed by the shallow trench isolation (STI) [5], which can lead up to a 20% variation in the transistor drain current in deep submicron CMOS processes [6]. Although there exist layout techniques such as dummy fill insertion that can mitigate LDEs to some degree [7], layout optimization for logic gates [8], [9], [10], [11], [12] and placement techniques [13], obtaining an accurate model that can predict LDEs is crucial for optimizing circuit performance and avoiding design respins.

The studies for LDE models for circuit simulation [3], [14], [15], [16] were largely initiated by Pelgrom's seminal work on matching transistors [17], highlighting the significance of acknowledging LDEs in analog/mixed-signal circuits [18] and SRAM circuits [19] designed in deep-submicron technologies. In the early stages, the LDE research was devoted to analyzing the physical causes of these effects, such as mechanically-induced stress caused by the isolation dielectrics such as STIs [5], [6] and inter-layer

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dielectrics (ILD) [20]. Other contributors including well proximity [21] were subsequently discovered to be critical. The BSIM4(-CMG) model, which accounts for these LDEs [6], [16], [22], [23], [24], has been used as the golden reference in many integrated device manufacturers (IDMs) and electronic design automation (EDA) industry. Recently, attention has been turned to novel LDEs in advanced deep submicron CMOS technologies, such as high-k metal gate (HKMG) [10], [25] and FinFET [26], [27] processes, raising the concerns on LDEs as the technology scales further [9], [28], [29], [30], [31]. The physical mechanisms underlying these effects are complex with high degrees of interdependencies, and it is particularly challenging to maintain high accuracy of the physics-based models across multiple process generations [1]. Especially, the LDEs beyond 10-nm DRAM technologies have not been well studied and a majority of IDMs rely on their own proprietary models, which tend to be relatively simplistic, describing only the monotonic and symmetric changes with respect to the layout parameters.

However, in deeply-scaled IC technologies such as the current 10nm-class DRAM technologies, LDEs may not be a monotonic function of the geometrical parameters, such as the diffusion lengths, spacings to the adjacent STIs, and gate-to-contact distances [28]. The currently-available LDE models [6], [22], [24], [28] cannot accurately express their non-monotonic dependencies as they only use monotonic functions such as the inverse of a first-order polynomial. Characterizing the non-monotonic dependencies in experimental measurements also presents a challenge because it requires a large number of test transistors spanning the multi-dimensional space of the geometry parameters.

To address these challenges, this study presents an area-efficient test module for measuring the LDEs in 10nm-class DRAM technology and proposes a novel, empirical model that can accurately capture the non-monotonic characteristics of the LDEs. The proposed test module uses an SRAM-like addressable array to contain as many as 240 transistors within a small area of the scribe line [32], [33]. The proposed LDE model uses a simple basis function that adds an exponential factor to the previously used monotonic function, and it can fit the measured LDE data with a mean absolute error (MAE) of 0.7% for the drain current in the saturation region ($Idsat$) and 4.7 mV for the threshold voltage (Vth). This LDE model can be easily incorporated into current industry-standard models and provide accurate predictions on the LDEs for the layouts of various analog and digital peripheral circuits in DRAMs.

II. PROPOSED MODEL AND TEST STRUCTURE

A. DEFINITION OF LAYOUT PARAMETERS

As illustrated in Fig. 1, we define the layout shape of a transistor including the surrounding geometry using eight parameters: i) SA and SB denote the diffusion lengths in the left and right directions, respectively; ii) $STIL1$ and $STIL2$ denote the lateral spaces between STIs; iii) $STIV1$ and $STIV2$ denote the vertical spaces between STIs; iv) CA and CB denote the left and right gate-to-contact distances, respectively. We characterize the performance variation caused by these eight geometrical parameters considering the transistor performance based on the threshold voltage shift ΔVth and drain current shift $\Delta Idsat$.

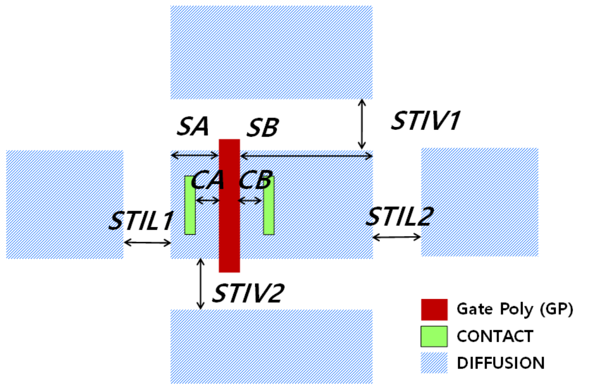

FIGURE 1. Schematic of a transistor device-under-test (DUT) structure and definition of the surrounding layout parameters used in the proposed model.

B. PROPOSED NON-MONOTONIC LDE MODEL

This study aims to obtain an empirical model for a pair of layout parameters for each pair of side directions. This model should also account for both symmetric and asymmetric layouts; therefore, we utilize two empirical functions for the symmetric and asymmetric cases. To smoothly approximate non-monotonic behaviors, we introduce a novel basis function that multiplies an exponential term $e^{-1/x}$, which rapidly varies while the parameter x is small and becomes constant elsewhere, to the conventional reciprocal function $1/x$. For the symmetric case in which a pair of layout parameters (i.e., x_1 and x_2) vary together, the contributions of the symmetric variation are defined by the function:

$$S(x_1, x_2) = e^{-1/(a(x_1+x_2+b))} \times \frac{d}{(x_1 + x_2 + c)}, \tag{1}$$

where a, b, c, and d are the fitting parameters used to accurately fit the measured data.

For the asymmetric case, the function describing only the asymmetric variation in the layout is

$$A(x_1, x_2) = 2\beta(n^2 - \frac{1}{4})(\frac{n(x_1 + x_2)}{n(x_1 + x_2) + x_1 - x_2} + \frac{n(x_1 + x_2)}{n(x_1 + x_2) - (x_1 - x_2)} - 2), \tag{2}$$

where β and n are fitting parameters. Notably, this equation is empirically derived such that $A(x_1, x_2) = 0$ when $x_1 = x_2$ and $A(x_1, x_2) = 1$ when $x_1 = 0$ or $x_2 = 0$. Therefore, $A(x_1, x_2)$ is non-zero only for an asymmetric layout.

By combining (1) and (2), we can model LDEs for the layout shown in Fig. 1 as follows:

$$F(x_1, x_2) = S(x_1, x_2) + S(x_1, x_2) \times A(x_1, x_2). \quad (3)$$

We use (3) to represent Vth and $Idsat$ variations as follows:

$$\Delta Vth(x_1, x_2) = F^{Vth}(x_1, x_2) - F^{Vth}(x_1', x_2'), \quad (4)$$

$$\Delta Idsat(x_1, x_2) = F^{Idsat}(x_1, x_2) - F^{Idsat}(x_1', x_2'). \quad (5)$$

Here, x_1' and x_2' denote the reference layout parameters used in core model extraction, and the functions in (4) and (5) become zero when $x_1 = x_1'$ and $x_2 = x_2'$. Each $\Delta Vth(x_1, x_2)$ value in (4) and each $\Delta Idsat(x_1, x_2)$ value in (5) have six fitting parameters: a, b, c, d, β, and n.

The proposed non-monotonic LDE model considers the variations in channel length L and width W by employing a binning method similar to that used in the BSIM model [34]. For example, for the upper and lower values of L_1 and L_2 in a bin range of $L_1 < L < L_2$, $\Delta Vth(x_1, x_2)$ can be obtained for each parameter of the sets $[a, b, c, d, \beta, n]_{L=L_1}$ and $[a, b, c, d, \beta, n]_{L=L_2}$. For clarity, we denote these values as $\Delta Vth_{L_1}(x_1, x_2)$ and $\Delta Vth_{L_2}(x_1, x_2)$. Then, the intermediate variation for ΔVth within the range $L_1 < L < L_2$ can be represented as follows:

$$\Delta Vth_{final}(x_1, x_2, L) = \Delta Vth_0(x_1, x_2) + \frac{\Delta Vth_l}{L}, \quad (6)$$

$$\Delta Idsat_{final}(x_1, x_2, L) = \Delta Idsat_0(x_1, x_2) + \frac{\Delta Idsat_l}{L}, \quad (7)$$

where the function introduced in (6) and (7) is expressed as follows:

$$\Delta Vth_0(x_1, x_2) = \frac{\Delta Vth_{L_2}(x_1, x_2)/L_1 - \Delta Vth_{L_1}/L_2}{(L_1^{-1} - L_2^{-1})^{-1}}, \quad (8)$$

$$\Delta Vth_l(x_1, x_2) = \frac{\Delta Vth_{L_2}(x_1, x_2) - \Delta Vth_{L_1}(x_1, x_2)}{L_1^{-1} - L_2^{-1}}, \quad (9)$$

$$\Delta Idsat_0(x_1, x_2) = \frac{\Delta Idsat_{L_2}(x_1, x_2)/L_1 - \Delta Idsat_{L_1}/L_2}{(L_1^{-1} - L_2^{-1})^{-1}}, \quad (10)$$

$$\Delta Idsat_l(x_1, x_2) = \frac{\Delta Idsat_{L_2}(x_1, x_2) - \Delta Idsat_{L_1}(x_1, x_2)}{L_1^{-1} - L_2^{-1}}. \quad (11)$$

The width W variation can be represented similarly by applying the same binning method and formula that is adjusted for W instead of L.

C. ADDRESSABLE ARRAY TEST CIRCUIT

The test devices were located in an addressable array circuit, as shown in Fig. 2. The transistors to be measured can be chosen by their row and column addresses. The voltages were applied to the four terminals of the transistor (i.e., the gate, drain, source, and bulk). DUT cells were placed in the space between each pair of probe pads along the row, and the switching circuits were placed under the probe pads. A unit module with 24 pads is generally used in the DRAM process; however, only 17 pads were utilized for the proposed array circuit, including five pads for row address, four pads for column address, four pads to force voltage to the gate, drain, source, and bulk nodes, two pads to sense the voltage of the drain and source nodes, and power and ground pads of the address circuits (VDDA, VSSA). In this study, we set the supply voltage at the VDDA pad to 2.0V during the measurements. The remaining pads are utilized by directly connecting to drain and source ports of DUTs in the array circuits for comparing the measurement accuracy. As shown in Fig. 2, the unit array circuit has 20 blocks of circuits with

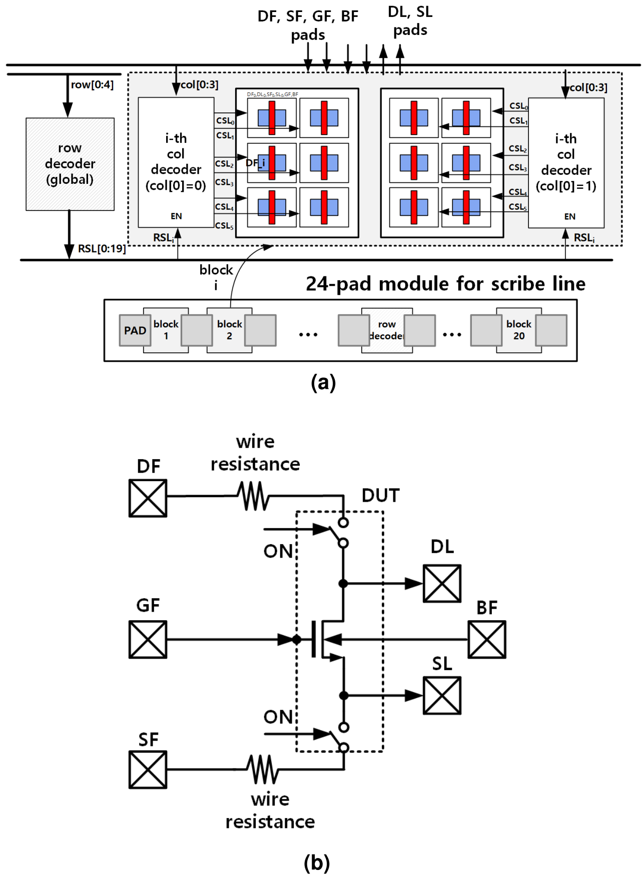

FIGURE 2. Schematic of a part of the addressable array test structures in the scribe lines. (a) Addressable array circuit concept in the scribe-line pad module. (b) Ohmic IR drop compensation technique in each DUT cell.

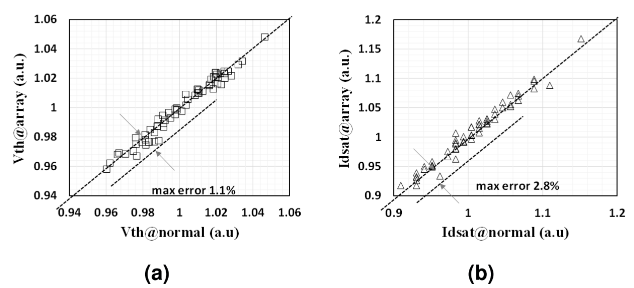

FIGURE 3. Comparison between measurements obtained by the addressable array test and ordinary measurements for the normal threshold voltage n-type MOSFETs (63 data points). The threshold voltages (left) and drive currents (right) were measured using both testing methods.

TABLE 1. Description of the LDE parameters. L and W denote the length and width of the transistor, respectively. # of points indicates the number of sweep points required to measure each parameter.

Parameter	Description	# of L	# of W	# of points
$SA(B)$	Diffusion length	3	2	12-18
$STIL1(2)$	Lateral space	3	2	12-18
$STIV1(2)$	Vertical space	3	2	12-18
$CA(B)$	Gate-to-contact distance	3	2	6

a pair of column decoder circuits and a single-unit DUT cell containing 12 transistors between a pair of switching circuits at both sides.

We measured Vth and $Idsat$ for the test devices using a test algorithm that can compensate for the voltage drop and leakage current. The switching circuit used for compensating the ohmic IR voltage drop is shown in Fig. 2. The voltage drop occurs owing to the wire resistance depending on the distance from the probe pad to the selected DUT cell. This can be compensated for by iterating the force voltage at the DF node (i.e., V(DF)), as shown in Fig. 2 (b). While iteratively increasing the value of V(DF) until the voltage reaches the desired value (e.g., VDD), the test program measures the voltage near the drain port of the transistor V(DL) and if it equals the desired drain supply voltage, then it stops the current iteration and repeats the same procedure by selecting another transistor located at the next address.

Since a large number of transistors share the same pad, it is necessary to cancel the leakage contributions from the off-state transistors when measuring the current of one specific transistor. To do so, the test algorithm makes two measurements on the drain current and computes the difference. The first measurement is made with V(DF), V(DL), and V(GF) set to the desired voltages, and the second measurement is made with V(GF) forced to 0. This can effectively cancel the leakage contributions from the off-state transistors.

The accuracy of the addressable array test was validated through comparisons with ordinary pad structures, as shown in Fig. 3. The linear relationship between the Vth and $Idsat$ data measured using ordinary and array-type test circuits validated the accuracy of the addressable array technique. The maximum observed errors were only 1.1% for Vth and 2.8% for $Idsat$.

D. PARAMETER EXTRACTION

We extracted the LDE from ΔVth and $\Delta Idsat$ independently. The entire sequence used to extract the LDE model parameters is summarized in the following four steps:

- Step 1: Extract a, b, c, and d in (1) from ΔVth data of the symmetric layout.
- Step 2: Extract β and n in (2) from ΔVth data of the asymmetric layout.
- Step 3: Extract a, b, c, and d in (1) from $\Delta Idsat$ data of the symmetric layout.
- Step 4: Extract β and n in (2) from $\Delta Idsat$ data of the asymmetric layout.

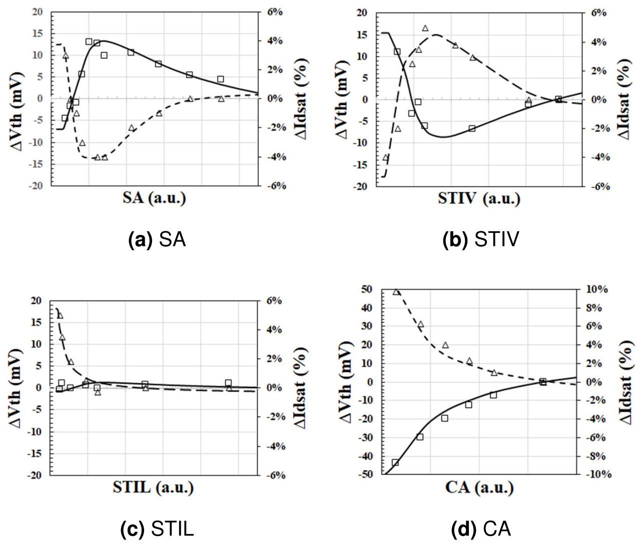

FIGURE 4. Comparisons between the experimental data and proposed models for four symmetric cases (squares: ΔVth data; triangles: $\Delta Idsat$ data; lines: model).

III. EXPERIMENTAL RESULTS

We experimentally demonstrated the proposed LDE model by implementing an array test circuit in a 10nm-class DRAM process. Thirteen modules were fabricated, each containing 240 DUTs. All 3120 transistors with different device types and geometries were implemented in scribe lines in the form of an addressable array circuit and 802 transistors were fitted for characterizing STI-related LDEs. The combinations of each parameter tested in the circuits are summarized in Table 1. The supply voltages for the row and column address pads were set to 3 V to ignore the voltage drop in the NMOS switch connected to the DUTs. The drain voltages were swept in the range of 0 to 1.2 V. Before fabrication, all pad module designs were validated using circuit simulations for IR drop compensation. The proposed LDE model accounting for $\Delta Idsat$ and ΔVth is realized as a sub-circuit model in the HSPICE™circuit simulator [35]. The sub-circuit model contains a core model parameter as an instance of BSIM4, and the variations of Vth and $Idsat$ can be easily added using the built-in current scaling parameter `mulid0` and threshold voltage shifting parameter `delvtho`. $\Delta Idsat$ is converted by the ratio $(\Delta Idsat + Idsat0)/Id0$ to the original drain current value $Idsat0$ extracted from the corresponding circuit simulation.

Fig. 4 shows a comparison between the measurement and proposed models for the sample case of symmetric layouts (e.g., $SA = SB$) for three cases of LDEs: $SA(SB)$, $STIL1(\cdot 2)$, $STIV1(\cdot 2)$, and $CA(CB)$. It should be noted that each transistor used in Fig. 4 is different because the scope of this study is not to discuss the physical aspects of LDEs but to show the accuracy of the proposed model for capturing the non-monotonic nature including the asymmetric variation of the LDE parameters. For the other cases not shown in

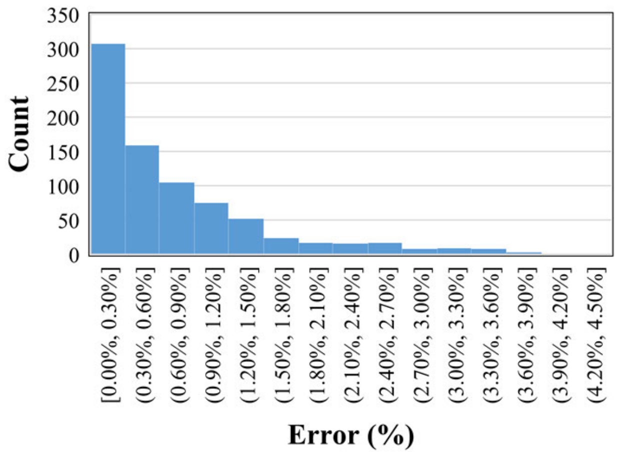

FIGURE 5. Error histogram of $\Delta Idsat$ for 802 transistors.

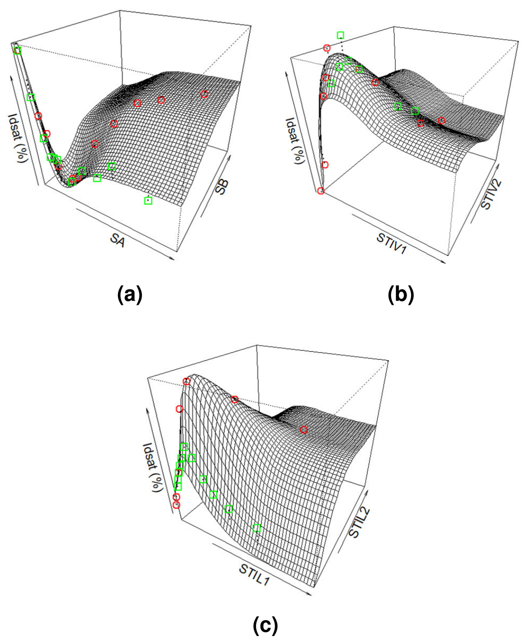

FIGURE 6. Comparisons of $Idsat$ between the measurements and proposed model for $SA(B)$, $STIV1(2)$, and $STIL1(2)$ (green symbols: data for symmetric cases; triangular symbols: $\Delta Idsat$ data for symmetric cases; surface: model).

this paper, the proposed model can fit the data with small errors owing to the use of six additional fitting parameters. Our proposed model accurately matched the measured data by capturing the inflection points that originate from the non-monotonic nature of the measurement data. The MAEs were 0.7% for $Idsat$ and 4.7 mV for Vth. The error histogram for $Idsat$ is shown in Fig. 5. Note that errors for Vth are not included because most ΔVth data (over 700 points) do not sufficiently show clear trends for parameter extraction.

As shown in Fig. 5, our model describes the LDEs for the asymmetric parameter variations for (SA,SB), ($STIL1$,$STIL2$), and ($STIV1$,$STIV2$). The surface shows the proposed model, and the green symbols indicate the measured data for the asymmetric cases, which agree with each other. The accuracy of this modeling methodology should be investigated in future studies using circuit simulations because most transistors in practical chip implementations are surrounded by asymmetrically shaped STIs rather than symmetrically shaped STIs.

IV. CONCLUSION

This study developed a model that can describe the non-monotonic, asymmetric dependences of LDEs on layout parameters, which are pronounced in 10nm-class DRAM processes. This was achieved by proposing a general yet sophisticated formula to describe the non-monotonic LDE characteristics obtained by simultaneously observing various physical factors influencing the LDE by implementing large-scale test structures in the form of addressable arrays. Moreover, the proposed model accounted for the asymmetric layout parameter variations. The proposed model can provide accurate predictions on the changes in transistor characteristics owing to the layout shapes, yet it is simple enough to be included in the industry-standard compact models, such as BSIM. The presented LDE model and characterization methodology can help optimize the circuit layout designs for 10nm-class DRAM processes and beyond. Although this work demonstrated the effectiveness of the proposed model only with describing the STI-dependent effects, we believe it can be further extended to other LDEs such as well-proximity effects and metal-gate proximity effects, while covering the wider range of layout geometries as well.

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