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RESEARCH ARTICLE

Linear Gain Controller Aided Iterative Soft Sequential Acquisition for Primitive Polynomials

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ABSTRACT In 5G cellular communication systems, achieving low latency is crucial to support the 'tactile' Internet with response times of less than one millisecond. Traditional initial synchronization methods face challenges due to high delays. This manuscript presents a novel approach using an EXtrinsic Information Transfer (EXIT) chart-aided method to investigate the concurrence of m-sequences using Iterative Soft Sequence Estimation (ISSE) in a communication channel. The ISSE technique leverages the concept of an Automatic Gain Controller (AGC), which gradually increases the gain as the number of chips in the m-sequence generator grows, both at the transmitter and the receiver. Our ISSE method stands out by achieving sequence synchronization at the receiver with as few as F successive chips for a sequence of $(2^F - 1)$ chips. We base our work on the EXIT chart, eliminating the need for interleavers, which introduce transmission delays. To address the delay issue, we exploit the inherent interrelationship of the m-sequence generator's concern chips, which have a duration of $(2^F - 1)$, as influenced by the Linear Feedback Shift Register (LFSR) in our ISSE model. We observe that low-order Primitive Polynomials (PPs) exhibit lower Erroneous Loading Probability (P_e) than higher-order PPs at a specific Signal-to-Noise Ratio (SNR). PPs with identical order but fewer connection taps outperform those with more connection taps. The EXIT chart analysis reveals that lower-order PPs exhibit a larger opening tunnel between the outer and inner curves, resulting in higher achievable rates in our proposed system. Moreover, PPs with lower order achieve higher Mutual Information (MI) more efficiently with the assistance of our ISSE system compared to higher-order PPs.

INDEX TERMS Acquisition time (AT), pseudo-noise (PN), iterative soft sequential estimation (ISSE), m-sequence.

NOMENCLATURE

Name	Abbreviation
3GPP	3rd Generation Partnership Project.
5G	5th Generation.
AGC	Automatic Gain Controller.
AMI	Average Mutual Information.
AT	Acquisition Time.
AWGN	Additive White Gaussian Noise.
BCH	Bose Chaudhuri Hocquengem.
BPSK	Binary Phase Shift Keying.
BS	Base Station.
CDMA	Code Division Multiple Access.
DU	Delay Uunit.
DRSSE	Differential Recursive Soft Sequential Estimation.
DS-CDMA	Direct Sequence-Code Division Multiple Access.
DS-UWB	Direct Sequence Ultra Wide Band.
EXIT	EXtrinsic Information Transfer.
FH	Frequency Hopping.
IoT	Internet of Things.
IS	Interim Standard.
ISSE	Iterative Soft Sequential Estimation.

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MI	Mutual Information.
MS	Mobile Station.
LLRs	Log Likelihood Ratios.
LFSR	Linear Feedback Shift Registers.
PN	Pseudo-Noise.
PPs	Primitive Polynomials.
PTL	Phase-Tracking Loop.
RASE	Rapid Acquisition Sequential Estimation.
RSSE	Recursive Soft Sequential Estimation.
SCR	Soft Chip Register.
SISO	Soft-In-Soft-Out.
SNR	Signal to Noise Ratio.
SS	Spread Spectrum.
TL	Tracking Loop.

Symbols	**Abbreviation**
β	Gain of AGC.
α_i	Channel State.
m	M-sequences.
f_i	Generated chips.
x_i	Received chips.
$L(x_i)$	The soft output of the SISO decoder.
P_e	Erroneous Loading Probability.
π	Product Operation.
n_i	AWGN noiseis has zero mean.
$L_e(f_i)$	*Extrinsic information*.
L_{apr}	*A priori information*.
$F \times I$	Total number of chips processed.
$N_\tau D$	Mean Acquisition Time.
τ_D	Dwell time.
dB	Decibel.
$g_1(D)$	$1+D^2+D^5$.
$g_2(D)$	$1+D+D^2+D^4+D^5$.
$g_3(D)$	$1+D+D^3+D^4+D^{13}$.

I. INTRODUCTION

The extensive use of digital gadgets and the Internet of Things (IoTs) has effectively increased information traffic [1], [2], [3], [4]. As a result, efficient transmission of data through the communication channel is crucial to effectively utilize the available bandwidth [5], [6], [7]. Obtaining synchronization promptly and quickly is necessary to ensure secure communication with minimal errors or error-free transmission [2], [5], [6], [8], [9]. To enhance system efficiency, iterative decoding techniques are adopted, facilitating the exchange of *extrinsic information* among decoders to improve channel capacity and achieve synchronization [2], [6].

Therefore, the desired objective in modern communication is to achieve synchronization as quickly as possible to secure the information of the user present in the communication environment [6], [10], [11], [12], [13], [14]. Furthermore, accurate synchronization plays a critical role in the cellular channel while, using any spectrum band [2], [15], [16], [17]. Conventionally, the initial step in the procedure of synchronization is to acquire code acquisition.[1]

Thus, using Pseudo Noise (PN) codes for synchronization is adopted as illustrated in [6], [10], [11], and [21]. Once synchronization concurs, then the data is demodulated [11], [21]. In most of the communication regulations, a diverse number of *m*-sequences are adopted for synchronization [11], [22], [23]. In the 5^{th} Generation (5G) standards for initial acquisition the 3^{rd} Generation Partnership Project (3GPP) also exploits the use of *m*-sequences for synchronization [24], [25], [26], [27], [28], [29], [30].

In the history of initial synchronization, Sequential Estimation was proposed by [31], leveraging the states of the Linear Feedback Shift Register (LFSR) and exploiting *m*-sequences [12], [21], [32], [33]. The primary objective of this approach is to accurately reconstruct the output of the *m*-sequence at the receiver by capturing F stages of the sequence. Acquiring an *m*-sequence with a period of $(2^F - 1)$ is particularly advantageous, as the acquisition device effectively recovers F consecutive chips. These chips are then fed into the *m*-sequence generator at the receiver, where the LFSR function produces chips that precisely resemble the originally transmitted sequence [12], [21]. However, during data reception, a few chips may be affected by noise, leading to an Erroneous Loading Probability (P_e) at the receiver [12], [21]. Thus, the main concern lies in acquiring and reconstructing the *m*-sequence, relying on sequential evaluation [31]. Ward [31] demonstrated that, for reasonable Signal-to-Noise Ratio (SNR) values, this acquisition technique yields a lower average acquisition time compared to the traditional sliding correlator-based approach described in [34].

Therefore, in spread spectrum transmissions, the energy of the generated signal is spread across hundreds of chips, resulting in a typically low chip SNR. Consequently, evaluating the successive chips through a chips-by-chip-based process and relying solely on hard decisions can be unreliable [11], [12], [21], [35]. To address this, Kilgus [36] proposed a decoder for *m*-sequences that utilizes a majority logic design to achieve synchronization. Building upon this work, Yiu and Ward [37] introduced a sequential estimation concept for acquisition and synchronization. However, the models mentioned above primarily rely on coherent detection and hard decision techniques. This approach is unrealistic since achieving accurate carrier phase tracking typically requires a higher SNR prior to despreading [6], [12].

For the aforementioned discussions, we propose an iterative Soft Input Soft Output (SISO) decoder that incorporates the concept of Automatic Gain Controller (AGC). This decoder operates in a constant region during each iteration, gradually increasing the gain as the number of chips in the

[1]Which is defined as the procedure used to receive spread PN code from the transmitted despread code [6], [10], [18], [19], [20]. Moreover, initial synchronization is initiated by a method of successive decision, where the major task is accomplished by the two sequences, namely by the coarse time alignment procedure, where a single code-chip duration is used to detect the phase and the information.

m-sequence generator increases. The AGC aids the SISO decoder in activating the ''loading command'' when the output values from the AGC reach a sufficiently high level to achieve a low P_e. This concept draws inspiration from the turbo coding philosophy for the SISO technique [3], [12], [21], [50], which operates on the consecutive Log Likelihood Ratio (LLR) values associated with the successive chips of the m-sequence generator. By capitalizing on the essential characteristics of m-sequences, we advocate for the Iterative Soft Sequence Estimation (ISSE) acquisition technique, which relies on F successive chips using a SISO detector. We demonstrate that the ISSE technique is linearly dependent on the LFSR in generating the m-sequence. Hence, our proposed ISSE acquisition technique presents an optimistic approach for acquiring m-sequences.

Traditional code synchronization typically involves two steps: code acquisition in the initial stage and code phase tracking for fine alignment to achieve synchronization [6], [51], [52], [53]. In this paper, our primary focus is on code acquisition for synchronization. Several methodologies have been proposed for code acquisition in wireless communication, including serial search approaches [40], [54], [55], parallel search approaches [52], [56], and sequential estimation approaches [3], [6], [12], [21], [35]. With the increasing demand for higher capacity, efficient spectrum utilization has become crucial in the cellular industry. In evaluating spectrum efficiency, we propose the ISSE acquisition scheme with AGC, which achieves fast synchronization with fewer iterations in the decoder. This helps the decoder achieve better gain and lower P_e for fast initial synchronization.

In Fig. 1, we illustrate the evolution of initial acquisition in the field of communication. The novel features of our paper are as follows:

- We propose the use of AGC for initial synchronization in the ISSE system, improving synchronization capability.
- Convergence analysis is performed using novel EXIT charts. Our proposed EXIT charts operate without interleavers, enhancing the synchronization capability by reducing unnecessary delays.
- Our proposed system enhances synchronization capability by providing additional gain. Simulations show that Primitive Polynomials (PPs) achieve higher Average Mutual Information (AMI) compared to PPs that do not employ AGC for synchronization.
- We demonstrate that higher-order sequence-generator PPs have a higher P_e compared to their low-order counterparts. When comparing polynomials with identical order, PPs with non-consecutive taps perform better than those with successive taps.
- Our approach incorporating AGC achieves a lower Acquisition Time (AT) than the traditional sequential estimation procedure.

The structure of this paper is as follows: Section II presents a detailed discussion of our AGC-aided ISSE acquisition method, focusing on its key aspects and system model. In Section III, we provide a comprehensive analysis of the convergence of our acquisition method using EXIT charts. This analysis helps us gain insights into the performance and behavior of the proposed approach. To validate and demonstrate the effectiveness of our methodology, Section IV presents simulation results. These results showcase the performance of the AGC-aided ISSE acquisition and provide a basis for evaluating its efficiency and accuracy. Finally, in Section V, we summarize our findings and draw conclusions regarding the methodology proposed in this manuscript.

II. PROPOSED SYSTEM MODEL

In the ever-evolving landscape of wireless communication, achieving synchronization has emerged as a paramount concern [2], [6], [22], [25], [26], [57], [58], [59]. To address this challenge, we propose a novel concept: the iterative soft sequential acquisition technique, which leverages the Automatic Gain Controller (AGC) in conjunction with Primitive Polynomials (PPs) derived from the LFSR. These PPs play a crucial role in generating the fundamental building blocks of communication systems, known as m-sequences, which are extensively employed for initial synchronization across all generations of mobile communication [2], [6], [22], [26], [58]. The AGC operates in a constant region during each iteration, strategically activating the loading command within the SISO decoder to facilitate synchronization. Its primary function is to evaluate the values fed from the Soft Chip Registers (SCR) by amplifying them linearly based on the soft output of the SISO decoder. This amplification process aims to enhance the performance compared to the previous iteration. We thoroughly examine the maximum values achieved by the SISO decoder at its peak iteration, which triggers the activation of the loading command. As the soft outputs of the SISO decoder gradually converge to sufficiently high values, the loading command is activated, ensuring a satisfactory low P_e. The effectiveness of this process is influenced by the gain of the AGC, denoted as β, and the iterative gain applied by the SISO decoder. Additionally, a delay unit is incorporated to store the latest soft outputs of f_i chips from the AGC, which are subsequently amplified by the β gain of the AGC.

Fig. 2 depicts the proposed ISSE acquisition scheme, which operates by five fundamental blocks, namely: a) m-sequence generators, b) Soft Chip Register (SCR), c) SISO decoder, d) AGC and e) phase tracking loop. We explore the basic concept of the ISSE acquisition technique, prior to detailing these components. The generator of the receiver seen at the bottom of Fig. 2 which has the same structure as that of our transmitter side as portrayed at the top of Fig. 2 and the SCR also has the same structure as that of the generator (m-sequence), except that in the Delay Units (DU) the soft information is stored which are then amplified by the AGC, instead of the chips 0 or 1. Thus, the DU stores the consecutive soft-chip value in the form of the Log-Likelihood

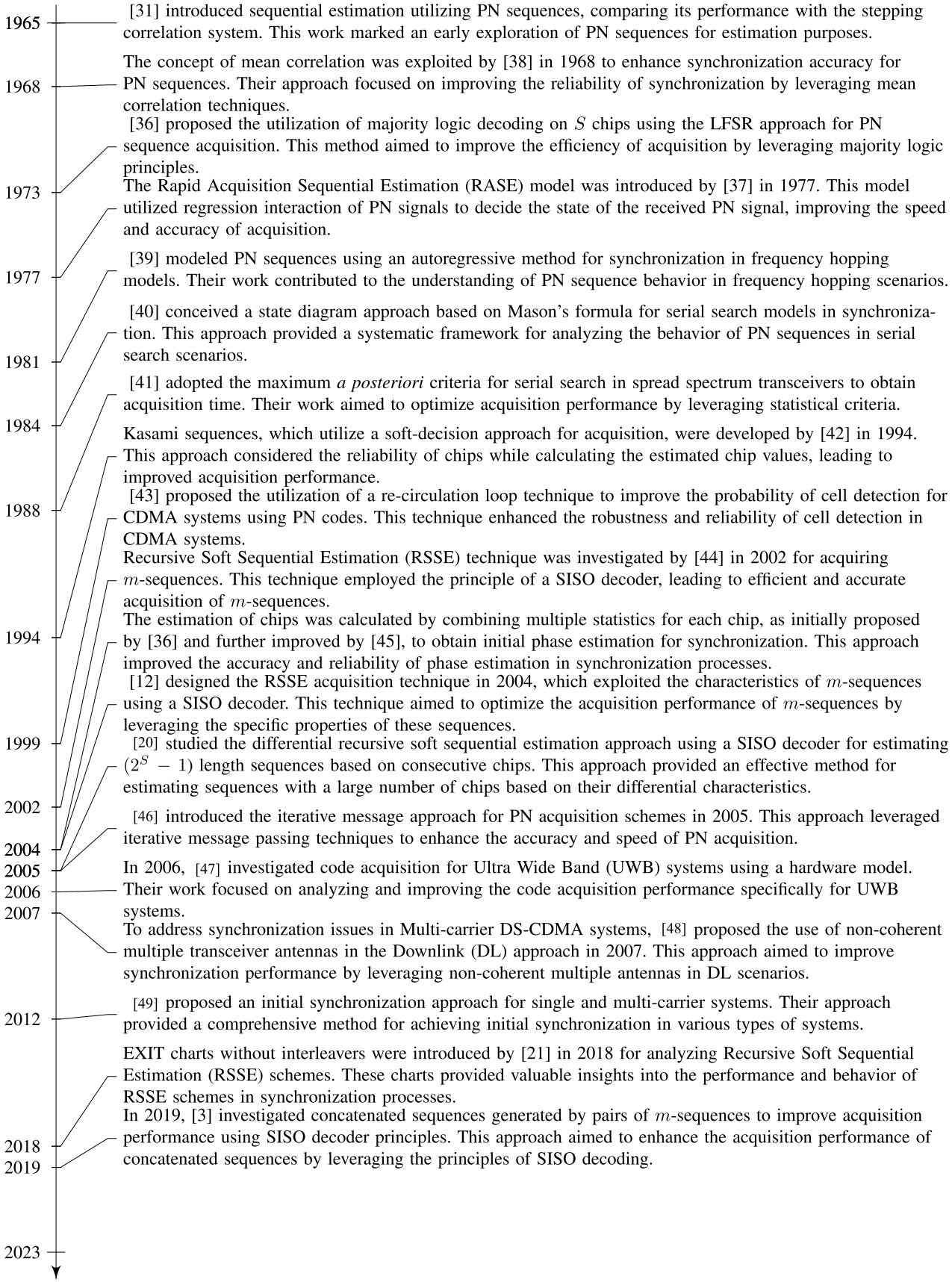

FIGURE 1. Timeline of initial acquisition research.

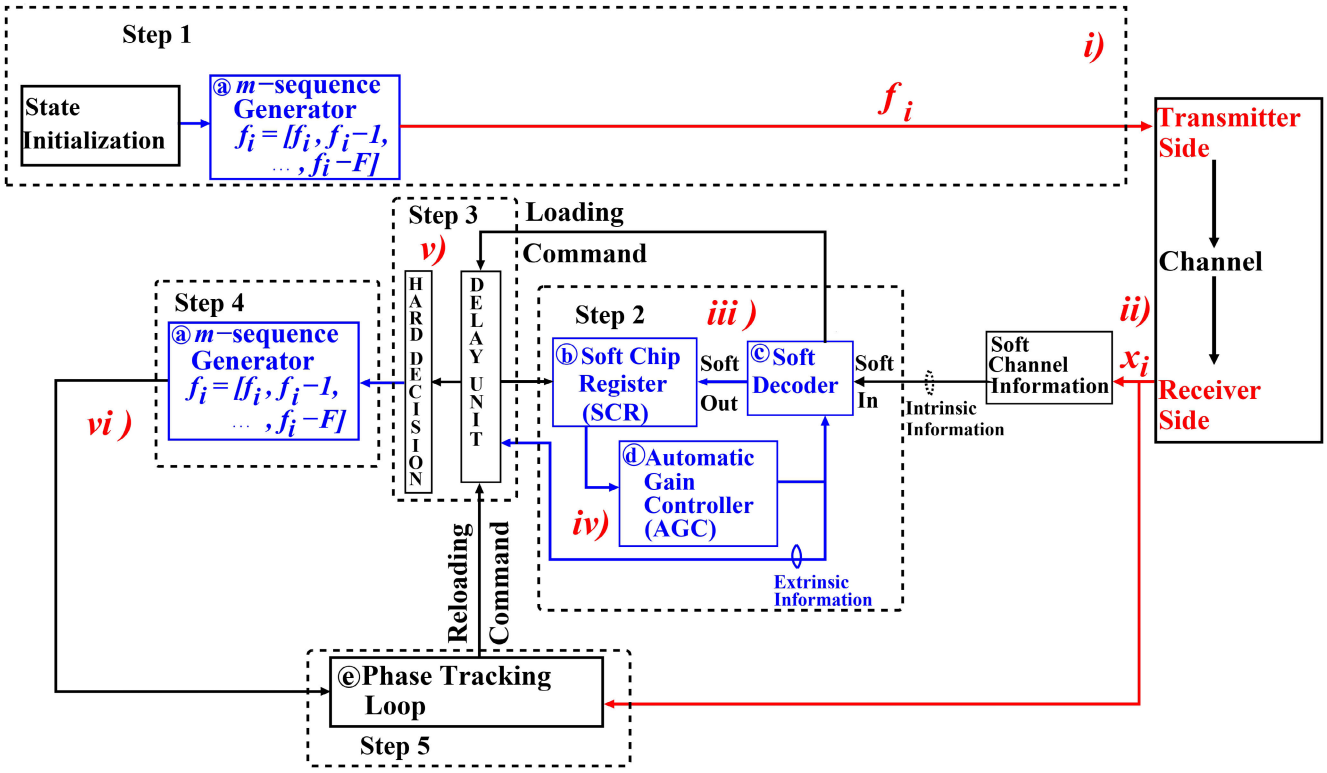

FIGURE 2. A block diagram of the ISSE model for iterative synchronization, where Steps 1 to 5 indicates the basic operation evolved in the ISSE model, while ⓐ to ⓔ blocks involved in the ISSE model. Finally, i) to vi) shows the initial outputs of each block.

Ratios (LLRs), which are amplified by the AGC[2] of Fig. 2. Upon receiving the LLR, they are transferred to the DUs of the generator as indicated in Fig. 2. The SISO detector processes both the extrinsic information acquired for each chip by the previously processed LLR values received and amplified by the AGC and the intrinsic information received from the channel. The output values which are received by SCR from the soft decoder are transferred to the block known as AGC, where all the values are amplified and stored in the respected DUs. The basic procedures involved in our ISSE techniques are expressed as under:

Step 1 To generate the *m*-sequence, an initialization process is carried out at the transmitter side, as illustrated in Fig.2. The generated chips are broadcast in terms of the phase-coded carrier signal without data modulation. Both the transmitter and the receiver possess knowledge of the chip values and the PPs, as indicated in Fig.2. At the receiver, a matching set of taps is utilized, which aligns with the taps used in the transmitter for generating the PPs as depicted in the block diagrams shown in Fig. 2.

Step 2 The SISO decoder contains a sample x_i from the respected channel as indicated in Fig. 2, which is associated with the generated chip f_i at the transmitter, computes the LLR of f_i based on x_i. Prior to transmission, the SCRs of Fig. 2 are initialized to be zero. The SCR has identical units as that of the transmitter side. The soft output $L(x_i)$ of the SISO decoder is measured. The function of SCR is to transfer the latest soft output of F chips of the SISO decoder to the AGC. These F chips are linked to the successive chips f_i' generated from the *m*-sequence generator. The AGC amplifies these f_i successive chips, aiding the SISO decoder in activating[3] the ''loading command'' as indicated in Fig. 2.

Step 3 Then f_i successive chips are calculated by performing hard decisions onto the final values stored in the delay unit from the AGC as indicated in Fig. 2.

Step 4 After that the resultant values are loaded into the generator of Fig. 2, where the initial binary values are evaluated by *m*-sequences generator. This evaluation takes place only if the generator successfully acquires the correct chip from the receiver.

[2]The values are transferred to the AGC by the SCR in the form of LLR, which are then amplified according to the value of β which is set between 2.0 to 3.0 by doing an exhaustive search as illustrated in these books and the papers [60], [61], [62], [63], [64]. Throughout the process, the AGC is operating in its linear region.

[3]Moreover, the function of AGC is to amplify and store the latest soft output of 'f_i' chips into the delay unit. Thus helping the SISO decoder to activate the loading command, when the LLR values from AGC become adequately high to sure the low P_e to achieve correct initial synchronization.

Step 5 The information signal received after despreading by the Phase Tracking Loop (PTL), where the phase of the signal is accomplished correctly by the PTL. If the phase is not accomplished correctly, which means the PTL is unable to track the signal hence phase is not accomplished. Hence, newly number of chips 'F' is stuffed into the DUs of the generators of Fig. 2, this process is known as the ''reloading command''. This operation will continue until the code is accomplished by PTL. Accordingly, the purpose of PTL is to recover and secure the output correctly over a diverse noisy channel, ensuring that the signals match at both the transmitter and receiver sides, thereby enhancing the SNR.

Fig. 3 illustrates an example of each output signal for the block diagram depicted in Fig. 2. The following provides a concise summary of each output from the block:

i) At the transmitter side, the four chip values of the generator are plotted, which are mapped to +1 and -1, respectively. These values are fed to the receiver via the channel as depicted in Fig. 3.
ii) In Fig. 3, these chips' values are corrupted by the noise as well as by the fading at the receiver side. The iterative decoding principle is employed, where soft information is obtained from the channel's output as depicted in Fig. 3.
iii) The soft input information representing f_i is then entered into the SISO decoder. The SISO decoder calculates the information of the chips in terms of LLRs. The amplitude of the LLR values will be increased during each iteration mainly by the AGC β gain[4] and by the iterative obtained by the SISO decoder [3], [6], [12], [21], [65]. The information data gathered from the channel represents the intrinsic information which is added with the extrinsic information by the AGC as shown in Fig. 3.
iv) The value obtained by the soft output of the SISO decoder from the SCR, is dispatched to the AGC as depicted in Fig. 2, where the values are amplified constantly thus aiding to achieve a better gain than the previous iteration. The output from the AGC to the SISO decoder will yield a higher gain in less time than the previous proposed system [21], which helps to activate the ''loading command'' as observed in Fig. 3. Furthermore, we examine the maximum values for the SISO decoder at our utmost iteration, which enforces the ''loading command'' by the SISO system. Thus, the ultimate value of the soft outputs of the SISO decoder evolves to an adequately high value for assuring a satisfactorily low P_e. The delay unit store the latest soft output values of f_i chips from the AGC[5] which are amplified by the β gain and by the iterative gain as shown in Fig. 3.
v) After obtaining the ''loading command'' by the SISO decoder as illustrated above in iv) a binary hard decision is done on the store values at the DU. This can be seen in step v of Fig. 3.
vi) The values obtained by the DUs are then fed to the LFSR of the local m-sequence generator as shown in Fig. 3, where the desired output is obtained for the m-sequence. It can be observed from Fig. 2 that the output precisely matches the transmitted signal. This indicates that the information is accurately received, the phase demodulation is performed correctly, and the desired information is retrieved successfully at the receiver side using our designed ISSE model.

In Fig. 4, the *a-posteriori* LLR outputs of a single decoder are shown for various iterations. Specifically, the outputs of the SISO decoder with and without AGC are presented after 50, 100, and 1000 iterations, which represent the final iteration for our SISO decoder in this result. Initially, the input sequence of the SISO detector consists of logical zeros. Consequently, it can be observed that the LLR values of the received chips consistently increase as the decoder gains more confidence in the chip values. The hard-decision outputs of these *a-posteriori* LLRs determine the final chip values of $+1$ or -1. The results in Fig. 4 demonstrate that incorporating the AGC to support the SISO decoder enhances the confidence of the detector in estimating the receiver's loading probability. It can be inferred that the AGC-aided system consistently outperforms our previous system proposed in [21] in every iteration. Specifically, when the first 50 iterations were conducted in both systems, the maximum LLR values calculated without AGC failed to approach the threshold value of zero. In contrast, the values ranged from -4.8 to -5 for the previous system [21] without AGC, whereas for the AGC system, the values ranged from -0.5 to -0.85, which are closer to the threshold value of zero, although none of the values exceeded the threshold. Furthermore, after a hundred iterations in the SISO decoder, the AGC performance surpasses the previous system of [21]. As depicted in Fig. 4, the majority of LLR values received from the AGC cross the threshold value, indicating that this system model will achieve better synchronization results compared to the approach utilized in [21]. In the final iteration, both systems obtain maximum LLR values, but the confidence of the SISO decoder using the AGC approach is significantly higher than the previous system [21]. This outcome demonstrates that employing the AGC model enables faster synchronization in less time.

Now, let us delve into the individual blocks utilized in the generation of the proposed ISSE model. This model encompasses several key components that work together to achieve effective initial synchronization. By examining the functionality and interactions of these blocks, we can gain a comprehensive understanding of the underlying principles

[4]This is selected as the maximum gain of the AGC without distorting the signal to operate at the linear region.

[5]This gain is adjusted in such away that AGC is utilized without distorting the input signal so that the AGC cannot move to saturated region.

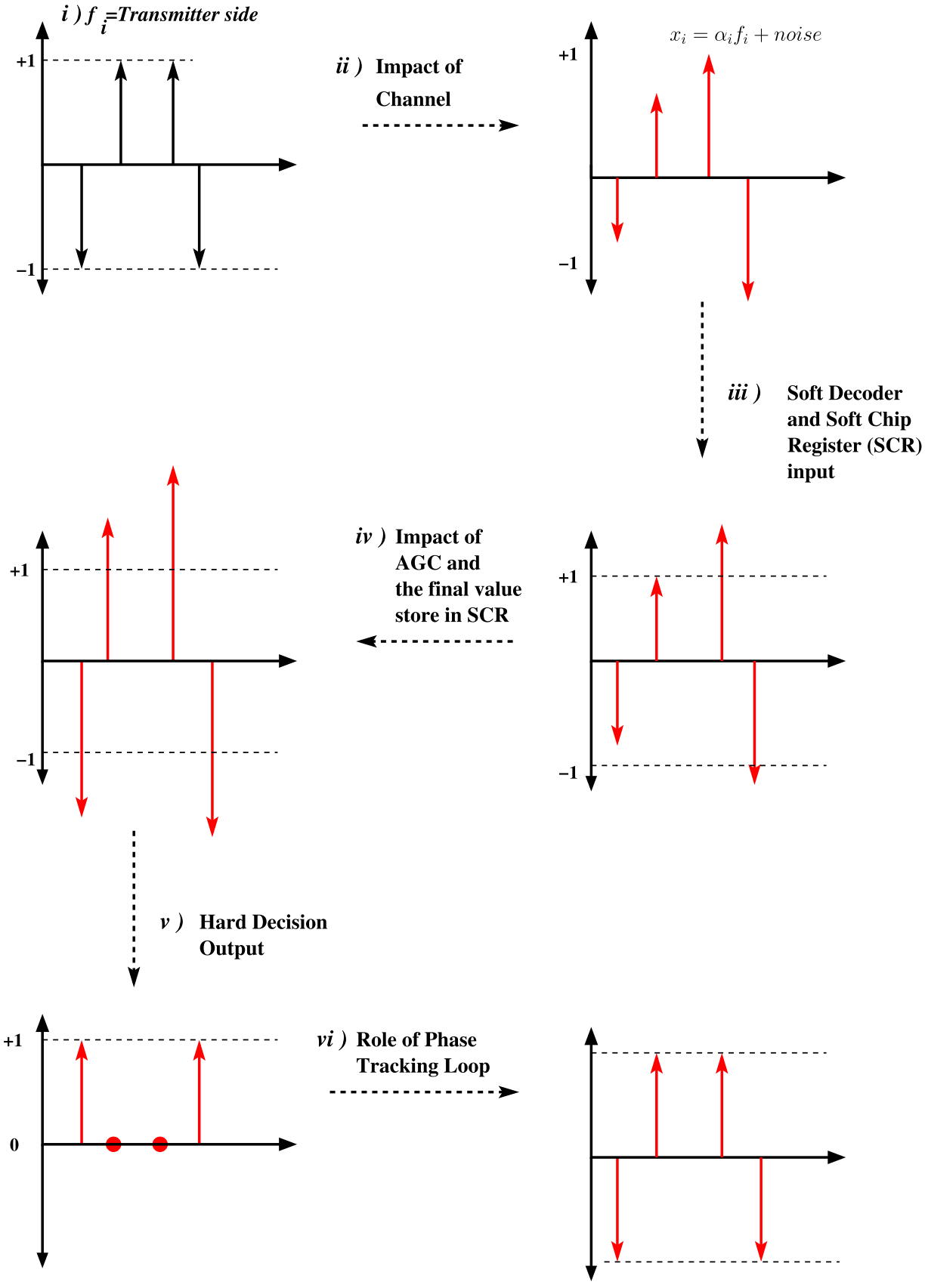

FIGURE 3. The signal obtained at each block of our ISSE system.

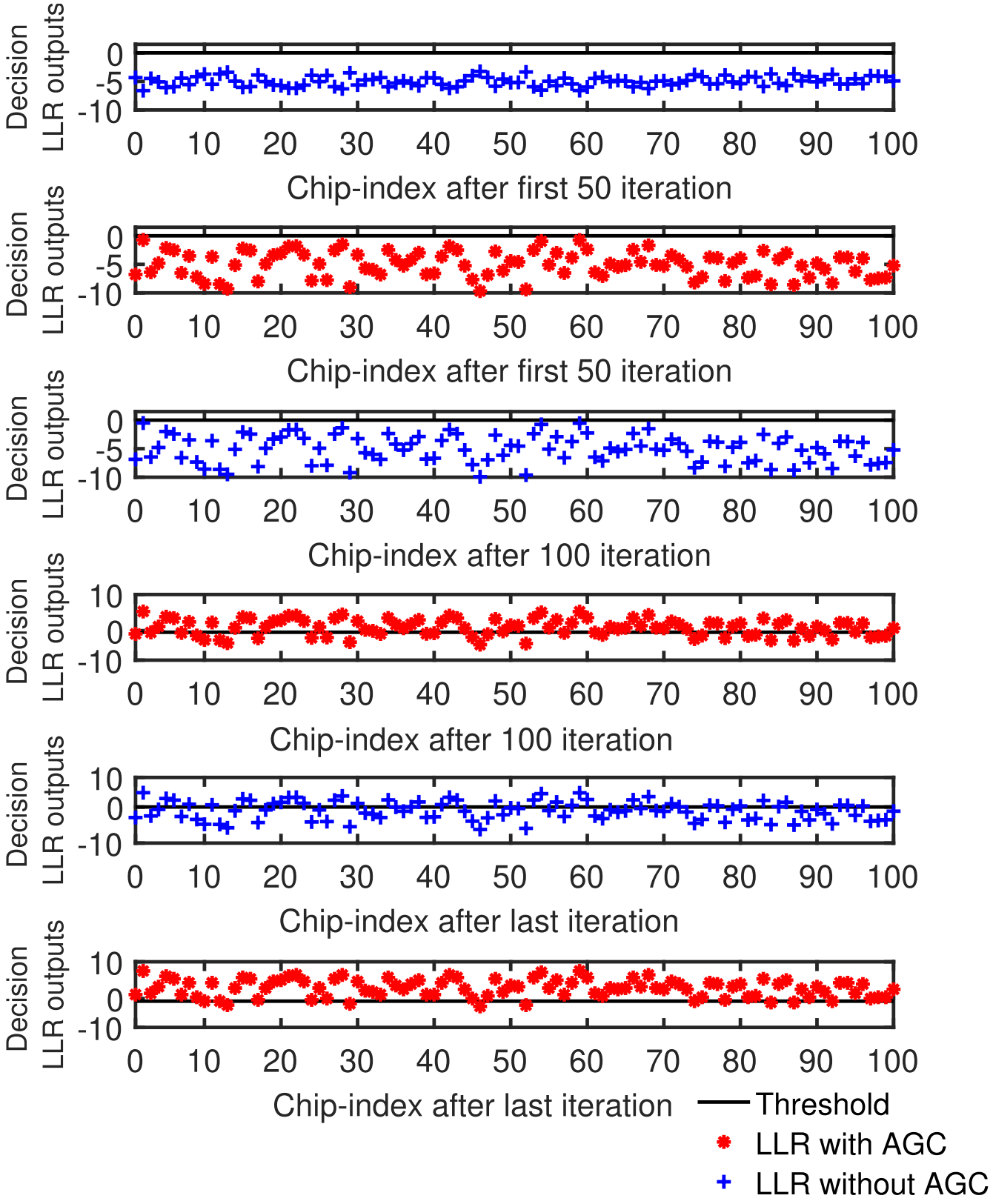

FIGURE 4. To comprehend the role of the AGC in the ISSE iterative acquisition model, a comparison is made between the soft outputs of the current proposed scheme and the previous one [21].

of the ISSE model and how it operates to enhance system performance.

A. m-SEQUENCE GENERATOR

These m-sequences are so-called maximum length sequences [6], [66], [67] which are produced by an LFSR. The LFSR tap connections are determined by the so-called PPs. The terminology is due to the fact that the PPs cannot be further factorized [6], [68]. In Fig. 5, 'D' denotes the unit time delay and the coefficients $g_1, g_2, \ldots, g_F$. Furthermore, these coefficients play a crucial role in determining the presence or absence of tap connections at each delay unit during the generation of the PPs. Each coefficient represents whether a particular tap connection is present or not. If the coefficient is assigned a value of 1, it signifies that the corresponding tap connection is present, while a value of 0 indicates that the tap connection is absent. By manipulating these coefficients, we can control the connectivity of the taps within the system, thus influencing the generation of the PPs [6], [66]. Hence the PPs are formulated as:

$$g(D) = 1 + D^{f_1} + D^{f_2} + \cdots + D^{f_m=F}, \tag{1}$$

where the index set $f_1, f_2, \ldots,$ represents the connection-tap index of the PP used for producing the m-sequences which is expressed as $g(D)$, which cannot be reducible [6], [11], [12], [21], [68]. The m-sequences which are produced by the scheme of Fig. 5, behave recursively and the recursion equation is expressed as:

$$f_i = f_{i-f_1} f_{i-f_2} \cdots f_{i-(f_N=F)} = \prod_{n=1}^{N} f_{i-f_n}, \quad \text{for } i = 0, 1, \ldots, I, \tag{2}$$

where, the chip-values are expressed as f_i [6] and the product operation is expressed as $\prod(\cdot)$. In the framework of the sequential evaluation-based acquisition procedure, the generator's states are evaluated by adopting the iterative method for m-sequences, where F-shift register is used to generate m-sequence generated having a duration of $(2^F - 1)$ chips-having cyclic Bose Chaudhuri Hocquengem (BCH) code-length of duration $(2^F - 1)$ [12], [36], [69], [70]. Thereupon, the receiver established $(2 \times (2^F - 1))$ consecutive patterns of the generated m-sequence to evaluate initial F chips by adopting iterative detection with the aid of its number of samples. Note that the SCR and the m-sequence generator exploit the identical connection taps.

B. SOFT CHIP REGISTER AND SISO DECODER

At the receiver side, the SCR contains F number of soft-chip-register. These registers stores the LLR values from the SISO decoder. The SCRs and the m-sequence generator lean on the same connection-taps as that of the transmitter side.[7]

The spontaneous LLR values of the F consecutive chips are transferred from the SCR[8] to the AGC. The main purpose of AGC is to provide the constant gain to the LLR values, which are processed by the SCR to the AGC.[9] Thus, the AGC is providing a better gain from the previous iteration so that ''loading command'' can be processed faster than the previous system.

Moreover, at the initial proceeding, the generated chips of the m-sequences have a similar likelihood of zeros and ones, thus the SCRs values are initialized to be zero [12], [21]. The LLR values generated by these F chips will accomplish the hard decision which is processed by the AGC into the delay unit so that correct bits can be decoded into the generator as portrayed in Fig. 5. The SISO decoder utilizes the prior measured LLR values by the AGC as the *a priori* information, which is transmitted from the AGC, where each LLR value is linearly amplified. The information gathered from the channel is indicated as *intrinsic information* which is evaluated by the SISO decoder. The value obtained by the soft output of the SISO decoder from the AGC is dispatched to the SCR. Please note that during each iteration the values which are transferred from SCR to the AGC will amplify the signal constantly thus helping in achieving a better gain than the previous iteration. Thus, the yielded output will have a higher gain[10] than the previously proposed system [12], [21]. Moreover, at the utmost iteration, we examine the maximum values of our SISO decoder, and thus a ''loading command'' is conceived, given that the ultimate value of the soft outputs of the SISO decoder has evolved to an adequately high value for assuring a satisfactorily low P_e. The associating chips are computed by performing hard decisions which are present at the delay unit which contains the recent LLR values[11] as shown in Fig. 5.

C. SOFT CHANNEL OUTPUTS FROM THE AMPLIFIER

The received signal x_i which is assigned to the f_i chip is expressed as:

$$x_i = \alpha_i f_i + n_i, \qquad i = 0, 1, \ldots, \tag{3}$$

where n_i has a zero mean and expressed as AWGN noise, α_i is the channel state and N_0 is the noise power spectral density. For x_i, the LLR of f_i is denoted as:

$$L(f_i|x_i) = \log\left[\frac{P(f_i = +1|x_i)}{P(f_i = -1|x_i)}\right] = L_{f_i} x_i + L(f_i), \quad i = 0, 1, \ldots, \tag{4}$$

where $L_c = 4\alpha \frac{E_c}{N_0}$, and $L(f_i) = 0$, as the chip's value f_i is equiprobable and have a binary value. Observed from

[6] f_i consisting of $+1$ or -1 value, where a logical zero is expressed as $+1$ and a logical one is expressed as -1 respectively.

[7] The PP is well-known namely, to the receiver and to the transmitter. The DUs in m-sequence generator are identical to that of the number of SCRs.

[8] The LLR which are processed by the SISO decoder are first transferred to the SCR and then to the AGC from the SCR, where each LLR is amplified and stored in the SCR by the AGC as shown in Figs. 2 and 5.

[9] If the AGC is not operating in the constant region all the values are distorted and thus we cannot achieve correct values as illustrated in [60], [61], [62], [63], [64], [71], [72], [73], and [65].

[10] Consisting of the AGC plus the iteration gain of the SISO decoder.

[11] Dispatched from the AGC to the delay unit.

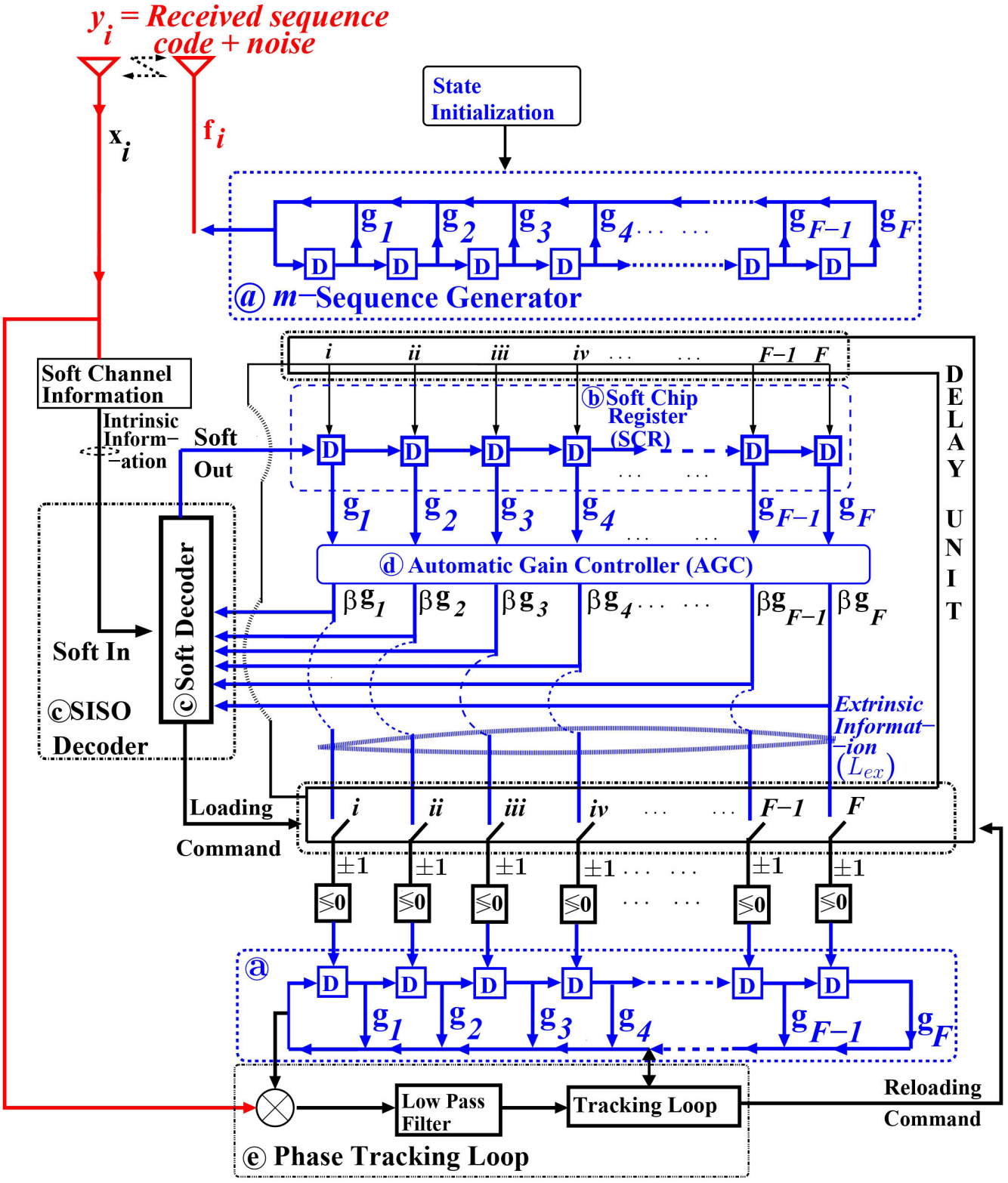

FIGURE 5. A portrayal of our ISSE model is depicted, where *i*, *ii*, *iii*, . . ., *F* in DUs represent the positions of the registers, which are analogous to those in the *m*-sequence generator.

Eq. (2) that prior to the soft outputs of the SISO decoder evaluates at the time indicators of $(i - f_1), (i - f_2), (i - f_3), \ldots, (i - f_N)$ are the tap connection, which is fed to the SISO detector. Hence, the extrinsic information calculated

is used for achieving the accurate detecting likelihood of f_i of the chip. During each iteration the values are transferred from SCR to the AGC block, where the LLR values are constantly multiplied by the β gain thus, obtaining better output from the previously transmitted signal. Assuming the prior number of soft outputs is F of the SISO decoder $\beta \times \left\{L_{ex}(f_{i_{-1}}), L_{ex}(f_{i_{-2}}), \ldots, L_{ex}(f_{i_{-F_N}})\right\}$, where β is the gain of the amplifier which is set to be 2.0 to 3.0. From Eq. (4), the extrinsic information exploited for achieving the accurate detecting likelihood of f_i is represented as [11], [12], and [21]

$$L_e(f_i) = L_{apr}f_i \approx \beta\Big[\prod_{n=1}^{N} \text{sign}(L_{ex}(f_{i-f_n}))\times \min\left\{|L(f_{i-f_1})|\right\}, \left\{|L(f_{i-f_2})|\right\}, \ldots, \ldots, \left\{|L(f_{i-f_N})|\right\}\Big] \quad i = 0, 1, \ldots. \tag{5}$$

where we suppose that $L_e(\beta f_{-\infty}) = \ldots = L_e(\beta f_{1-f}) = L_e(\beta f_{-2}) = L_e(\beta f_{-1}) = 0$. At last, the channel's output information $L(f_i|x_i)$ in Eq. (4) and the extrinsic information $L_e(f_i)$ in Eq. (5)[12] yields the SISO decoder output which is expressed as the soft output, which is linked with the concern chips to f_{out} as

$$L\left(f_{\text{out}}\right) = L\left(f_i \mid x_i\right) + L_e\left(f_i\right) = L_f x_i + L\left(f_i\right) + \beta\left[\prod_{n=1}^{N} \text{sign}\left(L\left(f_{i-f_n}\right)\right) \times \left(\min\left\{\left|L\left(f_{i-f_1}\right)\right|\right\}, \left\{\left|L\left(f_{i-f_2}\right)\right|\right\}, \ldots, \left\{\left|L\left(f_{i-f_N}\right)\right|\right\}\right)\right] \quad i = 0, 1, \tag{6}$$

When the channel's output SNR is adequately high, the LLR of the recent F successive chips is gradually improved by the number of iterations, because during each iteration the re-liabilities affiliated with the F chips will increase by the decoder as well as by the AGC gain β[13] through the sequential procedure. Thus, achieving maximum value for the fast synchronization

Thus, after each iteration, we get β gain which helps to improve the overall detection probability. Hence, P_e of the generated sequence is reduced. Thus, the acquisition device becomes effective in obtaining the accuracies linked with the F successive chips by measuring the magnitudes of the LLR gathered in the DUs. If AGC evolves effectually high after a set of operations for obtaining the LLR values, then the SISO decoder activates the loading command to enter either $+1$ or -1 chip values into the DUs of the sequence generator by performing the binary-hard-decision. During the last iteration I, extrinsic LLRs are measured, for that reason, all the measured values in the DU are uploaded at our receiver side. Let presume that I is the total iterations involved in our model then the total number of chips is to be measured is $F \cdot I$.

[12]Illustrates the Normalized Min-sum decoder as β is used thus achieving a better gain than the Minsum decoder.

[13]The purpose of the AGC is to maintain a constant gain as AGC is operating in a closed-loop operation. During iteration, the magnitude of the new LLR values will be increased by the AGC from the previous value. Thus, helping to activate the loading command from the SISO decoder.

On every occasion, when the SISO decoder obtains a channel output value x_i corresponding to a chip f_i chip, the SISO detector estimates the LLR response by utilizing Eqs. (5) and (6) for the calculation of the intrinsic information. Thus, the SISO decoder examines the channel output x_i, which is associated with the concern chip of f_i, the SISO decoder evaluates the LLR values by utilizing Eq. (5). It then determines the intrinsic information by utilizing Eq. (6). During each iteration the LLR values will be increased effectively by the iterative sequential procedure as well as by the AGC gain β thus, achieving maximum value for the system to acquire fast synchronization.

D. PHASE TRACKING LOOP

Again, for attaining satisfactory carrier phase tracking the SNR is inadequately high, prior to despreading. The low-pass filter received the despread signal as indicated in Fig. 5. After the signal is dispatched to the Tracking Loop (TL). The aim of TL is to achieve the phase accurately and then the code is acquired perfectly.[14] This procedure will keep on going until the correct code is achieved by this device.

III. EXIT CHART ANALYSIS FOR *m*-SEQUENCE DESIGN

Brink introduces the concept of EXtrinsic Information Transfer (EXIT) methodology for the iterative system [74], [75], as an efficacious tool for evaluating the convergence analysis for the iterative decoding procedures. The elementary principle of the EXIT chart is to evaluate a significantly low Bit Error Ratio (BER) at the specific SNR value without performing bit-by-bit detection-based simulations using a high number of detection iterations. For further elaboration, the exact EXIT chart approach exploits the condition of iterative SISO components by adopting Gaussian distribution. However, the accuracy of the classic EXIT chart depends mainly upon the performance-prediction corrodes, unless we calculate the function of an adequately long interleaver between the inner and outer detectors for rendering the LLR values at the inputs of both components uncorrelated Gaussian distributed.

In this manuscript, we introduced a novel design of the EXIT chats for progressing convergence attributes of our ISSE model. Thus, evaluating the advancement of the output/input Mutual Information (MI) alien by the receiver's SISO decoders for the consecutive iterations.

Three major ingredients of Fig. 6 are the parts of the EXIT chart which are indicated in Fig. 7, which consist of inner detectors, outer detectors, and iterative trajectories. The information can be gathered in parallel, without affecting information on each component. More explicitly, detecting trajectory is like staircase-shaped, which helps to estimate the MI values of the outer and inner EXIT curves, which are independent of each other. This can be done if the interleavers are facilitated among the outer and inner detecting systems. Therefore, the autonomous simulation of the outer and inner

[14]Which indicates that TL will activate the ''re-loading command''. Thus, TL is ineffectively in-tracking the phase information accurately.

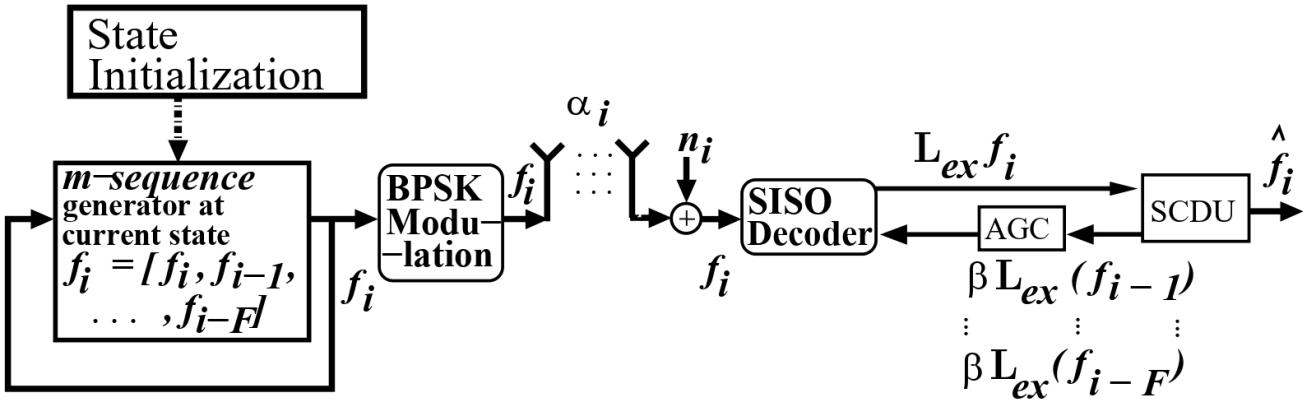

FIGURE 6. The proposed model for the ISSE EXIT chart of Fig. 5.

decoders' EXIT curves is achieved by the hypothesis of having considerably long interleavers, though the imitation of the staircase-shaped detecting trajectory employs an interleaver having a finite length. Hence, the stair-case-shaped detecting trajectory cannot accurately resemble the performance calculated by the outer and inner EXIT curvatures. Furthermore, the interleaver length should be adequately high to avoid mismatch among them [75], [76].

Furthermore, interleaver introduces an inherent delay in the system [75], [76]. As a result, we investigate a fundamental resemblance with the self-concatenated decoding strategy of [75] and [76], in which an interleaver was used to relocate the decoder's output before processing it to its input. However, in this manuscript, we used the EXIT charts without interleavers. This is performed by employing the iterations elicited while decoding the same bit sequence. Instead, we use iterations to exploit the intrinsic correlation of the m-chip, as created by the LFSRs in Fig. 6, which is magnified by the AGC. This is the influential factor that distinguishes it from the conventional EXIT charts.

Fig. 6 demonstrates the dual inputs of the SISO decoder which consist of the output from the channel as well as the output from the AGC as indicated in Fig. 5. Hence, the outer and inner decoder's EXIT curves are similar, but they are exposed regarding the diagonal line depicted in Fig. 7. Furthermore, we examine a theoretical resemblance amongst our existing initial acquiring problem and the self-concatenated detecting design of [76]. Despite of this our approach has a significant dissimilarity as in [76] an interleaver was utilized for altering the output of the detector before processing its feedback to its input. As opposed to this, we organize this by providing with the iterations involved for detecting the same bit succession and processing it with the linear gain of the AGC express as β. This was done by the online utilization of the inherited interrelationship of the chips of the m-sequence generator, as illustrated by the LFSR of Fig. 6. Therefore, these are the fundamental characteristics that differentiate our original EXIT-chart from the traditional EXIT approach.

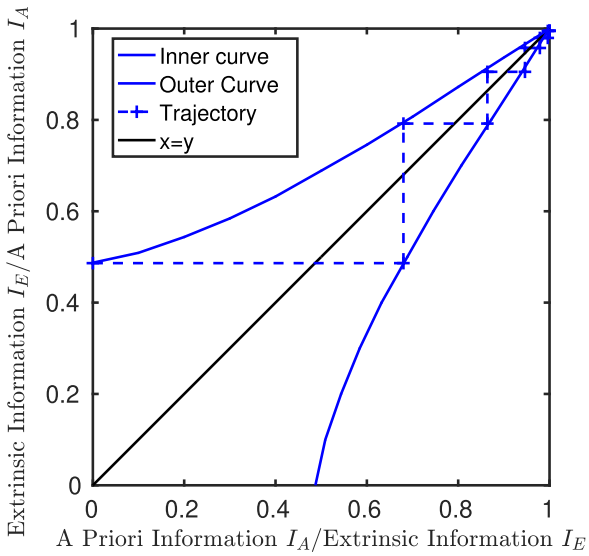

FIGURE 7. EXIT chart for the ISSE scheme by utilizing $g_1(D) = 1 + D^2 + D^5$ over Nakagami Fading channels when $m_f = 3.0$ at SNR $= -4$ *dB*.

The SISO decoder's output modifies which, corresponds to the *a priori* LLR values L_{ex} consisting of the extrinsic LLR values of the previous iteration with the AGC gain i.e β. The m-sequence transmitter's stage is programmed to a predestined condition, which is acknowledged by both the transmitter and the receiver of Fig. 6.

Moreover, the BPSK scheme is utilized where the value of the I^{th} transmitted chip f_i becomes the initial value of the LFSR of the m-sequence generators at the transmitter side. During receiving, the obtained signal is feedback to the SISO decoder with the gathered extrinsic LLR values multiplied by the β gain of the AGC so that $L_{ex}(\beta f_{i-1}), \cdots, L_{ex}(\beta f_{i-T})$ of Fig. 6, in the final detecting iterations I, which are evaluated for the I prior transmitted chips. Derived from these prior extrinsic LLRs, the *a priori* LLR of f_i is evaluated from Eq. (4). Later Eq. (6), is used to measure the extrinsic LLR of f_i, and the identical technique is utilized for the subsequent

chip f_{i+1}. The purpose of AGC is to shift the latest measured T extrinsic LLRs and stored them in the delay unit. Once a set of detecting iterations is done, a hard decision is accomplished and the approximate stage of the $\hat{\boldsymbol{f}}_{\boldsymbol{i}}$ is achieved for the m-sequence.

A. SELF-CONCATENATED APPROACH

A self-concatenated model is developed from the EXIT chart which does not crossover with the diagonal line starting from the point (0, 0) and ending at point (1, 1) of the EXIT chart. In the self-concatenated technique of [75] and [76], the identical detector/decoder unit is exploited twice, namely one as the inner and the other as the outer SISO component, as illustrated in Fig. 6. The SISO decoder consists of dual inputs which are, the output from the m-sequence generators' that is f_i, and the other is the output from the AGC.

The (2^F-1) chips of the m-sequences are already acknowledged to both the receiver and the transmitter, which are generated from m- chips by the LFSR. During each SISO iteration, the content in the LFSRs will change, thus we need to record and store the previous values of $\hat{\boldsymbol{f}}_{\boldsymbol{i}}$, which is equal to the $\beta\times\ (2^F\ -\ 1)$ values of the m-sequence generator having the identical period of the m-sequence generator.

Moreover, we do invok iterations for detecting the same bit succession, but rather we utilize the online utilization of the inherited interrelationship of the chips of the m-sequence generator associated with the chips of the m-sequence having a duration of (2^F-1), as affected by the LFSR of Fig. 6, where the chips are processed by the AGC to attain the maximum value at less time. When receiving, the SISO decoder's output will modify regarding the *a priori* LLR values βL_{ex}, which is composed of the gain of the AGC with the extrinsic LLR values of preceding iterations.

Fig. 6 illustrates our proposed model for the EXIT chart analysis of the ISSE scheme. In this model, a single detector is consistently used with diverse inputs. The initial input of the SISO decoder is the output of the channel, representing the received signal. The second input of the SISO decoder is obtained from the AGC (Automatic Gain Control).[15] Both the receiver and the transmitter have prior knowledge of $\beta\times(2^F-1)$ generations of the m-sequence generators. These generators are essentially known patterns of binary sequences. The SISO detector is designed to compute the *a priori* LLR values, denoted as $L_{apr}(f_i)$, based on Eq. (6). Importantly, the receiver utilizes the information from specific m-sequence generators chosen during the computation of the *a priori* LLR values. It should be noted that the selection of these generators may vary at each SISO iteration. As a result, the latest computed extrinsic LLRs will be stored at each iteration to account for this variation.

[15]Please note that for our simulation, we set β to 2.5, operating in the linear region. The AGC effectively adjusts the extrinsic LLR (Log-Likelihood Ratio), which is calculated beforehand.

B. MUTUAL INFORMATION

To compute the MI between the generated chips and the connected extrinsic LLRs, we employ a time-averaging technique. This technique involves calculating the average MI over a specific duration, enabling us to obtain a more accurate and reliable estimation. In our approach, we specifically utilize the LLR-based MI method, which takes into consideration the LLR values associated with the received chips. This approach has been extensively discussed and detailed in references [21], [75], [76]. By incorporating the LLRs in the MI computation, we are able to capture the influence of channel conditions and the reliability of the received information on the overall mutual information. This allows us to gain insights into the information content and quality of the transmitted and received signals, enhancing our understanding of the system's performance.

IV. SIMULATION RESULTS

Our ISSE model's performance is evaluated through a range of simulation results in Nakagami-m fading channels. In these simulations, we consider the total number of chips entered into the Soft-In Soft-Out (SISO) detector, denoted as $F\times I$. Here, F represents the order of the polynomial expressed by the Primitive Polynomial (PP), I represents the number of iterations, and we maintain a constant Nakagami-m fading channel parameter of $m_1 = 3.0$

During these simulations, we maintain a constant channel magnitude over a sequence of F successive chips. We consider three different PPs that are commonly used in cellular communication systems: $g_1(D) = 1 + D^2 + D^5$, $g_2(D) = 1+D+D^2+D^4+D^5$, and $g_3(D) = 1+D+D^3+D^4+D^{13}$. The selection of these PPs is based on their number of taps and polynomial order. Specifically, $g_1(D)$ and $g_2(D)$ have a 5^{th} order, while $g_3(D)$ has a 13^{th} order. Additionally, both $g_2(D)$ and $g_3(D)$ have a total of five connecting taps, with two of them being successive taps. On the other hand, $g_1(D)$ has three connecting taps, none of which are successive. Before analyzing the MI and the EXIT chart, we evaluate the performance of the P_e versus SNR expressed in dB.

Fig. 8 presents the reliability associated with the polarity of an m-sequence chip transmitted over a Nakagami fading channel. The decision reliability of the SISO detection is evaluated individually for each chip using Eq. (6). In Fig. 8, the solid line represents the conventional hard decision-based acquisition model, where the absolute value of the channel output is associated with the detected chips using the conventional decoder. As illustrated in Fig.8, the decision reliability of the conventional hard decision approach remains within the range of 0 to 10, regardless of the number of chips processed by the decoder, as the polarity of each chip is determined independently during the detection process. Furthermore, our AGC-aided acquisition scheme surpasses other sequential schemes proposed in previous works [12], [21]. By comparing the results of AGC with and without AGC, we observe enhanced reliability in making correct decisions

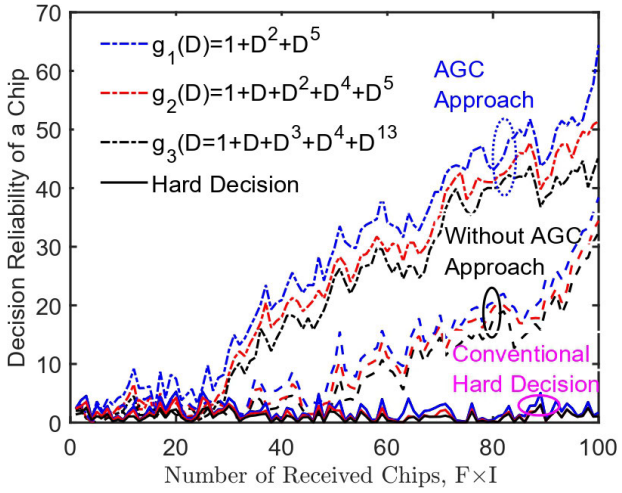

FIGURE 8. Decision reliability amongst the received number of chips transmitted over a Nakagami Fading channel when involved in the ISSE process.

when the AGC is utilized in the ISSE system. In each iteration, we achieve a linear gain from the previous iteration, leading to improved performance in less time. Consequently, the AGC accelerates the system's reliability more rapidly and effectively compared to the previously proposed models [12], [21]. This improvement can be attributed to the multiplication of the *a priori* information obtained from prior chips transmitted by the SISO decoder by the β gain of the AGC, as shown in Eqs. (5) and(6). The forthcoming simulation results will provide further evidence to support this argument.

In Fig.9, we evaluate the acquisition performance for a period of $N = 2^{13} - 1 = 8191$ chips, generated by a thirteen-order PP represented as $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$, which has two consecutive taps out of a total of five taps. In the traditional serial search acquisition model [34], the integration dwell time, denoted by τ_D, typically spans tens to hundreds of chip intervals. According to [34], the mean acquisition time of a conventional serial search is calculated as $N_{\tau_D}/2 = 4095\tau_D$, which corresponds to a significantly larger number of chips that is more than 520 chips for a sequence of length 8191, even when the SNR value is high and the detection probability reaches one. Therefore, the ISSE acquisition scheme demonstrates a substantial improvement over the conventional serial search-based acquisition and RSSE model [12], [21] in terms of achievable acquisition time performance.

Fig. 9 represents the acquisition performance of the PP $g_3(D)$ using different approaches. The solid lines in the Fig. 9 depict the acquisition process without adopting the Automatic Gain Control (AGC) approach, while the dashed lines represent the acquisition process with AGC. Furthermore, when the AGC approach is not used, the $g_3(D)$ is acquired at an SNR value of 1.7 *dB* by processing $520 = 40 \times 13$ chips in the iterative SISO decoder, as and can be observed by the solid line in the Fig. 9. This means that the system needs a relatively higher SNR to achieve the desired acquisition performance. However, by incorporating the AGC approach, the acquisition performance is significantly improved. With AGC, the same $g_3(D)$ can be acquired at a lower SNR value of 1 *dB* by processing a larger number of chips, specifically $2600 = 200 \times 13$, as indicated by the solid line in Fig.9. The AGC approach effectively enhances the system performance by adjusting the gain β dynamically, resulting in better SNR values and improved acquisition capabilities. For instance, by processing $520 = 40 \times 13$ chips in the iterative SISO decoder with AGC, the SNR achieved is -3 *dB*. By further increasing the number of processed chips to 2600, the SNR is improved to -4 *dB*. This demonstrates that employing the AGC approach allows for a more efficient acquisition process and enhances the system's performance in terms of the SNR versus P_e performance. In view to this result we conclude that utilizing the AGC approach in the acquisition process improves the system's performance by reducing the required SNR for acquiring the same PP. Thus improving in better SNR values and enhances the system's acquisition capabilities, resulting in improved performance. Note that even invoking 2600 chips for achieving acquisition at the particular value of SNR -4 *dB*, the AT of 2600 chips spans is significantly less than that of the traditional models [31], [34], [55], which demand an AT for the *m*-sequence having a duration of $N = 2^{13} - 1 = 8191$ chips. It is inferred from Fig. 9, the system performance improves, when more number of received chips are processed, in the ISSE decoder. Thus, we can deduce that the acquisition performance can be enhanced if AGC technique is adopted in the system which will also improve the SNR value to 2 to 3 *dB* when compared without AGC model, as shown by the dotted lines in Fig. 9.

The results portrayed in Fig. 10, were evaluated when broadcast over the Nakagamic channel when $m_l = 3.0$. In Fig. 10, we examined the P_e versus the SNR for an *m*-sequence utilizing three diverse PPs. Note that when $I = 1$ the P_e utilizes, the hard decision approach using ISSE SISO decoding. Fig. 10 exhibits that the performance of all the PPs tends to improve as the value of I increases.However, more power is required at the transmitter, and higher computational complexity is required for decoding the received chips. We examine, $g_1(D)$ dominates the other two PPs as it constitutes three taps, which are non-consecutive. Despite $g_2(D)$ and $g_3(D)$ having two consecutive taps, out of five total taps, $g_3(D)$ is inferior to $g_2(D)$ as it belongs to higher-order PP. It is inferred that the performance of the P_e is associated with the number of connecting taps, as well as the polynomial order. From the findings of Fig. 10, we infer that by processing chips, in the iterative SISO decoder, a correct detection is accomplished. Moreover, by deploying AGC, we attain better SNR at a given P_e because of the linear characteristics of AGC, and the basic principle of iterative schemes. Moreover, AGC aided the SISO decoding, as the linear gain of the AGC is multiplied by the chips processed in the SISO decoder. Thus, the system attains sufficient gain, from the previous iteration, to activate the loading command,

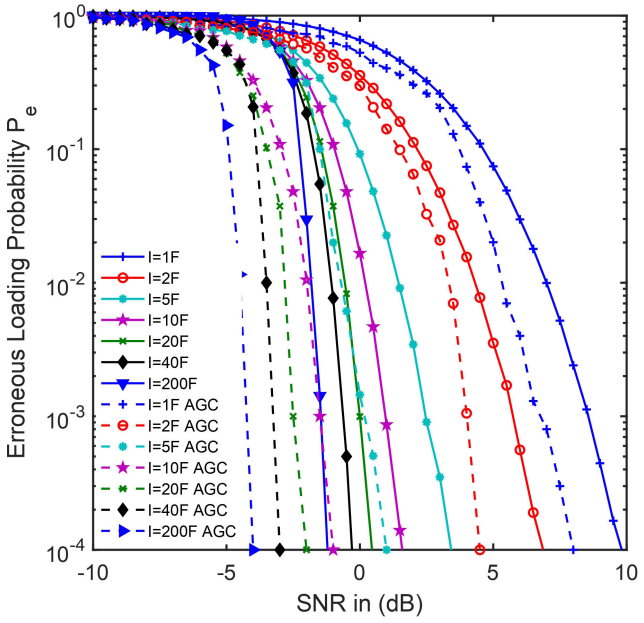

FIGURE 9. Performance analysis of P_e across SNR for varying chip numbers in the ISSE system with $g_3(D)$ over AWGN. The dotted line represents the AGC model, while the solid lines depict the model without AGC.

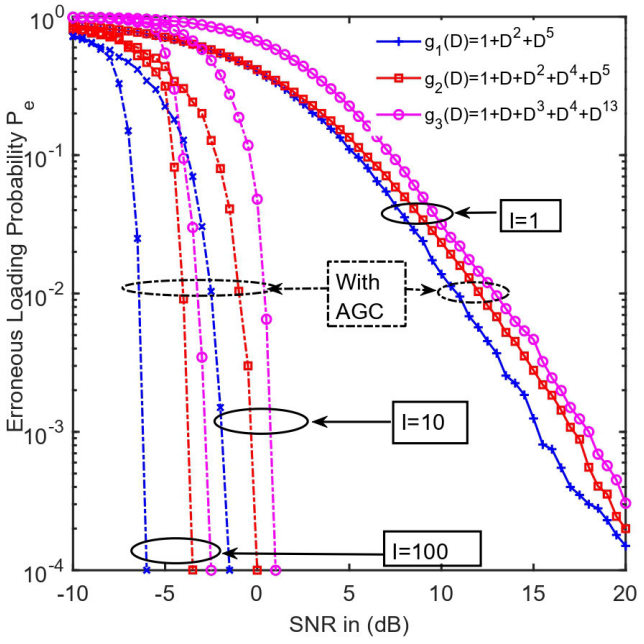

FIGURE 10. Performance in terms of P_e athwart to the SNR, when different chip processes in Nakagami fading channels with $m_I = 3.0$ utilizing ISSE model with AGC.

to acquire a better SNR value. For example, when performing $I = 100$ iteration instead of $I = 10$ the ISSE SISO decoder accomplish 3 dB SNR gain. Thus, the SNR value is -4 dB when processing total chips $100 \times 5 = 500$ chips for PP of $g_1(D)$, similarly for the $g_2(D)$ and $g_3(D)$ we achieve almost 3 dB gain which also confirms that using AGC approach we can enhance the system performance. Fig. 10 shows that

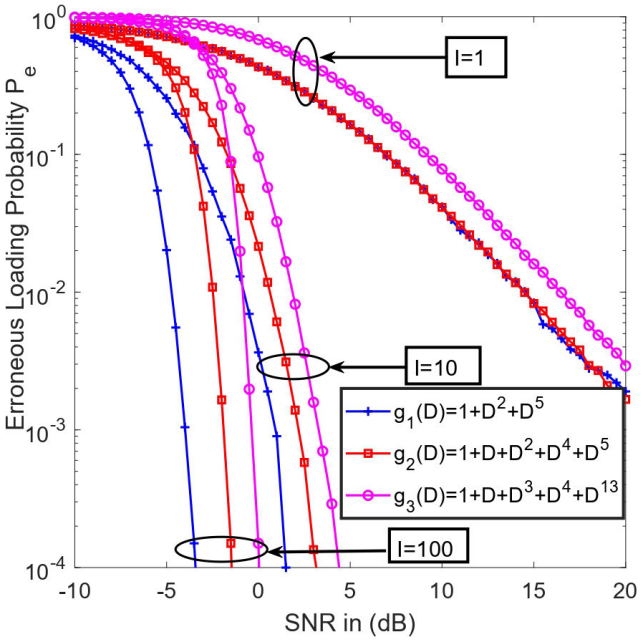

FIGURE 11. Performance in terms of P_e athwart to the SNR, for different chip processes in Nakagami fading channels with $m_I = 3.0$ using the ISSE model without AGC model.

the PPs $g_1(D)$ and $g_2(D)$ outperform $g_3(D)$ as they belong to 5^{th} order polynomial, while $g_1(D)$ outclass the other two polynomial as it consists of non-consecutive-connecting taps. In other words, the extrinsic information is hegemonies by all the feedback taps which are involved to calculate the minimized LLR values. Moreover, the PP utilizing a low number of taps connections yields a higher likelihood of generating the extrinsic information for the SISO decoding acquiring model, than those PPs having more connecting taps. As in the later stage, the average LLR might be high like in the case of $g_2(D)$ w.r.t $g_1(D)$, where in $g_1(D)$ has low LLR because of having fewer connecting taps as more number of connecting taps are easily affected by the noise. Thus, because of the destructive nature of noise, more chip is easily affected by it as compared to less number of taps. Moreover, more connecting taps require larger memory hence, they cannot attain better gain through an iterative procedure. Therefore, PPs having less connecting taps provide better accuracies than the other PPs having more connecting taps.

From Fig. 11 it is observed that the performance of the PPs for $I = 100$ is superior to that of $I = 10$, since by processing a higher I value more iterations are processed by the SISO decoder. Furthermore, by performing more iterations I, the SISO detector will ultimately reach the endpoint (1,1) for the ideal convergence as P_e will become insignificantly low. It can be concluded, the performance of PP is related to the value of I, as I increases the performance of PP increases. We can deduce that $g_1(D)$ dominates, the other two PPs, because of having three total connecting taps, none of them are consecutive, hence, the performance of $g_1(D)$ is better. Despite $g_2(D)$ and $g_3(D)$ having two consecutive taps out

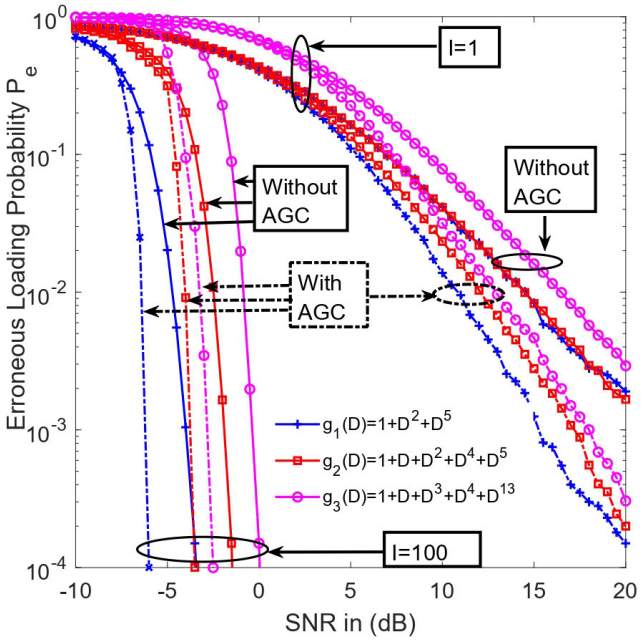

FIGURE 12. Comparison of ISSE scheme performance with and without AGC in terms of Erroneous Loading Probability P_e across SNR, while processing different numbers of chips in the ISSE model using Nakagami fading channels with $m_l = 3.0$.

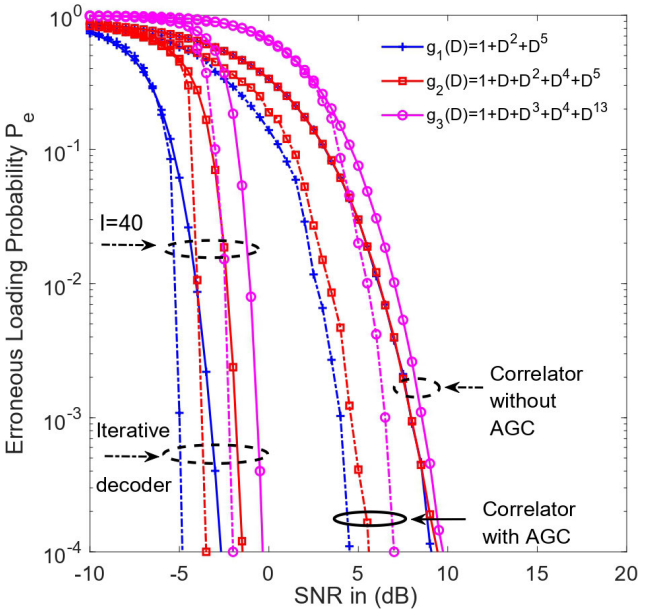

FIGURE 13. Comparison of ISSE scheme performance with and without AGC in terms of Erroneous Loading Probability P_e across SNR, while processing different numbers of chips in the ISSE model using AWGN channels.

of a total of five connecting taps, thus, $g_2(D)$ outperforms $g_3(D)$, because it belongs to 5^{th} order PP, as compared to $g_3(D)$. From Fig. 11, we deduce that the pursuance of the receiver relies on the polynomial order and the number of connecting taps present in generating the m-sequence. Therefore, the receiver has a contingent when $g_1(D)$ is employed because the detection efficiency of the receiver improves when connecting taps are less as opposed to that employing $g_2(D)$ and $g_3(D)$. Since the detection capability, is linked with the connecting taps plus the polynomial order. Fig. 11 is generated without deploying the AGC model, where the shaping value m_l is kept fixed to 3.0, the comparisons are drawn in terms of the P_e versus the SNR, for three different generator polynomials. The result confirms that $g_1(D)$ outperforms the other two PPs, because of having less connecting indices, while producing the m-sequence whereas $g_2(D)$, and $g_3(D)$, have two successive taps, thus the performance of $g_3(D)$ is worse than $g_2(D)$ because it belongs to higher-order polynomial 13^{th}. Hence, it can be inferior that more taps and higher-order consume more energy. Thus, they do not benefit much from the iterative decoding procedure.

In Fig. 12, we have compared both the approaches by deploying with/without AGC, the comparison is concluded, in terms of the P_e versus the SNR performance, which is recorded for three diverse, PPs. In this simulation, the Nakagami shaping parameter was kept constant to $m_l = 3.0$. Fig. 12 demonstrate that by utilizing AGC concept we attain better gain in all respect when comparing the system without the AGC approach. For $P_e = 10^{-4}$, we obtain better SNR values for the AGC approach, as compared to the one that is exploiting without AGC. The result confirms that the performance of the polynomials for $I = 1$ is inferior to that when $I = 100$ hence, by processing more chips, more decoding iterations, are engaged and every time, the iteration is multiplied by the linear gain of the AGC when deployed in the ISSE scheme, thus enhancing the system performance. For example: when utilizing ISSE without AGC, $g_1(D)$, $g_2(D)$ and $g_3(D)$ obtained respective SNR values 32 dB, 33 dB and 35 dB at $P_e = 10^{-4}$ when $I = 1$ whereas adopting AGC the same polynomial g_1, g_2 and g_3 obtained respective SNR values 21 dB, 22 dB and 24 dB at $P_e = 10^{-4}$ when $I = 1$ and for $I = 100$ at $P_e = 10^{-4}$ we achieve SNR for $g_1(D) = -3.0$ dB, $g_2(D) = -1.5$ dB and $g_3(D) = 0.0$ dB without AGC and with AGC -6 dB for $g_1(D)$, for $g_2(D)$ -3.0 dB and for $g_3(D)$ -2.5 dB, which illustrate that adopting AGC we can improve system performance because every iteration will have the linear gain of AGC which will improve the system performance. Furthermore, in Fig. 12, we analyze that increase of I, the performance of all polynomials tends to improve significantly.

In Fig. 13 comparison is drawn in the ISSE model with those of the correlator for m-sequence with diverse lengths when receiving over AWGN channel with and without AGC. Fig. 13 reflects that the PP can be acquired at a particular value of SNR -0.5, -2, and -3 dB by entering 40 iterations without using AGC approach. Despite, adopting the AGC the PP is obtained at a particular value of SNR -2.5, -4, and -5 dB by entering 40 iterations in a correlator, the PN code acquisition model operates at a particular value of SNR 5, 6 and 7 dB in order to attain the P_e of 10^{-4} whereas without using AGC the PN acquisition model operates at a

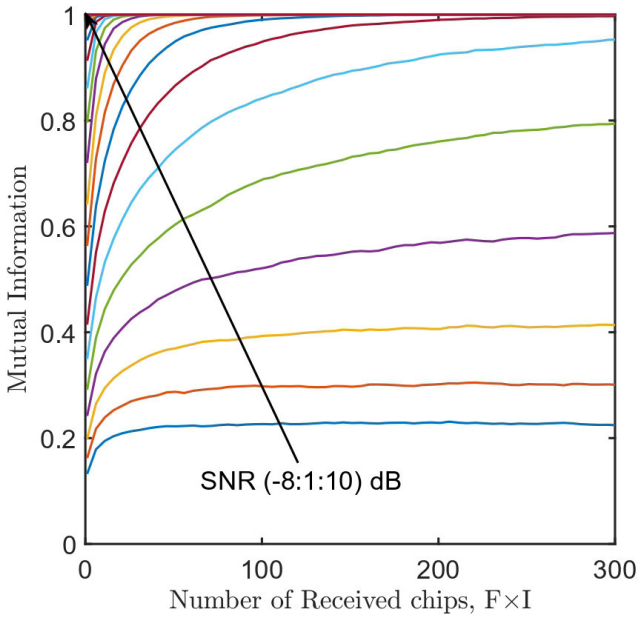

FIGURE 14. Mutual information athwart the number of received chips for the PP $g_1(D)$ characterized by different SNR values spanning from −8 to 10 *dB*.

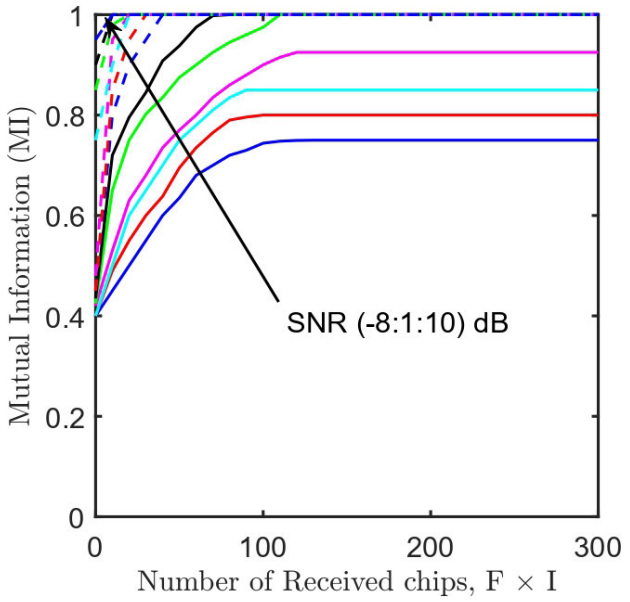

FIGURE 15. Mutual information athwart the number of received chips for the PP $g_1(D)$ characterized by different SNR values spanning from −8 to 10 *dB* when deployed in AGC model.

particular value of SNR of 10 *dB* in order to attain the P_e of 10^{-4}. Thus, the achievable SNR gain in the ISSE acquisition model at an P_e of 10^{-4}, is around 7, 6 and 5 *dB* when using AGC methodology in $g_3(D)$, $g_2(D)$ and $g_1(D)$ respectively. From these results, we deduce that the PP using a lower number of connecting taps utilizes low memory elements. Thus, their soft values have enough self-belief that helps to acquire a better SNR value at a particular P_e. Moreover, fewer taps are less mitigated by noise than those possessing more connecting taps, as more taps consume more power, and they do not benefit more from the iterative methodology.

In Fig. 14, we have evaluated our result, where we have not exploited the AGC approach. In Fig. 14, the ratio amongst the number of received chips and the MI is drawn. As when the SNR is increased, the MI is improved significantly. From Fig. 14, it can be observed that for SNR above -3 *dB*, the MI is capable of converging to one with less than 300 number of received chips. It is deduced that at a higher SNR value, the total number of received chips will improve, and obtain a more reliable estimation of *m*-sequence.

In Fig. 15, we have evaluated our AGC approach. In Fig. 15, the ratio among the number of received chips, and the MI is drawn. From Fig. 15, it can be observed that for SNR above -5 *dB*, the MI is capable of converging to one with less than 300 number of received chips. It is revealed that at a higher SNR value, the total number of received chips will be improved and obtained a more reliable estimation of *m*-sequence.

From Figs. 14, and 15, we can deduce the performance comparison between our proposed system with the previous one of [21] and [12]. It can be observed that the AGC approach convergences much faster, and requires less than

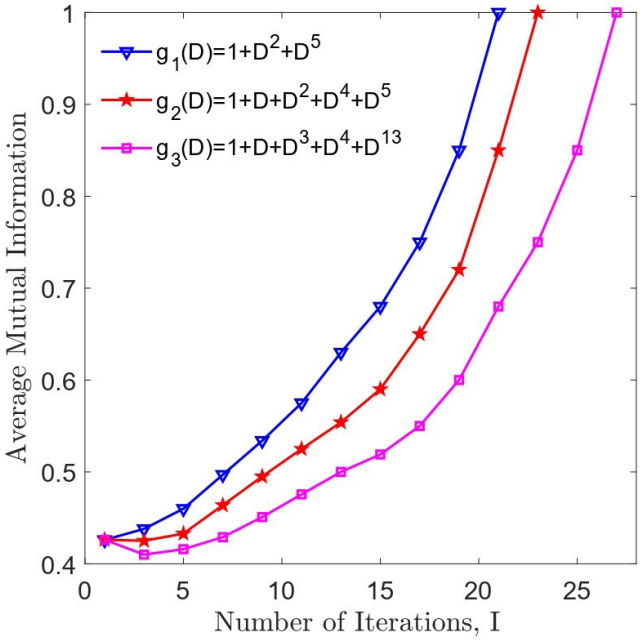

FIGURE 16. The Average Mutual information (AMI) athwart the number of decoding iterations processes in the SISO decoder over Nakagami channel $m_l = 3.0$ for $g_1(D)$ (blue), $g_2(D)$ (red) and $g_3(D)$ (magenta).

20 iterations to obtain MI= 1. The SISO decoder needs a total of 80 received chips, to obtain $MI = 1$ at SNR=-2 *dB*. Furthermore, when AGC is not exploited, we need a total of 250 received chips to obtain $MI = 1$, at SNR=-2*dB*. Thus, we can infer that by using the AGC system, we can improve system performance.

Fig. 16 shows that the performance of $g_1(D)$ and $g_2(D)$ is better than $g_3(D)$ because both polynomials have similar

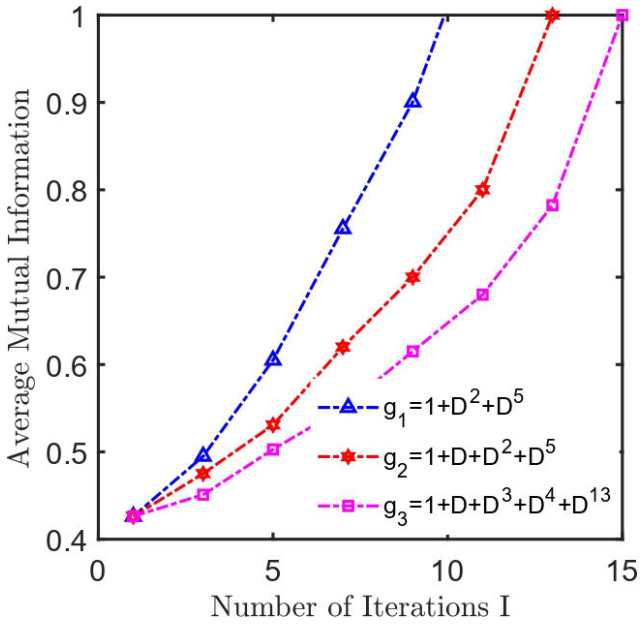

FIGURE 17. The Average Mutual information (AMI) athwart the number of decoding iterations processes in the AGC SISO decoder over Nakagami channel $m_l = 3.0$ for $g_1(D)$ (blue), $g_2(D)$ (red) and $g_3(D)$ (magenta).

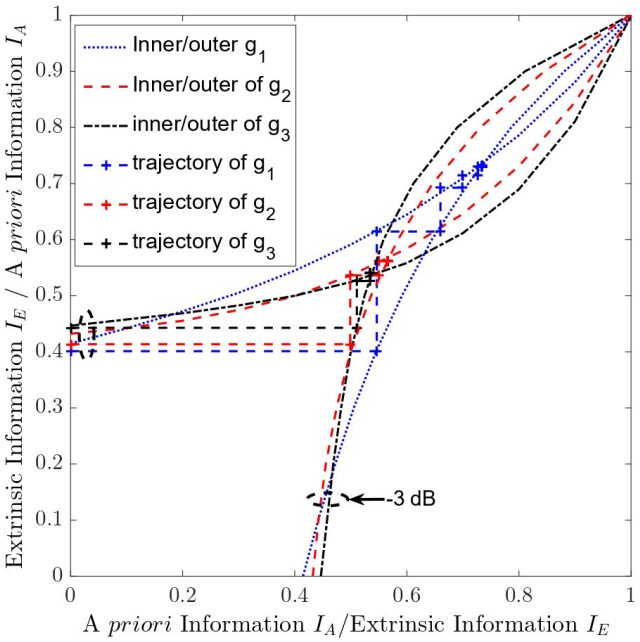

FIGURE 18. EXIT charts for the PPs $g_1(D)$ (blue), $g_2(D)$ (red), and $g_3(D)$ (black) under Nakagami fading channels with $m_l = 3.0$, at an SNR of -3 *dB*.

order that is 5 whereas $g_3(D)$ belongs to order 13, where $g_1(D)$ outperform because of having two less number of taps as compared to $g_2(D)$ and $g_3(D)$. While comparing the performance of $g_2(D)$ and $g_3(D)$ we observe that $g_2(D)$ belongs to order 5 and $g_3(D)$ belongs to order 13, due to this reason that the performance of $g_2(D)$ is better as it belongs to lower order as compared to $g_3(D)$. It can be deduced that $g_1(D)$ required 21 iteration to reach one as it has a total of three taps none of them is consecutive whereas$g_2(D)$ needs 22 iteration and $g_3(D)$ requires 26 iteration. From Fig. 16 it can be concluded that a polynomial achieves quicker AMI if it belongs to the family of low-order polynomials and has less number of taps like $g_1(D)$.

Fig. 17 demonstrates the Average Mutual Information (AMI) against the number of iterations at a particular SNR value of 0 *dB* by using the AGC approach, when diverse PPs are deployed. It is conceived that $g_1(D)$ needs a total of 10 iterations to achieve unity, whereas $g_2(D)$ needs 12 iteration to achieve unity and $g_3(D)$ requires 15 iteration to achieve the desired goal. This simulation indicates that PPs having more connecting taps have adverse performance because more taps are easily affected by the noise than their counterparts possessing less taps when comparing $g_2(D)$ with $g_1(D)$ respectively.

Table. 1 comparison can be drawn between two things namely one on our simulation results that is P_e against SNR, and other on the number of iterations, utilized when the ISSE scheme is deployed with and without AGC. Thus, when AGC is deployed in our purposed model the PPs performances become better, as $g_1(D)$ needs a total of ten iterations to attain unity, whereas $g_2(D)$ needs twelve iterations, and $g_3(D)$ requires fifteen iterations, to attain unity. Despite this scenarios, when AGC is not utilized in the system, then $g_1(D)$ needs a total of twenty-one iterations to attain unity gain, whereas $g_2(D)$ requires twenty-two iterations and $g_3(D)$ requires twenty-six iterations as listed in Table. 1. This confirms that the AGC scheme outperforms the prior system of [21]. Since, during each iteration, the LLR values will increase effectively by the iterative sequential procedure, as well as by the AGC gain β, thus, achieving maximum unity gain for the system to acquire fast synchronization while utilizing AGC model in ISSE scheme.

Fig. 18 illustrates our previous purposed scheme without utilizing AGC, for a self-concatenated scheme for the ISSE model, at an SNR$= -3$ *dB*. It is depicted from Fig. 18 that all detecting trajectories roughly match their constituent curves, inner and outer curves. In Fig. 18, it can be observed that the PPs failed to achieve the [1,1] position, as our outer and inner curves of the EXIT chart cross-over prior to this end-point. Furthermore, no improvement is observed beyond the cross-over point, where the decoding trajectory intersects the inner and outer curves. As expected, relying on the information gathered in Fig. 15, where the results of MI and the number of received chips are plotted. We also infer that the PP, which has a large memory, tends to exhibit extremely low assurance in its soft approximation. For this reason, they do not adequately gain from an iterative system.

Fig. 19 demonstrates an EXIT chart for our self-concatenated approach for the ISSE technique using the AGC approach, at a particular SNR$= -3$ *dB* when the shaping parameter of Nakagami fading was kept constant to $m_l = 3.0$. According to the EXIT chart principle, the inner and

TABLE 1. Comparisons among the number of iterations as well as the SNR values expressed in *dB* at $P_e = 10^{-4}$, when evolved in the ISSE Model while deploying With/without AGC.

Polynomial Order	Generated Polynomial	Total Number of Taps	SNR expressed in dB		Number of Iterations	
			Without AGC	With AGC	Without AGC	With AGC
5^{th}	$g_1(D)=1+D^2+D^5$	3	-3.0 dB	-6.0 dB	21	10
5^{th}	$g_2(D)=1+D+D^3+D^4+D^5$	5	-1.0 dB	-3.0 dB	22	12
13^{th}	$g_3(D)=1+D+D^3+D^4+D^{13}$	5	0.0 dB	-2.5 dB	26	15

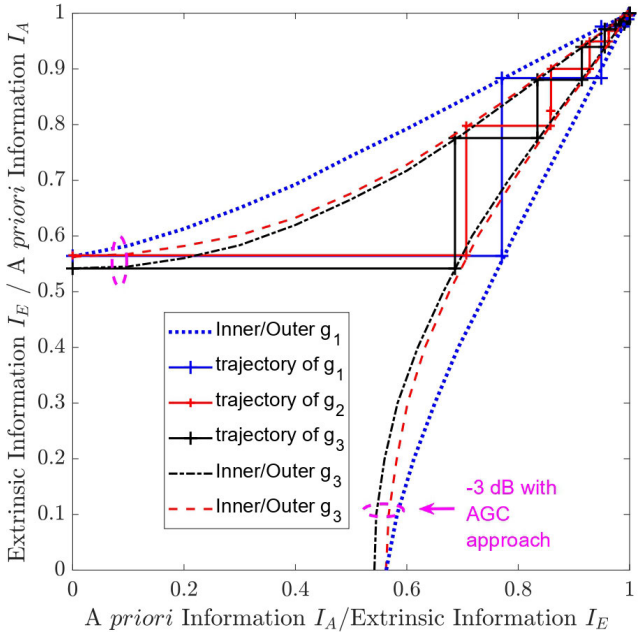

FIGURE 19. EXIT chart using AGC approach of $g_1(D)$ (blue), $g_2(D)$ (red) and $g_3(D)$ (black) over Nakagami channels when $m_l = 3.0$, at an SNR=-3 *dB*.

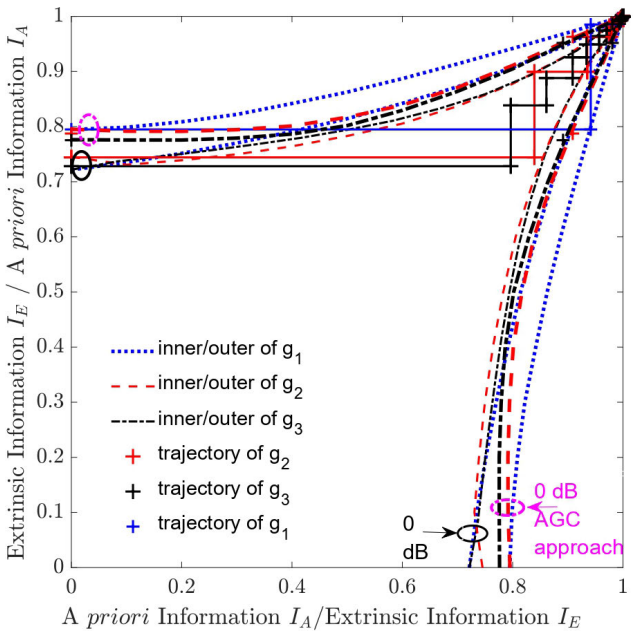

FIGURE 20. EXIT charts for the PPs $g_1(D)$ (blue), $g_2(D)$ (red), and $g_3(D)$ (black) under Nakagami fading channels with $m_l = 3.0$, at an SNR of 0 *dB*, with and without the AGC approach.

outer component curves are matched to decoding trajectories, when an open tunnel exists, between outer and inner curves, at higher SNR values. Thus, obtaining an infinitesimally low BER by using an iterative receiver. Additionally, in Fig. 19, we infer that utilizing an AGC, a better match exists between the outer and inner EXIT curves, as well as the trajectory, which occurs at the SNR value of 3 *dB*. Furthermore, in Fig. 19 we deduce that the PP $g_3(D)$ needs more decoding iterations to attain the right corner [1, 1] location, as compared to $g_1(D)$ and $g_2(D)$. This simulation indicates that the EXIT chart results, obey the trend of MI and AMI of Figs. 14 and 17 and similar information is also depicted in Table. 1 respectively. Thus, comparing different PPs, PPs belonging to lower-order outshine the higher-order PPs, since, they use less memory, and need fewer data to compute. Therefore, they benefit more from an iterative scheme which helps in computing the soft estimation, accurately, and promptly, than those having more taps.

In Fig. 20, a comparison in terms of the EXIT chart is carried out between the approach using with/without AGC. The simulation is generated, at an SNR= 0 *dB*, and the shaping parameter of Nakagami fading was kept constant to $m_l = 3.0$. During the simulation, all the outer and inner component curves match their decoding trajectories, which implies that there exists an open tunnel among the outer and inner curves of the SISO decoder, thus obtained an infinitesimally low BER by the iterative receiver. Thus, the trajectories need less iteration to attain the maximum point [1, 1] on the right corner, when using a higher SNR value, as can be observed in Fig. 20. Therefore, it is summarised that using the AGC approach, a wide opening exists between our outer and inner curves of the EXIT chart. For this reason, our stair-like shape decoding trajectory matches these curves. It can be inferred that by utilizing the AGC approach, we can achieve a better result. For this reason, our values are multiplied by the linear gain of the AGC, during each iteration, which helps to possess a wide opening, in our decoding trajectory of the EXIT chart. In Fig. 20, it is observed that the PP $g_1(D)$ needs less decoding iteration to attain the rightmost corner at [1, 1] position for the given SNR values. In lieu of $g_2(D)$ requires little more

TABLE 2. Comparison of the proposed System with the literature available for synchronization.

Evaluation Performance	Comparison Carried out on the Concerned Approaches		
Approaches discussed in the paper	**Hard Decision Approach [19]**	**Sequential Estimation Approach [9],[11]**	**Our Purposed Approach**
Decision Reliability versus the Number of Received Chips	The magnitude associated with PPs remains constant, which is between 0 to 10, even processing more chips in the decoder, as the polarity of each chip is decided separately by the decoder as illustrated in Fig. 4	In the model proposed by [9], [11], the magnitude associated with PPs varies as more chips are processed in the SISO decoder. For example, $g_1(D)$ has a magnitude of 36 when 100 chips are processed in the SISO decoder. Similarly, when the same number of chips i.es 100 chips are processed at the SISO decoder of $g_2(D)$ and $g_3(D)$, they have a magnitude of 34 and 32 respectively as illustrated in Fig. 4	In our current model, the magnitude associated with PPs increases dramatically, as the same number of chips are processed in the SISO decode. For example, $g_1(D)$ has a magnitude of 63 when 100 chips are processed in the SISO decoder. Similarly, when the same number of chips i.es 100 chips are processed at the SISO decoder of g2(D) and g3(D), they have a magnitude of 58 and 45 respectively as illustrated in Fig. 4
EXIT Chart	Not utilized	When the EXIT chart approach is implemented in the above model, 21 iterations were required for $g_1(D)$ to acquire synchronization at an SNR value of *0* dB. Whereas $g_2(D)$ and $g_3(D)$ need 22 and 26 iterations to achieve synchronization as indicated in Fig. 16	When the EXIT chart approach is implemented in the above model, 10 iterations were required for $g_1(D)$ to acquire synchronization at an SNR value of 0 dB. Whereas g2(D) and g3(D) need 12 and 16 iterations to achieve synchronization as indicated in Fig. 17
Pe versus SNR performance	At $P_e=10^{-4}$ the SNR value is 35 dB for $g_1(D)$, similarly, at the same P_e the value of $g_2(D)$ is 37 dB, and for $g_3(D)$ the value is 40 dB when iteration I=1 as demonstrated in Fig. 12. The system utilizes the hard decision approach listed in [19]. In this system, neither the SISO decoder nor the AGC was not involved.	For the sequential system when $P_e=10^{-4}$ the SNR value is -3.0 dB for $g_1(D)$, similarly, at the same P_e the value of $g_2(D)$ is -1.5 dB, and for $g_3(D)$ the value is 0 dB when iteration I=100 processed into the SISO decoder as demonstrated in Fig. 12. Thus, this system utilizes the SISO decoder with delay units of *m*-sequence as illustrated in [9], [11].	For the proposed system when $P_e=10^{-4}$ the SNR value is -3.0 dB for g1(D), similarly, at the same P_e the value of g2(D) is -1.5 dB, and for g3(D) the value is 0 dB when iteration I=100 processed into the SISO decoder as manifested in Fig. 12. Thus, this system utilizes the SISO decoder with the impact with AGC through the delay units of *m*-sequence as illustrated in Fig. 2
Approaches discussed in the paper	**Correlator Model [22], [23]**	**Sequential Estimation Approach [9],[11]**	**Our Purposed Approach**
Correlator Analysis	The correlator performance is 10 dB for all the PPs at the $P_e = 10^{-4}$ which is evaluated using models of [20]-[23].	When the above models are used, the PPs $g_1(D)$ is acquired at -3 dB by processing 40 iterations in the SISO decoder. Similarly, when the $g_2(D)$ is employed in the above model. The $g_2(D)$ achieved -2 dB by processing the same number of chips which is 40 into the SISO decoder. Thus, when $g_3(D)$ is deployed on the above-mentioned system it acquired -0.5 dB while 40 iterations are processed into the SISO decoder as indicated in Fig. 13.	When the proposed model is used, the PPs ($g_1(D)$, $g_2(D)$, and $g_3(D)$) are acquired at −5, −4, and −2.5 dB by entering 40 iterations in the SISO decoder, which means the AGC approach is better than the rest schemes as depicted in Fig. 13
Approaches discussed in the paper	**Serial Search-based Acquisition Scheme [20]**	**Sequential Estimation Approach [9],[11]**	**Our Purposed Approach**
Acquisition Time	The mean Acquisition time of the serial search-based acquisition scheme is calculated as $N\tau D/2 = 4095\tau D$, where τD is the integration dwell time, which is ten to a hundred chips, lets the minimum chips be 10 then, $N\tau D/2 = 4095 \times 10 = 40950$ which is high, when a period of $N = 2^{13} - 1 = 8191$ chips, is produced by a PP of 13 orders, the PP expressed as $g_3(D)$ as shown in Fig. 9	Similarly, when the same PP $g_3(D)$ having a period of $N = 2^{13} - 1 = 8191$ is acquired at an SNR = 1.7 dB by entering $520 = 40 \times 13$ chips in the iterative SISO decoder without adopting the AGC approach. This PP is acquired at a less SNR value of 1 dB by entering $2600 = 200 \times 13$ chips in the iterative SISO decoder, which is also very less than 40950 chips processed by a serial search model. This indicates that this approach is better than the serial search approach as depicted in Fig. 9.	When the same PP $g_3(D)$ having a period of $N = 2^{13} - 1 = 8191$, is acquired an SNR = −3.0 dB by entering $520 = 40 \times 13$ chips in the proposed model. This PP is acquired at a less SNR value of −4.0 dB by entering $2600 = 200 \times 13$ chips in the proposed model, which is also very less than 40950 chips processed by a serial search model. This indicates that the proposed approach is far better than the serial search approach and sequential Estimation approach as can be visualized in Fig. 9

decoding iterations to reach the respective point i.e [1, 1] on the right corner, thus the performance of $g_1(D)$ and $g_2(D)$ is better than $g_3(D)$ as both of them belongs to 5^{th} order whereas $g_3(D)$ belongs to order 13^{th}. This reflects that the higher-order PPs possess slower convergence capacities than the lower-order PPs, as they exhibit large memory. For this reason, they do not benefit effectively from an iterative procedure. From these results, we deduce that the PP using a lower number of connecting taps utilizes low memory elements. Thus, their soft values have enough self-confidence that helps to acquire a better SNR value at a particular P_e. Moreover, fewer taps are less mitigated by noise than those possessing more connecting taps, as more taps consume more power, and they do not benefit more from the iterative methodology.

Table. 2 confirms the credibility of the proposed ISSE model. The proposed system outperforms the conventional and iterative sequential techniques in all aspects which are listed in Table. 2. Possessing these attractive characteristics, our ISSE scheme is competent for effective initial synchronization of PPs with a low AT. Furthermore, it can be deduced from Table. 2 that the proposed system outperforms all the approaches available in the literature for acquiring the initial synchronization for the *m*-sequences to transmit data over any channel.

V. CONCLUSION

We conclude that lower-order PPs outperform higher-order PPs, as their performance is influenced by both the polynomial order and the number of taps. Lower-order PPs with fewer taps demonstrate superiority over those with more taps, as the taps are directly affected by noise, impacting the PPs' performance in terms of P_e versus SNR. This observation is further supported by the analysis of the EXIT chart. PPs with fewer connecting taps result in less error propagation compared to their counterparts with more taps. In essence, PPs with more connecting taps exhibit poorer performance, as the noise easily affects multiple taps, hindering the benefits of iterative procedures. Despite obtaining a single low LLR, the average LLR may remain high in later stages. Additionally, PPs with fewer taps yield a wider EXIT chart, indicating faster sequence acquisition at lower SNR values. The P_e simulations validate the reliability of the suggested EXIT chart model.

It is revealed that the ISSE acquisition technique using the AGC approach entails some execution difficulty and an initial synchronization time, which depend on the number of periods involved in producing the *m*-sequence. Moreover, the ISSE acquisition technique is suitable for acquiring *m*-sequences transmitted through diverse mediums, such as AWGN and

fading channels. Therefore, the ISSE process is implemented at the chip level of the m-sequence generator, where these values are linearly multiplied with the β gain of the AGC during each iteration. This contributes to a wider opening in the EXIT curves and facilitates faster and more efficient chip synchronization.

Due to these appealing attributes, the ISSE acquisition design establishes optimal initial synchronization techniques for acquiring long m-sequences transmitted through diverse channels. It has been demonstrated that the ISSE acquisition technique outperforms both conventional serial search-based acquisition methods and conventional parallel search-based [34] acquisition methods.

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