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RESEARCH ARTICLE

New Compact Load Network for Doherty Power Amplifiers Based on L-Section Matching Network of the Carrier Amplifier and Post-Matching Network

YIFEI CHEN[1], WOOJIN CHOI[1,2], JAEKYUNG SHIN[1,2], HYEONGJIN JEON[1,2], SOONCHEOL BAE[1], SOOHYUN BIN[1], SUNWOO NAM[1], YOUNG CHAN CHOI[1], HYUNUK KANG[3], KANG-YOON LEE[1], (Senior Member, IEEE), KEUM CHEOL HWANG[1], (Senior Member, IEEE), AND YOUNGOO YANG[1,2], (Senior Member, IEEE)

[1]Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea
[2]Para-PA Inc., Suwon 16419, South Korea
[3]Samsung Electronics Company Ltd., Suwon 16677, South Korea

Corresponding author: Youngoo Yang (yang09@skku.edu)

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ABSTRACT This paper presents a new compact load network for Doherty power amplifiers (DPAs) with only two matching networks, such as an output matching network of the carrier amplifier, and the post-matching network (PMN), even in the presence of parasitic circuits of the packaged transistor. The load network of the carrier amplifier can be configured using a simple L-section matching structure for the complex load impedance. No matching network is required between the peaking amplifier and the current combining junction. As a result, the proposed load network can have a very compact structure with only a short transmission line, and a shunt element for the carrier amplifier, in addition to the PMN. To verify the proposed circuit, a DPA based on two packaged GaN-HEMTs was designed and implemented to have a peak output power of more than 43 dBm for the 3.5-4.0 GHz band. By the measurement results using a 5G NR signal with a peak-to-average power ratio (PAPR) of 7.9 dB and a signal bandwidth of 100 MHz, a power gain of more than 10.5 dB, and a drain efficiency (DE) of 49.5-55.4% at an average power of 36.5 dBm in the frequency band was exhibited. After applying digital pre-distortion (DPD), an adjacent channel leakage power ratio (ACLR) of -51.0 dBc was achieved.

INDEX TERMS Doherty power amplifier, load modulation, efficiency, compact load network, GaN.

I. INTRODUCTION

High-order modulation schemes with increased PAPRs and channel bandwidths have been employed to achieve the high data rate required for modern wireless communication systems. As an efficient structure for these modulated signals, especially at a large output power back-off (OBO) condition, DPAs with an ability of load impedance modulation have been adopted for wireless communication infrastructures, and are very popular [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]. Hence, an appropriately designed load network with a simple structure and good performances becomes essential to the advanced DPAs.

Compact load networks for the DPAs have been reported in some previous works [1], [2], [3], [4], [5], [6], [7], [8], [9]. Reference [1] included the output capacitance of the transistors of the carrier and peaking amplifiers to design equivalent

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transmission lines using integrated lumped components (high-pass, π-type) for the carrier and peaking amplifiers. The PMN was removed by selecting appropriate impedances for the output power of the transistors. However, the application of this method could be limited to packaged transistors that have more complex parasitic circuits. In the method reported in [2], the internal parasitic elements of a packaged transistor were simply assumed to be a shunt capacitor, which was included in a low-pass π-type quarter-wave transmission line based on lumped components. However, the effects of the bonding inductance and the interconnection in the package also need to be considered to accurately design the circuits at the high and broad frequency band. Recently, a load network for the carrier amplifier based on a quasi-lumped quarter-wave transmission line that includes the parasitic networks was introduced [3]. Though the load network of the carrier amplifier was implemented in a very compact size, a relatively large matching network was still required for the peaking amplifier. Reference [4] reported a method to remove the quarter-wave transmission line and an offset line by using a lumped output balun. However, additional matching circuits are still required between the transistor and the balun.

In this paper, a symmetric DPA with a new compact load network is proposed. The proposed load network only consists of an output matching network for the carrier amplifier and a post-matching network, even in the presence of parasitic circuits of the packaged transistor. The load network of the carrier amplifier can be configured using a simple L-section matching network consisting of a shunt element applied after the transistor, and a short transmission line connected after the shunt element for the complex load impedance. The transistor of the peaking amplifier is directly connected to the current combining junction, without any additional matching circuit. The load impedances for the carrier and peaking amplifiers according to the frequency can be optimized based on the power and efficiency contours at the internal plane of the transistors by tuning the frequency characteristics of the shunt element in the L-section network. An extended OBO of about 7 dB was achieved with the proposed structure. A DPA was designed and implemented to verify the proposed compact load network using package GaN-HEMTs (CG2H40010F) for the 3.5-4.0 GHz band. The measurement was carried out using a CW signal and a down-link 5G NR signal with a PAPR of 7.9 dB and a channel bandwidth of 100 MHz. The measured performances were compared to those from the previous works.

II. ANALYSIS AND DESIGN OF THE PROPOSED LOAD NETWORK

A. ANALYSIS OF THE PROPOSED LOAD NETWORK

Fig. 1 shows the load network of the conventional Doherty amplifier. An output matching network (OMN_C), an offset line, and a quarter-wave transmission line compose the load network of the carrier amplifier. The quarter-wave transmission line works as an impedance inverter for the load impedance modulation for the carrier amplifier. The load network based on the output matching network (OMN_P) and offset line provides the required impedance transformation at the peak power level and an open-circuited condition at the low power level for the peaking amplifier.

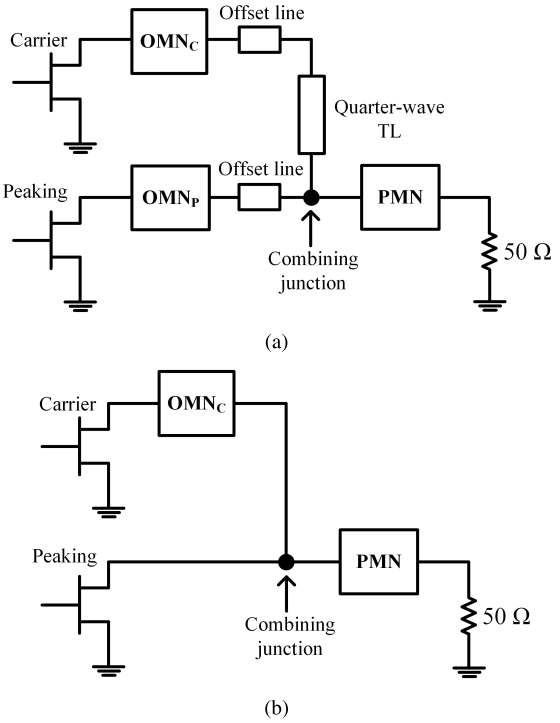


FIGURE 1. Block diagrams of the load networks: (a) conventional, (b) proposed (TL: transmission line).

For a DPA, two impedance conditions should be matched at both the peak power level and the low power level. Although OMN_C also has the ability to transform the impedance, in most cases, it is generally designed to match one of the impedance conditions for the conventional DPAs. Therefore, an offset line and an impedance inverter should be additionally applied after the OMN_C to have the required impedance modulation. Similarly, since OMN_P is designed without consideration of the electrical length, an offset line should be added after the OMN_P to have a high output impedance. Fig. 1(b) shows the proposed structure of the DPA load network. Based on an in-depth analysis of the load network, the complicated circuits can be replaced by a simple L-section matching network for the carrier amplifier. The matching network of the peaking amplifier can be totally removed, even while the parasitic elements due to the package exist. As a result, the proposed load network of the DPAs has a very compact form, even with an extended back-off range of more than 6 dB.

For a hybrid circuit design using packaged transistors, the parasitic elements of the transistor and the package effect can be modeled as a multi-section low-pass network. To obtain

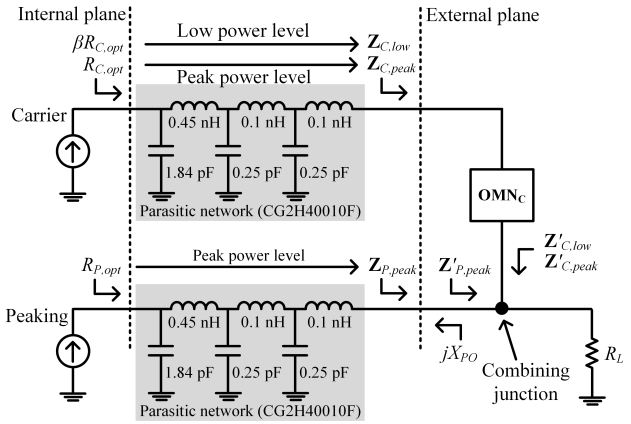


FIGURE 2. Operational diagram of the proposed load network with parasitic elements for the package.

an optimum load impedance at the internal plane (intrinsic drain terminal) of the transistor, a corresponding optimum complex load impedance is required at the external plane of the packaged transistor. If the optimum load impedance of the peaking amplifier at the external plane can be provided by OMN$_C$ and PMN, the peaking amplifier can be directly connected to the combining junction without any additional matching networks.

To obtain the required load impedance at the external plane of the peaking amplifier at the peak power level, the relations between the load impedances of the carrier amplifier and the peaking amplifier at both the low power and peak power levels should be clarified. As shown in Fig. 2, for the carrier amplifier, the load impedances before the combining junction at the low power and peak power levels are represented as $Z'_{C,low}$ and $Z'_{C,peak}$, while $Z_{C,low}$ and $Z_{C,peak}$ are the optimum load impedances of the carrier and peaking amplifiers at the external plane, respectively. Then, $Z_{P,peak}$ is the optimum load impedance of the peaking amplifier at the peak power level, and jX_{PO} is the output reactance of the peaking amplifier at the external plane. According to the comprehensive analysis of the DPA load network presented in [15], the load impedances of the carrier and peaking amplifiers before the combining junction for the proposed structure can be related as follows:

$$\frac{1}{Z'_{C,peak}} = \frac{1}{2R_L} - j\left(\frac{1}{X_{PO}} + \frac{\alpha}{R_L}\right), \tag{1}$$

$$\frac{1}{Z'_{C,low}} = \frac{1}{R_L} - j\frac{1}{X_{PO}}, \tag{2}$$

$$\frac{1}{Z'_{P,peak}} = \frac{1}{2R_L} + j\left(\frac{1}{X_{PO}} + \frac{\alpha}{R_L}\right), \tag{3}$$

where, α is a constant related to the load modulation ratio of β, which is expressed as follows:

$$\alpha = \sqrt{(\beta - \frac{1}{2})(\frac{1}{2} - \frac{1}{\beta})}. \tag{4}$$

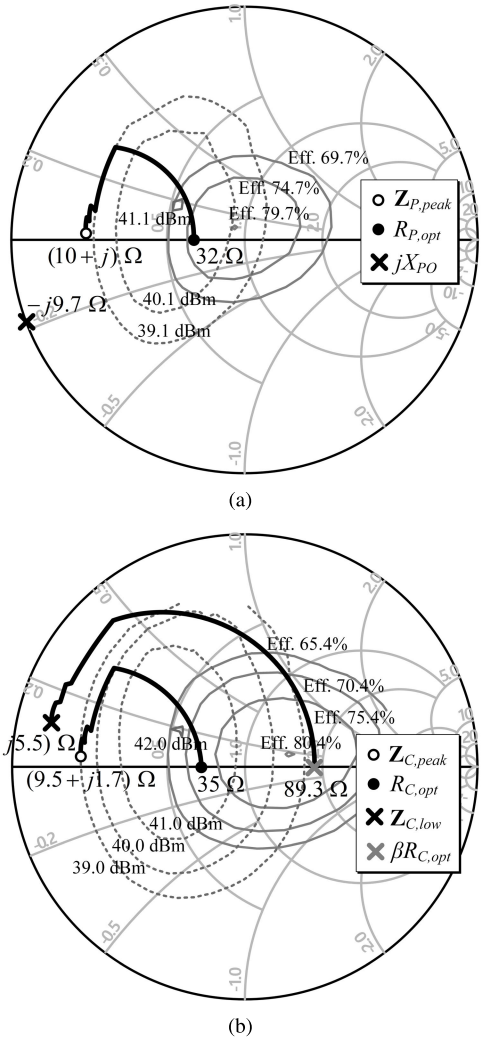


FIGURE 3. The load impedances on output power (gray dotted) and efficiency contours (gray solid) derived at the internal plane and external plane (black solid): (a) peaking amplifier, (b) carrier amplifier.

For conventional DPAs, β is chosen first, then, α can be obtained, so that the corresponding impedances can be found from (1)-(3). However, for the proposed DPA without any matching network of the peaking amplifier except for the parasitic elements from the package, following relations for the impedances can be derived.

$$Z'_{P,peak} = Z_{P,peak}, \tag{5}$$

$$R_L = \frac{|Z_{P,peak}|^2}{\mathrm{Re}(Z_{P,peak})}, \tag{6}$$

$Z_{P,peak}$ is determined using the parasitic elements and an optimum load resistance of $R_{P,opt}$, of the peaking amplifier. The value of $Z_{P,peak}$ determines both R_L and $Z'_{P,peak}$. Then, α should be also derived using (3)-(6) as follows:

$$\alpha = \frac{1}{\mathrm{Re}(Z_{P,peak})}\{\mathrm{Im}(Z_{P,peak}) + \frac{|Z_{P,peak}|^2}{X_{PO}}\}. \tag{7}$$

Since α is determined from (7) using the parameters from the peaking amplifier, the load modulation ratio, β, can be

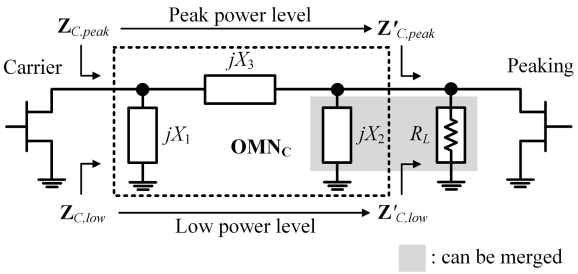


FIGURE 4. π-type network for the OMN_C.

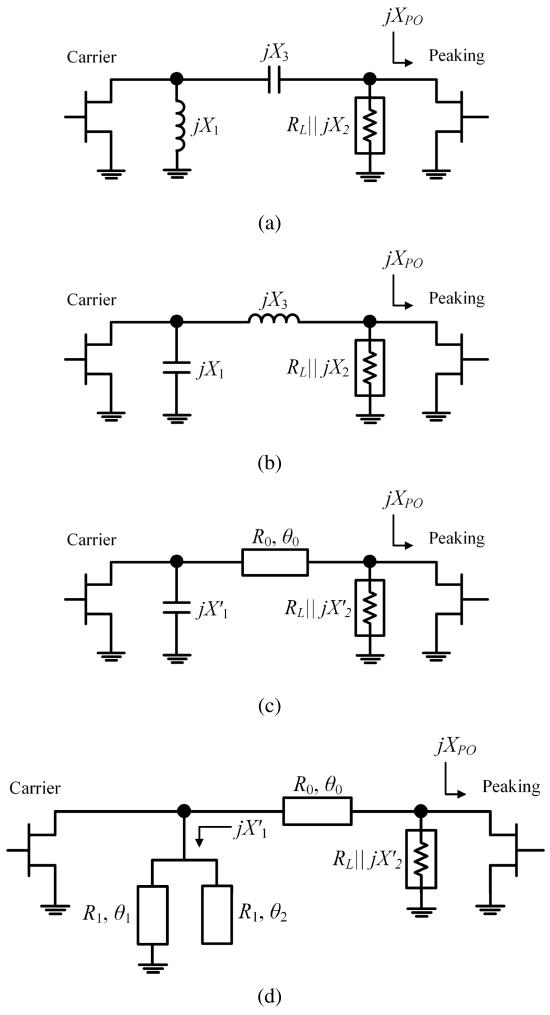


FIGURE 5. Synthesized networks for OMNC: (a) high-pass, (b) low-pass, and (c) low-pass with a series transmission line. (d) Modified low-pass with a series transmission line.

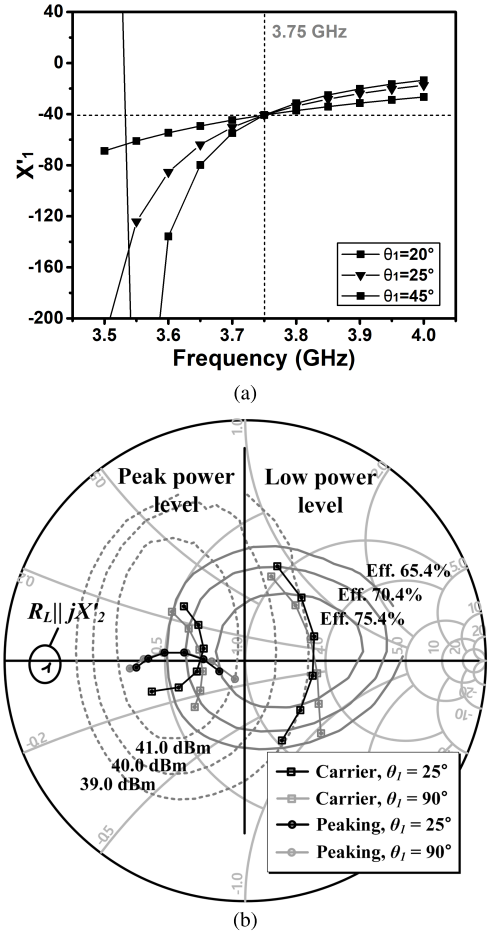


FIGURE 6. Simulated values of X'_1 in (a) and the load impedances at the internal plane and package plane (black solid)with output power (dotted) and efficiency (gray solid) contours in (b) for the frequency range 3.5-4.0 GHz. (Contours were extracted for the carrier amplifier.).

obtained using (4). For this method, β is no longer a predetermined value but a dependent value on parasitic elements of the package. can be adjusted by adding an additional series element after the parasitic elements which separates $Z'_{P,peak}$ from $Z_{P,peak}$.

Although the parasitic network of the peaking amplifier transforms a complex value of $Z_{P,peak}$ to a real value of $R_{P,opt}$, the peak currents of the carrier and peaking amplifiers toward the combining junction should be combined at the load, R_L. At the low power level, the parasitic network of the peaking amplifier operates as a reactive load connected in shunt with R_L for OMN_C. For the load modulation at both peak and low power levels, the load impedances of the carrier amplifier before the combining junction can be derived using (1)-(3) and (7) as follows:

$$Z_{C,peak} = (Z_{P,peak})^*, \tag{8}$$

$$Z_{C,low} = \frac{|Z_{P,peak}|^2}{2\mathrm{Re}(Z_{P,peak})} || jX_{PO}. \tag{9}$$

For the output matching of the carrier amplifier, OMN_C simultaneously transforms $Z'_{C,peak}$ to $Z_{C,peak}$ and $Z'_{C,low}$ to $Z_{C,low}$ at the peak power and low power levels, respectively. For a given parasitic network of the transistor and at the center frequency, the $Z_{C,peak}$ and $Z_{C,low}$ correspond to the optimum load impedances of $R_{C,opt}$ and $\beta R_{C,opt}$ at the internal plane of the transistor, respectively. According to the operational conditions of the carrier amplifier, the ABCD parameters of

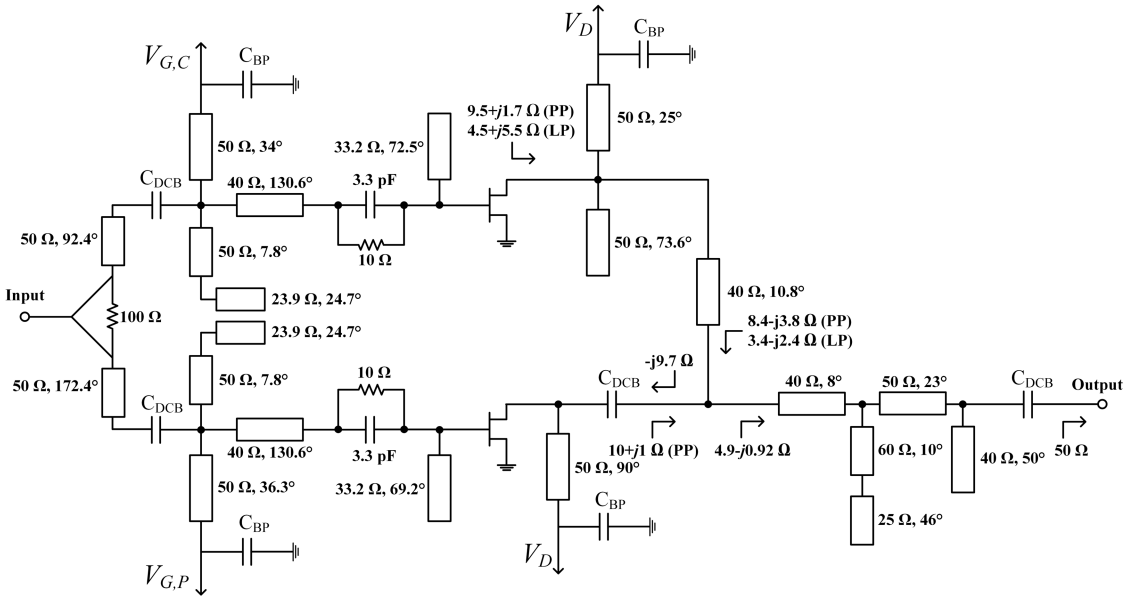


FIGURE 7. Overall circuit schematic of the proposed DPA. (DCB: DC block, BP: bypass, PP: peak power, LP: low power).

the OMN_C can be obtained as follows:

$$\begin{bmatrix} \mathbf{A}_C & \mathbf{B}_C \\ \mathbf{C}_C & \mathbf{D}_C \end{bmatrix} = \pm\sqrt{\frac{\beta(2\beta-1)}{\beta^2-1}} \begin{bmatrix} \mathbf{A}_i & -\mathbf{B}_i \\ -\mathbf{C}_i & \mathbf{D}_i \end{bmatrix} \begin{bmatrix} \sqrt{\frac{R_{C,opt}}{R_L}}\beta\alpha & j\sqrt{R_{C,opt}R_L}(\beta-1) \\ j\sqrt{\frac{1}{R_{C,opt}R_L}}(1-\frac{1}{2\beta}) & \sqrt{\frac{R_L}{R_{C,opt}}}\alpha \end{bmatrix}, \quad (10)$$

where, A_i, B_i, C_i, and D_i constitute the ABCD matrix of the parasitic network of the transistor. Since a network with the same impedance transformation property can have a phase delay of shorter or larger than 180°, the derived network matrix can have a positive or negative sign.

Fig. 3 shows the load impedances of the peaking amplifier in (a) and the carrier amplifier in (b) on the simulated power and efficiency contours at the internal plane for Cree's GaN-HEMT, CG2H40010F. The optimum load impedances of the peaking and carrier amplifiers were determined based on the power and efficiency contours. For the peaking amplifier, a load impedance ($R_{P,opt}$) of 32 Ω at the internal plane of the transistor, which corresponds to a complex load impedance ($Z_{P,peak}$) of $(10+j1)$ Ω at the external plane, was chosen to have an output power of about 40.9 dBm and an efficiency of more than 75%. The output impedance at the external plane was approximated as an output reactance jX_{PO} of $-j9.7$ Ω. Then, from (4) and (7), the load modulation ratio can be calculated as 2.55, which yields a back-off range of 7.1 dB. After that, from Fig. 3(b), the optimum load impedance of the carrier amplifier at the internal plane, $R_{C,opt}$ can be selected as 35 Ω to have β of 2.55 and a peak output power of 41.3 dBm. Therefore, $Z_{C,peak}$ of $(9.5+j1.7)$ Ω and $Z_{C,low}$ of $(4.5+j5.5)$ Ω are found as two optimum load impedances at the peak and low power levels to have the desired load modulation ratio at the internal plane for the carrier amplifier based on the simulation results shown in Fig. 3(b).

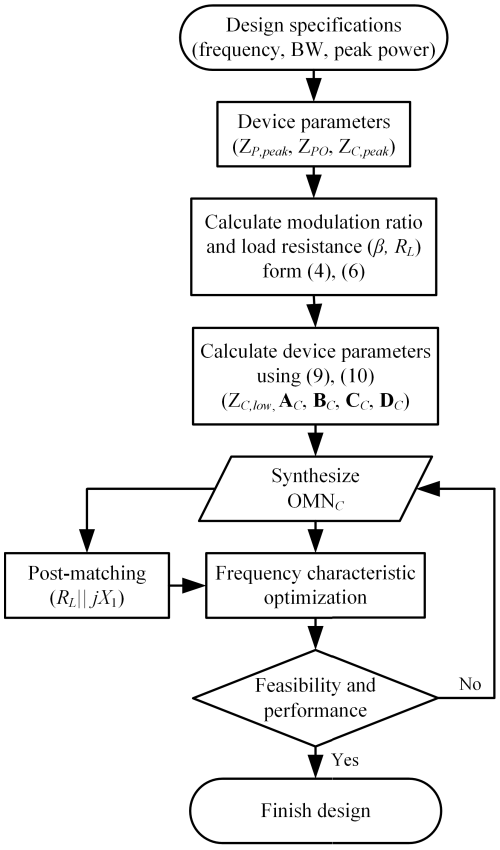


FIGURE 8. Design procedure for the proposed DPA.

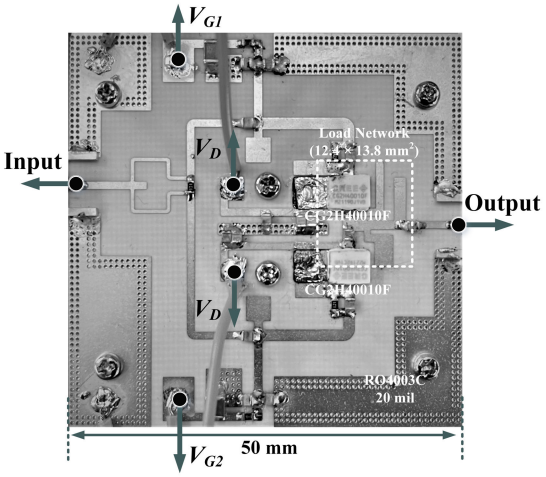


FIGURE 9. Photograph of the implemented DPA.

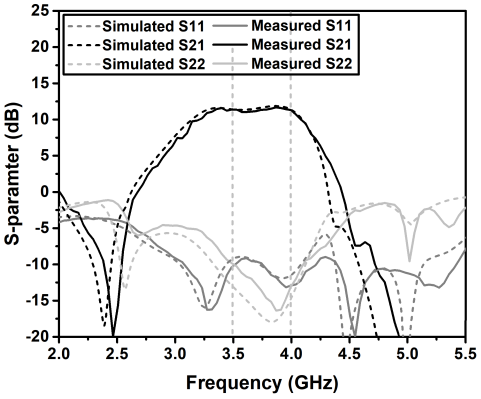


FIGURE 10. Simulated and measured S-parameters of the DPA.

B. DESIGN of OMN$_C$

To have an appropriate load impedance modulation of the carrier amplifier, the load impedance $Z'_{C,peak}$ should be matched to $Z_{C,peak}$ at the peak power level, while the load impedance $Z'_{C,low}$ should be simultaneously matched to $Z_{C,low}$ at the low power level. Since the π-type network can be designed to have electrical properties of any lossless 2-port network at a given frequency, a π-type network was adopted for OMN$_C$. As shown in Fig. 4, the π-type network consists of one series component with a reactance of X_3 and two shunt components with reactance of X_1 and X_2, respectively. The component values of the π-type network for the output matching of the carrier amplifier can be obtained using the derived ABCD parameters of OMN$_C$ in (10) as follows:

$$jX_1 = \frac{B_C}{D_C - 1}, \tag{11}$$

$$jX_2 = \frac{B_C}{A_C - 1}, \tag{12}$$

$$jX_3 = B_C. \tag{13}$$

Hence, the shunt element, jX_2, of the π-network and the load, R_L are connected in shunt at the same node, thus they can be merged to comprise a new PMN with a load impedance

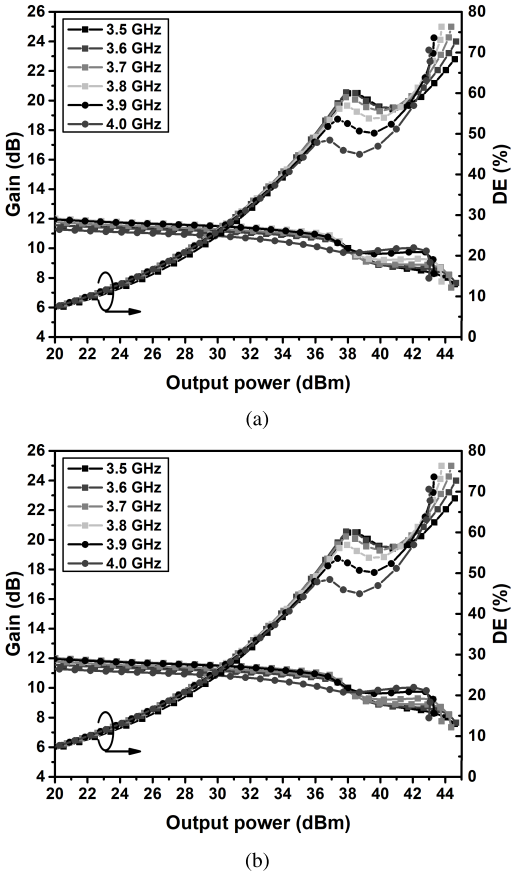


FIGURE 11. (a) Simulated, and (b) measured, DE and gain of the designed DPA at the 3.5-4.0 GHz band.

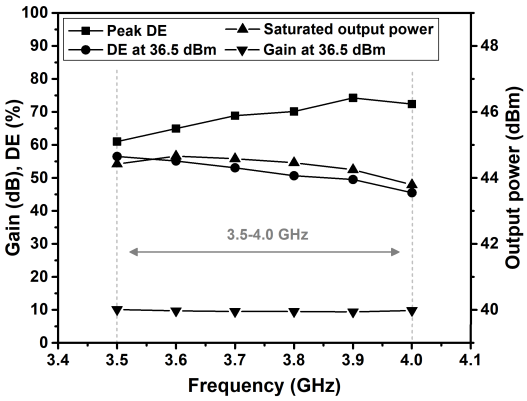
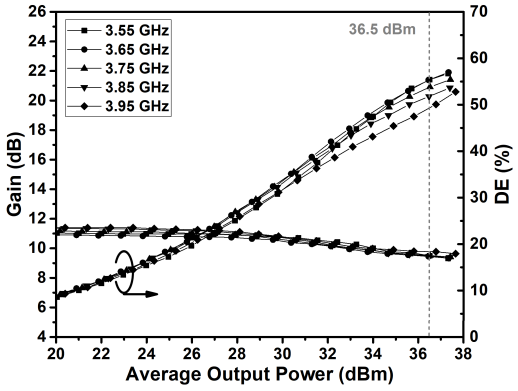


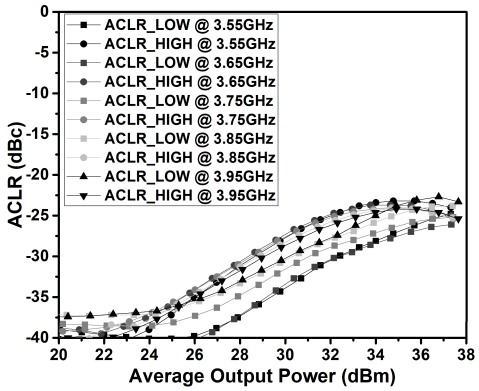
FIGURE 12. Measured saturated output power levels and DEs at the peak power levels and the low power levels.

of a complex value of $(jX_2||R_L)$. Then, a new OMN$_C$ only has a simple L-section network except jX_2. Since (8) has both positive and negative signs, the π-type network can be synthesized with either a high-pass structure or a low-pass structure, depending on the sign.

Figures 5(a) and (b) shows the synthesized high-pass and low-pass networks, respectively, using lumped components. For the high-pass network, the values of reactance X_1, X_2, and X_3 were calculated as 4.2, 4.4, and -7.5, respectively.



(a)



(b)

FIGURE 13. The load impedances on output power (dotted) and efficiency contours (solid) derived at the internal plane: (a) peaking amplifier, (b) carrier amplifier.

To implement X_1 and X_2 using short-circuited stubs, transmission lines with lengths of less than 1 mm have to be used, which could make the circuits too sensitive over the frequency band. For the low-pass network, a series transmission line can be used to replace the lumped inductor having a reactance of X_3, as shown in Fig. 5(c). The component values of the low-pass network using a series transmission line should be re-calculated using the following equations.

$$jX_1' = \frac{B_C}{D_C - \cos\theta_0}, \tag{14}$$

$$jX_2' = \frac{B_C}{A_C - \cos\theta_0}, \tag{15}$$

$$\sin\theta_0 = \frac{B_C}{jR_0}, \tag{16}$$

where R_0 and θ_0 are the characteristic impedance and the electrical length of the series transmission line. In this work, a low-pass network with a very short series transmission line having a characteristic impedance of 40 Ω was selected for the design. According to (14)-(16), the values of X_1', X_2', and θ_0 can be obtained as -40.2, -40.7, and 10.8°, respectively. Then, the complex load impedance becomes $(4.9 + j0.92)$ Ω at the combining junction.

To further improve the performance of the DPA over the desired frequency band X_1' was implemented using a parallel resonant circuit based on an open-circuited stub and a short-circuited stub connected in parallel, as shown in Fig. 5(d). The lengths of the two shunt stubs with the same characteristic impedance, R_1 of 50 Ω, were optimized to provide the required reactance X_1', and to provide better frequency response for the load impedance of the carrier amplifier. Fig. 6(a) shows the change of the reactance X_1' over the frequency band according to the various values of θ_1. The load impedances of the carrier and peaking amplifiers at the internal plane can be changed according to the frequency characteristics of X_1', and they are plotted with output power and efficiency contours on the Smith chart in Fig. 6(b). It can be found from Fig. 6(b) that θ_1 of 25° for the short stub can provide load impedances that have relatively constant output power and high efficiency.

III. OVERALL CIRCUITS AND DESIGN FLOW

Fig. 7 shows the overall schematic of the proposed DPA using microstrip lines and lumped elements. A two-section post-matching circuit was designed between the combining junction and 50 Ω load to implement $(4.9 + j0.92)$ Ω in broadband at the combining junction. A quarter-wave transmission line was deployed after the transistor to terminate the second harmonics, and to supply DC voltage for the peaking amplifier. For the PMN, two-section matching network was adopted including a cascaded open-stub with additional low characteristic impedance of 25 Ω for better frequency characteristics. For the input matching networks, an open-circuited stubs were adopted to make L-section matching networks for both the carrier and peaking amplifiers. A parallel connection of a resistor and a capacitor was applied to improve the stability especially at the low frequency range. A Wilkinson power divider with an even power division is used at the input network. Fig. 8 shows the design procedure for the proposed DPA.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

The DPA was implemented on a PCB based on Rogers's RO4003C with a dielectric constant of 3.66 and a thickness of 20 mil (0.508 mm). The overall circuit size is 50 × 50 mm^2 and the effective load network size is as small as 12.4 × 13.8 mm^2. Fig. 9 shows a photograph of the implemented DPA. The carrier amplifier is biased to have class-AB operation with a quiescent current of 37 mA, while the peaking amplifier is designed to have class-C operation with a gate voltage (V_{G2}) of -6.5 V. The drain supply to both amplifiers is 28 V. As shown in Fig. 10, the simulated and measured S-parameters of the implemented DPA are closely matched.

Fig. 11 shows the simulated and measured power gain and DE according to the output power level using CW signals at the frequency band 3.5-4.0 GHz. The simulated results in Fig. 11(a) show a peak output power of more than 43.0 dBm and a power gain of about 10.4 dB. The simulated DEs

TABLE 1. Performance comparison among this work and previous works.

Ref.	Frequency (GHz)	Topology	Gain (dB)	P_{sat} (dBm)	P_{avg} (dBm)	DE_{avg} (%)	ACLR* (dBc)	OBO (dB)	PAPR (dB)	Signal BW (MHz)	Signal	Size (mm^2)	Device
[1]	2.6	Symmetric	13.7	44.0	37.6	43.0	-31.0/N/A	6	6.5	10	LTE	5×5	GaN MMIC
[3]	3.4-3.8	Symmetric	9.5-11.5†	43.6-.44.4	35.8-36.6	47-54.2	-23/-42	7.8	7.9	100	5G NR	66×78	CG2H40010F
[9]	3.4-3.6	Asymmetric	26.2-26.6	43.0	35	41.5-43.1	-24/-50	8.0	7.2	20	LTE	400	GaN MMIC
[14]	3.45-3.75	Asymmetric VS+OCC	9.5-11.8	41.8-43.5	34.6-36.8	33.3-54.1	-25/-45	8.5	7.9	100	5G NR	71×64	CGH40006P CG2H40010F
[15]	3.4-3.7	Symmetric VS+OCC	11.9-12.7	41.7-42.3	33.7	55.3-60.9	-25.5/-42.6	8.5	7.9	100	5G NR	75×65	CGH40006S
[16]	3.5-4.0	Symmetric LMC	11.1-13	41.7-42.7	34.5	49.6-54.4	-26.5/-49.5	8.0	7.9	100	5G NR	60×66.5	CGH40006S
[18]	3.3-3.55	Asymmetric	12-15	47.5	39.0	50.6	-26/-46.7	7.5-8.0	7.5	20	LTE	125×80	CGH40025 CGH40035
[26]	2.8-3.6	Symmetric	8-13.5	43-44.2	37-38.2	44.0-56.0	N/A	6.0	0	0	CW	N/A	CG2H40010F
This work	3.5-4.0	Proposed load network	10.4-11.8	43.8-44.7	36.5	45.5-56.5	-24.8/-51.0	7.0	7.9	100	5G NR	50×50	CG2H40010F

VS: virtual stub, OCC: out-phased current combining, LMC: load modulation combiner, *: Without DPD / With DPD, †: Graphically estimated

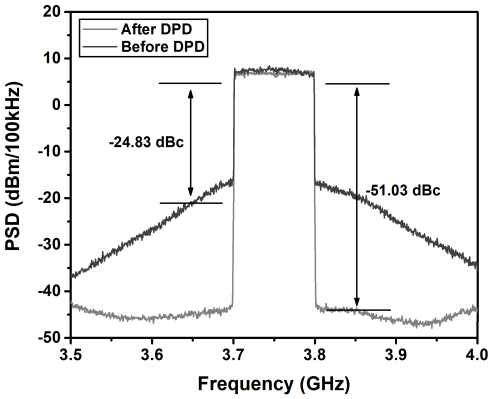


FIGURE 14. Measured PSDs using the 5G NR signal before and after DPD at the carrier frequency of 3.75 GHz.

of 48.4-57.5% were obtained at an OBO of 7 dB for the frequency range 3.5-4.0 GHz. For the measured performance shown in Fig. 11(b), the proposed DPA exhibited a power gain of 9.8-10.1 dB and a DE of 45.5-56.5% at an OBO of 7 dB over the frequency band. Fig. 12 shows the obtained power and efficiency performances over the frequency range of 3.5-4.0 GHz, which corresponds to a fractional bandwidth of 13.3%. The measurement results show good agreement with the simulation results.

Fig. 13 shows the measured performance using a 5G NR modulated signal with a signal bandwidth of 100 MHz and a PAPR of 7.9 dB to investigate the linearity performance of the proposed DPA. According to Fig. 13(a), a power gain of over 10.5 dB and a DE of 49.5-55.4% were achieved at an average output power of 36.5 dBm in the frequency band 3.5-4.0 GHz. To improve the linearity, a DPD based on a memory polynomial was applied, resulting in an ACLR level improvement of more than 26.2 dB, as shown in Fig. 14. Table 1 summarizes the measured performances and compares them with the previously published works.

V. CONCLUSION

This paper presents a new compact load network of the DPA with only two matching networks: the output matching network of the carrier amplifier (OMN_C) and the post-matching network after the combining junction (PMN). The parasitic network inside the transistor package was accurately modeled and considered in the design of the proposed load network. The OMN_C was designed using only a compact L-section structure based on an analysis of the hybrid π-type network applied for the carrier amplifier. For the shunt component of OMN_C an optimized parallel network using short and open stubs, instead of a capacitor or an open stub, was proposed to improve the performance over the bandwidth. A DPA based on packaged GaN-HEMT was designed, implemented, and evaluated for verification at the frequency band 3.5-4.0 GHz. The implemented DPA has a dimension of 50×50 mm^2 including a compact load network with a dimension of 12.4×13.8 mm^2. The evaluation results of the implemented DPA using a 5G NR signal with a signal bandwidth of 100 MHz and a PAPR of 7.9 dB show a high DE of 49.5-55.4% at an average output power of 36.5 dBm with an ACLR level of -51.0 dBc after DPD. The proposed load network was verified through its small size and high performance.

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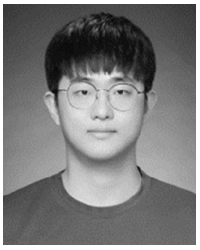
YIFEI CHEN was born in Hebei, China, in 1994. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Korea University, Seoul, South Korea, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea.

His current research interests include the design of RF/mm-wave power amplifiers, broadband techniques, and mm-wave integration circuits.



WOOJIN CHOI was born in Siheung, South Korea, in 1993. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2018, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering.

His current research interests include the design of RF power amplifiers for base stations, broadband techniques, and MMICs.

JAEKYUNG SHIN was born in Seoul, South Korea, in 1993. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Korea Aerospace University, Goyang, South Korea, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea.

His current research interests include the design of RF/mm-wave power amplifiers, efficiency enhancement techniques, broadband techniques, and microwave power transmission.

HYEONGJIN JEON was born in Mokpo, South Korea, in 1994. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2020, where he is currently pursuing the Ph.D. degree with the Department of Information and Communication Engineering.

His research interests include the design of RF/mm-wave power amplifiers, RF/analog integrated circuits, efficiency enhancement techniques, linearization techniques, broadband techniques, and wireless power transfer systems.

SOONCHEOL BAE was born in Daegu, South Korea, in 1995. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2019, where he is currently pursuing the M.S. degree with the Department of Electrical and Computer Engineering.

His current research interests include the design of RF/mm-wave power amplifiers, RF and analog integrated circuits, and wireless power transfer.

SOOHYUN BIN was born in Seoul, South Korea, in 1996. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2022, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering.

His current research interests include the design of RF/mm-wave power amplifiers, RF/analog integrated circuits, efficiency enhancement techniques, linearization techniques, broadband techniques, and microwave power transfer systems.

SUNWOO NAM was born in Incheon, South Korea, in 1991. He received the B.S. degree from the Department of Electronic Engineering, Kwangwoon University, Seoul, South Korea, in 2014. He is currently pursuing the M.S. degree with the Department of Semiconductor Display Engineering, Sungkyunkwan University, Suwon, South Korea.

His research interests include the design of RF/millimeter-wave power amplifiers, RF/analog integrated circuits, efficiency enhancement techniques, linearization techniques, broadband techniques, and wireless power transfer systems.

YOUNG CHAN CHOI was born in Seoul, South Korea, in 1996. He received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2020, where he is currently pursuing the Ph.D. degree with the Department of Information and Communication Engineering.

His research interests include the design of RF/mm-wave power amplifiers, efficiency enhancement techniques, linearization techniques, broadband techniques, and mm-wave integrated circuits and systems.

HYUNUK KANG received the Ph.D. degree from the Department of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea, in 2020.

He joined Samsung Electronics Company Ltd., in 2020, where he has been with the H/W Research and Development Group. His current research interests include 5G RF power amplifier design, linearity and efficiency improvement techniques, and 5G RF advanced techniques.

KANG-YOON LEE (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, South Korea, in 1996, 1998, and 2003, respectively. From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, USA, where he was the Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University, as an Associate Professor. Since 2012, he has been with the Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea, where he is currently an Associate Professor. His research interests include the implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.

KEUM CHEOL HWANG (Senior Member, IEEE) received the B.S. degree in electronics engineering from Pusan National University, Busan, South Korea, in 2001, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2003 and 2006, respectively. From 2006 to 2008, he was a Senior Research Engineer with Samsung Thales, Yongin, South Korea, where he was involved with the development of various antennas including multiband fractal antennas for communication systems and cassegrain reflector antenna and slotted waveguide arrays for tracking radars. He was an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea, from 2008 to 2014. In 2015, he joined the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, the design of multiband/broadband antennas and radar antennas, and optimization algorithms for electromagnetic applications. He is a Life Member of KIEES and a member of IEICE.

YOUNGOO YANG (Senior Member, IEEE) was born in Hamyang, South Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2002. From 2002 to 2005, he was with Skyworks Solutions, Inc., Newbury Park, CA, USA, where he designed power amplifiers for various cellular handsets. Since 2005, he has been with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. His research interest includes RF power amplifiers.