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RESEARCH ARTICLE

Compact Analog Chaotic Map Designs Using SOI Four-Gate Transistors

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ABSTRACT This work introduces three novel chaotic map circuits. Two of the map circuits use two *p*-channel and one *n*-channel silicon-on-insulator (SOI) four-gate transistor (G^4FET) while the third design uses two *n*-channel and one *p*-channel G^4FET. The multi-gate structure of G^4FET is leveraged to obtain four independent bifurcation parameters in the chaotic map with a simple three-transistor design. A chaotic oscillator design is proposed using this discrete-time chaotic map circuit, and the chaotic behavior is evaluated using bifurcation plot, Lyapunov exponent (LE), Correlation coefficient, Shannon entropy, and Stability analysis. The application of this multi-parameter chaotic oscillator is presented in a chaos-based reconfigurable logic gate, and the significant expansion of parameter design space compared to existing single-gate transistor-based maps is also demonstrated. Finally, a simple extension scheme for developing multi-dimensional robust chaotic map with even larger parameter space is presented and verified with specific instances of 2-D and 3-D maps.

INDEX TERMS Chaos, chaotic oscillator, discrete chaotic map, G^4FET, hardware security, nonlinear dynamics, SOI.

I. INTRODUCTION

In 1965, Intel's co-founder, Gordon E. Moore, made an observation that set the benchmark for the semiconductor industry. His observation soon became widely known as Moore's law, which states that the number of transistors on a computer chip doubles every two years, resulting in an exponential increase in functionality, and the advancement in the semiconductor industry has been dictated by the urge to keep up with this law ever since. But Moore's Law has been slowing down for a while as the scaling of transistors has become more difficult in recent years. This has forced the researchers to find alternative ways to integrate more functionality in a given area [1] i.e. to attain better performance without increasing the number of transistors. One way to do this is by increasing the number of computations a device can perform. One viable candidate can be a chaos-based reconfigurable logic circuit, but they mainly have one control parameter per circuit [2]. This is a limiting factor since we know an important performance metric of the chaotic logic circuit for security applications is the design space or functionality space, which is strongly dependent on the number of available control parameters [3].

A way of solving the problem can be to use a multi-gate device such as G^4FET [4]. G^4FET is a prime candidate for such applications as it can provide four independent gates to control carrier transport through a conduction channel. The main difference between a conventional MOS (Metal Oxide Semiconductor) structure and an SOI structure is the buried oxide which isolates the body from the substrate [5]. It combines both MOS field-effect and junction field-effect for conduction control within a single transistor body [6]. It retains usual SOI advantages, which give it an edge over bulk CMOS design [7]. It has low parasitic capacitance due to the oxide layer isolation, so the delay and dynamic power consumption of the device are lower compared to bulk CMOS [8]. It is also immune to latch-up and has a reduced short-channel effect [9], [10]. In addition to the benefits

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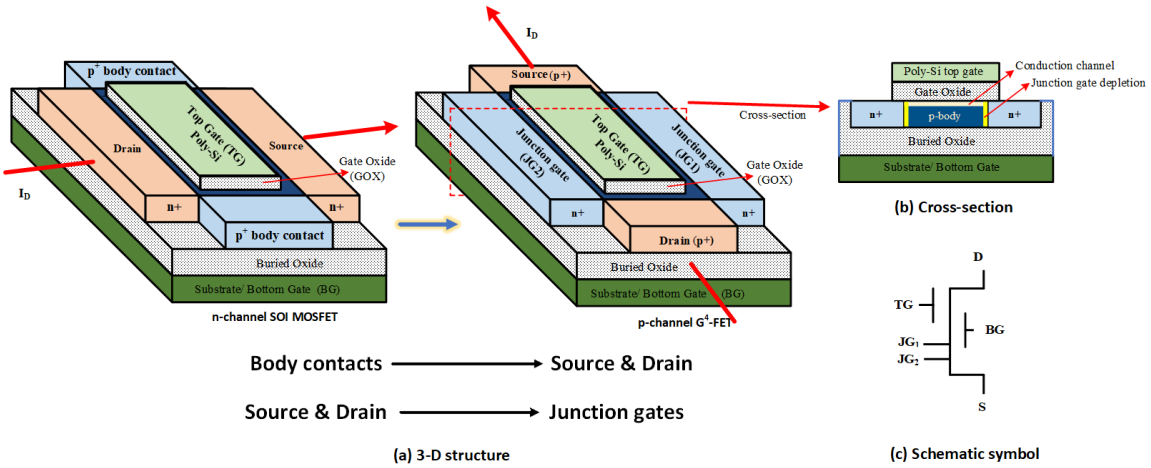


FIGURE 1. p-channel G^{4}FET structure and its equivalence to an n-channel SOI MOSFET with two body contacts.

mentioned, the SOI process also offers higher radiation tolerance, and the leakage currents are smaller due to the better sub-threshold characteristics of the devices [7]. The device is also more suitable for low-power applications as the threshold voltage is less dependent on the back gate bias compared to bulk CMOS due to the oxide layer [11], [12]. Utilizing the four gates separately or in combination can be useful for analog, RF, mixed-signal, and Digital applications [13]. Also, the use of multiple independent gates of G^{4}FET reduces transistor count as compared to standard CMOS implementation [14].

One-dimensional (1D) chaotic systems are known for their simplicity, making them relatively easier to implement. However, recent research publications in the field of chaos-based hardware security have put forth the idea of utilizing higher-dimensional maps such as two-dimensional [15] or three-dimensional chaotic systems [16]. The reasoning behind the introduction of these high-dimensional maps is to guarantee security against modern signal estimation techniques [17], [18], [19]. By transitioning to higher-dimensional chaotic maps, researchers aim to address the limitations associated with 1D systems and achieve improved levels of security.

In this paper, we are proposing three discrete-time chaotic map circuits using G^{4}FET that provide four independent control parameters while using only three transistors in the design. We also present a chaotic oscillator design based on these chaotic maps and analyze its performance with respect to four control parameters. Then we demonstrate its application in designing a reconfigurable and flexible logic gate and highlight the extension of parameter design space. It should be noted that though we have chosen G^{4}FET in this work, the design methodology outlined in this work is general and can be used with any multi-gate transistor. In addition, we are also introducing a simple extension scheme that enables the development of multi-dimensional robust chaotic maps with an extended parameter space. This scheme provides researchers with more flexibility and control over the systems' behavior and improved security levels.

MOSFET		G^{4}FET
PMOS	⟷	N-Channel
NMOS	⟷	P-Channel
Width	⟷	Length
Length	⟷	Width

FIGURE 2. Transformation parameters from MOSFET layout to G^{4}FET.

TABLE 1. Transistor sizing for all three Topologies.

Topology	$\frac{W_1(um)}{L_1(um)}$	$\frac{W_2(um)}{L_2(um)}$	$\frac{W_3(um)}{L_3(um)}$
I	6.3/0.7	40.6/0.7	2.8/0.7
II	7/0.7	18.9/0.7	0.7/0.7
III	18.2/0.7	0.7/0.7	10.5/0.7

The remainder of the paper is organized as follows: Section II describes the device structure of the G^{4}FET, followed by the proposed chaotic oscillator design. The chaotic performance of the oscillator is analyzed in section III using bifurcation plots, Lyapunov exponent, Correlation coefficient, Shannon entropy, and stability analysis. This is followed by the proposed reconfigurable logic generator application in section IV. Section V presents the extension scheme for multi-dimensional chaotic maps with large parameter space. Finally, the conclusion is drawn in section VI.

II. DEVICE STRUCTURE

A standard partially or fully depleted silicon-on-insulator (SOI) process can be used to manufacture the multi-gate device known as G^{4}FET without any additional fabrication procedures [4], [20]. An n-channel MOSFET is converted to a p-channel G^{4}FET using two independent body contacts on each side of the channel. The source-drain of the n-channel MOSFET acts as the two junction gates of the G^{4}FET, while the body contacts act as the source and drain of the

four-gate transistor. The channel conduction can be modulated via four independent gates, rendering it a suitable candidate for designing novel circuits that can perform more functions with fewer transistors [21], [22], [23]. The four independent gates of G^{4}FET are the two lateral junction gates (JG1 and JG2) and the two vertical oxide gates. The two vertical oxide gates consist of the polysilicon top gate and the bottom gate, which is made up of the substrate and the buried oxide. The threshold voltages of the top and bottom gates are influenced by the junction gate voltage.

The structure of a p-channel G^{4}FET is illustrated in Figure. 1. The drain current comprising of the majority carriers flow in the direction perpendicular to that of the n-channel SOI MOSFET. The junction gates are reversed biased and can be used to control the channel width as they have similar functions to a JFET, whereas the vertical oxide gates behave like a traditional MOSFET gate [22]. Figure. 2 summarizes the transformation parameters from the MOSFET layout to the G^{4}FET device.

The G^{4}FET is a scalable device. A narrower G^{4}FET channel can be achieved through a shorter MOSFET length where the action of the lateral gates is further increased. The channel length of the G^{4}FET is also scalable as the channel width of the regular SOI MOSFETS. The G^{4}FET length can also be reduced below 0.5 μm if needed [24]. The vertical gates in G^{4}FET are used to create depletion, accumulation, or inversion of free carriers in silicon epi-layer near the top and bottom gates. The electrical characteristic of G^{4}FET is derived from the relationship among these different gates [20]. The top-gate threshold voltage is denoted as V_{TH}, while the V_{BG}^{acc} and V_{BG}^{inv} are the bottom gate voltages causing the onset of accumulation and inversion, respectively. A summary of the mathematical model of the threshold modulation is given below [20]. A few of the terms used in the model:

Junction-gate capacitance, $C_{JG} = \varepsilon_{\mathbf{Si}}/W$

Top oxide capacitance, $C_{ox1} = \varepsilon_{\mathbf{ox}}/t_{\mathrm{ox1}}$

Bottom oxide capacitance, $C_{ox2} = \varepsilon_{\mathbf{ox}}/t_{\mathrm{ox2}}$

Three geometry-dependent constants, α, β and γ, are defined as follows:

$$\alpha = \frac{2\sqrt{2}}{tanh(\frac{2\sqrt{2}t_{si}}{W})}, \beta = \frac{\gamma C_{JG}/C_{ox1}}{1+\alpha C_{JG}/C_{ox2}}, \gamma = \frac{2\sqrt{2}}{sinh(\frac{2\sqrt{2}t_{si}}{W})}$$

The other terms, φ_F, φ_b and V_P are defined below as,

$$\varphi_F = -V_T \ln(\frac{N_d}{n_i}), \varphi_b = \frac{E_g}{2} + V_T \ln(\frac{N_d}{n_i}), V_P = \varphi_b - \frac{qN_dW^2}{8\varepsilon_{si}}$$

where, t_{si} is the silicon film thickness, V_T is the thermal voltage, W is the width of the transistor, t_{ox1} is the top oxide thickness, t_{ox2} is the buried oxide thickness, E_g is the silicon energy bandgap, N_d is the donor concentration in the body, n_i is the intrinsic carrier concentration, ε_{si} is the permittivity of silicon, and ε_{ox} is the permittivity of silicon oxide.

The onset voltage of inversion and accumulation for the bottom-gates, V_{BG}^{inv} and V_{BG}^{acc}, are shown below,

$$V_{BG}^{inv} = V_{FB2} + (1+\alpha\frac{C_{JG}}{C_{ox2}})2\varphi_F - (\gamma-\alpha)\frac{C_{JG}}{C_{ox2}}(V_P) + (1+\gamma\frac{C_{JG}}{C_{ox2}})V_{JG} \quad (1)$$

$$V_{BG}^{acc} = V_{FB2} + (\gamma-\alpha)\frac{C_{JG}}{C_{ox2}}(V_{JG}-V_P) \quad (2)$$

The bottom-gate may be inverted, depleted, or accumulated. When it is in inversion i.e. $V_{BG} < V_{BG}^{inv}$,

$$V_{TH} = V_{FB1} - \gamma(\frac{C_{JG}}{C_{ox1}})(2\varphi_F + V_P) - \alpha(\frac{C_{JG}}{C_{ox1}})(V_{JG}-V_P) \quad (3)$$

When the bottom-gate is depleted i.e. $V_{BG}^{inv} < V_{BG} < V_{BG}^{acc}$,

$$V_{TH} = V_{FB1} - \beta(V_{BG}-V_{FB2}) + (\gamma-\alpha)(\frac{C_{JG}}{C_{ox1}} + \beta\frac{C_{JG}}{C_{ox1}})(V_{JG}-V_P) \quad (4)$$

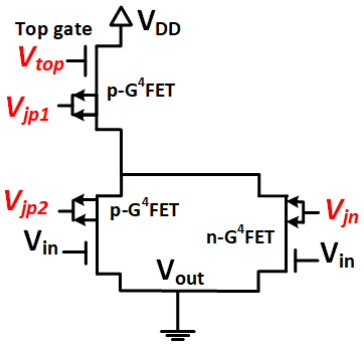
When the bottom-gate is in accumulation i.e. $V_{BG} > V_{BG}^{acc}$,

$$V_{TH} = V_{FB1} + (\gamma-\alpha)(\frac{C_{JG}}{C_{ox1}})(V_{JG}-V_P) \quad (5)$$

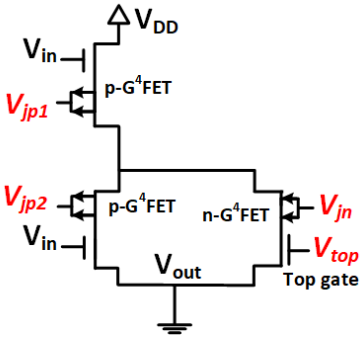
Here, the flat band voltages of the top gate and the bottom gates are represented by V_{FB1} and V_{FB2}, respectively. Based on the above relationships among different gates, a G^{4}FET macromodel is developed in [22]. All of our circuit results are generated in the Cadence Spectre simulator using this model.

A. CHAOTIC MAP

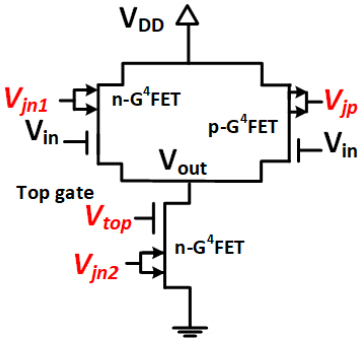
Figure. 3 shows three different proposed topologies that can be used as chaotic maps. Table 1 gives the aspect ratios (W/L) of the constituent *p*-channel and *n*-channel G^{4}FET transistors in each topology. Both topologies-I and II consist of three SOI four-gate transistors, two of which are *p*-channel G^{4}FETs while the third one is a *n*-channel G^{4}FET. Topology-III on the other hand constitutes of two *n*-channel G^{4}FETs and one *p*-channel G^{4}FET. For all three G^{4}FETs in each topology, the bottom gates are grounded, and both junction gates are shorted. Figure.5 - Figure.7 shows the four transfer curves for each of the three topologies corresponding to the four control parameters. Transistor sizing has been carefully chosen to get an approximate inverted V-shaped curve from $Topology-I$ and $Topology-II$ and an approximate V-shaped transfer curve from $Topology-III$ as we know from Feigenbaum's research [25] that any differentiable uni-modal characteristic has the potential to generate chaos. It can be seen from the figures. 5(b), 6(b), and 7(a) that there is minimal change in the transfer curve, this is because the junction gates cannot modulate the channel effectively because of the larger width of the corresponding *p*-channel or *n*-channel G^{4}FET.



(a) Topology-I



(b) Topology-II



(c) Topology-III

FIGURE 3. G^{4}FET-based chaotic maps (GCM).

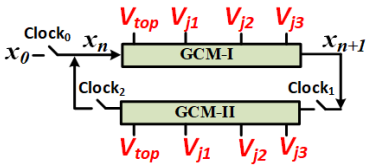
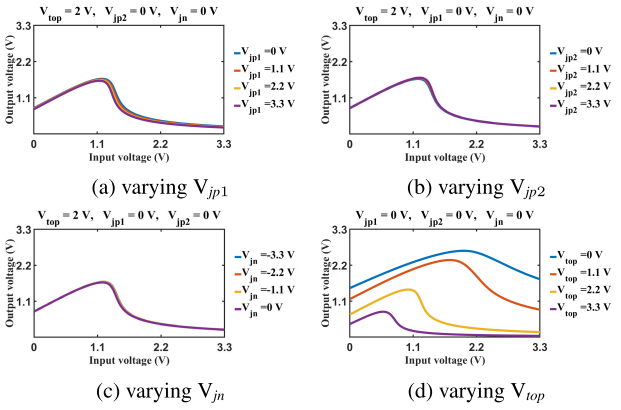


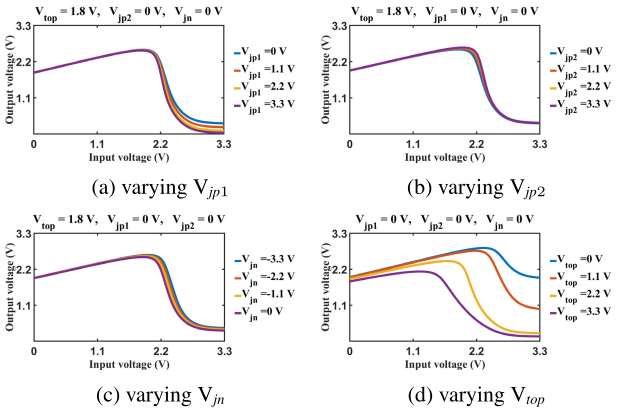
FIGURE 4. GCM-based chaotic oscillator.



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 5. Transfer curve of Topology-I.



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 6. Transfer curve of Topology-II.

B. CHAOTIC OSCILLATOR

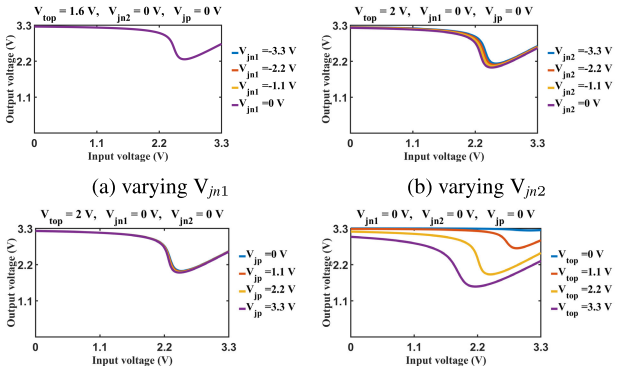
Our proposed chaotic oscillator is designed by connecting two G^{4}FET-based chaotic maps or GCM back to back in a feedback loop as seen in Figure. 4. V_{top}, V_{j1}, V_{j2}, V_{j3} are the four control parameters of the chaotic maps. The initial state, x_0, is applied to the oscillator by $Clock_0$. At every iteration, an input voltage, x_n, passes through GCM-I in the forward path and generates the output, x_{n+1}. To reduce the hardware cost, the use of capacitors for the sample and hold operation was forgone. Instead, the two non-overlapping clocks $Clock_1$ and $Clock_2$ help in the sample operation and dictates the oscillator operation. The gate capacitance of GCM-II, on the other hand, helps in the hold operation. The output, x_{n+2}, from the feedback path is then fed back to GCM-I as the input for the next iteration. During every clock cycle, we sample two outputs, x_{n+1} and x_{n+2}. GCM-I and GCM-II can correspond to any of the topologies discussed in this paper.

III. PERFORMANCE ANALYSIS

The chaotic behavior of our proposed maps is examined in three ways: i) visual illustration using bifurcation plots, ii) chaotic entropy assessment using three established entropy measures: Lyapunov exponent (LE), Correlation Coefficient, and Shannon Entropy, iii) evaluation utilizing the stability analysis of fixed points.

A. BIFURCATION PLOT

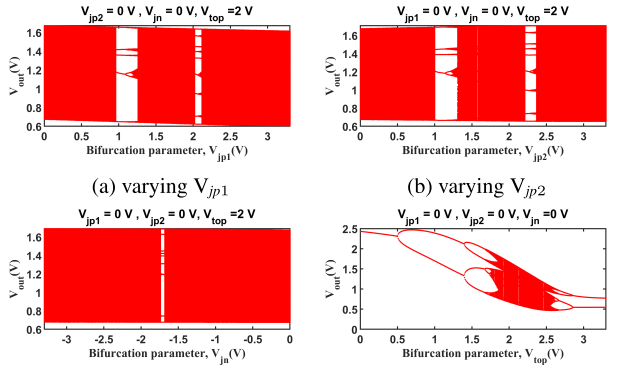
We utilized bifurcation plots to visually demonstrate the chaotic behavior exhibited by our proposed maps. These types of plots are employed to visually demonstrated the transformation of a system with the change of the control parameter, from periodic region to period-doubling or bifurcation to eventually regions of chaos. In Figure.8- Figure.10,



(a) varying V_{jn1} (b) varying V_{jn2}

(c) varying V_{jp} (d) varying V_{top}

FIGURE 7. Transfer curve of Topology-III.



(a) varying V_{jp1} (b) varying V_{jp2}

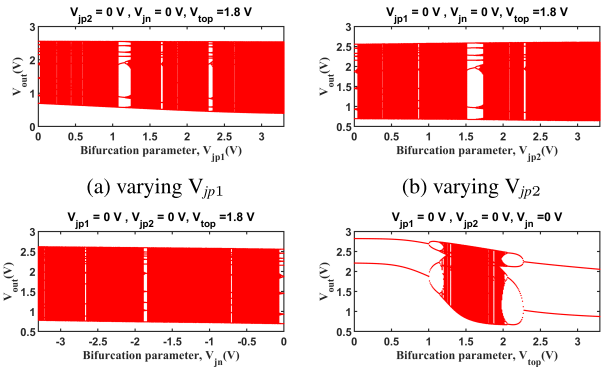
(c) varying V_{jn} (d) varying V_{top}

FIGURE 8. Bifurcation of Topology-I.

we present the bifurcation plots for all three topologies. Starting with Figure. 8, it shows the bifurcation plots of Topology-I, showcasing four independent bifurcation parameters as illustrated in Figure. 3 (a): V_{jp1}, V_{jp2}, V_{jn}, and V_{top}. Each of these parameters is represented in Figure. 8 (a)-(d) to illustrate the effect of changing one parameter while keeping the other three values fixed. This process is repeated for all three topologies, encompassing their respective control parameters.

For Figure. 9, the four independent parameters are V_{jp1}, V_{jp2}, V_{jn} and V_{top} as it has two p-channel and one n-channel G^{4}FET similar to Topology-I, while Figure. 10 illustrates the bifurcation plots for Topology-III that have parameters: V_{jn1}, V_{jn2}, V_{jp} and V_{top} as it has one p-channel and two n-channel G^{4}FET.

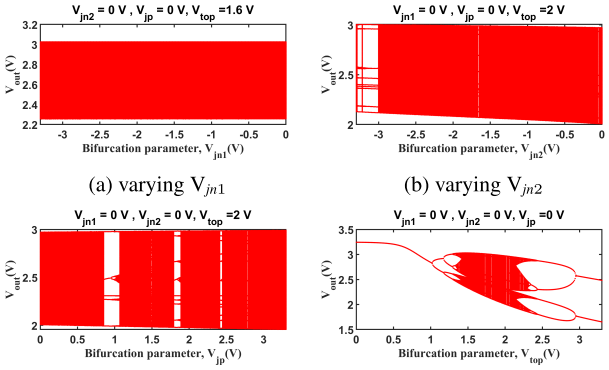
To generate these plots, a discrete-time sequence was recorded from the chaotic oscillator for 15000 iterations. The first 1000 were discarded to get the steady-state values. The remaining 14000 steady-state analog values are plotted for each of the four control/bifurcation parameters separately. The darker regions correspond to the chaotic behavior of the circuit with respect to the control parameter values. In the remaining portion of the plots, all values in the steady-state sequence either remain fixed to a single value (i.e. fixed point) or fluctuate periodically within some distinct levels (i.e. periodic orbit).



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

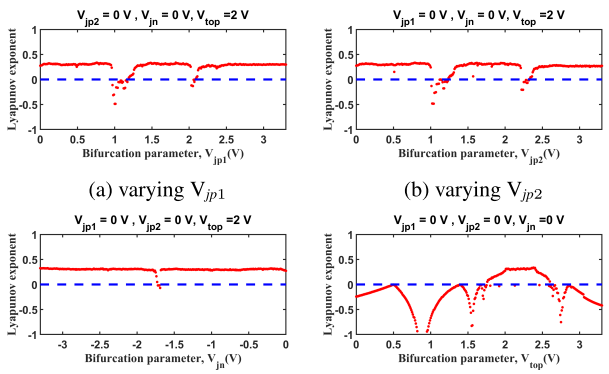
FIGURE 9. Bifurcation of Topology-II.



(a) varying V_{jn1} (b) varying V_{jn2}

(c) varying V_{jp} (d) varying V_{top}

FIGURE 10. Bifurcation for Topology-III.



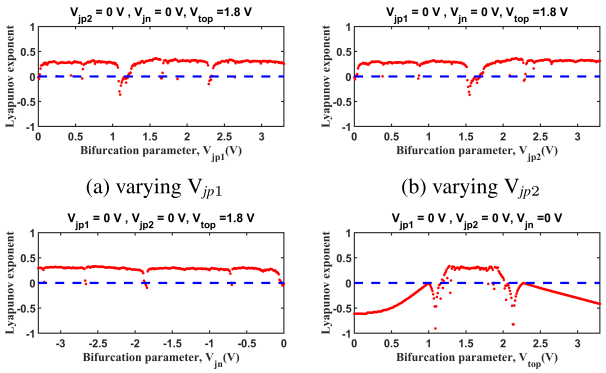
(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 11. LE of Topology-I.

B. LYAPUNOV EXPONENT

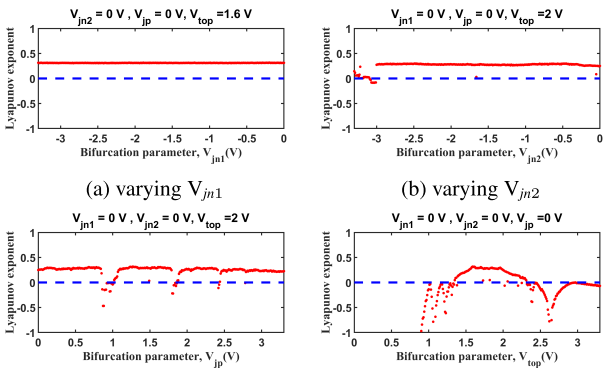
In a chaotic sequence, any two infinitesimally close trajectories, starting from two slightly different initial conditions, can diverge exponentially fast. This sensitive dependence on the initial condition can be quantified using the entropy metric called Lyapunov exponent (LE) [26]. Fixed points and periodic orbits are indicated by negative values, while the positive LE values represent the chaotic attractor. A larger positive value of LE also indicates a faster divergence of



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

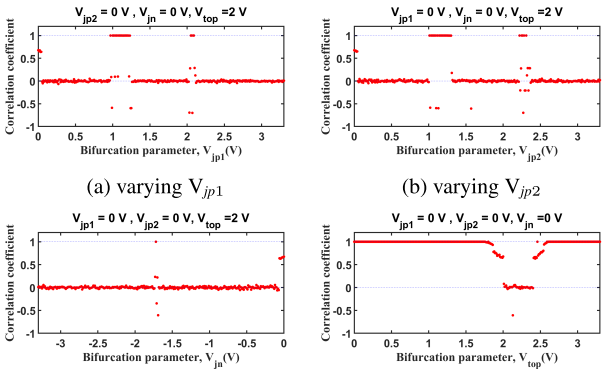
FIGURE 12. LE of Topology-II.



(a) varying V_{jn1} (b) varying V_{jn2}

(c) varying V_{jn} (d) varying V_{top}

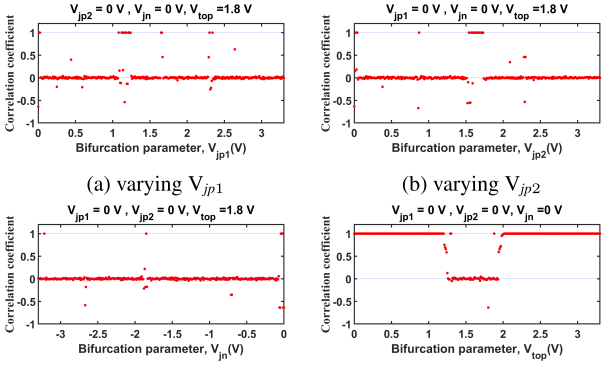
FIGURE 13. LE for Topology-III.



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 14. CC of Topology-I.



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 15. CC of Topology-II.

output trajectory.

$$\lambda = \lim_{n\to\infty} \frac{1}{n} \sum_{i=0}^{n-1} ln|f'(x_i)|. \tag{6}$$

where, LE is denoted by λ, and $f'(x_i)$ indicates the first derivative of the $i'th$ iteration of oscillator output and n is the iteration number. The higher the LE value, the more unpredictable the chaotic system is. If a nonlinear circuit is not sensitive to initial conditions, then the LE value is either zero or negative. Figure.11- Figure.13 show the corresponding LE values of each of the three topologies where for each plot, one bifurcation parameter is varied while the other three are set to a fixed value. It can be seen from the plots that the positive LE values are consistent with the dark-red region of their corresponding bifurcation plot, confirming the presence of chaos. Regions of fixed points (i.e. period of 1) and periodic orbits with 2 or more periods are characterized by negative values of LE.

C. CORRELATION COEFFICIENT

The Correlation coefficient (CC) is another widely known entropy metric used to measure the sensitivity dependence on the initial condition as well as control parameters Pearson's equation [27] to determine the correlation between two data sequences, namely X and Y, is defined as follows,

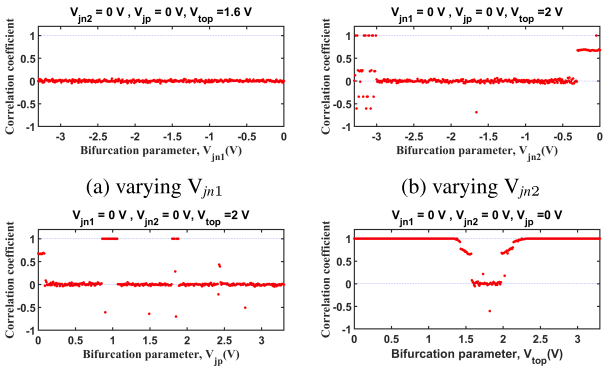
$$CC = \frac{E[(X - \mu_X)(Y - \mu_Y)]}{\sigma_X \sigma_Y} \tag{7}$$

where the expectation operator is denoted by $E[.]$. The mean value and standard deviation are represented by μ and σ, respectively. CC value close to 0 indicates extremely low or minimal correlation, whereas highly correlated data sequences give a CC value close to $+1/-1$.

Two sets of sequences were generated with two very close (1 nV apart) initial states, and everything else is kept the same. The initial state dependency is then calculated using (7) and plotted in Figure.14 - Figure.16 by varying the control parameter value (1 nV variation) while keeping everything else the same it can be seen that, in the chaotic region, even that slight initial state variation results in two almost uncorrelated sequences (CC is close to 0) which indicates strong chaotic property. However, in the periodic regions (non-chaotic regions), tiny difference in initial conditions eventually diminishes in steady-state output values, and that results in a correlation coefficient of 1.

D. SHANNON ENTROPY

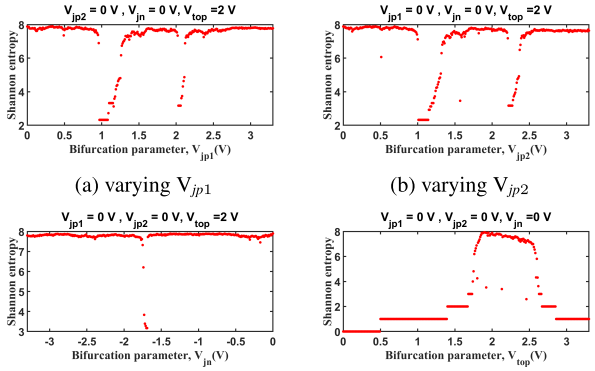
The Shannon Entropy (SE) is a popular metric utilized to measure the entropy of a random number. If we divide the signal range of X into n equal bins, SE (denoted by H) can be



(a) varying V_{jn1} (b) varying V_{jn2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 16. CC for Topology-III.



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 17. SE for Topology-I.

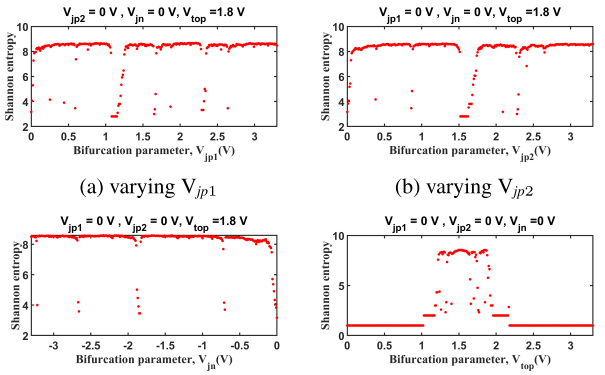
written as shown in (8) [28].

$$H(X) = -\sum_{i=1}^{n} Pr(x_i) log_2 Pr(x_i) \tag{8}$$

Here, $Pr(x_i)$ is the probability of signal value residing in the i^{th} bin. We set n to 1024 ($n = 2^{10} = 1024$) and collected 10,000 data points for each V_c. Then Eq. (8) was used to calculate the SE for each control parameter. The theoretical maximum value is $log_2 n = log_2 1024 = 10$, which occurs when the distribution is perfectly uniform. The value of SE increases with an increase in the amount of ergodicity involved in the data sequence. The corresponding SE results for each of the bifurcation parameters of all three topologies are shown in Figure.17- Figure.19. Higher SE values corresponding to chaotic regions can be noted in the figures, whereas values close to 0 mark the non-chaotic region.

E. STABILITY ANALYSIS

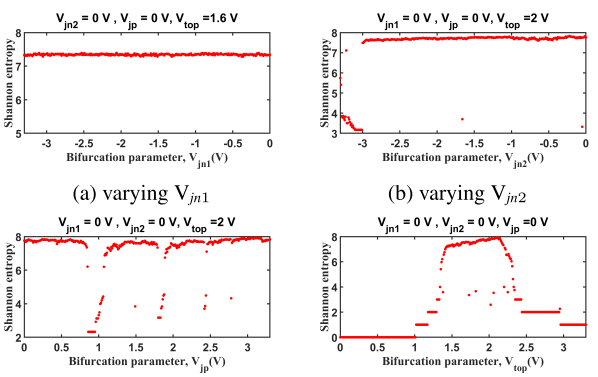
In addition to utilizing bifurcation plots and traditional chaotic entropy measurements such as the Lyapunov Exponent, Correlation Coefficient, and Shannon Entropy, another approach to examine the chaotic behavior of a non-linear circuit is by analyzing the stability. Fixed points refer to those points where the next state (X_{n+1}) of the map circuit is equal to the present state (X_n). In Figure. 20, the fixed points are



(a) varying V_{jp1} (b) varying V_{jp2}

(c) varying V_{jn} (d) varying V_{top}

FIGURE 18. SE for Topology-II.



(a) varying V_{jn1} (b) varying V_{jn2}

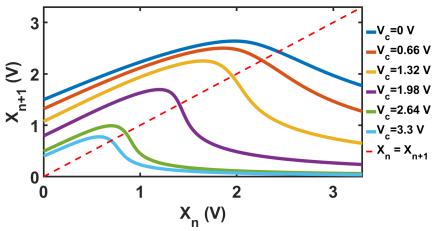
(c) varying V_{jp} (d) varying V_{top}

FIGURE 19. SE for Topology-III.

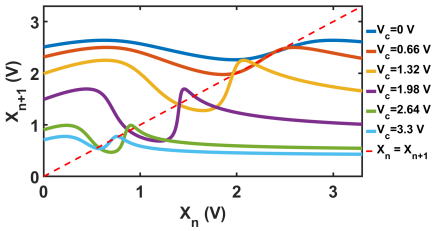
represented by the intersection points of each transfer curve with the red dashed lines. The stability of a fixed point can be determined by examining the slope of the intersection between the transfer curve and the line $X_n = X_{n+1}$. If the slope is greater than 1, then the fixed point is considered unstable [26], [29].

Figure. 21 illustrates the bifurcation plot of Topology-I (varying V_{top}) with its corresponding slope of the transfer curve. In this plot, we can observe the presence of fixed points within specific ranges of control voltage (V_c) values. For instance, there are fixed points between 0 V and V_c = 0.5 V, a period of 2 between $V_c = 0.5$ V and $V_c = 1.39$ V, and another period of 2 between $V_c = 2.86$ V and $V_c = 3.3$ V, and so on. The bifurcation plot provides insight into the existence of fixed points for different values of V_c. It is important to note that the iterated sequence value (X_n) does not remain fixed at a single point for the entire V_c range, despite the intersections shown in Figure. 20(a). This occurs because not all fixed points are stable. Only the fixed points that are stable are visible as a fixed level in the bifurcation plot.

In the bottom plot of Figure. 21, we can observe the slopes of the transfer curves at the intersection point. The plot indicates that the slope is less than 1 (which is the condition for a stable fixed point) for values of V_c between 0 V and 0.5 V. This range precisely corresponds to the region of fixed points in the bifurcation plot.



(a) Single



(b) Cascade

FIGURE 20. Transfer Characteristics of Topology-I varying V_{top}.

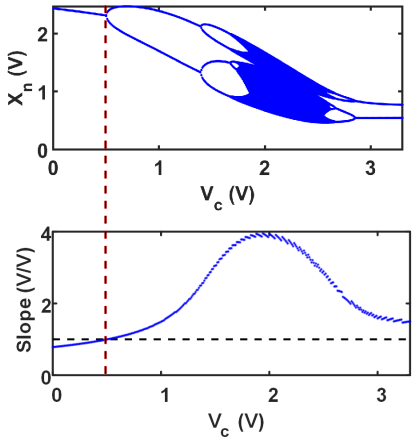


FIGURE 21. Bifurcation (top) and slope (bottom) of the transfer curves at the intersection between the transfer curves and $X_n = X_{n+1}$ - line of the chaotic map.

Figure. 22 depicts the bifurcation plot along with the calculated slopes at the intersection points in the case of cascaded maps. This is achieved by cascading the same two maps in series where one map's output goes into the second map's input. A comparison between the bifurcation plots of Figure. 21 and Figure. 22 shows that when cascading two maps, the even-numbered periods observed in the single case are halved. For instance, the regions that correspond to a period of 2 in the single case are now represented as fixed points in the cascaded bifurcation plot.

Therefore, to determine the positions of regions with a period of 2 in the original single map, we can examine the intersection between the transfer curve of the cascaded map (shown in Figure. 20(b)) and the line $X_n = X_{n+1}$. The slope at these intersections is illustrated in the bottom plot of Figure. 22. By analyzing the plot, regions with a period greater than 2 can be identified, as they correspond

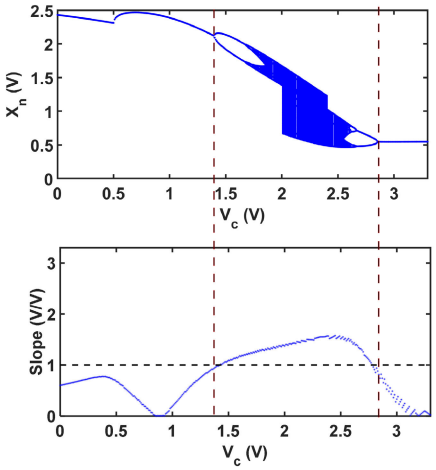


FIGURE 22. Bifurcation (top) of the cascade configuration and slope (bottom) of the cascade transfer curves at the intersection between the cascaded transfer curves and $X_n = X_{n+1}$ - line of the chaotic map.

to slopes greater than 1. Similar trends are also observed in the Figures.25 (d) and (h).

Figure. 23 to Figure. 25 demonstrates the slope profiles at the intersections between the transfer curves and $X_n = X_{n+1}$ -line for each of the three proposed topologies, along with their corresponding bifurcation plots. The slope profiles indicate that the slopes are greater than 1 for the entire range of the control voltage V_c (except for cases with Varying V_{top}), suggesting the absence of fixed regions or periods of 2 in the bifurcation plots, which is further confirmed by their corresponding bifurcation plots.

IV. APPLICATION: RECONFIGURABLE LOGIC GATE

Based on our proposed chaotic oscillator, we are demonstrating the operation of a 2-input reconfigurable logic gate. Figure. 26 shows the schematic of the chaos-based logic generator scheme. To enhance the design space, we employ a 3-bit padding sequence, P_s $[P_2\ P_1\ P_0]$, which is concatenated with the 2-bit data bus, $[I_A\ I_B]$, resulting in a 5-bit input. It is important to note that this approach can be adapted for any desired number of inputs. This digital signal is then converted to analog by a digital-to-analog converter (DAC) and used as seed value (x_0) for the chaotic oscillator. The analog domain from 0 V to 1 V is quantized into 32 (i.e. 2^5) voltage levels. The control voltage that acts as the bifurcation parameter determines whether the generated sequence will exhibit chaotic behavior. The oscillator's output is then compared against a reference voltage,V_{ref}, to get the digital 1/0 output. Any analog voltage that is greater than V_{ref} is equal to a binary value of 1, otherwise, it is assigned a binary value of 0. The digital conversion is done using the following equation:

$$Output_n = \begin{cases} 1, & \text{if } x_n > V_{ref} \\ 0, & \text{otherwise.} \end{cases} \tag{9}$$

The number of possible functions for an n-input logic gate is 2^{2^n}. Thus, there are a total of 16 possible functions

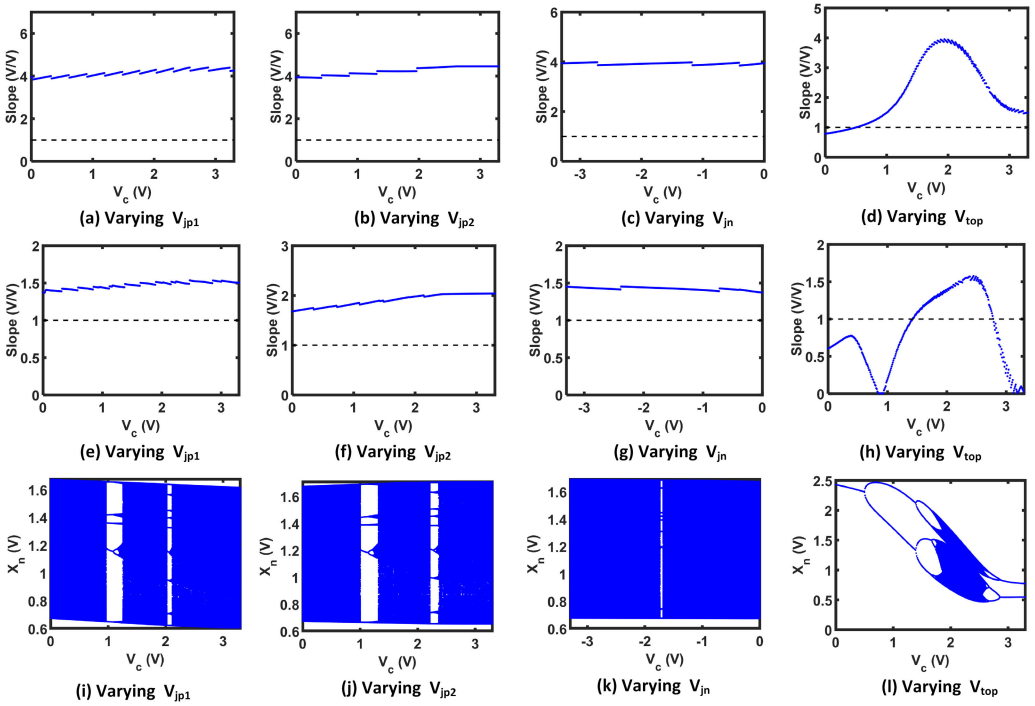


FIGURE 23. Slopes of Topology-I transfer curves at the intersections between the transfer curves and $X_n = X_{n+1}$ - line: (a-d) Single map; (e-h) Cascade of two maps; (i-l) Corresponding bifurcation plots of the single maps.

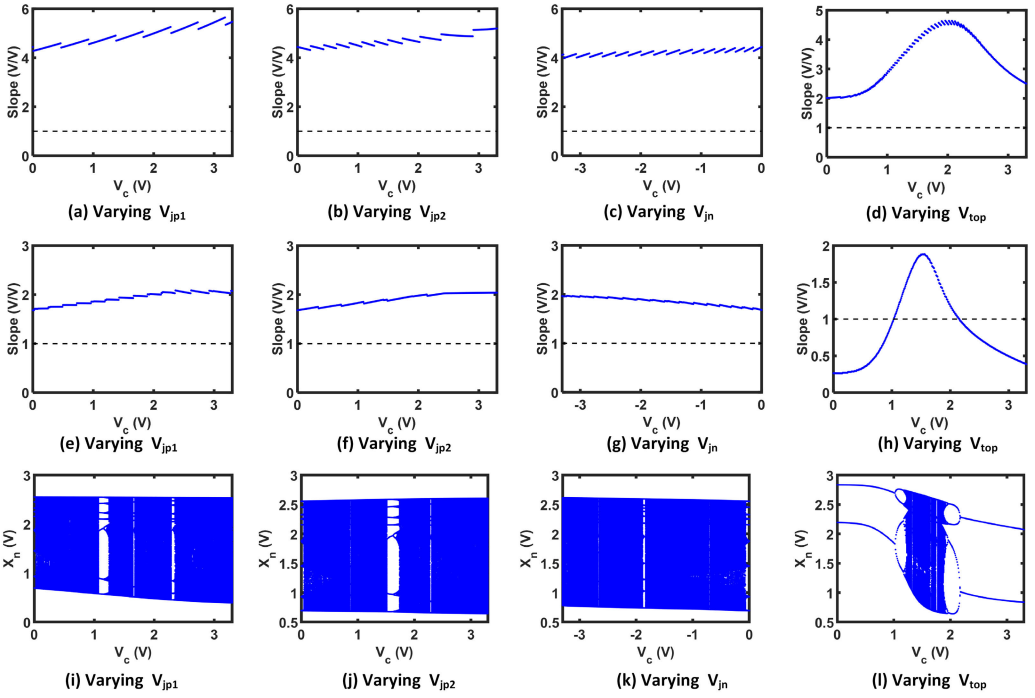


FIGURE 24. Slopes of Topology-II transfer curves at the intersections between the transfer curves and $X_n = X_{n+1}$ - line: (a-d) Single map; (e-h) Cascade of two maps; (i-l) Corresponding bifurcation plots of the single maps.

for a 2-bit digital input. These functions are numbered in decimal, starting from 0 (0000) to 15 (1111). Among these 16 functions, some numbers correspond to well-known logic operations. For example, AND, NAND, OR, and NOR are represented by '0001', '1110', '0111', and '1000', respectively. The advantage of our approach is that all sixteen of these 2-input functions can be generated using a single chaotic logic circuit, resulting in a highly reconfigurable

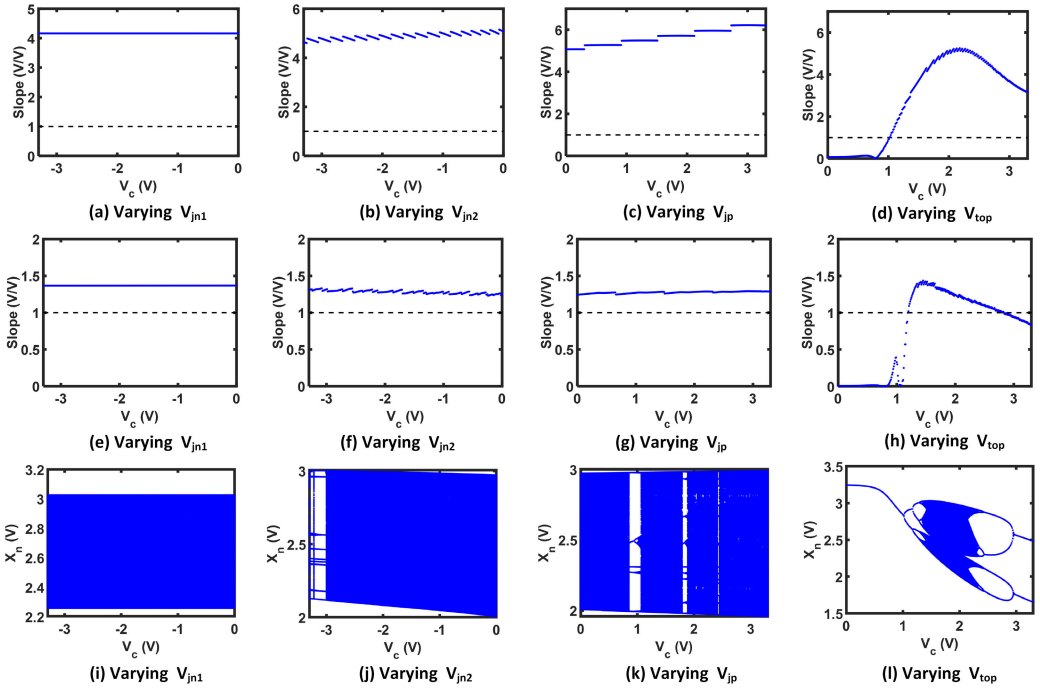


FIGURE 25. Slopes of Topology-III transfer curves at the intersections between the transfer curves and $X_n = X_{n+1}$ - line: (a-d) Single map; (e-h) Cascade of two maps; (i-l) Corresponding bifurcation plots of the single maps.

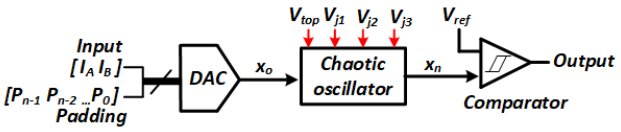


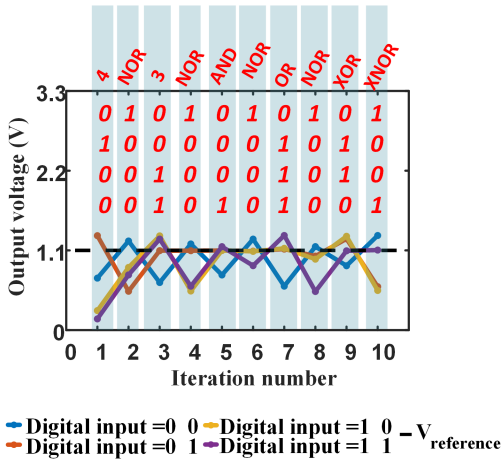
FIGURE 26. G^{4}FET-based logic generator circuit.

system. This is an important feature as the reconfigurability of chaotic circuits can lead to obfuscation against power profile-based side channel attack [30]. This sets them apart from the conventional CMOS-based logic gates where each operation has a distinct power signature and can be distinguished from each other [31].

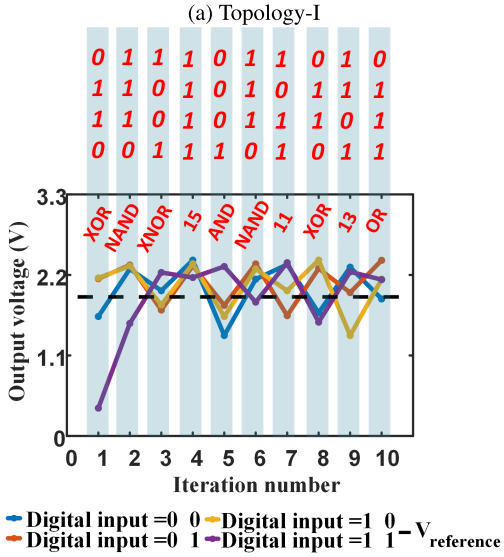
Figure. 28 shows the evolution of the analog output voltage across the first ten iterations for all three topologies. For this figure, the configuration parameters are as follows, a) $V_{\text{top}} = 2.26\ V, V_{\text{jp1}} = 0\ V, V_{\text{jp2}} = 0\ V, V_{\text{jn}} = 0V$, P_s = '001', V_ref = 1.10 V; b) $V_{\text{top}} = 1.67\ V, V_{\text{jp1}} = 0\ V, V_{\text{jp2}} = 0\ V, V_{\text{jn}} = 0V$, P_s = '101', V_ref = 1.90 V; c) $V_{\text{top}} = 2.06\ V, V_{\text{jn1}} = 0\ V, V_{\text{jn2}} = 0\ V, V_{\text{jp}} = 0V$, P_s = '101', V_ref = 2.20 V. At each iteration, we get a particular logic operation, as can be seen from the figure. The same logic function can be implemented using multiple configuration settings making the logic gate flexible. For example, Figure. 27 (a) shows four NOR operations, at the 2$^{\text{nd}}$ iteration, 4$^{\text{th}}$ iteration, 6 $^{\text{th}}$ iteration, and another at the 8$^{\text{th}}$ iteration. For these four NOR operations, the configuration setting differs only in their iteration number. Thus, The logic functionality can also be altered by changing any of the seven parameters: V_{top}, V_{j1}, V_{j2}, V_{j3}, V_{ref}, P_s, or the iteration number. We have introduced a new metric called the Reconfigurable Parameter Count (RPC), which captures the number of unique parameter counts possible with this reconfigurable circuit. It can be defined as follows:

$$RPC(n) = 2^l \times EPS \times n \times N_{v_{ref}}, \tag{10}$$

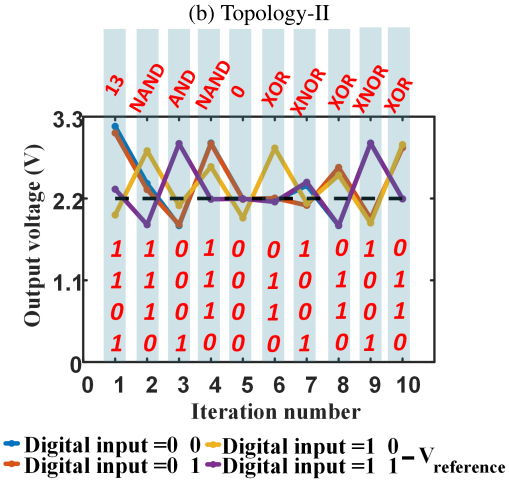
If a system has p parameters and each parameter can have N distinct values, then the Entire Parameter Space (EPS) can be defined as $EPS = N^p$ [32]. $N_{v_{ref}}$ is the total number of comparator reference voltage levels, l is the total number of control bits in the padding sequence, and n is the iteration number. The comparison of RPC between our work to two published works [33], and, [2], is shown in Figure. 28. The comparison also includes 2-D and 3-D maps, where the constituent maps have six and nine control parameters, respectively. The 2-D and 3-D scheme has been discussed in detail in the next section. It is highly desirable to have a large RPC for obfuscation application, as multiple reliable configurations can be chosen for implementing a single function which ensures the security of chaos-based computing systems against power analysis-based side channel attacks [30], [34]. Our proposed design requires only a few iterations to achieve a very large RPC, which is a result of multiple control parameters introduced in this design. The number of individual functions such as AND, OR, XOR, NAND, NOR, and XNOR also increases with the increase in design space. The increase in individual RPC of six of the sixteen possible logic for all three topologies is also shown in Figure. 29. To plot this figure, we are taking control parameter values only over the



(a) Topology-I



(b) Topology-II



(c) Topology-III

FIGURE 27. Evolution of analog chaotic output voltage for first ten iterations. Each iteration corresponds to one logic operation.

chaotic range and keeping the range of V_{ref} between 0 V to 3.28 V, taking about 64 values. The number of the existence of different functions varies, but it is possible to obtain

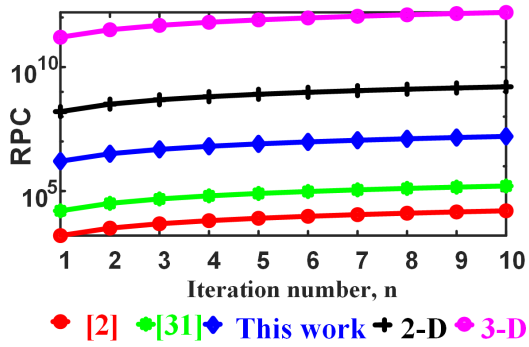
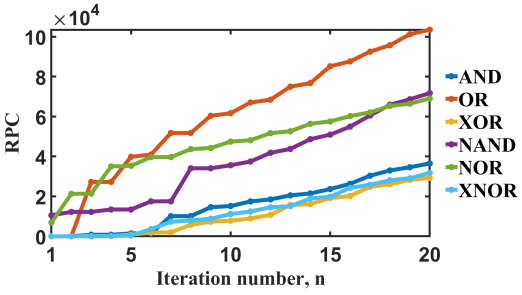
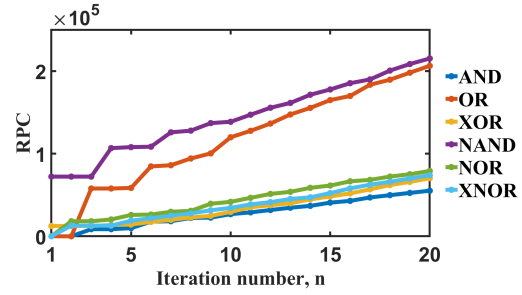


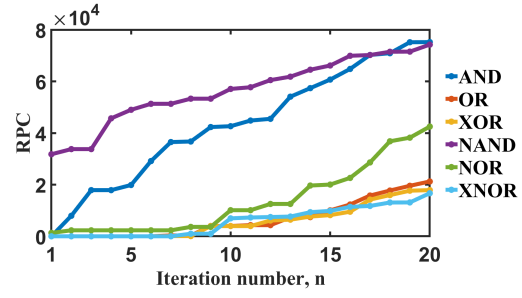
FIGURE 28. Comparison of Reconfigurable Parameter Count between published works, our proposed work, and the multi-dimensional extensions.



(a) Topology-I



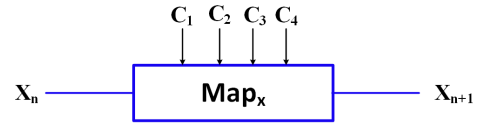
(b) Topology-II



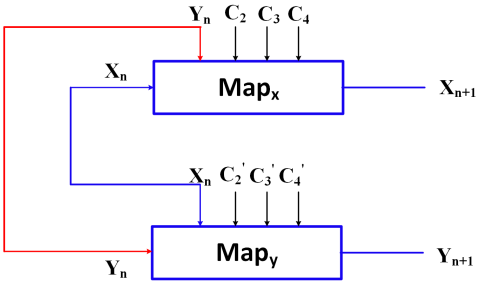
(c) Topology-III

FIGURE 29. Change of individual Reconfigurable Parameter Count of six logic functions with iteration.

all the functions by changing the control parameters of the logic gate. This flexibility of implementing a single function with a large number of distinct configurations is highly desirable as it ensures improvement in security applications such as Physically Unclonable Functions (PUF) [35] and logic obfuscation [36].



(a) Current 1-D G^{4}FET map with four control parameters



(b) Combining 2 different 1-D maps to create a 2D map with six control parameters

FIGURE 30. General Framework of 2-D chaotic map.

V. EXTENSION OF MULTI-DIMENSIONAL MAPS

The G^{4}FET device, with its four available control parameters, presents an opportunity to expand the design space and venture into multi-dimensional chaotic oscillators. By leveraging these parameters, we can extend one-dimensional maps into multi-dimensional maps. To illustrate this concept, we present 2-D and 3-D schemes which offer greater flexibility and potential for various security applications.

Higher dimensionality of mapping does introduce more complexity, however, it is important to note that complexity is not always detrimental. In certain applications, higher complexity is desirable as it can yield significant improvements in terms of security. For instance, higher dimensional chaotic maps have shown remarkable effectiveness in secure communication by performing better than existing 1D chaotic maps in terms of resisting transmission noise [37], [38]. Leveraging this higher dimensionality not only enhances the key space but also enables secure transmission of audio signals, making it particularly advantageous in audio encryption [39], [40]. Furthermore, in terms of image encryption, the enhancement in key space bolsters resilience against common attacks [41], [42]. In these cases, embracing higher dimensionality proves highly beneficial, as it allows secure communication, enhances audio encryption, and increases the protection of images against common threats.

The ideal outcome is to attain the full range of dynamic complexities exhibited by a higher-order map while keeping the hardware overhead to a minimum. In this case, our simple construction leveraging the unique multi-gate characteristics of G^{4}FET holds tremendous potential.

A. 2-D MAP

Figure. 12 illustrates the 2-D scheme, which builds on the foundation of 1-D chaotic maps by introducing additional control parameters to create more complex chaotic behavior.

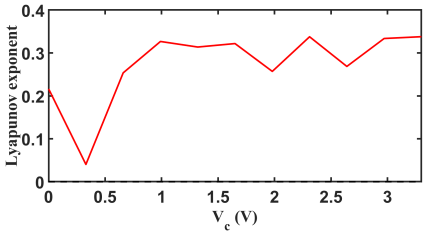


FIGURE 31. LE plot for 2-D scheme.

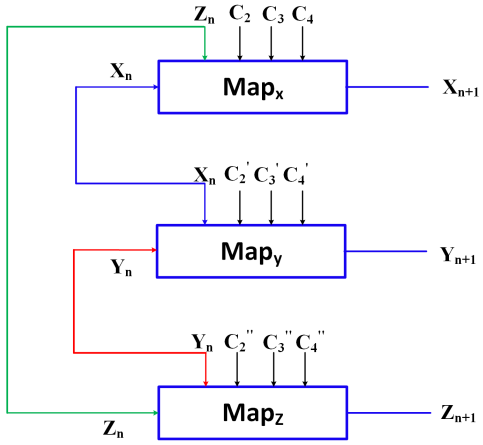


FIGURE 32. General Framework of 3-D chaotic map.

In this design, the input X_n controls Map_Y, while Y_n serves as one of the controls for Map_X. Although Figure. 12 uses $Topology - I$ for Map_X and $Topology - II$ for Map_Y, any combination of the three proposed topologies can be utilized.

In the case of Map_X, the control parameters are assigned as follows: $C_1 = Y_n = V_{jp1}$, $C_2 = V_{jp2}$, $C_3 = V_{top}$, and $C_4 = V_{jn}$. For Map_Y, the control parameters are designated as: $C_1' = X_n = V_{jp2}$, $C_2' = V_{top}$, $C_3' = V_{jp1}$, and $C_4' = V_{jn}$. As a result, each variable modulates its respective map as well as the other map. The 2-D map contains a total of six control parameters: $C_2, C_3, C_4, C_2', C_3'$, and C_4'. However, in our specific case, we consider C_3, C_4, C_3', and C_4' as constant values.

The 2-D Lyapunov Exponent plot is depicted in Figure. 31 and it demonstrates that our proposed 2-D scheme produces robust chaos with increased chaotic complexity. As a result, our system offers enhanced security. Robust chaotic behavior is a desirable characteristic in chaotic systems, as it finds applications in various security domains such as robust random number generation and chaos-based logic [17], [19], [43], [44], [45].

$$X_{n+1} = Map_X(X_n, Y_n, C_2, C_3, C_4), \tag{11}$$

$$Y_{n+1} = Map_Y(Y_n, X_n, C_2', C_3', C_4') \tag{12}$$

B. 3-D MAP

Another possibility for enhancing the design space is by exploring a 3-D scheme, as shown in Figure. 32. This scheme incorporates all three maps: Map_X, Map_Y, and Map_Z, with

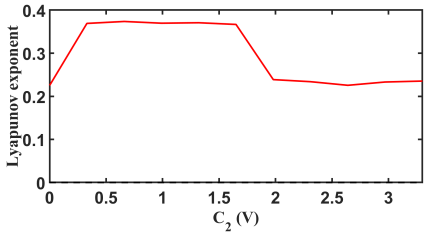


FIGURE 33. LE plot for 3-D scheme.

Topology − *I*, *Topology* − *II*, and *Topology* − *III* assigned to each map, respectively. In the case of Map_X, the control parameters are defined as follows: $C_1 = Z_n = V_{jp1}$, $C_2 = V_{jp2}$, $C_3 = V_{top}$, and $C_4 = V_{jn}$. For Map_Y, the control parameters are: $C_1' = X_n = V_{jp2}$, $C_2' = V_{top}$, $C_3' = V_{jp1}$, and $C_4 = V_{jn}$. Finally, for Map_Z, the control parameters are: $C_1'' = Y_n = V_{jp}$, $C_2'' = V_{top}$, $C_3'' = V_{jn1}$, and $C_4'' = V_{jn2}$. The corresponding equations (13), (14), and (15) for each map are also shown.

This 3-D scheme allows us to utilize all three proposed topologies, providing increased flexibility in our design. As a result, we now have nine control parameters ($C_2, C_3, C_4, C_2', C_3', C_4', C_2'', C_3''$, and C_4'') instead of the four, significantly expanding the design possibilities. The Lyapunov Exponent (LE) plot of our 3-D scheme is depicted in Figure 33, consistently exhibiting positive LE values over the whole operating range, which indicates robust chaotic behavior.

$$X_{n+1} = Map_X(X_n, Z_n, C_2, C_3, C_4), \tag{13}$$
$$Y_{n+1} = Map_Y(Y_n, X_n, C_2', C_3', C_4') \tag{14}$$
$$Z_{n+1} = Map_Z(Z_n, Y_n, C_2'', C_3'', C_4'') \tag{15}$$

One potential direction for future research is to keep the junction gates independent while including the bottom gates as additional control parameters. This approach would allow for a more extensive exploration of the design space, offering even greater flexibility in the behavior of the system.

In the 2-D scheme, by incorporating the bottom gates as control parameters while keeping the junction gates independent, the number of control parameters can be expanded to 18, if desired. This significant increase in control parameters would provide researchers with a broader range of options to tailor the chaotic behavior of the system to their requirements and explore its potential applications.

Similarly, in the 3-D scheme, including the bottom gates as control parameters along with the junction gates would extend the number of control parameters to 27. This substantial increase in parameter space would unlock new opportunities for designers by increasing functionality as well as flexibility.

VI. CONCLUSION

In this paper, three simple nonlinear G^4FET-based chaotic map circuits are introduced. The elegance of each design is that they offer four independent bifurcation parameters with a simple nonlinear circuit consisting of only 3 SOI transistors. The chaotic map is employed in a chaotic oscillator design. The chaotic behavior of the oscillator is analyzed using bifurcation plots, Lyapunov exponent, correlation coefficient, Shannon Entropy, and Stability analysis. The application of the proposed chaotic oscillator is demonstrated in a reconfigurable logic gate. Extension schemes such as 2-D and 3-D expansion for developing multi-dimensional chaotic map is presented. Potential future work is also discussed along with enhancement in Reconfigurable Parameter Count.

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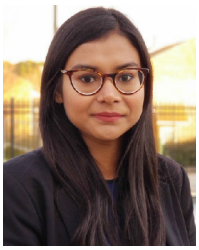

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