

RESEARCH ARTICLE

Experimental Demonstration of Approximate Communication Based on Radio-Over-Fiber Systems

TOSHIKI ISHIMARU¹, TAKATOMO MIHANA¹,
MICHIHIRO KOIBUCHI², (Senior Member, IEEE),
TETSUYA KAWANISHI³, (Fellow, IEEE), AND MAKOTO NARUSE¹

¹Department of Information Physics and Computing, Graduate School of Information Science and Technology, The University of Tokyo, Tokyo 113-8656, Japan

²National Institute of Informatics, Chiyoda-ku, Tokyo 101-8430, Japan

³Department of Electronic and Physical Systems, Faculty of Science and Engineering, Waseda University, Tokyo 169-8555, Japan

Corresponding authors: Toshiki Ishimaru (gregor-samsa501@g.ecc.u-tokyo.ac.jp) and Takatomo Mihana (takatomo_mihana@ipc.i.u-tokyo.ac.jp)

This work was supported in part by Grant-in-Aid for Scientific Research under Grant JP20H00233, and in part by the Transformative Research funded by the Japan Society for the Promotion of Science under Grant JP22H05197.

ABSTRACT The importance of multi-valued data transmission for improving communication throughput has become apparent with the explosive growth of communication and computing demands. Although modulation schemes with denser constellations can provide increased data rates, they require a higher signal-to-noise ratio. On the other hand, sparser constellation formats offer reliable communication thanks to their greater tolerance to noise, but the throughput is inferior to that with denser constellations. Here, we introduce an approximate computing/communication that involves the critical notion of quality of information to tolerate the trade-off between throughput and reliability, which will be important in future high-performance optical communications and interconnects. In this study, we experimentally demonstrate a dynamically configured transmission scheme where different modulation formats are adopted according to the importance of bit sequences on the basis of Radio-over-Fiber (RoF) systems in transmitting floating-point numbers. The proposed system demonstrated an increased gross throughput of at least 25.1%, while errors in the transmitted floating-point numbers were uniformly bounded.

INDEX TERMS Approximate computing, approximate network, digital modulation, floating-point number, optical interconnection, Radio-over-Fiber.

I. INTRODUCTION

A. BACKGROUND AND OVERVIEW OF THE PAPER

Digital communication systems are susceptible to non-deterministic bit flips. However, current standards and protocols for digital communication systems, at least those for wired ones, require almost error-free data transfer. For example, IEEE Standard 802.3 [1] requires a mean bit error rate (BER) at the physical layer service less than or equal to 10^{-8} . Reducing bit flips may require additional signal/bit processing and consume more energy, which can negatively

The associate editor coordinating the review of this manuscript and approving it for publication was Yogendra Kumar Prajapati¹.

impact other performance metrics such as throughput. For example, forward error correction (FEC) adds redundant bits to the data bits in order to detect and correct bit flips, which often results in increased latency [2]. Another issue is related to linear modulation schemes [3]. Although those with denser constellations offer greater throughput, they require higher transmission energy to achieve a low bit error rate and tolerate the stringent signal-to-noise ratio [3], [4].

The idea of approximate computing [5] relaxes such rigid requirements for error-free data transfer and is suitable for applications that can tolerate errors. Recent studies have shown that various applications can produce results of acceptable quality even in the presence of errors such as bit

flips. With this resiliency to errors, many techniques have been proposed for computing while accepting errors and approximations [5], [6], [7], [8], [9], [10]. This approach can be viewed as an exploitation of the gap between the quality of the service that the user requires and the quality that the application provides. The literature has demonstrated that approximate computing significantly enhances improved energy efficiency and computation speed [5].

When applications employ approximate computing, communication systems do not need to be error-free. In such cases, we can take advantage of the nature of linear modulation schemes to achieve higher throughputs at the expense of a higher bit error rate. The concept of quality of information becomes significant in the context of approximate computing. From the viewpoint of quality, applications demand a certain level of data accuracy. Accordingly, the error-prone communication link should also guarantee the accuracy of transmission to some extent.

In many cases, the data under study contains bit portions that have minimal impact on the overall data accuracy, while other portions are critical. For instance, floating-point numbers represent a critical example. Bit errors in the exponent of the number may lead to significant errors in the represented number, while errors in the least significant bits in the mantissa may be negligible. Consequently, we can transfer each portion of the data bits with different levels of protection from bit errors based on their sensitivity to the overall accuracy. By switching the modulation schemes bit-sequence-by-bit-sequence, we can maintain overall accuracy while increasing throughput. This unequal protection of bits is feasible because, as previously mentioned, different modulation schemes provide different bit error rates.

Against such a background, this paper experimentally demonstrates an approximate communication scheme that provides unequal protection to bit sequences, whereby several modulation formats are dynamically switched based on the information content on the basis of Radio-over-Fiber systems. The main contributions of the present work are:

- 1) Proposing a scheme with higher throughput and configurable quality of the result while the data to send are not manipulated (Sec. II)
- 2) Presenting evidence that shows that the scheme experimentally works (Sec. V).

Our investigation of the scheme conducted in the present study will pave the way toward further exploration of the ultimate optical communication and interconnect systems, when the proposed scheme enables the use of a massive multivalued modulation format with high bit error rates where the trade-off between information transmission capacity and the required signal-to-noise ratio becomes an even more serious concern, meaning that the approach of approximate communication approach significantly affects the overall system.

The remaining sections are organized as follows. The remainder of Sec. I reviews related work. Section II summarizes the proposed transmission scheme. Section III

analyses errors in floating-point numbers and throughputs. Section IV describes the experimental setup. Section V presents the results. Section VI concludes the paper.

B. RELATED WORKS

Here we review related work in the literature.

- 1) Most approximate communication techniques can be categorized into compression, relaxed synchronization, and value prediction as surveyed extensively in [6]. The present study does not exploit these conceptual aspects.
- 2) Approximation of baseband processing is relevant regarding the dynamic reconfiguration of signals [7]. However, the present study does not exploit stochastic computing [7] principles.
- 3) Data transmission over error-prone networks has been discussed in the literature [8], [9], [11]. In particular, [11] explores the impact of changing the modulation format in view of ultrafast optical networks. However, concrete designs for applications such as floating point number transmissions and experimental demonstrations of optical networks have yet to be examined.
- 4) Unequal protection of a datum has been discussed in the literature [10], [11], [12]. In particular, [10] demonstrated approximate computing by transferring important data at a high supply voltage, while transferring non-critical data at a lower supply voltage. In contrast, the present study does not involve dynamically configuring the voltage level of data transmission; instead, it reconfigures the modulation format.
- 5) Floating-point number approximation has been discussed in various contexts, including, for example, unconventional computer arithmetic [13] and reduced-precision computing [14]. As mentioned earlier, whereas ways of dynamically changing the modulation format depending on the importance of data have been examined in the literature [11], concrete implementations in the case of floating-point numbers, as well as implementations in RoF-based experimental apparatuses, have not been explored in the literature.

II. PROPOSED TRANSMISSION SCHEME

Figure 1 shows a conceptual diagram of the proposed scheme. When information is transferred over a digital communication channel, the received information may differ from the sent information. If the difference is too large, the received information cannot be considered to be the same as the sent information. An information representation typically has parts where errors during transmission lead to significant differences in the overall information (critical parts), and other parts where errors do not make much difference (non-critical parts). The scheme transmits critical parts using a reliable modulation scheme, and non-critical parts using a high-capacity modulation scheme. With this unequal protection, the overall information can be transmitted in less time with acceptable errors. To ensure acceptable

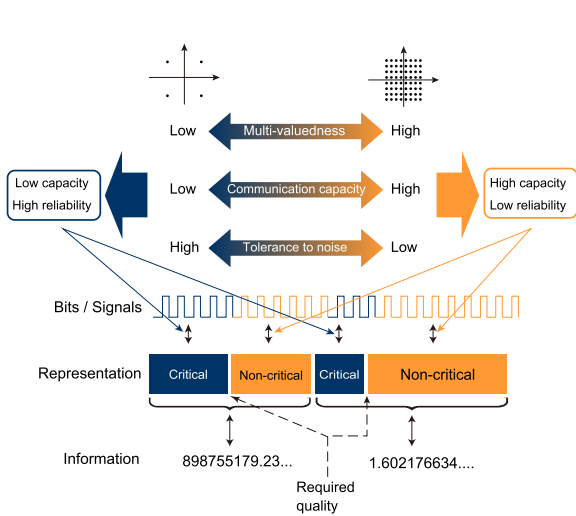


FIGURE 1. Concept of the proposed scheme. Information content is divided into critical and non-critical parts. The critical parts are handled using a high-reliability modulation scheme, while the non-critical parts are handled using a high-capacity scheme.

errors, it is important to choose where to separate critical and non-critical parts based on the information being transmitted.

The proposed scheme is designed for transmitting floating-point numbers, which approximate real numbers. The double-precision floating point format (FP64) defined in [15] consists of a sign bit, 11 bits allotted for the exponent (exponent bits), and 52 bits for the trailing significand field (also known as the fraction or the mantissa). Let $\mathbb{B} = \{0, 1\}$ and represent the sign bit as $s \in \mathbb{B}$, the bits for the exponent as $e = \{e_i\}_{i=1}^{11} \in \mathbb{B}^{11}$ and the bits for the trailing significand field as $b = \{b_i\}_{i=1}^{52} \in \mathbb{B}^{52}$. The exponent E , fraction T and the real value x assumed by a given FP64 datum are:

$$\begin{aligned}
 E &= \sum_{i=1}^{11} e_i 2^{11-i} - 1023, \\
 T &= \sum_{i=1}^{52} b_i 2^{-i}, \\
 x &= (-1)^s (1 + T) 2^E.
 \end{aligned} \tag{1}$$

The payload format in the proposed scheme, as shown in Fig. 2, follows the basic idea of [11]’s: it sends the sign, exponent, and several bits of the significand of floating-point numbers with a slower, lower-BER modulation scheme, while the remaining bits are sent with a faster, higher-BER modulation scheme. We call the former modulation scheme and its bits-symbol map “Mod 1” and the later “Mod 2”. It is important to note that the transmission scheme in the proposed approach does not modify the order of the bits in the data. This means that all 64 bits of an FP64 datum are transmitted in their original order, without any lossy compression, truncation, or reordering of bits.

We now define the Modulation Switching Point (MSP) for each FP64 datum. The MSP indicates that the first MSP bits

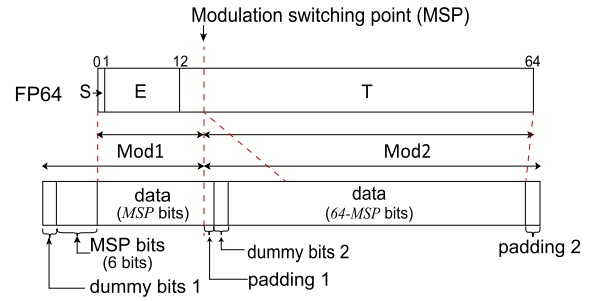


FIGURE 2. Structure of FP64 and payload format for an FP64 datum. The data is divided into two sets at the index MSP. Dummy bits and paddings are added to each set in order to eliminate the effect of modulation switching and to ensure that the bit length is an integer multiple of bits per symbol.

of an FP64 datum are mapped and modulated in Mod 1, while the next $(64 - MSP)$ bits are in Mod 2. Since the MSP may differ among FP64s, we add MSP bits (6 bits) immediately before the sign bit, which are then mapped to the symbols by Mod 1. To ensure that the bit length is an integer multiple of the bits per symbol provided by the modulation scheme and to account for the time it takes to switch between the two modulation schemes, the proposed scheme inserts dummy bits and paddings into the points where the modulation scheme changes. Specifically, it inserts “dummy bits 1” before the MSP bits and “padding 1” after the first MSP bits of the FP64 datum, which are then handled by Mod 1. For the remaining bits, the scheme adds “dummy bits 2” between “padding 1” and the last $(64 - MSP)$ bits of the FP64, and “padding 2” after the FP64 bits. Mod 2 then maps and modulates these bits. Therefore, the scheme maps and modulates dummy bits 1, MSP bits, the first MSP bits of an FP64, and padding 1 by Mod 1, while dummy bits 2, the last $(64 - MSP)$ bits of the FP64, and padding 2 are mapped and modulated by Mod 2, as shown in Fig. 2.

III. ERROR ANALYSIS

Errors in transmitted data originate from data manipulation, such as lossy compression, the transmission setup, and the characteristics of transmission channels. As stated in the previous section, we do not manipulate data during transmission. Therefore, any errors in transmission depend solely on the latter two factors.

A. ERRORS IN FLOATING-POINT NUMBERS

We will now analyze the relationship between errors in the received FP64 datum and the probability of bit errors. To begin, we define some notation. Suppose that an FP64 datum is sent through an erroneous transmission channel. The received datum has the sign bit s' , exponent bits $\{e'_1, e'_2, \dots, e'_{11}\}$, and significand bits $\{b'_1, b'_2, \dots, b'_{52}\}$. In the same way as (1), we define E' , T' , and m' as follows:

$$E' = \sum_{i=1}^{11} e'_i 2^{11-i} - 1023,$$

$$T' = \sum_{i=1}^{52} b'_i 2^{-i},$$

$$x' = (-1)^{s'} (1 + f') 2^{E'}.$$
(2)

With these notations, we can represent the absolute error between the values represented by the sent and received FP64 datum as follows:

$$|x - x'| = 2^E |(-1)^s (1 + T) - (-1)^{s'} (1 + T') 2^{E'-E}|.$$
(3)

Now we define bit masks $F \in \mathbb{B}$, $\{G_1, G_2, \dots, G_{11}\} \in \mathbb{B}^{11}$, and $\{H_1, H_2, \dots, H_{52}\} \in \mathbb{B}^{52}$ by

$$F = s \oplus s',$$

$$G_i = e_i \oplus e'_i \quad \text{for } i = 1, 2, \dots, 11,$$

$$H_i = b_i \oplus b'_i \quad \text{for } i = 1, 2, \dots, 152,$$
(4)

where \oplus is the bit-wise xor operator $\mathbb{B} \times \mathbb{B} \rightarrow \mathbb{B}$. Note that if a bit mask is 1, the corresponding bit has been flipped during the transmission. A useful property of the bit-wise xor operator would be that for any $a, b \in \mathbb{B}$, the following hold:

$$b = a \oplus (a \oplus b),$$

$$b(-1)^a = a \oplus b - a.$$
(5)

Using this property, for example, $|T - T'|$ can be written as

$$\sum_{i=1}^{52} H_i (-1)^{b_i} 2^{-i}.$$
(6)

Considering the probabilistic nature of bit errors during transmission, we can treat all the values regarding the received FP64 as random variables. This probabilistic behavior can be reduced to bit flips, which are directly represented in F , G_i , and H_i . Therefore it is enough to define the notation of the probability of $F = 1$, $G = 1$, and $H = 1$ by

$$p = \Pr(F = 1),$$

$$q = \Pr(G_i = 1) \quad \text{for } i = 1, 2, \dots, 11,$$

$$r = \Pr(H_i = 1) \quad \text{for } i = 1, 2, \dots, 52,$$
(7)

where $\Pr(X)$ denotes the probability of the event X .

For the remainder of the discussion, we assume that the sign bit does not flip; that is, $s = s'$. Equation (3) provides a trivial upper bound of the error

$$|x - x'| \leq 2^{\max\{E, E'\}}$$
(8)

If $E = E'$ we can get a tighter bound

$$|x - x'| = 2^E |T - T'|$$

$$= 2^E \left| \sum_{i=1}^{52} H_i (-1)^{b_i} 2^{-i} \right|$$

$$\leq 2^{E - \arg\max_j (H_j=1)+1}$$
(9)

B. THROUGHPUT OF THE PROPOSED SCHEME

Now we assume that we use for modulation phase shift keyings (PSKs), which represent each symbol by the phases of signals. Let Mod 1 be M_1 -PSK and Mod 2 be M_2 -PSK, and the bit length of dummy bits 1 and 2 be b_1, b_2 respectively. Then the symbol length of an FP64 datum S_f is

$$S_f = \frac{b_1 + m + 6}{\log_2 M_1} + \frac{b_2 + 64 - m}{\log_2 M_2},$$
(10)

where $m = MSP$. We write the symbol rate as S . As the number of FP64 data that can be transmitted in unit time is S/S_f , the gross throughput T_g is

$$T_g = \frac{S}{S_f} (b_1 + b_2 + 70).$$
(11)

We define net throughput T_n by the bit length of an FP64 datum multiplied by the number of FP64 data that can be transmitted in unit time, written as

$$T_n = 64 \frac{S}{S_f}.$$
(12)

Compared with the case where all the data are transmitted in Mod 1, the ratio of net throughput becomes

$$\frac{64S/S_f}{S} = \frac{64}{S_f}.$$
(13)

C. TRUNCATED MOD 2

We now consider the case where a portion of the bits that are to be modulated in Mod 2 is cut from the data and is not transmitted. This operation is a form of lossy compression, which appears in [16]. We call this operation ‘‘Trnc’’, as bits in Mod 2 are truncated. On the receiver side, an FP64 datum is recovered by padding the received bits with 0s to the length of an FP64 datum. If bits in Mod 1 do not contain errors, we can calculate the error in an FP64 datum truncated at MSP by

$$(error) = \begin{cases} 2^E \sum_{j=m-11}^{52} b_j 2^{-j} & \text{for } m \geq 12, \\ 2^E |1 + T - 2^{E'-E}| & \text{for } 1 \geq m \geq 12, \end{cases}$$
(14a)
(14b)

where

$$E' - E = \sum_{j=m-1}^{11} a_j 2^j.$$
(15)

If MSP is fixed, the throughputs of the Trnc case are written as

$$T_g = \log_2 M_1 S,$$

$$T_n = 64 \frac{\log_2 M_1 S}{(MSP)}.$$
(16)

This suggests that implementing the truncation operation can improve the throughput performance, but at the expense of exponentially increased error.

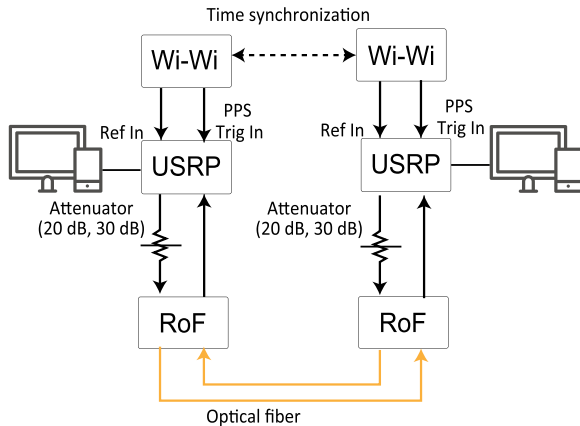


FIGURE 3. Schematic diagram of the experimental system consisting of Radio-over-Fiber (RoF), software-defined radio (USRP), and precision time synchronization modules by wireless two-way interferometry.

IV. EXPERIMENTAL SETUP

To evaluate the proposed scheme we conducted experiments using the apparatuses depicted in Fig. 3. We utilized two software-defined radios (SDRs) programmed with National Instrument's NI-USRP and LabVIEW Field-Programmable Gate Array (FPGA) modules, with each SDR connected to a host computer. The Tx and Rx antennas of the SDRs were connected to Radio-over-Fiber (RoF) modules via electrical cables. We inserted a 20 dB attenuator between the Tx of the USRPs and the Rx of the RoFs, except for the measurement of BER of BPSK, where a 30 dB attenuator was used. The optical Rx and Tx of the RoFs were wired with 10 m single-mode optical cables. We transferred symbols at a rate of 5×10^5 symbols/s with a carrier frequency of 2.4 GHz.

The wireless two-way interferometry (Wi-Wi) system is capable of synchronizing clocks with picosecond-level precision [17]. We utilized its 10 MHz clocks and 1 PPS signals as references for the USRPs since the current proposed system requires a common reference clock to operate.

We chose Mod 1 and Mod 2 from the set of M-ary differential phase shift keying (Differential M-PSK) techniques. The details of the modulation and demodulation operations are described in B, while the characteristics of the transmitter and receiver are outlined in C. We tested two methods to switch between modulation schemes: one that modulates/demodulates all the bits/signals in each scheme and combines the resulting signals/bits afterward, and the other that switches the symbol-bit map defining the correspondence between bits and symbols according to the bit/signal index during a single modulation/demodulation process. Ultimately, we chose the latter method due to its shorter required dummy bit length.

The parameters we varied in our experiments were the output power of the transmitter, as well as the modulation schemes, which included Mod 1, Mod 2, and MSP. The output power can be used to adjust the signal-to-noise ratio, but due to the inherent instability of channel noise, this ratio cannot

be uniquely determined by the output power. As a result, the output power is related to errors in FP64 data through the BER of the channel, and is not related to the throughput. In contrast, Mod 1, Mod 2, and MSP are related to both errors and throughput.

Finally, the length of the dummy bits n_1 and n_2 are decided using the following formula:

$$n_i = \log_2 M_i, \quad (17)$$

where M_i represent the number of symbols that M_i -PSK can generate.

V. RESULTS

A. DATA DEPENDENCY OF ERRORS AND THEIR DISTRIBUTION

As discussed in the analysis presented in Sec. III, the upper bound of the absolute error in a received FP64 datum increases as the exponent of the datum becomes larger. Figure 4 plots the experimentally observed distributions of absolute error for different exponents of the original FP64 data. In addition, for reference, Fig. 4 shows the mean absolute error when the bits in Mod 2 are truncated. Mod 1, Mod 2, MSP and the output power are set to QPSK, 8-PSK, 12 and -1.387 dBm with a 20 dB attenuator (typical SNR per bit was 9.60 dB), respectively. No bit error is observed at the sign bit and the exponent bits, which are transmitted in QPSK. The exponents of the transmitted data are uniformly distributed from -5 to 4, while the mantissas are randomly chosen from the uniform distribution. The maximum error increases by roughly a factor of 2 for each increment in the exponent, and the mean error grows at almost the same rate. It should be noted that data with no error, which are invisible in Fig. 4, accounted for 54.0 % of the total data. For the Trnc case, the errors are as large as the maximum error observed in the case when Mod 2 is 8-PSK. Also as (14a) implies, the errors in the Trnc case converge to their mean. It depends on the application whether such accuracy loss is critical.

B. THROUGHPUT AND ERROR

As pointed out in Sec. III, throughput is related to Mod 1, Mod 2 and MSP, while absolute error is related to the signal-to-noise ratio. Thus when we examine the relationship between the throughput and the error, we should fix the signal-noise ratio, or at least the output power. We set the output powers for each Mod 2 as listed in Table 1. For the remainder of this subsection, Mod 1 is set to QPSK and unless otherwise noted, MSP is set to 12. Mod 2 and the output power are set according to Table 1. Bit errors in the sign and exponent bits were not observed.

Figure 5 illustrates the mean error in received FP64 data and throughput as a function of the modulation format in Mod 2 when the exponent is specified by $E = -1$. For Trnc, as it truncates all the fraction bits when $MSP = 12$, the mean error becomes larger. Herein, net and gross throughput are defined by (12) and (11), respectively. When Mod 2 is QPSK, the dummy bits and MSP bits are not added since there

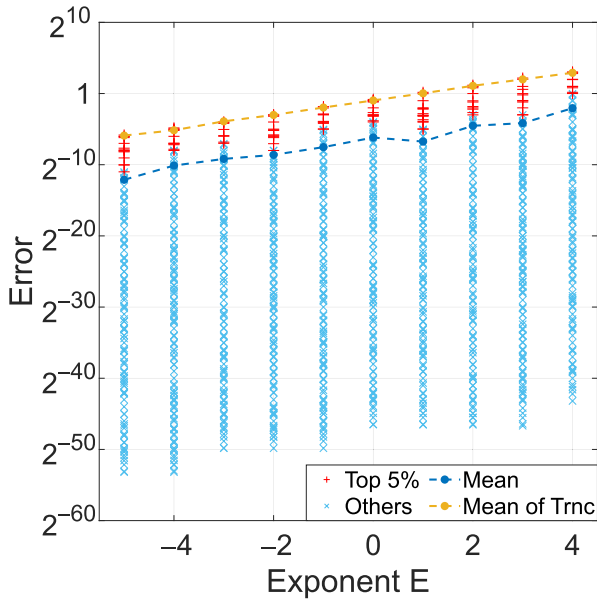


FIGURE 4. Distribution of the absolute error for each exponent of the original FP64 data. The errors of received 1163774 FP64 data are plotted. The red crosses are the top 5% largest errors for each exponent E , and sky-blue Xs are the others. Note that the Y-axis has a log with base 2 scale.

TABLE 1. The output powers for each modulation scheme to compare errors. Mod 1 is set to QPSK.

	QPSK	8-PSK	16-PSK
Output power[dBm]	0.613	0.613	1.613
Typical SNR per bit [dB]	10.0134	10.7723	10.0609
Typical BER	0	0.00036	0.064

is no switching of modulation schemes. We observed that the modulation scheme with denser constellations provides higher net and gross throughput, as well as larger mean error in FP64 data. The Trnc scheme outperforms others in terms of the net throughput. For the 8-PSK and 16-PSK cases, the increases in net throughput compared to the QPSK case were, in this settings of signal-to-noise ratio, 7.5% and 24.2%, respectively, though those in gross throughput were 30.6% and 57.5%, respectively. Therefore we confirm that when Mod 2 is M -PSK with larger values of M , the throughputs becomes higher while the mean errors in floating-point numbers increases, thus the trade-off between throughput and the error holds.

The function of MSP is now examined. Figure 6 summarizes the observed mean error and throughput as a function of MSP with respect to each exponent E . Mod 2 is set to 8-PSK. The mean error decreases roughly by a factor of 2 as MSP increases. If MSP enters the exponential bits, the mean error should increase since the exponent may become larger. This occurs only at $MSP = 4$ in Fig. 6, where the mean error becomes around 10^{183} . The plotted throughputs in Fig. 6 indicates that, as expected, that larger MSPs decreases both net and gross throughputs. Therefore, there is a trade-off between larger error and higher throughput.

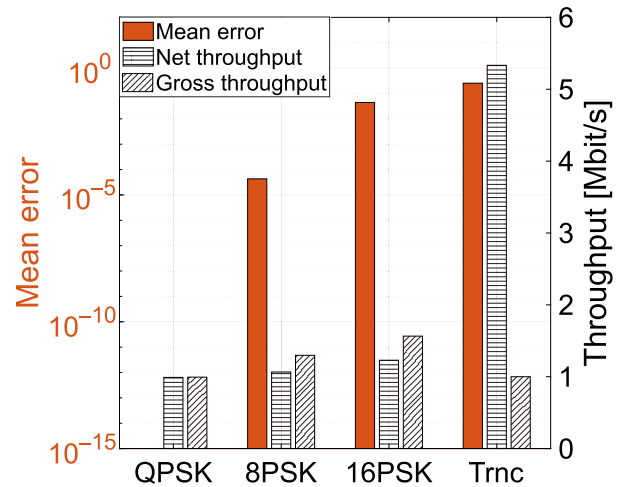


FIGURE 5. The mean error and throughput were measured for Mod 2 using various formats, while the exponent is fixed at $E = -1$. In Trnc, the bits corresponding to Mod 2 are truncated. No errors were observed in QPSK modulation.

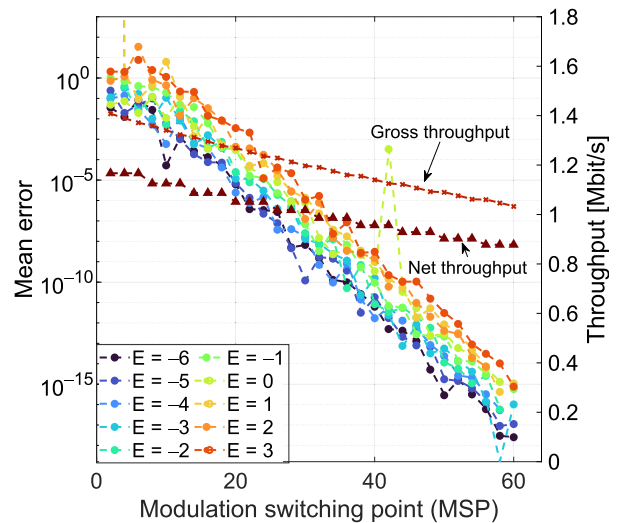


FIGURE 6. The mean error and throughput were evaluated as a function of MSP for each exponent E , using 8-PSK modulation for Mod 2.

C. BOUNDING ERROR BY DYNAMIC CONFIGURATION OF MSP

Using the property of MSP from the former subsection, we can achieve the uniform bound of absolute errors in received FP64 data. Let the required error bound be 2^{e_t} , as previously defined. We use (9) to determine the MSP to satisfy $|r - r'| < 2^{e_t}$. With adequate SNR per bit, Mod 1 can be seen as “error-free”; we can assume that no bit error occur before MSP. In this case, the sufficient condition of MSP would be:

$$|x - x'| < 2^{E-n+12} \leq 2^{e_t} \quad (18)$$

where m is MSP. Thus, $MSP = m = E - e_t + 12$ would be enough.

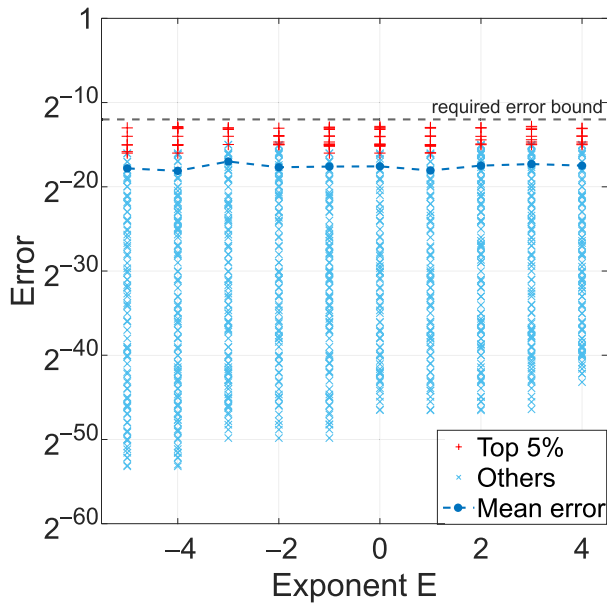


FIGURE 7. Error distribution when MSPs are dynamically configured based on the value of the exponents. The output power was set to -1.387 dBm and SNR per bit was 8.38 dB. Comparing the distribution with Fig. 4, the error was bounded by 2^{-12} .

By setting MSP as such and $e_t = -12$, we observed the distributions of absolute error as shown in Fig. 7. Remarkably, all the errors were confirmed to be smaller than the required bound. With $E - e_t$ larger than 52 (with $e_t = -12$, $E > 40$, which is on the order of 10^{12}), we have to set MSP to 64, transmitting all the bits in Mod 1. The throughput of this transmission scheme depends on the data and required error bound. FP64 data of the larger absolute values or smaller bounds take more time to be transmitted. The experimental case had net throughput of 1.0092 Mbit/s and gross throughput of 1.2543 Mbit/s. Thus, in this case, the gross and net throughput increased, compared to the QPSK case of Fig. 5, by 25.1% and 1.0% , respectively. Note the decrease of throughput depends on the data.

VI. CONCLUSION

The increasing demand for higher communication and computing capacity highlights the need for multi-valued data transmission to improve communication throughput. Denser constellation modulation schemes can provide higher data rates but require a higher signal-to-noise ratio, while sparser constellation formats offer greater noise tolerance at the expense of lower throughput. Approximate computing introduces the concept of quality of information to balance the trade-off between throughput and reliability, which is crucial for future high-performance optical communications and interconnects. In this study, we experimentally demonstrate a dynamically configured transmission scheme where two different modulation formats are adopted based on the importance of the bit sequence in transmitting floating-point numbers over Radio-over-Fiber (RoF) systems

TABLE 2. Structure of the header.

Field name	Size (bits)	Value	Description
Guard Bits	16	0xFFF	padding
Sync Number	16	0xE98A	unique word ¹
Header	32	0xFFAAFFAA	indicates the header
Datasize	32	any	payload size in bits
Mod	8	1 to 6	1: BPSK, 2: QPSK, 3: 8-PSK, 4: 16-PSK
Reserved	8	0 to 64	not used
MyID	16	any	ID of the sender
SendID	16	any	ID of the receiver
Index	16	any	packet index
Time	32	HHMMSSuu	timestamp

with Software-defined radio (SDR) and wireless two-way interferometry (Wi-Wi). To be specific, the proposed system transmits the sign, exponent, and most significant bits of the mantissa with a modulation scheme that is highly tolerant to noise, while least significant bits of the mantissa are managed by a modulation scheme that can transmit a large number of bits per symbol. The boundary between the modulation schemes was called the Modulation Switching Point (MSP), which is even dynamically configured in real-time depending on the information content to be transmitted. We experimentally confirmed and characterized the trade-off between the resultant error of the floating-point numbers and the throughput depending on the setting of MSP and the modulation format employed for the less-critical information content. Finally, we experimentally demonstrated that by dynamically changing the MSP depending on the exponent of the floating-point numbers, the resultant error is always smaller than a specified bound. With these results we believe that we have introduced a novel approximation that can be employed in digital communication systems. The next step would involve extending the proposed scheme to other data structures and further speedup of the scheme.

**APPENDIX A
PACKET FORMAT**

Header Format: The scheme involves adding a 384-bit header to each packet. The first 192 bits are modulated using Mod 1, while the remaining 192 bits are modulated using Mod 2. Both have the same structure, which is listed in Table 2. We repeated exactly the same header because we needed it in the other modulation/demodulation method we tested.

**APPENDIX B
MODULATION SCHEME**

Figure 8 shows a block diagram of demodulation executed on a host computer. Before that, the SDR amplifies the incoming signals, downconverts them to the baseband I/Q components, digitizes, and then passes the signals to the host computer. The demodulation process on the host computer can be roughly divided into three stages, as shown by gray rectangles in Fig. 8. The host executes the process by switching the maps to convert symbols to bits, according to the index of the signal they are processing. The first stage in the top gray

¹Though it is not necessary, this field is allocated for extensibility.

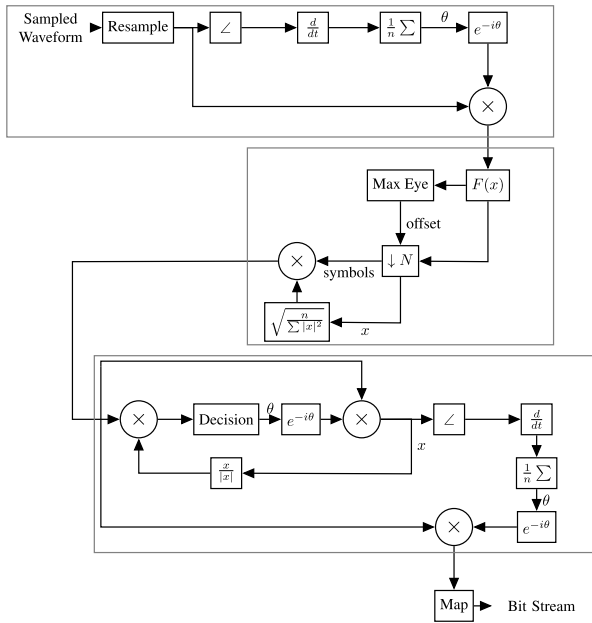


FIGURE 8. Block diagram of demodulation. All the blocks are digitally processed on host computers.

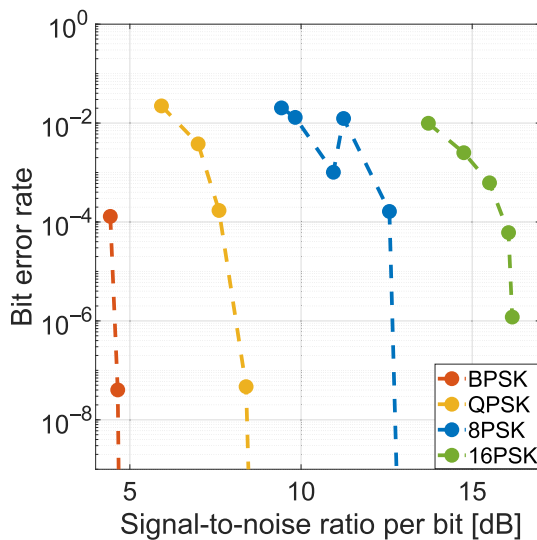


FIGURE 9. Measured relationship between signal-to-noise ratio per bit and BER.

rectangle is resampling and removal of “large” frequency offsets based on the method from [18]. The second stage in the middle rectangle performs filtering, downsampling, and normalizing. Here the block “Max Eye” determines from which samples symbols should be extracted using the Max Eye algorithm. The final stage in the bottom rectangle removes “fine” frequency offsets, and finally the symbols go to the Map block to be mapped to a bit stream.

APPENDIX C TRANSMITTER AND RECEIVER CHARACTERISTICS

We measured the signal-to-noise ratio versus bit error rate for each modulation, which is shown in Fig. 9. We confirmed

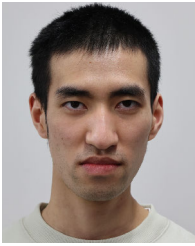
that the transmission channel noise is the sum of a DC offset and additive white Gaussian noise (AWGN), without correlation between the in-phase noise and quadrature-phase noise.

ACKNOWLEDGMENT

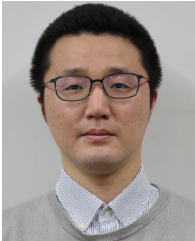
The authors would like to thank Nobuyasu Shiga, Satoshi Yasuda, and Kenichi Takizawa regarding the wireless two-way interferometry devices and associated technological support.

REFERENCES

- [1] *IEEE Standard for Ethernet*, IEEE Standard 802.3-2018 (Revision of IEEE Standard 802.3-2015), 2018.
- [2] G. Tzimpragos, C. Kachris, I. B. Djordjevic, M. Cvijetic, D. Soudris, and I. Tomkos, “A survey on FEC codes for 100 G and beyond optical networks,” *IEEE Commun. Surveys Tuts.*, vol. 18, no. 1, pp. 209–221, 1st Quart., 2016.
- [3] P. J. Winzer, “High-spectral-efficiency optical modulation formats,” *J. Lightw. Technol.*, vol. 30, no. 24, pp. 3824–3835, Dec. 2012.
- [4] T. Kawanishi, “Precise optical modulation and its application to optoelectronic device measurement,” *Photonics*, vol. 8, no. 5, p. 160, May 2021.
- [5] S. Mittal, “A survey of techniques for approximate computing,” *ACM Comput. Surv.*, vol. 48, no. 4, pp. 1–33, Mar. 2016.
- [6] F. Betzel, K. Khatamifard, H. Suresh, D. J. Lilja, J. Sartori, and U. Karpuzcu, “Approximate communication: Techniques for reducing communication bottlenecks in large-scale parallel systems,” *ACM Comput. Surv.*, vol. 51, no. 1, pp. 1–32, Jan. 2018.
- [7] C. Zhang and H. Wang, “Approximate computation for baseband processing,” in *Approximate Computing*, 1st ed., W. Liu and F. Lombardi, Eds. Cham, Switzerland: Springer, 2022, pp. 563–594.
- [8] B. Ransford and L. Ceze, “SAP: An architecture for selectively approximate wireless communication,” Oct. 2015, *arXiv:1510.03955*.
- [9] S. Sen, S. Gilani, S. Srinath, S. Schmitt, and S. Banerjee, “Design and implementation of an ‘approximate’ communication system for wireless media applications,” *SIGCOMM Comput. Commun. Rev.*, vol. 40, no. 4, pp. 15–26, Aug. 2010.
- [10] A. B. Ahmed, D. Fujiki, H. Matsutani, M. Koibuchi, and H. Amano, “AxNoC: Low-power approximate network-on-chips using critical-path isolation,” in *Proc. 12th IEEE/ACM Int. Symp. Netw.-on-Chip (NOCS)*, Turin, Italy, Oct. 2018, pp. 1–8.
- [11] D. Fujiki, K. Ishii, I. Fujiwara, H. Matsutani, H. Amano, H. Casanova, and M. Koibuchi, “High-bandwidth low-latency approximate interconnection networks,” in *Proc. IEEE Int. Symp. High Perform. Comput. Archit. (HPCA)*, Austin, TX, USA, Feb. 2017, pp. 469–480.
- [12] J. Lee, C. Killian, S. Le Beux, and D. Chillet, “Distance-aware approximate nanophotonic interconnect,” *ACM Trans. Des. Autom. Electron. Syst.*, vol. 27, no. 2, pp. 1–30, Nov. 2021.
- [13] L. Sousa, “Nonconventional computer arithmetic circuits, systems and applications,” *IEEE Circuits Syst. Mag.*, vol. 21, no. 1, pp. 6–40, 1st Quart., 2021.
- [14] A. Sabbagh Molahosseini, L. Sousa, A. A. Emrani Zarandi, and H. Vandierendonck, “Low-precision floating-point formats: From general-purpose to application-specific,” in *Approximate Computing*, 1st ed., W. Liu and F. Lombardi, Eds. Cham, Switzerland: Springer, 2022, pp. 77–98.
- [15] *IEEE Standard for Floating-Point Arithmetic*, IEEE Standard 754-2008, 2008.
- [16] Y. Hu and M. Koibuchi, “Accelerating MPI communication using floating-point compression on lossy interconnection networks,” in *Proc. IEEE 46th Conf. Local Comput. Netw. (LCN)*, Edmonton, AB, Canada, Oct. 2021, pp. 355–358.
- [17] N. Shiga, K. Kido, S. Yasuda, B. Panta, Y. Hanado, S. Kawamura, H. Hanado, K. Takizawa, and M. Inoue, “Demonstration of wireless two-way interferometry (Wi-Wi),” *IEICE Commun. Exp.*, vol. 6, no. 2, pp. 77–82, Feb. 2017.
- [18] F. Classen and H. Meyr, “Two frequency estimation schemes operating independently of timing information,” in *Proc. GLOBECOM*, Houston, TX, USA, 1993, pp. 1996–2000.



TOSHIKI ISHIMARU is currently pursuing the degree with the Department of Mathematical Engineering and Information Physics, Faculty of Engineering, The University of Tokyo, Tokyo, Japan. His research interests include cyber-physical systems and advanced computing and networking technologies, including approximate computing.



TAKATOMO MIHANA received the B.E., M.E., and Ph.D. degrees in engineering from Saitama University, in 2017, 2019, and 2022, respectively. Since 2022, he has been an Assistant Professor with the Department of Information Physics and Computing, Graduate School of Information Science and Technology, The University of Tokyo.



MICHIHIRO KOIBUCHI (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees from Keio University, Yokohama, Kanagawa, Japan, in 2000, 2002, and 2003, respectively. He is currently a Professor with the National Institute of Informatics, and SOKENDAI, Tokyo, Japan. His research interests include high-performance computing and interconnection networks. He published over 100 peer-reviewed technical conferences and journal articles (nine in IEEE

TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, five in IPDPS, four in HPCA, and three in IEEE TRANSACTIONS ON COMPUTERS).



TETSUYA KAWANISHI (Fellow, IEEE) received the B.E., M.E., and Ph.D. degrees in electronics from Kyoto University, Kyoto, Japan, in 1992, 1994, and 1997, respectively. From 1994 to 1995, he was with the Production Engineering Laboratory, Panasonic. In 1997, he was with the Venture Business Laboratory, Kyoto University, where he was engaged in research on electromagnetic scattering and near-field optics. In 1998, he joined the Communications Research Laboratory, Ministry of Posts and Telecommunications (now the National Institute of Information and Communications Technology), Tokyo, Japan. In 2004, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, University of California at San Diego, San Diego, CA, USA. Since April 2015, he has been a Professor with Waseda University, Tokyo. His current research interests include high-speed optical modulators and RF photonics.



MAKOTO NARUSE received the B.E., M.E., and Ph.D. degrees in engineering from The University of Tokyo, in 1994, 1996, and 1999, respectively. After working as a Research Associate and an Assistant Professor with The University of Tokyo, from 1999 to 2002, he joined the National Institute of Information and Communications Technology, Ministry of Internal Affairs and Communications, Tokyo, in 2002. In 2017, he was an Invited Processor with Universit Grenoble Alpes, Grenoble, France. Since 2019, he has been a Professor with the Department of Information Physics and Computing, Graduate School of Information Science and Technology, The University of Tokyo.

...