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RESEARCH ARTICLE

A High-Efficient 95.6% Rectifier With Passive AC-DC Voltage Quadrupler for Low-Frequency Electromagnetic Energy Harvesting System

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ABSTRACT This article present high efficient electromagnetic energy harvesting system for low frequency applications. The proposed circuit is composed of two stages. In the first stage electromagnetic (EM) rectifier uses an improved rectifier structure with active diodes powered internally by a passive ac-dc positive and negative voltage quadrupler. This boost input peak voltage 0.6 V to +0.8 V and -0.8 V and power internally unbalance-size comparators (Comp_1 and Comp_2). The unbalance size comparator minimize the delay by introducing input offset in order to minimize the reverse leakage current. Due to this, the efficiency is improved to 95.6% at 0.6 mA load current. The second stage is step up dc-dc converter with proposed soft start circuit and min-max duty generator circuit. The proposed soft start circuit prevent dc-dc converter circuit from inrush current. The inrush current reduce the efficiency of dc-dc converter and can drain out the battery energy. In order to avoid undesirable feedback voltage, the dc-dc converter uses a min-max duty generator. The high-side and low-side driver control signals are generated by a dead-time generator to avoid the high-side and low-side power switches operating simultaneously. The step-up converter is designed by using 130 nm CMOS technology. The input voltage of dc-dc is the output of EM rectifier, which is 1V and output voltage is 1.3V at 0.5mA load current. The efficiency of step-up dc-dc converter is 94.2% and the system efficiency is 90% at 10 Hz frequency.

INDEX TERMS Electromagnetic (EM), piezoelectric (PZT), energy harvester, EM rectifier, step up dc-dc converter.

I. INTRODUCTION

Low-power wireless sensor networks (WSNs) are frequently available due to advancements in electronic circuits for smart buildings, the automobile sector, and implantable electronics [1], [2]. While low-power design techniques increases the lifespan of WSNs, the sensor nodes' lifespan are restricted by the size of the batteries used to power them. Battery volume makes up the majority of the system since it does not decay as quickly as sensor electronics [2]. Additionally, it can be expensive and nearly impossible to replace and maintain these batteries due to the sensor's position [3]. A workable option for prolonging the life of a WSN node is to collect energy from energy sources and to run without batteries or recharge them [4].

To harvest accessible energy in the environment, various methods such as photovoltaic, vibrational, thermal, and electromagnetic (EM) have been proposed [2], [5]. To collect

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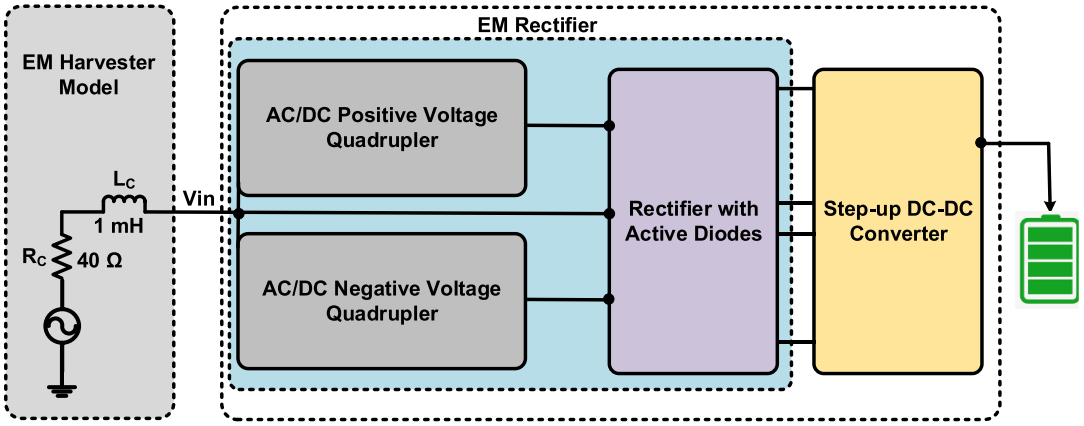

FIGURE 1. Block diagram of electromagnetic energy harvesting system.

energy from one source and convert it into useful forms, various power management circuits have been designed [6], [9]. However, since most energy sources are unpredictable and inconsistent, relying on a single source of energy to power WSNs, reduces system stability [10]. As a result, the duration and performance of the WSN can be increased by using an effective hybrid architecture, where the system uses a variety of energy sources in a synergistic manner.

Electrostatic (ES), piezoelectric (PZT), and electromagnetic (EM) transducers can extract the kinetic energy in vibrations [11], [12], [13]. A higher electrical density is produced by the PZT and EM harvesters [14]. High AC voltage is advantageous for interface electronics for PZT energy harvesters [15], [16], [17]. The PZT interfaces high output impedance which requires the usage of an extra impedance matching network, increases complexity and power losses. In comparison to PZT and ES energy harvesters, EM energy harvesters are better suited to low frequency, which makes the processing of generated voltage easier. In particular, a low-frequency electromagnetic source that is easily captured with an electromagnetic energy harvester is the focus of this article, such as energy harvesting (EH) from electromagnetic (EM) energy sources [18], human body movement [19], buildings and the vehicles vibration as well [20]. It is inappropriate to directly power the electronic equipment due to the modest amount of the induced voltage and power from low-frequency EM sources [18]. As a result, a high power conversion ac-dc boost converter is required. The motivation behind EM rectifiers is to harness and utilize the abundant electromagnetic energy in our surroundings for practical applications. By converting this energy into usable electrical power, EM rectifiers enable enhanced wireless power transfer, energy harvesting, and contribute to the development of more efficient and sustainable technologies.

In the previous works, pulse width modulation (PWM) controlled conventional ac-dc converter [21], pulse frequency modulation (PFM) control [22], reconfigurable switching control [23] are shown. However, due to the dynamic power loss, the PCE is low. Recent years have seen the appearance of asynchronous ac-dc converters, which are more effective for EM energy harvesting due to the inferior switching rate than the converter with modulated clock [20], [24]. In [20] controls the charge pumps with two comparators and achieves alteration with a start-up voltage of 220 mV, although the PCE is only 50%. In [21] a high PCE is attained (up to 91%) but a low-drop-out (LDO) regulator was added to control the output voltage, which lowers the overall PCE.

In this paper, a low-voltage EM rectifier is designed for energy harvesters. In EM harvester model, RC and LC circuits are designed to resonate at a specific frequency to match the frequency of the harvested EM signals. This allows for efficient energy transfer from the EM signals to the harvester. The values of the RC and LC circuits are chosen 40 ohm and 1mH respectively to achieve the desired resonant frequency. With the help of a passive ac-dc positive and negative voltage quadrupler, an active diode rectifier circuit effectively rectifies the harvested voltage and unbalance-size comparators to reduce the delay by introducing input offset and minimize the reverse leakage current, which increase the power conversion efficiency of EM rectifier. On the same chip, a step up dc-dc converter enhances the rectified voltage enough to drive a practical load. The block diagram of electromagnetic energy harvesting system is shown in Fig. 1. The 130 nm standard CMOS process was used for the design and fabrication of the main chip.

The rest of the paper is organized as follows. The system architecture is described in Section II. Section III shows the experimental results. Finally, conclusions are in Section IV.

II. SYSTEM ARCHITECTURE

The block diagram of the circuit in Fig.1, shows the conversion of the ac signal generated by the vibrations of the EM harvester into dc. The system uses an active diode rectifier circuit and is powered by a passive ac-dc quadrupler circuit. The active diode architecture minimizes voltage drop and is more suitable for generating high load currents than passive diode-connected structure. An unbalance comparator circuit and CMOS switch make up the active diode structure. On the positive and negative output sides, respectively, PMOS and NMOS pass transistor-based switches are employed because

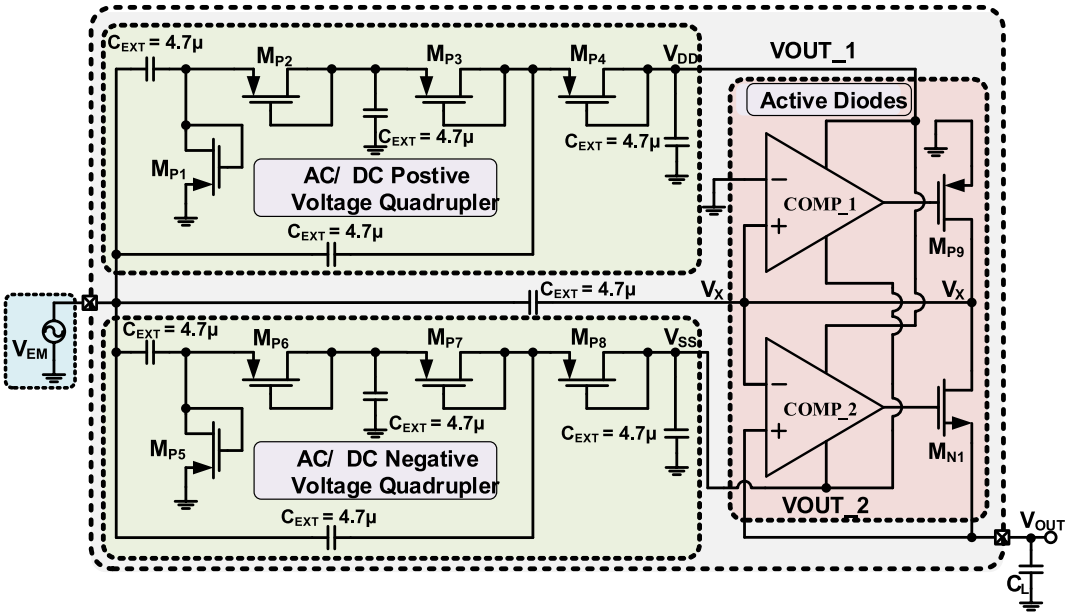

FIGURE 2. Block diagram of the EM rectifier.

PMOS has the maximum conductance at high voltages and NMOS at low voltages. The switch comparators can be powered by a passive ac-dc quadrupler with minimal drop-out voltage and operated at very low currents (tens of nano-amps). The EM harvester input is used by the passive ac-dc quadrupler to provide sufficient positive and negative voltages to power up the comparators. Unbalance comparators, one with an NMOS input stage to process the positive phase of the input signal and another with a PMOS input stage to process the negative phase, improve the performance of the active diode ac-dc circuit. A dc-dc converter is used in this system to step-up output of EM rectifier voltage from 1 V to 1.3 V.

A. RECTIFIER WITH UNBALANCE COMPARATORS

The rectifier circuit diagram shown in Fig. 2 is an enhanced version of the rectifier shown in [5]. For avoiding significant voltage loss, the circuit employs two active diodes rather than passive diodes, increasing the efficiency of the rectifier. The two different unbalance size comparator with NMOS input transistor and PMOS input transistor can be controlled to have lower conduction losses compared to passive diodes and ordinary comparator as well. They typically have lower forward voltage drops, which can reduce power losses by reducing reverse leakage current and improve overall efficiency. They can switch ON and OFF much faster compared to passive diodes. They are precisely controlled to regulate the rectification process, allowing for better control of the output voltage and improved performance. The MOS switches (MN1, MP9) are turned ON or OFF by the comparators, which are driven by AC/DC positive and AC/DC negative voltage, based on the input and output rectifier voltage. They function as, when VEM is higher than comparator COMP_1 will turn on the PMOS (MP9). Similarly, when VEM is lower

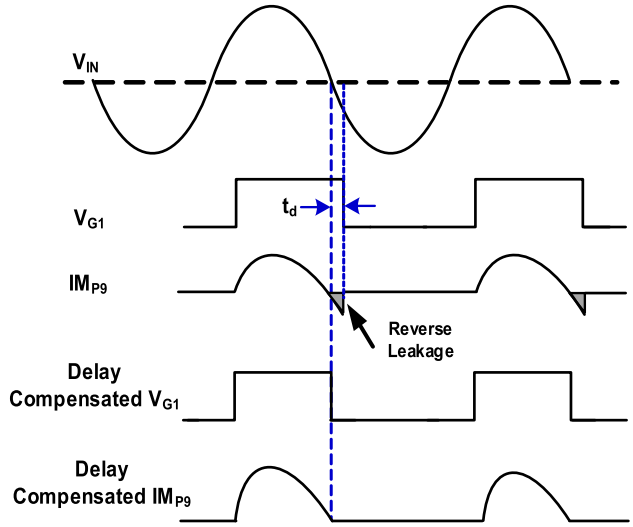

FIGURE 3. Timing diagram of EM rectifier.

than comparator COMP_2 will turn on the NMOS (MN1). The size of the unbalance comparators and the switching transistors has a significant impact on the efficiency of the rectifier.

It is clear that growing the transistor's size causes the turn-on resistance to decrease, which lowers conduction losses. The parasitic capacitance of larger transistor also increases switching losses. In a regular-sized transistor, conduction losses prevail over switching losses due to the lower switching frequency (10 Hz). Low frequency is used to reduce electromagnetic interference (EMI). Higher frequencies can generate more EMI, which may need to be filtered out to avoid interference. The use of a low frequency can help to minimize EMI and ensure reliable operation. Increasing the frequency of EM rectifier can generally lead to higher power

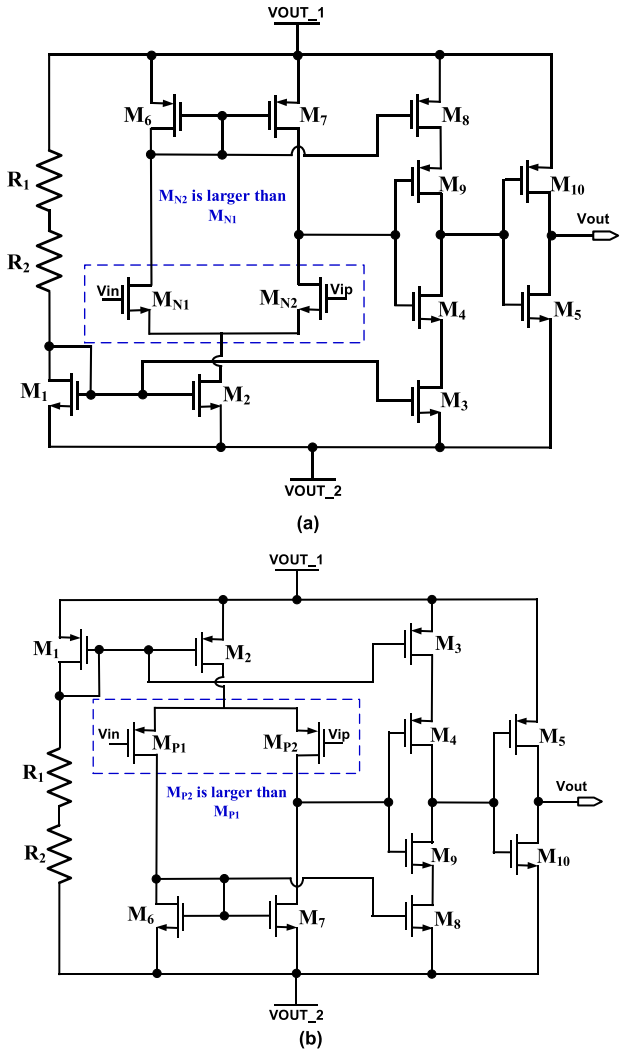

FIGURE 4. Unbalance-size comparator with. (a) NMOS input transistors and (b) PMOS input transistors.

TABLE 1. Power consumption analysis of EM rectifier.

Parameters	EM Rectifier
Conduction losses	3.2%
Switching losses	0.15%
Internal circuit losses	1.05%
Total losses	4.4%
Input Power	3.085 W
Output Power	2.95 W
Efficiency	95.6 %

density as well. In order to reduce overall losses, we can use simulation tools to optimize the transistor size taking these considerations into account. The choice was made to use a large size PMOS (PW/L=7500/0.13) and a large NMOS (NW/L=2500/0.13).

The performance of the comparators, on the other hand, influences the rectifier efficiency. As previously mentioned, a comparator is used with an active diode to switch a transistor ON and OFF while reducing the voltage drop. Due to comparator's delay, the active diodes are unable to block the reverse current, resulting in conversion loss. Consider the

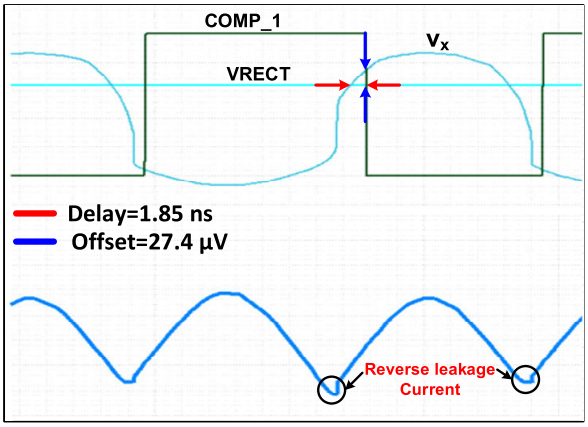

FIGURE 5. Delay and Offset of Unbalance-size comparator.

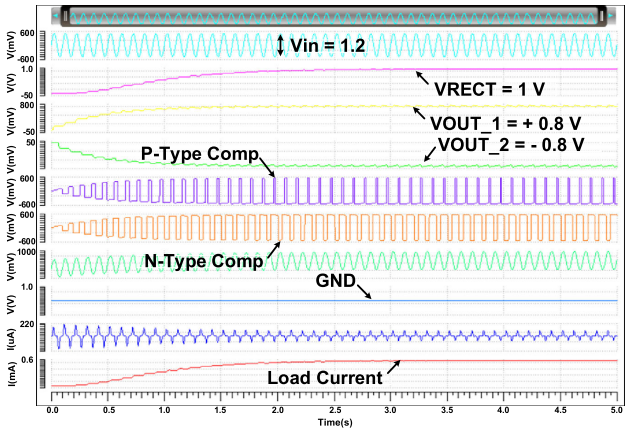

FIGURE 6. Simulation result of EM rectifier.

positive conversion circle, as shown in Fig.3. When V_{EM} starts to decline and drops below the positive output voltage, the switch M_{P9} stays ON because of the comparator td delay. As a result, a reverse leakage current flows from the Vx node to the VEM node, causing power losses. It is noteworthy that, in order to increase the power conversion efficiency, the comparator driving the power switches must be turned on/off rapidly enough to block the reverse current. In Fig. 4 (a) and (b), the proposed comparators are shown. Offset is a crucial reference indicator in engineering design that is used to assess the comparator's overall performance. As a result, one of the important method to address offset issues in various comparators is the offset calibration technique, which has a significant impact on the performance of the entire comparator system. Many things, such an input mismatch, can result in offset. Output offset could also be caused by oversized devices.

In our designed comparator, the input differential pair is purposefully made unbalanced with a slightly larger MN2 than MN1, similarly MP2 than MP1. By using larger transistors in the input differential pair, the comparator have a faster response time, as the larger transistor charge and discharge the input nodes more quickly. This potentially result in faster switching of the rectifier circuit and reduce switching losses. This minimize the reverse leakage current by minimizing the

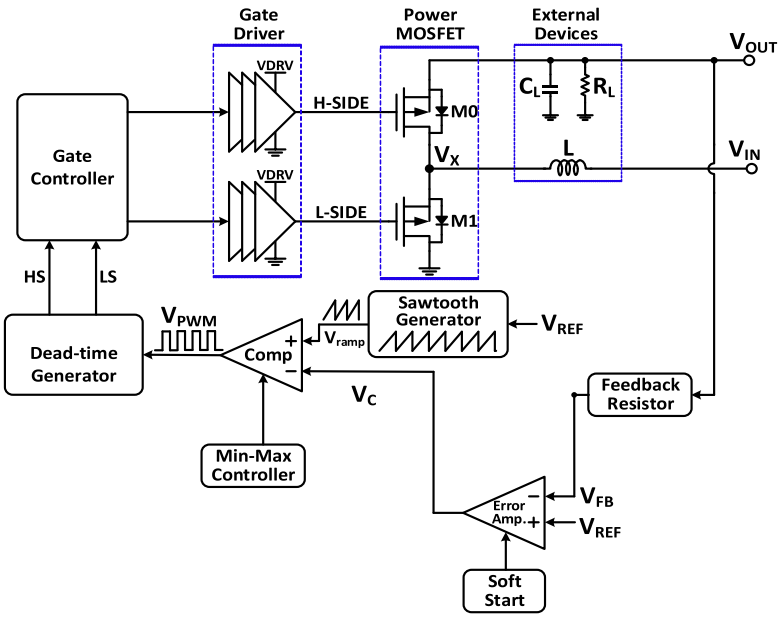

FIGURE 7. Block diagram of DC-DC converter.

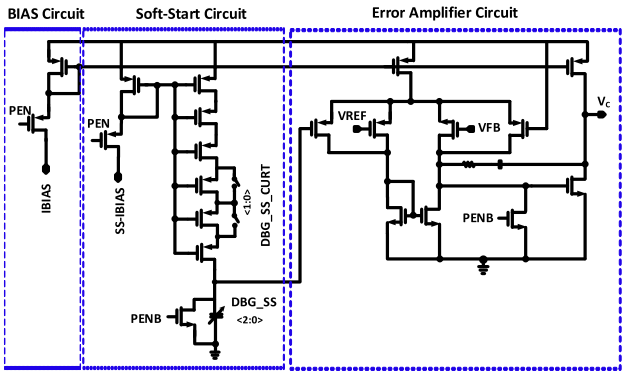

FIGURE 8. Soft start-up circuit.

TABLE 2. Results of soft-start circuit.

DBG_SS<2:0>	Inrush Current (A)
000	1.2
001	1.1
010	1
011	0.95
100	0.82
101	0.76
110	0.64
111	0.64

DBG_SS_CUR <1:0>	Soft-Start Current(nA)
11	13.5
10	8.18
01	6.34
00	4.55

delay and improve efficiency as shown in Fig. 5. Due to delay td in the conventional comparator, the switch M_{P9} remains "on" when V_{EM} begins to fall in the positive transition. As a result, the reverse leakage current flow from M_{P9} to V_{EM}, resulting in power loss. The switch can be turned "off" in advance to reimburse the delay td by introducing an input offset. The proposed comparator has less power consumption as compare to the unbalanced comparator used in [5]. The unbalanced differential pair is sized to account for the entire delay due to process variation. Simulation result of EM rectifier is shown in Fig. 6. Since the rectifier output voltages are boosted by the dc-dc boost converter, the little voltage drop has minimal influence on the output voltage. Power loss, on the other hand, may be considerably decreased while consuming no more power. The Power analysis of EM rectifier is shown in Table 1. Furthermore, to increase the rectifier performance, two comparators with NMOS input transistors and PMOS input transistors are designed separately due to the different input common mode voltage.

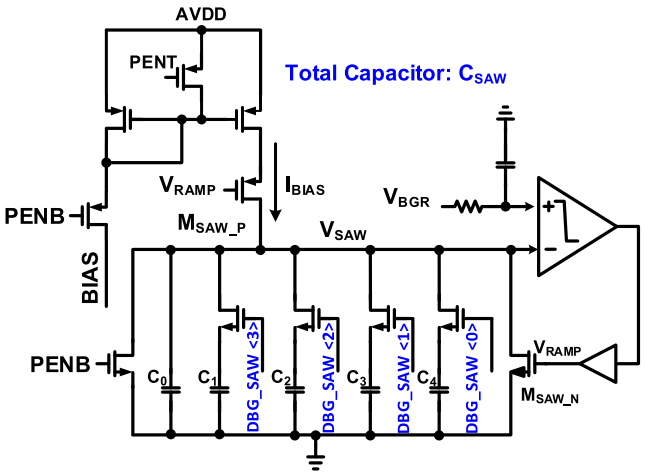

FIGURE 9. Saw-tooth generator.

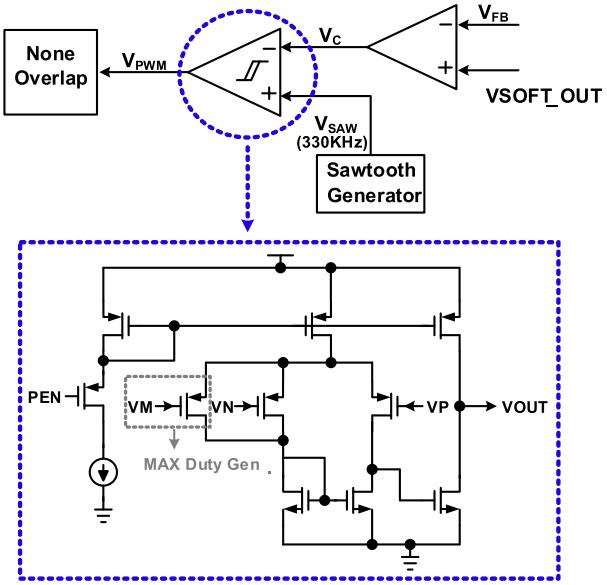

FIGURE 10. Max duty generator.

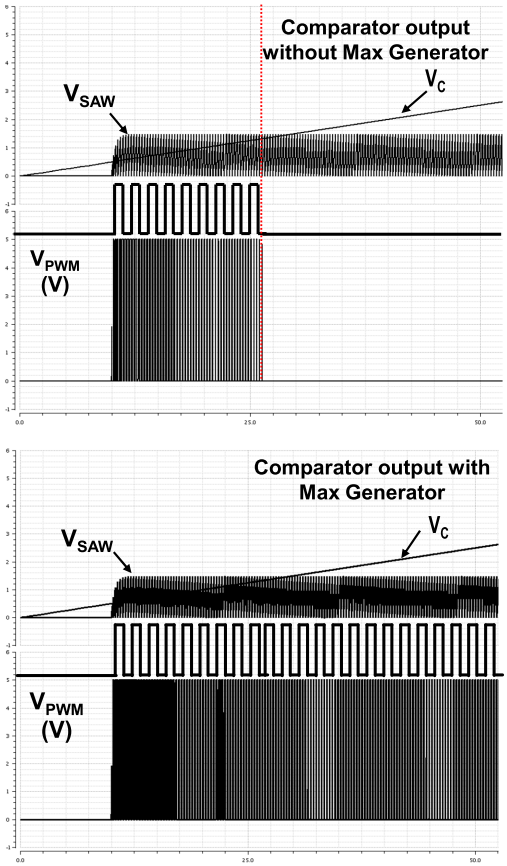

FIGURE 11. Simulation result of min-max duty generator.

B. STEP-UP DC-DC CONVERTER

The inclusive structure of the proposed step-up converter is shown in Fig. 7. The Step-up converter is basically an electronic circuit which convert low voltage of dc into a high dc voltage. In proposed boost converter, two MOSFET switches are alternatively closed and opened, that periodically switches the inductor (L) between input and output terminals, thus obtaining the desired boosted output voltage. In PWM, the duty cycle of gate drive signals that control the power switches are proportional to the control voltage (V_C). The voltage difference between the feedback (V_{FB}) voltage and the reference (V_{REF}) configuration is known as the error amplifier voltage (V_C). A spike of current drawn, when dc-dc converter start operating, is called inrush current. Inrush current causes the system electromagnetic interference to be conducted and emitted [25]. The inrush current reduce the efficiency of boost dc-dc converter and can drain out the battery energy. Due to EM energy harvester's environment, very low energy is poised in Energy harvesting system. When the inrush current is substantially high, it will take a large portion of the harvesting Power. The total efficiency of energy harvesting system is reduce by this inrush current when it became significant high. Inrush current is generally higher from load current and prompts the upstream circuit breaker of the over current protection of the system IC. Therefore, Soft-start circuit is designed to suppress the inrush current, circuit diagram is show in Fig.8. Table 2, show the result of the soft-start circuit according to the trimming bit. DBG_SS<2:0> is controlled to adjust the size of the capacitor and adjust the inrush current. When DBG_SS_CUR<1:0> is adjusted, it is possible to control the amount of current charged to the capacitor of Soft-Start. The control voltage (V_C) is output voltage of controller. The error amplifier is utilized to give a control voltage (V_C) that is applied to the comparator. The comparator compares the V_C with a fixed ramp voltage generated by a saw-tooth generator shown in Fig. 9, and provides a pulsed signal. A saw-tooth generator produces a ramp signal with the required frequency. The peak value of saw-tooth generator provided to the PWM comparator is exactly proportional to the input voltage of the converter. Regardless of the control mechanisms used, a comparator is an essential circuit in the dc-dc converter control system. The proposed dc-dc converter specifications are listed in Table 3.

TABLE 3. Performance parameters of DC-DC converter.

Input Voltage	0.8~1 V
Output Voltage	1.3 V
PCE (%)	94.2
Type	PWM
Switching frequency	330 KHz
Inductor	4.7 µH
Load Cap.	10 µF
Load resistor	500 Ω

When feedback voltage V_{FB} is not in projected range at that time, output is not regulated, during the settling time and Error amplifier output to be lower or higher than saw-tooth highest voltage which cause unwanted feedback voltage value. When the maximum peak value of saw-tooth signal is lower than the output signal of error amplifier, then V_{PWM} is maintain by the pulse signal generator at zero or in this case, pulse signal generator is 0% of the duty cycle. When the output voltage of error amplifier is lower than the

TABLE 4. Performance comparison with prior works.

Parameter	[20]	[21]	[19]	[5]	[9]	[7]	This Work
Process	0.18 µm	0.18 µm	0.18 µm	0. 18 µm	0.35 µm	0.18 µm	0.13 µm
Output Voltage (V)	1.2	1	3	1	3	2	1
Input Voltage (V)	0.22	0.7	0.4	0.5	0.45	1.4	0.6
Operational Frequency (Hz)	3	20	8	50	64.4	53	10
Max PCE	50 %	91 %	28%	94%	95%	42 %	95.6%
Area (mm^2)	1.2	2.52	2.25	0.11 2	1.33	0.47	2.94

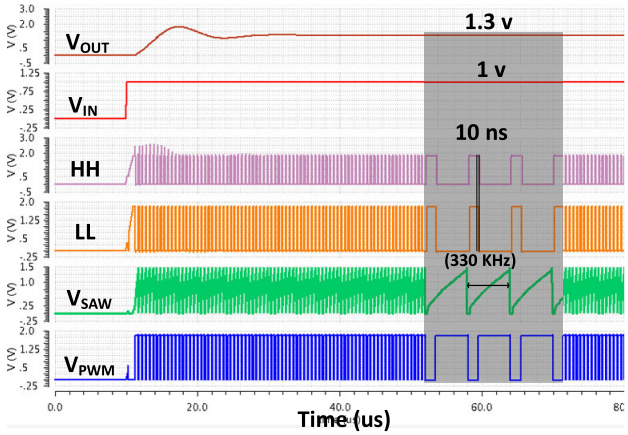

FIGURE 12. Simulation result of DC-DC converter.

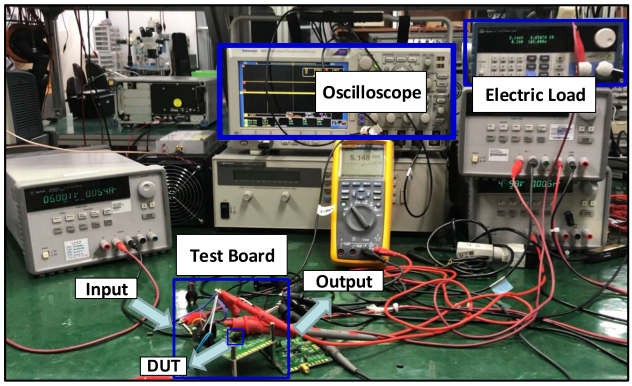

FIGURE 13. Measurement setup.

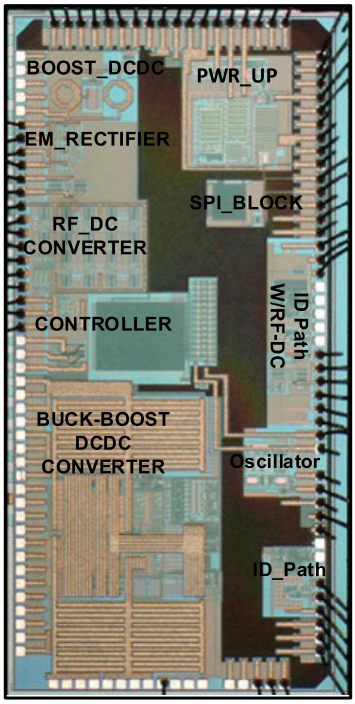

FIGURE 14. Microphotograph of the proposed chip.

least value of saw-tooth signal than PWM is maximum of the duty cycle and it is cause by the output voltage over-charging. The settling time of step-up converter is extend by this sensation. For this, the min-max duty generator controls by output voltage of error amplifier to overcome this situation Fig.10. shows the schematic of the min-max duty generator. When error amplifier output voltage is less then V_{MIN}, the value of V_{MIN} is selected and compared with V_{SAW} to generate pulse width modulation signal. The voltage V_{PWM} is maximized at 90% at this case. When the V_{MAX} is lower than the output voltage of error amplifier, the comparator originate output PWM at least 8% of the duty cycle because it is controlled by V_{MAX} voltage. Otherwise, the output error amplifier signal is directly compared with the saw-tooth generator signal to generate the V_{PWM}. Without the max generator, V_{PWM} will be set to 0 and the dc-dc boost converter won't work efficiently if the V_C voltage is higher than V_{SAW}. If there is max generator, although V_C is over V_{SAW}, the V_{PWM} which is comparator output is limited and made by comparting V_{MAX} and V_{SAW}, show in simulation result of Fig. 11.

Dead time generator circuit is fed by output comparator. High side and low side signal for power MOSFET is generated by dead-time generator. The pulse signal is fed to the non-overlap circuit that generates two drive signals (HS) and (LS) for the power switches (M0) and (M1) through the gate drive logic circuit respectively. Both high and low side signals are reciprocal from each other. The feedback resistor circuit

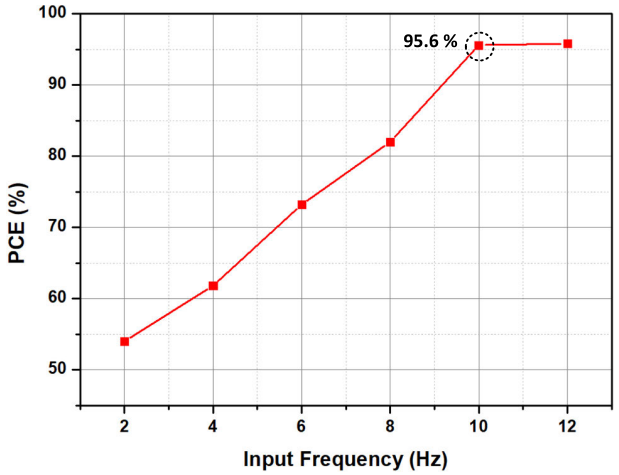

FIGURE 15. Measured efficiency of EM rectifier versus input frequency at 0.6 V input peak voltage.

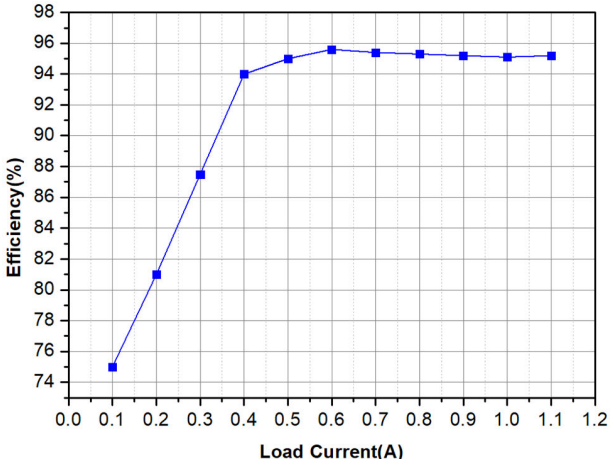

FIGURE 16. Measured efficiency of EM rectifier versus load current.

is used for biasing the input of the error amplifier. Simulation result of Step-up dc-dc converter is shown in Fig. 12.

III. MEASUREMENT RESULTS

Fig. 13, depicts the measurement setup. The low voltage EM Rectifier and step down dc-dc converter has been implemented in a 0.13 μm, which occupy area 2.94 mm^2. The chip micrographs are shown in Fig. 14. The active rectifier and dc-dc converter outputs are filtered by 10-μF capacitors with equivalent series resistance (ESR) less than 70-mΩ, whereas the dc-dc converter inductor is 4.7-μH with ESR of 120-mΩ.

Fig. 15, shows the measured efficiency of the low voltage EM rectifier when the resonant frequency is 10 Hz and Fig. 16, shows the measured efficiency of EM rectifier at different load current. It achieve low efficiency 75% at 0.1A but efficiency gradually increase at 0.2A, 0.3A, 0.4A and 0.5A respectively. It achieve maximum efficiency 95.6% at 0.6A load current. At 0.6A load current the input power of EM rectifier is 3.085W and output power is 2.95W.

Similarly, Fig. 17, shows the measured efficiency of dc-dc converter at different load current, dc-dc achieve low

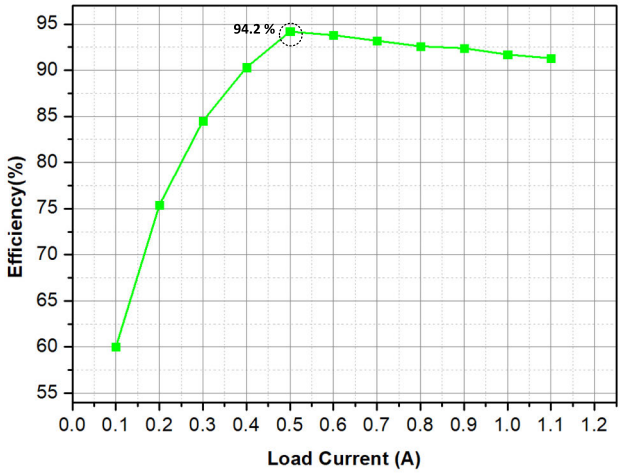

FIGURE 17. Measured efficiency of DC-DC converter versus load current.

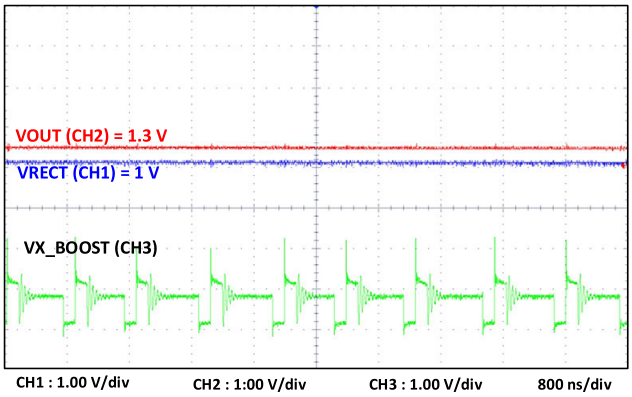

FIGURE 18. Measurement result of overall system.

efficiency 60% at 0.1A and gradually it's efficiency increase until 0.5A load current, at this load current dc-dc converter achieve maximum efficiency 94.2%. At 0.5A it has input power 2.95W and output power is 2.78W. Without the proposed unbalance comparators for core PMOS and NMOS transistors, the reverse leakage current exist because the gate voltage of the NMOS power transistor is high for the same duration even after the V_{EM} voltage becomes positive. Table 4 show performance comparison of proposed EM rectifier with prior works.

Fig.18, shows the measurement result of overall system. The efficiency of EM rectifier and dc-dc converter is 95.6% and 94.2% with output voltage of 1V and 1.3 V respectively at 0.5A and 0.6A load current. The overall system efficiency can be calculated by using formula:

$$\begin{aligned} \eta\_overall &= \eta\_rectifier \times \eta\_dc - dc \\ \eta\_overall &= 0.956 \times 0.942 \\ \eta\_overall &= 0.9006 \end{aligned} \tag{1}$$

Converting the decimal result to a percentage by multiplying by 100. So, the overall system efficiency with EM rectifier efficiency and dc-dc converter efficiency is approximately 90%.

IV. CONCLUSION

Low voltage EM rectifier and step-up dc-dc converter is designed in this paper. The received AC power from electromagnetic (EM) energy source is converted to the desired DC level by a step-up dc-dc converter. Unbalance comparators minimized the reverse leakage current of EM rectifier and the soft start circuit is used to prevent from inrush current in dc-dc converter. The overall power efficiency of the system implement at 0.13 μm technology is 90% at 10 Hz frequency.

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