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RESEARCH ARTICLE

Broadband Silicon Controlled Channel for Wireless Network-on-Chip at 60 GHz

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ABSTRACT This paper, which concerns the wireless network concept, presents the characterization and demonstration of silicon propagation channel control performed at around 60 GHz. The aim is to optimize the propagation channel in order to transmit signal in a large frequency band, this for broadcast internal Networks-on-Chip communication application. First, slot antennas in the frequency band [30–67 GHz] directly integrated on high resistivity silicon (HR-Si) surrounded by low-resistivity silicon (LR-Si) were designed and measured. The transmission and matching parameters are presented for inter-element spacings of 6 mm and 14 mm and demonstrate the interest of controlling the propagation channel by using absorbent boundaries from a controllable bias voltage. The results are also compared with the existing literature and show large 3 dB bandwidths. The S-parameters of the measured slot antennas are then integrated and simulated in the time domain using on-off keying (OOK) modulation, making it possible to evaluate the maximum throughput and bit-energy efficiency.

INDEX TERMS Dipole antennas, electromagnetic propagation, silicon, slot antennas, wireless network-on-chip.

I. INTRODUCTION

Nowadays, new applications such as artificial intelligence, big data or the internet of things are expanding rapidly, increasing demands for signal processing and computing power. To meet these demands, it is necessary to create faster and more powerful chips that consume little power with a smaller size. Networks-on-chip (NoC) are networks born from the need to establish more links within a chip and to improve internal communications. Current NoC are essentially wireline. As the physical limits to chip size reduction have almost been reached, NoC has emerged as a promising concept. The main problem associated with NoC is the transmission of information between the cores. Indeed, in order to meet the growing needs of the applications mentioned above, it is essential to both miniaturize and increase the data rate of the circuits. This increase in data rate, linked to an increase in the working frequencies of the circuits, leads to several undesirable effects on the propagated signals, such as mismatches, crosstalk, additional delays or desynchronization [1]. To overcome these problems, several approaches to new interconnects are considered in the literature, such as: (i) 3D interconnects, which have the advantage of providing short interconnects but at the cost of high power consumption, complex routing and thermal problems [2], [3]; (ii) carbon nanotube (CNT) interconnects, which have low losses but also problems related to the difficulty of controlling CNT diameter or misalignment [4]; (iii) RF interconnects, which are compatible with CMOS processes, with low power consumption and high throughput, have several disadvantages such as the occupied surface or the risk of interference with other components [5], [6]; and (iv) optical interconnections, which allow a large bandwidth, high communication rate and reduction of power consumption, but which remain expensive [7].

In the context of NoC circuits, the implementation of wireless interconnects seems to be a promising solution [8], [9]. Wireless links allow long distance communications between

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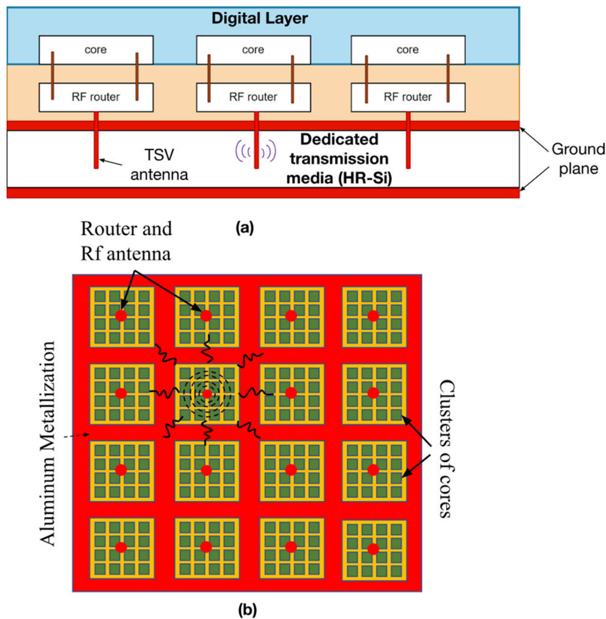

FIGURE 1. (a) Cross-section of the conceptual WiNoC architecture; (b) Top view with 16-antenna 256-core topology.

distant nodes without complex routing, facilitate the broadcast and permit simultaneous multicast communication [10] of data in parallel computation or for clock distribution. Most existing wireless network-on-chip (WiNoC) architectures are based on the on-off keying (OOK) modulation technique as it is very simple as well as power and area efficient [11]. However, OOK modulation needs smooth transmission coefficients over a large bandwidth to be able to transmit high data rates [12].

In the CMOS context, wireless interconnects involve antennas placed on the silicon substrate. Antennas on silicon, due to their low resistivity and high permittivity, have low efficiency. The energy is stored in the silicon substrate and is not really radiated into free space [13], [14]. For wireless interconnects, the energy therefore propagates mainly in the silicon and only a small part of the energy propagates in the air.

Due to the Silicon-Air boundaries around the substrate, wireless interconnects in a silicon context without a surrounding absorbing layer, imply a very small available bandwidth, and so are not suitable for OOK techniques. Previous studies have also shown the interest of controlling air-silicon boundaries ($\varepsilon_{Air} = 1$ vs. $\varepsilon_{rSi} = 11.9$) in order to reduce multipath and thus obtain wide bandwidths and energy efficiency [12], [15].

The WiNoC network concept proposed in this paper is based on this approach. Fig. 1 (a) shows a cross section of the WiNoC architecture. To improve the transmission efficiency of the propagating canal in the silicon substrate, a dedicated parallel-plate silicon waveguide for propagation is proposed. Signal propagation is achieved using a high-resistivity silicon (HR-Si) substrate placed between two metal plates to provide a 2D-only propagation medium. Fig. 1 (b) proposes a 16-antenna and 256-core topology. In this scenario the use of 16 TSV antennas can be considered as electrodes, multiple core clusters enable multicast and broadcast communications. Several papers in the WiNoC area have already taken up these mesh network architectures [16], until 256 core systems [17]. The impact of the total area is minimal, which greatly reduces the footprint of the "antennas".

Through-silicon via (TSV) antennas [18] can be used as RF antennas to transmit the signal to the HR-Si substrate, enabling wireless multi-core links within the substrate at levels above -3 dB. Given the size of the chips, intra-chip propagation must be feasible for an inter-element distance of 1 cm to 2 cm.

As the manufacture of TSV antennas is complex, slot antennas were subsequently developed in order to excite the propagation channel and validate by measurement our approach. The importance of the transmission level is secondary to the -3 dB bandwidth. The transmission level must be as constant as possible over the widest possible frequency band. For this study, the working frequency of the antennas was set at 60 GHz for 6-mm and 14-mm inter-element distances.

In this paper, the characterization and control of the dedicated channel is studied in order to maximize the bandwidth. Section II covers the related work. Section III then describes our approach, demonstrates the need to control the propagation between two metallization layers, and presents the design, simulation and measurement in the frequency band [30-67] GHz of two antennas etched in the upper metal plate of a silicon substrate using HFSS^{TM} electromagnetic simulation software based on Finite Element Method [19]. The realization of the absorbent boundaries from a controllable bias voltage is demonstrated, where HR-Si is combined with a low-resistivity silicon (LR-Si) absorbing layer. The transmission and bandwidth results are compared with various studies on WiNoCs from the literature. Then, the analysis in the frequency and time domain, and the possible data rates for each circuit with several LNA configurations are evaluated for different bias voltages. Finally, we present our conclusions and highlight several potential areas for improvement.

II. RELATED WORK

Several studies aiming to improve the performance of wireless networks can be found in the literature. On the one hand, the strong potential of WiNoC has been studied from an architectural point of view [20]. In [21], the voltage frequency island (VFI) split design, used in combination with new NoC architectures like the millimeter-wave small-world wireless NoC (mSWNoC), enabled power savings in multi-core chips. A detailed performance evaluation was used to determine the design trade-offs for different millimeter-wave wireless NoCs (mWNoCs) in [22]. On the other hand, the architecture proposed in [23] tends to reduce latency and increase throughput of wireless networks through CNT-based inter-subnetwork wireless interconnection. The need to reduce the power consumption and latency of circuits was

also studied in [24] via a mapping algorithm for the NoC application. To enhance inter- and intra-chip communication performance, the Zenneck surface wave interconnection technique is used in [25], resulting in reduced power consumption (by up to ∼1.3X), faster signal propagation speeds (up to 67%), and operation across a wide frequency bands. However, this study remains theoretical and has not yet been tested in practice. Other interconnects such as optical interconnects that can supplement WiNoCs have been studied and are summarized in [4]. In [26], optimizing optical networks-on-chip (ONoC) with wavelength division multiplexing (WDM) improves performances. However, ONoC suffers from thermal and delay problems. WiNoC technology is promising from a propagation point of view with the study in [27] of the intra-chip propagation channel at 200 GHz demonstrating the possibility to obtain a -3 dB wide bandwidth for high transmission levels. In [28], the WiNoC system reduces latency by up to 43.97% compared with existing architectures. In [29], work on the impact of temperature on silicon has been done for tunable resonators. The temperatures ranged from 30°C to 150°C. The study shows that the thermal properties of silicon have little impact on the resonators unlike FR4 for temperatures up to 100°C. Given the application of the WiNoC, the power will be low. Other studies highlight the importance of antenna placement on circuit performance [30], [31] but always with a narrow bandwidth. In [32], the inter-element transmission was improved via directional antennas that require the exact location of the receiving and transmitting antennas to be determined. However, the interference in the signal propagation does not allow a high bandwidth to be obtained.

In order to evaluate the characteristics of WiNoC systems, the OOK modulation has most often been used. This modulation offers the advantages of having low power consumption, being less complex than BPSK and QPSK modulations and being compatible with CMOS technology [33], [34].

Unlike metal NoC interconnects, WiNoC allows lower latency and power dissipation of the circuits [35]. Intra-chip communication is studied in [12] and [36] via on-chip antennas in K-band (26-40 GHz) and shows strong potential for broadcast communication. In the literature, few studies have performed a thorough electromagnetic analysis of the propagation channel at the intra-chip level.

The study in [37] focuses rather on the difficulties related to the propagation, such as the transmission frequency, operating temperature, dielectric losses or molecular absorption attenuation. The aim of the present work is to characterize and to improve the propagation channel on silicon at the intra-chip level by achieving high bandwidth for a wireless network-on-chip at 60 GHz.

III. SIZING OF THE PROPAGATION CHANNEL, FREQUENCY BAND [30–67 GHZ]

A. DESIGN

In this section, the propagation characteristics of the dedicated silicon layer are studied. With the aim of demonstrating the potential and interest of using lossy surrounding layers to optimize the bandwidth in the propagation channel, two antennas are proposed for transmitting signal in the channel. The process of making the absorbing layers will be covered in part B. The interest of metallizing the top side of the dedicated silicon substrate is shown in Fig. 2. The comparison of two propagation structures, without and with a metallic top plate is done. The antennas are designed to operate at 40 GHz with substrate thickness of 675 μm. The upper metallization and the aluminum ground plane limit radiation in the z-plane [27], [31] and thus increase the transmission levels. The advantage of a dipole is its simplicity of fabrication.

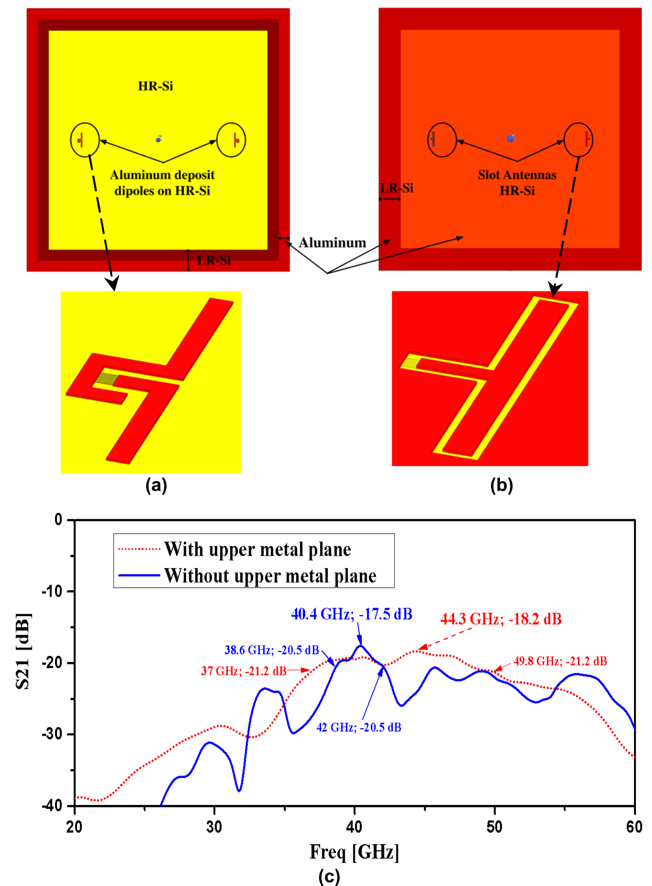

FIGURE 2. Influence of metallization on the top side of a silicon substrate in [20–60 GHz] frequency band (a) partial metallization; (b) total metallization; (c) S_{21} simulated parameters.

Fig. 2 (a) shows a circuit with partial aluminum metallization on the edges of the substrate (red side). The two dipoles are etched on high resistivity silicon (HR-Si) (yellow side) surrounded by a low resistivity silicon LR-Si acting as an absorber. In Fig. 2 (b), the aluminum metallization is total, as explained earlier, the dipoles are embedded in HR-Si to form a slot antenna. Antennas are surrounded by LR-Si. The LR-Si is formed by a doped HR-SI region, i.e. an integrated $N^{+}PP^{+}$ junction. Fig. 2 (c) shows HFSS^{TM} simulation results, in particular the transmission between antennas for both cases.

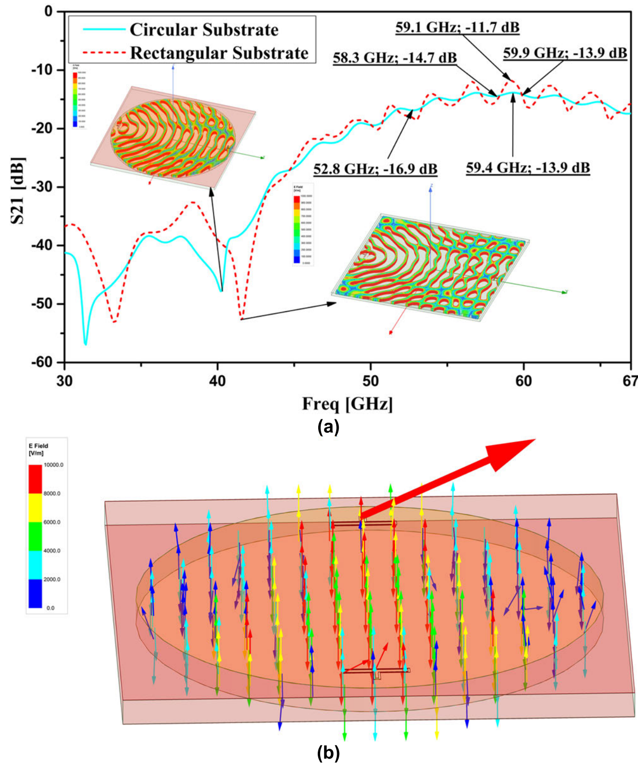

FIGURE 3. (a) Comparison between a circular and rectangular substrate on the parameters S_{21}, simulation HFSS^{TM}; (b) electric field vectors mapping at 60 GHz.

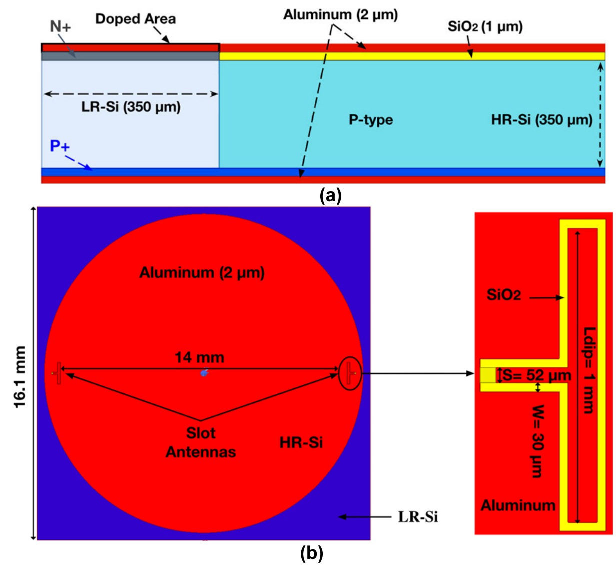

FIGURE 4. 14-mm inter-element distance: (a) cross-sectional view of the simulated structure; (b) top and front views of the structure and a slot antenna.

In the first case (blue curve), the dipole antennas are formed via an aluminum deposit on the top surface of the silicon substrate. much of the signal propagates in the silicon but a part of the energy is radiated into the air. To overcome this problem a parallel plate waveguide is proposed.

The use of a metal shield improves the propagation channel by reducing the number of modes. The velocity of the waves in the air and in the substrate is different, this difference introduces wave recombination which leads to ripples on the transmission versus frequency.

In the second case (red curve), slot antennas are etched into the aluminum. The propagation medium is then in the silicon substrate, the electromagnetic radiation is guided by the metal parallel plates waveguide, making it possible to reduce the transmission zeros and thus to increase the bandwidth to - 3 dB. Indeed, with a top-side metallization, the bandwidth at - 3 dB is multiplied by 4, passing from 3.5 GHz to 12.5 GHz for similar transmission levels, S21 = -18.2 dB with top-side metallization compared with S21 = -17.5 dB without top-side metallization.

To increase the bandwidth, the geometrical aspect of the substrate was studied considering a silicon parallel-plate waveguide, as presented in Fig. 3 (a). Transmission zeros EM field mapping are presented for both cases. The substrate size was reduced from 675 μm to 350 μm in order to propagate a single TE mode and thus allow 2D propagation as shown in Fig. 3 (b). The signal propagation comparison between rectangular and circular shapes was performed.

A structure with a circular substrate can improve the bandwidth in transmission by avoiding the recombinations present in the corners of the rectangular substrate. The transmission between antennas has less interference with a circular substrate, we obtain a bandwidth at -3 dB higher than 14 GHz against only 1.6 GHz for a rectangular substrate. These preliminary studies allowed us to move to a structure with doped silicon, as explained in the next section.

B. FABRICATION

Two distances between antennas were considered, one of 6 mm and the other of 14 mm, in order to make comparisons with the literature and to experimentally validate the concept and shape designed in the previous section. Fig. 4 (a) shows a cross-sectional view of the stacked silicon substrate used in this study. The top surface of the substrate and the ground plane are made of aluminum and are 2 μm thick. A layer of silicon dioxide SiO_2 ($\varepsilon_r = 4$) with a height of 1 μm serves as insulation. The Si-substrate is a P-type one with a thickness of 350 μm chosen to be equal to a guided wavelength λg/4 at 60 GHz. Slot antennas are positioned 350 μm from the doped zones, corresponding to λg/4 at 60 GHz. The LR-Si layer is obtained by biasing an N^+PP^+ junction in the substrate height. There is an N^+ doped area on the top side and a P^+ doped area on the bottom side, obtained with sol-gel solution deposition and a diffusion technique. This layer of silicon can be biased using a negative voltage between the upper and lower metal plates to decrease the resistivity in the substrate thickness and to have an LR-Si absorber [38], [39].

In this layer, therefore, the waves will be attenuated due to the high losses in the LR-Si, which will decrease the amplitude of the waves reflected at the air-silicon interfaces and attenuate the multipath constructive and destructive

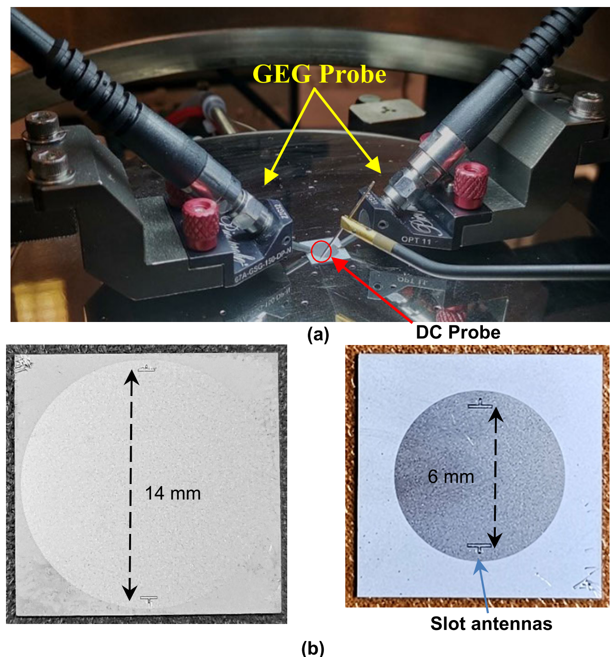

FIGURE 5. Pictures of the measurement device of the probe station device and measured circuits.

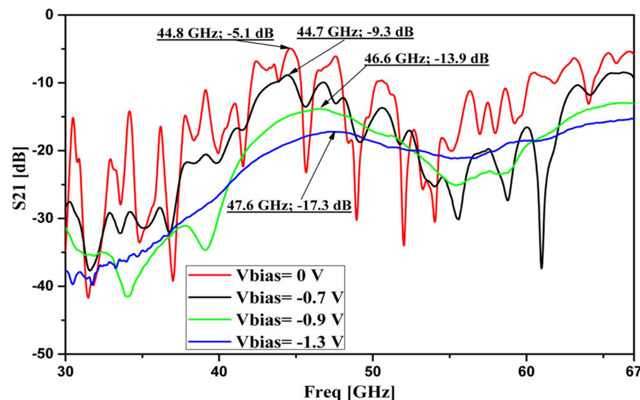

FIGURE 6. S_{21} transmission measurements between two slot antennas in a network for several polarization voltages at a 6-mm inter-element distance.

recombination of the waves [12]. It is possible to use a fixed bias when the process is controlled. However, it is difficult to determine its value with precision, because the sensitivity must be the same on all the biased junction. The goal is to apply a controlled voltage depending on the amount of dopant. This allows the determination of the resistivity value needed to provide high bandwidth for WiNoC communications.

The upper view of the structure is shown in Fig. 4 (b). This consists of a circular HR-Si substrate with two slot antennas etched into the upper metal plate of the silicon substrate and bordered by an LR-Si absorbent.

The antennas are placed at a distance corresponding to $\lambda g/4$ at 60 GHz from the LR part. Fig. 4 (b) shows the circuit dimensions of the slot antennas, designed to resonate at 60 GHz, and their 50 Ω coplanar feed for a 14-mm inter-element distance. This choice of 14 mm was determined by the size of the chips. If we consider chip sizes of 10 mm x 10 mm, an inter-element distance of 14 mm is achievable diagonally. The diameter of the HR-Si substrate is 15.4 mm, and the total width of the structure is 16.1 mm.

The design was completed, simulated and then measured considering a central frequency at 60 GHz. All simulations were performed with HFSS™ and the circuit was measured using a probe station and a ZVA67 network analyzer from Rhodes & Schwarz capable of operating at up to 67 GHz. All measurements were made in the 30–67 GHz bandwidth after calibration with a short, open, load and thru (SOLT) calibration kit to correct errors linked to the RF cables and the internal components of the analyzer.

The measurement setup is shown in Fig. 5 (a). This picture shows the measurement of a circuit for an inter-element distance of 6 mm. Two GSG probes, connected to the ZVA67, are placed directly on the coplanar waveguide (CPW) supply of the slot antennas. A DC probe is used to polarize the LR-Si substrate using a generator providing a negative voltage to forward bias the junction. In Fig. 5 (b), the two circuits characterized in this article are shown for inter-element distances of 14 mm and 6 mm.

The first measurements of the HR-Si substrate structures bordered with LR-Si were performed for an inter-element distance of 6 mm, this distance was initially chosen to study the different channel modes excitation. The diameter of the HR-Si substrate was 7.4 mm, and the total width of the structure was 10.5 mm.

The interest of controlling the air-silicon boundaries is demonstrated by the results shown in Fig. 6. The bias voltages on the LR-Si make it possible to optimize the -3 dB bandwidth. The bias voltages shown in Fig. 6 are the voltages measured on the circuit in the doped region. The higher the applied voltage, the smoother the transmitted signal and the higher the attenuation of the parasitic effects. The -3 dB bandwidths and the maximum transmission measured as a function of the bias voltage of the doped silicon are presented in Table 1 for inter-element distances of 6 mm and 14 mm.

The constraints of circuit fabrication required a minimum length/width of 10.5 mm. The circuit dimensions at an inter-element distance of 6 mm were 7.4 mm^2 in simulation. To satisfy this constraint, the length of the LR-Si was increased from 0.35 mm in the simulation to 1.55 mm in the fabrication, which explains the frequency shift as shown in Fig. 7.

Fig. 8 (a) shows that a matching maximum is present beyond the frequency band available on the measurements setup. After back simulations (green curve on Fig. 8), the simulations performed on the HFSS™ software agree with the measurements of the circuits.

The S_{11} matching level is -20 dB at 64 GHz, with a -10 dB-bandwidth higher than 8 GHz from 59 GHz to a frequency above 67 GHz. The doped silicon provides control over the

TABLE 1. Circuit characteristics measured for inter-element distances of 6 mm and 14 mm.

VBias (V)	Bandwidth at - 3 dB (GHz)	Transmission Max. (dB)	VBias (V)	Bandwidth at - 3 dB (GHz)	Transmission Max. (dB)
0	1.1	-5.1	0	0.9	-7.2
0.4	>2.5	-6.3	0.4	1.1	-8.5
0.4	>2.5	-7.2	0.5	1.5	-10.2
0.5	>2.6	-7.9	0.6	2.2	-11.3
0.7	>3.3	-10.7	0.8	8.3	-12.1
0.7	>4.2	-11.5	0.8	10.5	-12.9
0.8	>4.4	-12.2	0.8	10.6	-13
0.9	>4.4	-12.7	0.8	10.8	-13.6
0.9	>4.5	-13.3	0.9	12.5	-14
1.2	>4.7	-14.4	1	12.9	-15.4
1.3	>5	-14.8	1.1	13.3	-15.6
1.3	>5.1	-15.5	1.2	14.1	-15.7
6 mm inter-element distance			14 mm inter-element distance		

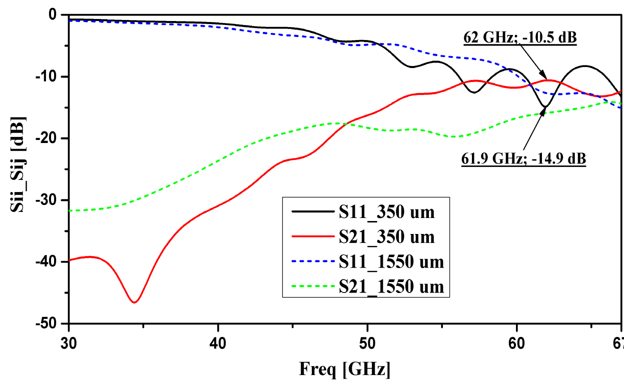

FIGURE 7. S-parameters in simulations for two different length doped zones of, 350 μm and 1550 μm.

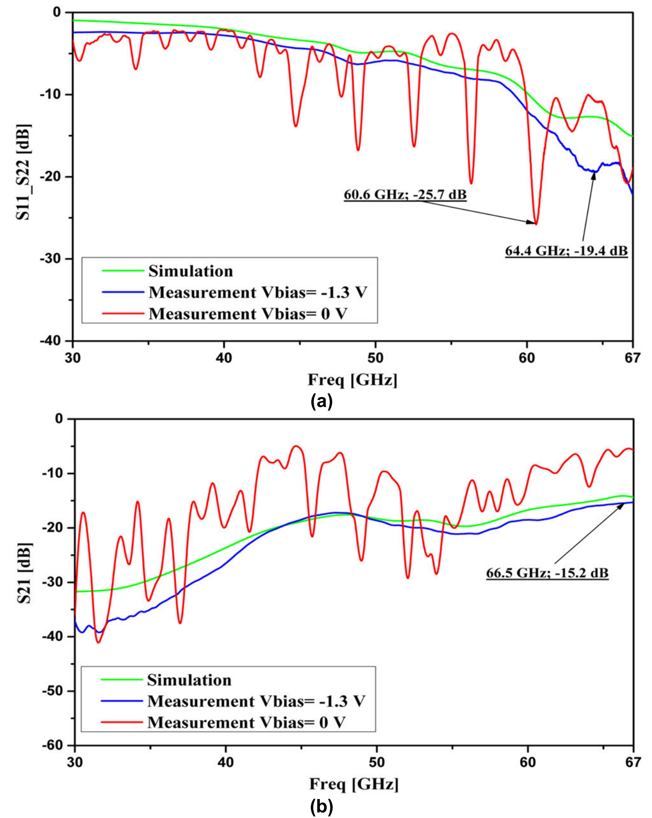

FIGURE 8. Measurements and simulation of a two slot antennas network with a 6-mm inter-element distance (a) S_{11}, S_{22}; (b) S_{21}.

resistivity of the LR-Si. Fig. 8 (b) shows that multipath recombination is decreased when a bias voltage Vbias = -1.3V is applied to the LR-Si substrate for a 6-mm inter-element distance. The transmission maximum measured over the [30–67 GHz] band is -15.2 dB for a -3 dB bandwidth above 6 GHz.

Fig. 9 (a) and (b) present the reflection and transmission coefficients between the two slot antennas at 14-mm inter-element distance with and without bias voltage (Vbias = -1.2V and Vbias = 0V). The significant effect of the polarization on the behavior of the LR-Si layer is clearly demonstrated considering both the S_{11} reflection coefficient and the S_{21} propagation coefficient. The minimum reflection level on the slot ports is obtained for a frequency near 60 GHz. The use of a -1.2 V bias voltage implies a resistivity modification of the layer, which greatly reduces the parasitic effects at the boundaries. This leads to a reduction in the number of resonances. Similar observations can be made regarding the transmission coefficient S_{21}. The transmission coefficient between the two slot antennas is smoother for a control voltage of -1.2 V than without a bias voltage (Fig. 9 (b)) and the transmission zeros are clearly suppressed. The bandwidth of the circuit is between 51.2 GHz and 65.3 GHz corresponding to the V-band [50-75 GHz].

Therefore, the available -3 dB-bandwidth is increased and reaches 14 GHz while it is only 0.9 GHz when Vbias = 0V. The maximum S_{21} level is reduced to S_{21} = -15.6 dB when the bias voltage is applied. At 6 mm, the maximum transmission level is improved by only 0.4 dB compared with the distance of 14 mm.

This small increase can be explained by the fact that the maximum transmission level reached for the 6-mm inter-element distance seems to be higher than 67 GHz. As the width of the LR-Si is multiplied by more than 4, the transmission is lower in this case. For an improvement of the transmission level, the optimal LR-Si length simulated is 0.35 mm, corresponding to λg/4 at 60 GHz. The low transmission level can be emphasized and a simple amplifier would increase this value thanks to the flatness of the transmission. The LNA gain can compensate the losses, as we will see in Part 4. This system does not require an equalizer or any other signal correction device [40], unlike in previous work [41].

The results for the bias were also obtained by electromagnetic simulation (green curve on Fig. 8 and Fig. 9) considering a LR-Si conductivity of 10 S/m. Correlations between measurements and simulations are thus proven, allowing the validation of the bandwidth optimization with the electromagnetic simulation software HFSS™. It is clear that the

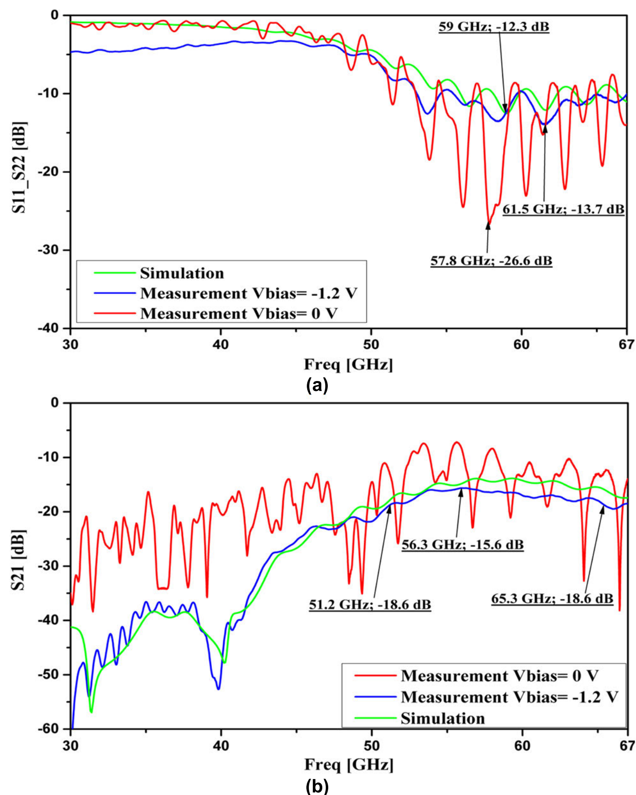

FIGURE 9. Measurements and simulation of a network of two slot antennas with a 14-mm inter-element distance (a) S_{11}, S_{22}; (b) S_{21}.

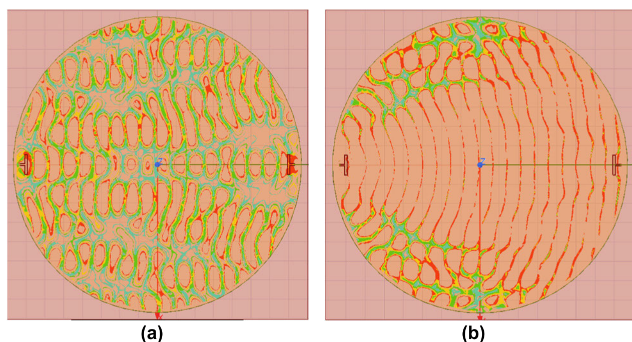

FIGURE 10. EM field mapping (HFSS^{TM}) at 60 GHz (a) without absorber; (b) with absorber.

absorber plays a fundamental role in the propagation of the signal with an attenuation of the transmission zeros as well as an increase in the useful 3-dB bandwidth.

Fig. 10 shows the scattering of the electromagnetic field in a silicon substrate with and without the application of a doped silicon layer. Without the absorber, Fig. 10 (a), the propagation undergoes reflections at its air-silicon boundaries and the field is not uniform.

These reflections cause numerous recombinations of the electromagnetic waves. Indeed, the mapping of the fields reveals areas where the wave is amplified (constructive interference) and areas where it is attenuated (destructive interference). The mapping of the EM fields with absorber,

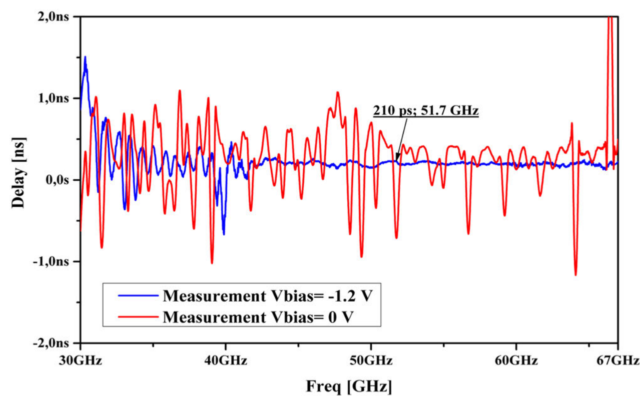

FIGURE 11. Group delay measured with and without bias for an inter-element distance of 14 mm.

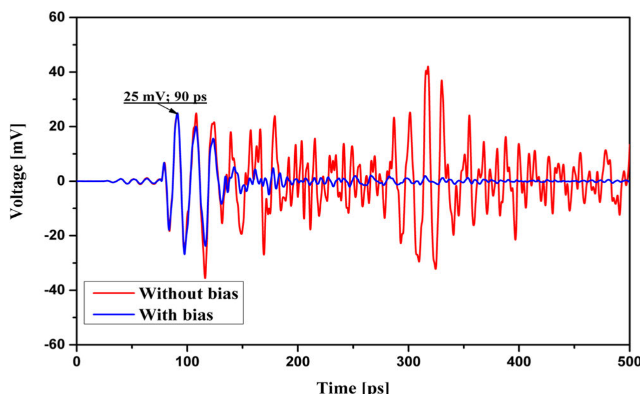

FIGURE 12. Temporal simulation in HFSS^{TM} with and without bias for an inter-element distance of 14 mm.

Fig. 10 (b), gives the image of propagation in a parallel metal structure of infinite dimensions. The low resistivity silicon allows to attenuate the EM recombinations and thus drastically reduce the transmission zeros.

Fig. 11 shows the group delay measured with and without absorber in the frequency band [30-67 GHz]. With bias, the group delay is flat within the operating bandwidth, which is very important in this system. A flat group delay is essential to confirm distortion free transmission and reception of signals. This group delay indicates a linear phase variation over the operating frequency of the antennas. This means that electromagnetic waves can be transmitted and received without dispersion. On Fig. 12, the temporal simulation results have been performed on HFSS^{TM} for an impulse of 1V and a width of 4 ps.

The propagation time between the two antennas is equal to 90 ps in both polarized and non-polarized conditions. Reflections are strongly attenuated when using an absorber.

Table 2 presents the state of the art of existing V-band propagation and compares this with the performance of the slot antennas in the present paper.

The circular substrate shape surrounded by a lossy silicon region acting as an absorber allows transmission at levels comparable to those found in the literature, but with

TABLE 2. Comparison of v-band transmission.

Ref	Frequency band (GHz)	Inter-element distance (mm)	Transmission Max. (dB)	Bandwidth at – 3 dB (GHz)
[18] (Simulations)	60-63	6	-3	<3
[12] (Simulations)	40-80	14.2	-18	28
[42] (Simulations)	50-70	5	-8 to -18	<2
[43] (Simulations)	58-62	10	-30	<4
[44] (Measures)	50-60	12	-14	<10
Slot antennas (Measures)	**30-67**	**6**	**-15.2**	**>6**
Slot antennas (Measures)	**30-67**	**14**	**-15.7**	**14.1**

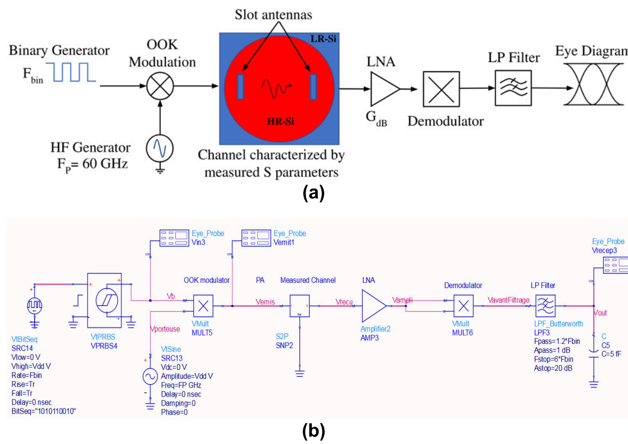

FIGURE 13. (a) Overview of the ADS simplified simulation; (b) ADS program providing the eye diagram and SNR of the measured circuits.

a significantly higher bandwidth of -3 dB. In RF systems requiring high throughput, such as high-speed wireless networks, there is a need for wideband communications. In this paper a -3 dB bandwidth around 14 GHz was obtained for a transmission level of -15 dB, allowing to transmit more data at higher data rates simultaneously. This is a demonstration of channel control in WiNoCs with one of the widest bandwidths available.

IV. TEMPORAL PROPAGATION CHANNEL STUDY IN THE FREQUENCY BAND [30-67 GHz]

The study of the propagation channel allowed us to evaluate the performance of the propagation channel in terms of bandwidth and transmission level. In order to demonstrate the interest, to estimate the possible throughputs and to compare our solution to the state of the art, a temporal study was carried out. As access to temporal measurements was not available (no signal generator or HF oscilloscope), an estimation of the signal-to-noise ratio from frequency measurements was performed using ADS (Advanced Design System) circuit simulations [45].

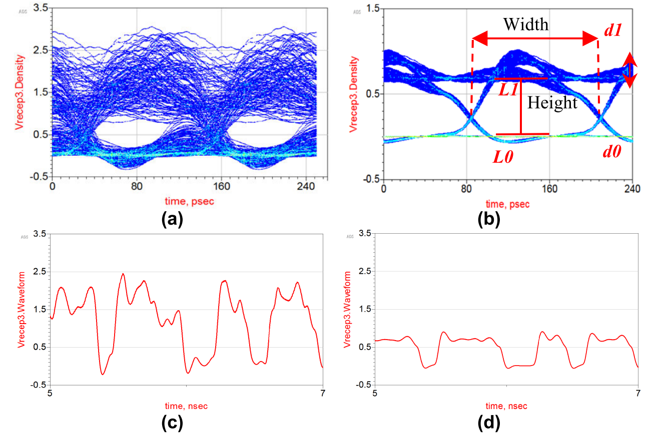

FIGURE 14. (a) Eye diagram without bias; (b) Eye diagram with bias, Vbias = - 1.2 V; (c) output voltage of the receiving part without bias; (d) output voltage of the receiving part with bias, Vbias = - 1.2 V.

This study consisted in estimating the characteristics of the measured propagation channel between two slot antennas for three bias voltages (Vbias = 0 V, Vbias = -1.2 V and Vbias = - 1.3 V). The studied circuits had two antennas located at an inter-element distance of either 6 mm or 14 mm. Fig. 13 (a) and (b) show the simplified simulation overview used to perform this analysis with the ADS circuit simulator and the ADS program providing the eye diagram and SNR of the measured circuits. A very simple OOK transceiver designed to assess the channel performances was used. A binary sequence and sine wave generator in an OOK modulation forms the transmitting part, which excites the propagation channel described by the measured S-parameters, collected in a Touchstone file. The receiver part contains a low-noise amplifier (LNA) with a variable gain G, and a demodulator consisting of a multiplier to facilitate filtering, which gives a signal:

$$b^2 cos^2 (\omega t + \varphi) = \frac{b^2(1 + cos (2\omega t + 2\varphi)}{2} \quad (1)$$

Using a Butterworth low pass filter, b^2 was obtained, which represents the binary symbol. The ADS© circuit simulation tool provides eye diagrams that allow the performances of V-band circuits to be evaluated. Several aspects of bit rate and amplifier gain provide the signal-to-noise ratio (SNR).

Fig. 14 (a) and (b) show the eye diagrams obtained without and with a -1.2 Vbias voltage for a binary data rate F_{bin} = 8 Gbps and an overall gain (LNA) of 25 dB. The noise returned on the LNA amplifier is zero (Nf = 0 dB), which allows us to quantify the noise due to the propagation channel. Considering the measurement results, the carrier frequency was set to 60 GHz.

Fig. 14 (b) shows the different parameters for calculating the SNR using (2): L1 level is the "1", L0 is the "0", d1 and d0 are the noise levels linked to L1 and L0. The height of the

TABLE 3. Eye diagram characteristics for two slot antennas, 14-mm inter-element distance.

F bin. (Gbit/s)	Vbias (V)	gain LNA (dB)	H (V)	W (ps)	SNR (dB)
4	0.4	10	x	208	6.3
		20	x	162	6.7
	0.8	10	0.04	243	18.6
		20	0.35	246	18.5
	1.2	10	0.2	245	19.3
		20	0.2	245	19.3
8	0.4	20	0.07	98	8.5
		25	0.21	113	8
	0.8	20	0.31	121	17.8
		25	1	126	17.7
	1.2	20	0.18	120	16.5
		25	0.57	120	16.5
10	0.4	10	x	x	8
		25	0.11	x	8
	0.8	10	0.03	93	16.9
		25	0.91	94	16.7
	1.2	10	0.016	88	15
		25	0.49	93	14.8
12	0.8	20	0.213	78	14.3
		30	2.13	79	14.3
	1.2	20	0.07	x	9.8
		30	0.85	x	11.4
14	0.8	30	1.5	53	11.3

eye diagram is noted H and its width W.

$$(\mathrm{SNR})_{\mathrm{dB}} = 20 \cdot Log_{10}\left(\frac{L_1 - L_0}{d_1 + d_0}\right) \tag{2}$$

Fig. 14 (c) shows the deterioration of the propagation channel without polarization. The levels are higher in Fig. 14 (c) than in Fig. 14 (d) but they also show more parasitic effects. Increasing the bias voltage reduces these effects.

Table 3 and 4 resume the eye diagram characteristics for two slot antennas at 60 GHz, for inter-element distances of 14 mm and 6 mm. These results are obtained considering bias voltages of -0.4 V to -1.2 V and -0.4 V to -1.3 V respectively, corresponding to the voltages measured on doped silicon. In addition, the overall gain (LNA) has an important impact on the power consumption of the circuits [46].

In Table 3, considering a binary data rate of 8 Gb/s and a 20 dB gain, the SNR level is not obtainable without polarization, while it is 16.5 dB with a -1.2 V polarization. The characteristics of the eye diagram give a height H = 0.18 V and a width W = 120 ps for a control voltage Vbias = -1.2 V. Without bias voltage, these characteristics are not obtainable.

For this same binary data rate of 8 Gb/s, Table 3 shows that a bias above a voltage of - 0.8V would be sufficient to obtain a high SNR, which could make it possible to reduce the consumption of the circuit. This demonstrates the interest of controlling the air-silicon boundaries by using a bias voltage. Indeed, a high power consumption followed by a high bit rate leads to a high overall gain in order to obtain a good SNR. In sum, the improvement of the SNR is related to the increase of the bias voltage.

The characteristics provided by the eye diagrams of the circuits with the 14-mm and 6-mm inter-element distances

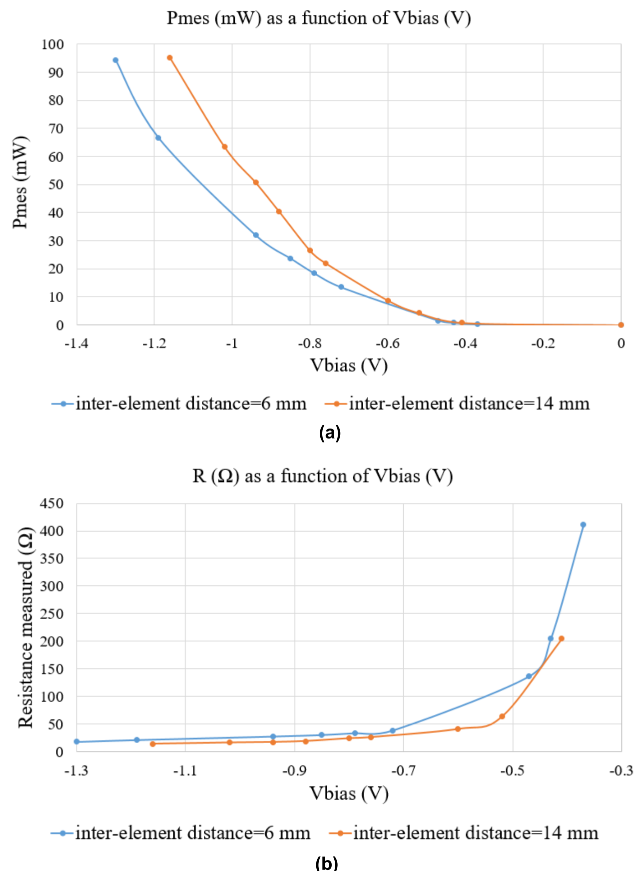

FIGURE 15. (a) Pmes (mW) as a function of Vbias (V); (b) R (Ω) as a function of Vbias (V).

allow us to evaluate the maximum throughput Fbin expected considering our measurement. This is 14 Gb/s for an SNR of 11.3 dB with 14 mm (Table 3) and 12 Gb/s for an SNR of 14.2 dB with 6 mm (Table 4). Based on [47], the bit error rate would be less than 10^{-7}, which is comparable to results in the literature [37].

The increase of Fbin degrades the SNR and thus the quality of the information transmission whatever the inter-element distance. It is necessary to limit the recombination of electromagnetic waves, which limits the bandwidth and, therefore, the available data rates.

Fig. 15 (a) shows the evolution of the power measured in the doped region on the 14-mm and 6-mm circuits as a function of bias voltage. The overall power measured in mW increases progressively as the negative bias voltage increases. If we consider a bias voltage of -0.8 V, the 14-mm inter-element circuit consumption is 26 mW for the maximum throughput of 14 Gb/s and a SNR of 11.3 dB, as shown in the eye diagram characteristics in Table 3. The bias of the lossy area corresponds to an energy of 1.86 pJ/bit. To this energy should be added the consumption of the digital and analog parts.

In the best case, the digital receiver consumes a maximum of 4.7 mW, as the power consumption of all sub-blocks is

TABLE 4. Eye diagram characteristics for two slot antennas, 6- mm inter-element distance.

F bin. (Gbit/s)	Vbias (V)	gain LNA (dB)	H (V)	W (ps)	SNR (dB)
4	0.4	15	x	66	6.2
		25	x	x	x
	0.8	15	0.04	237	15.7
		25	0.38	241	15.5
	1.3	15	0.06	245	21.1
		25	0.58	247	20.7
8	0.8	15	x	30	6.7
		25	0.05	x	6.8
	0.9	15	0.03	91	13.3
		25	0.28	92.5	13.6
	1.3	15	0.05	113	18.8
		25	0.49	114	18.7
10	0.8	15	x	2	5.4
		25	x	4	5.7
	0.9	15	0.06	x	8
		25	0.06	0.04	8.1
	1.3	10	0.01	64	17.6
		25	0.42	92.5	16.9
12	1.3	25	0.29	55	14.2

TABLE 5. Estimates of global consumptions for 6 and 14- mm inter-element distance.

F bin (Gbit/s) / Inter-element Distances (mm)	Best case: energy consumption (pJ/bit)	Worst case: energy consumption (pJ/bit)
14 mm / 14 Gbit/s	3	4.12
6 mm / 12 Gbit/s	9.3	10.55

reduced. For the worst case a consumption of the digital part of 20 mW was considered, corresponding essentially to the consumption of the analog-to-digital converter (ADC) [48]. The LNA consumption is 11.7 mW [49]. In total, the worst case power consumption would be around 58 mW (26 mW (bias absorbing area) + 20 mW (ADC) + 11.7 mW (LNA)) for a data rate of 14 Gbit/s, i.e. an energy consumption of 4.12 pJ/bit which is low. In the best case, the power consumption would be near 42.4 mW (26 mW (bias absorbing area) +4.7 mW (ADC) +11.7 mW (LNA)) which implies an energy consumption of 3 pJ/bit. Total consumptions estimates are presented in Table 5 for worst and best cases.

This power consumption compared with [50] needs to be put into perspective, because WiNoC communications will represent only a small percentage in the total consumption because they are principally used for broadcast communication [51].Indeed, this power consumption only happens during exchanges. Apart from the power consumption, the main interest of bias is to control the propagation channel in order to achieve a high bandwidth.

Fig. 14 (b) shows the variation of the measured resistance of the LR-Si area as a function of the bias voltage. The behavior of a diode is represented, and the curve indeed presents a high resistance when the bias voltage is low (Vbias = -0.4 V) as well as rapid variation of the resistance for voltages varying between -0.6 V and -0.4 V, then a constant evolution of the resistance between -0.6 V and -1.3 V.

The possibility to control the air-silicon boundaries in the case of WiNoC applications has been demonstrated. This controllable boundary behavior could be used for point-to-point or on-demand broadcast transmissions.

V. CONCLUSION

In this paper, the interest of controlling the propagation channel on silicon, in order to obtain large useful bandwidths for high data rates, has been demonstrated. First, the implementation of slot antennas inside a silicon substrate was considered. The propagation between two slot antennas, based on parallel plate propagation channels was simulated and measured in the [30–67 GHz] frequency band.

Circular substrates surrounded by a low-resistivity absorber were introduced to optimize available bandwidth. The air-silicon interaction is limited by the application of a low resistivity silicon (LR-Si), resonances are thus reduced. Simulation results and measurements on slot antennas are very promising. When a bias voltage of -1.2 V is applied to the absorbing layer, a bandwidth of -3 dB of 14 GHz (between 51 GHz and 64 GHz) was measured for the inter-element distance of 14 mm, which is one of the largest bandwidth found in the literature.

Subsequently, the propagation channel characteristics between two slot antennas were estimated via circuits simulation of OOK modulation on ADS software for inter-element distances of 14 mm and 6 mm. Different polarization voltages allowed to evaluate the maximum circuits throughput, which resulted in achieving data rates of 14 Gb/s and 12 Gb/s for bit-energy efficiencies of 1.86 pJ/bit and 7.83 pJ/bit, respectively at the level of the biased zone.

Solutions are suggested to improve the transmission coefficients and to widen the bandwidth to -3 dB, inspired by anechoic chambers for the shape of the absorber. The continuation of this study is in progress using several antennas on the same substrate and examining the effects of different border shapes.

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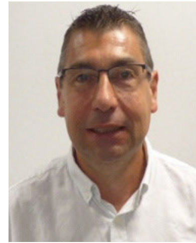

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