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RESEARCH ARTICLE

Algorithmic Optimization of Transistors Applied to Silicon LDMOS

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ABSTRACT We propose a pioneering approach that integrates optimization algorithms and technology computer-aided design to automatically optimize laterally-diffused metal-oxide-semiconductors (LDMOS) with a field-oxide structure. We define the ratio of the square of the breakdown voltage divided by the specific on-resistance as the figure-of-merit (FOM) and the objective function of our optimization. We compare the performance of three different algorithms: Nelder-Mead, Powell, and Bayesian Optimization. We show how the LDMOS performance evolves as each of the three optimization algorithms reach their optimized structure. We show that a straightforward Nelder-Mead optimization leads to a local optimum when optimizing over six input parameters. We find that Bayesian Optimization is the most data-efficient method to find the global optimized structure in the multi-domain design space.

INDEX TERMS Bayesian optimization, LDMOS, nelder-mead algorithm, power semiconductor device, powell algorithm, step gate field oxide structure.

I. INTRODUCTION

The mass production of consumer electronic devices has recently increased the demand for power integrated circuits [1], [2], [3]. Silicon-based laterally-diffused metal-oxide-semiconductor (LDMOS) field-effect transistors are widely used in low-voltage to high-voltage power electronic applications [4], [5], [6], [7], [8], [9]. LDMOS can easily be integrated with bipolar junction transistors and CMOS technology. Therefore, LDMOS transistors are the most popular power device to implement the ''smart power integrated circuits (IC),'' which have automotive, motor control, power management IC and factory automation applications.

Researchers and engineers are dedicated to pursuing a ''perfect'' switch with an infinite breakdown voltage (BV) and a zero resistance ($R_{ds(on)}$) in power electronic systems [10]. An ideal transistor can work as a switch without losing any energy during its duty cycle. The breakdown voltage in LDMOS transistors can be improved by increasing the length of the drift region and adjusting doping profiles to realize the reduced surface field (RESURF) condition [11], [12], [13]. On the other hand, to improve the on-state resistance, the total length of the power device needs to be reduced. Moreover, on-state resistance can also be improved by increasing the device width, but a device with simultaneous smaller width and length is preferred for cost. This increased device size cost is captured by the specific on-resistance ($R_{sp(on)} = R_{ds(on)} \times Area$, where Area is the total length of the device (half-pitch) times the width of the device in the Z-direction (1 μm in our simulations in the section II-A)). Therefore, there is a tradeoff between breakdown voltage and specific on-state resistance. The quality of a given technology is usually measured by a figure-of-merit (FOM) equaling $BV^2/R_{sp(on)}$. A key to lead experimental efforts is the use of technology computer-aided design (TCAD) simulations [14], [15].

For higher voltage applications, a field-oxide (FOX) is required in the LDMOS [16]. However, an open question is

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what the best shape for the FOX for an LDMOS is. To answer the question on what the best FOX shape is, the optimal doping profile that goes together with the FOX shape needs to be determined. Manually determining the optimal FOX is a painstaking process. A traditional method to understand the behavior of LDMOS with field oxide structure is to find the analytical solution [17], [18]. There is some research combine TCAD simulation and machine learning to accelerate the development of simulation works in different areas [19], [20], [21], [22], [23], [24], [25], but to date, no automated methodology is available to determine the optimal doping profile for a given FOX shape.

This article proposes a novel optimization framework to automatically optimize power device using the combination of TCAD and numerical optimization algorithms. We define six input parameters for a LDMOS with a stepped-gate field-oxide structure (SG-FOX). We evaluate three different optimization methods: Nelder-Mead, Powell, and Bayesian and apply them to TCAD simulations to improve the device's FOM and then compare the results from the three different optimization algorithms. The result shows that Bayesian Optimization takes fewer iterations than other optimization methods, while returning a comparable FOM compared to the Nelder-Mead and Powell. Therefore, Bayesian Optimization can be a more efficient optimization algorithm than the Nelder-Mead and Powell in finding the global extremum for the device optimization problem.

II. METHODOLOGY

In Subsection A, we introduce an SG-FOX LDMOS device and define the input parameters that we will change throughout our optimization. We also describe some characteristics of the SG-FOX LDMOS device. Subsection B defines the FOM to quantify the device performance and introduces the numerical optimization algorithms we use in this work. At the end of this section, we explain the optimization flow for this work in Subsection C.

A. DEVICE TCAD SIMULATIONS AND CHARACTERISITCS

Fig. 1 shows a schematic diagram of the initial device structure of an n-channel LDMOS with a SG-FOX structure. The concept of using SG-FOX in LDMOS was first introduced in 1995 [26], [27]. We use a p-doped background and Gaussian doping profiles to define the source, the drain, the body region, the drift region, and a p-type buried layer under the drift region. The source/drain are n^+ Gaussian profiles placed on the device surface on both sides. The body region is a p-type Gaussian profile placed on the uniform background. The drift region is built using three n-type Gaussian profiles. The first drift Gaussian is the main drift region, and the doping concentration value is higher than the uniform p-type background concentration but lower than the p-body Gaussian profile. The second drift Gaussian is used to control the leakage current on the device's surface and the channel length. The doping concentration of the second drift Gaussian should be higher than the first drift Gaussian. The third Gaussian

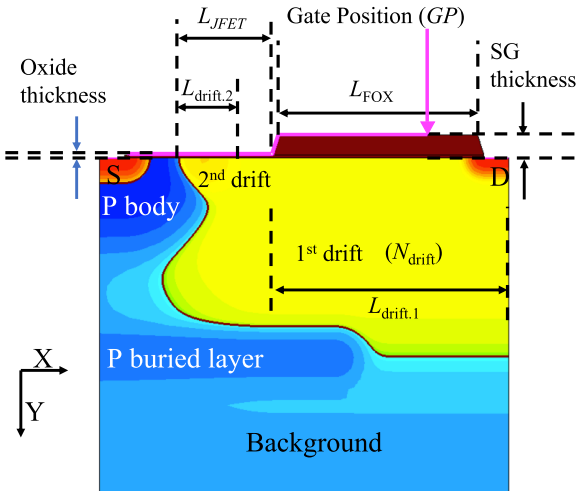

FIGURE 1. Schematic cross-section of a laterally-diffused metal-oxide-semiconductor (LDMOS) with SG-FOX structure. This device structure is the initial condition for the Nelder-Mead (NM) and Powell algorithms. For Bayesian Optimization (BO), the bounds of BO and other parameters are listed in TABLE 1.

doping is located under the drain Gaussian profile and has the same doping profile as the second Gaussian doping.

The following parameters do not change during optimization: The background is a p-type 2×10^{16} cm^{-3} uniform doping. The gate oxide thickness is 12 nm, and the step gate (SG) oxide thickness is 80 nm. The origin (X $= 0$ μm, Y $= 0$ μm) is at the top left corner of the device. The n^+ source/drain has a doping concentration peak value of 10^{20} cm^{-3}, and the length of the peak line is 0.1 μm. The p-body Gaussian body doping has a depth of 0.4 μm and a peak value of 2×10^{18} cm^{-3} starting from the silicon surface. The length of the peak line of the p-body is 0.1 μm. The drift region consists of three Gaussian doping profiles. The peak line of the first drift doping is located at a depth Y $= 0.3$ μm. The second drift doping starts at the surface with a doping concentration value 5×10^{17} cm^{-3} and starts at X $= 0.3$ μm. The third drift doping has the same doping concentration, doping depth, and length of the peak line as the second drift doping. The third drift doping peak line ends on the drain side of the device. A deeper p-buried layer is located on Y $= 0.8$ μm with a peak value 9×10^{16} cm^{-3}.

Six parameters, listed in TABLE 1, are optimized: 1) the peak doping concentration ($x_1 = N_{\text{drift}}$) of the first doping, 2) the length of the first Gaussian doping peak line ($x_2 = L_{\text{drift.1}}$), 3) the length of the second Gaussian doping peak line ($x_3 = L_{\text{drift.2}}$), 4) the gate position ($x_4 = GP$), 5) The length of SG-FOX ($x_5 = L_{\text{FOX}}$), 6) the length of the junction field-effect transistor (JFET) region ($x_6 = L_{\text{JFET}}$). The initial value and bounds for algorithms are also listed in TABLE 1.

We define these six parameters as input parameters to our optimizations. Changing the input parameters results in a device with a different FOX shape and drift region shape and has a large impact on the LDMOS performance. Our optimization problem is to find the highest FOM device by changing the input parameters.

TABLE 1. Six parameters in TCAD simulation as the inputs for the optimization problem. The initial values are for Nelder-Mead and Powell algorithms and the bounds are for Bayesian Optimization.

Symbol	Definition	Initial Value	Bound
N_{drift} (cm^{-3})	The peak value of the 1st Gaussian doping	5×10^{16}	5×10^{16} – 2.1×10^{17}
$L_{\text{drift.1}}$ (nm)	The length of the 1st Gaussian doping	950	750 – 1050
$L_{\text{drift.2}}$ (nm)	The length of the 2nd Gaussian doping	80	30 – 230
GP (%)	Percentage of the FOX would be covered by poly gate	75	10-99
L_{FOX} (nm)	The length of field oxide	800	200 – 1100
L_{JFET} (nm)	The length of JFET region	380	80 – 380

We use a commercial drift-diffusion package [28] to perform our simulations and use default silicon parameters. The Fermi-Dirac distribution is used for carrier distributions. We use the Lombardi model as the mobility degradation model at the silicon-insulator interface and the Philips unified mobility model in the bulk region. The generation-recombination, doping-dependent, temperature-dependent Shockley-Read-Hall, Auger, and the van Overstraeten models are used [29]. The bandgap narrowing model is also included.

We calculate the breakdown voltage (BV), the specific on-state resistance ($R_{\text{sp(on)}}$), and the leakage current (I_{leak}) in the TCAD simulation. The breakdown voltage is extracted from I_{DS}-V_{DS} simulations by ramping the voltage on the drain until the solver no longer convergences. We calculate the on-state drain-to-source resistance ($R_{\text{ds(on)}}$) by computing the current under the boundary condition $\text{V}_{\text{GS}} = 5$ V, $\text{V}_{\text{DS}} = 0.1$ V, and $\text{V}_{\text{BS}} = 0$ V. The specific on-state resistance is then $R_{\text{sp(on)}} = R_{\text{ds(on)}} \times Area$. The leakage current of the SG-FOX LDMOS device is defined as the drain current under the OFF-state bias condition ($\text{V}_{\text{GS}} = 0$ V, $\text{V}_{\text{DS}} = 5$ V, $\text{V}_{\text{BS}} = 0$ V). We design the SG-FOX LDMOS with an off-state leakage current smaller than 10^{-13} A/μm. We extract BV, $R_{\text{sp(on)}}$, and I_{leak} of the SG-FOX LDMOS device in each iteration of the optimization process.

B. OPTIMIZATION ALGORITHMS

We define the objective of our optimization as the figure of merit $\text{FOM} = BV^2/R_{\text{sp(on)}}$ in the six-dimensional input space we defined. This FOM is one of the most well-known metrics for evaluating the performance of power devices [30], [31]. A higher FOM indicates that the device has characteristics closer to an ideal switch. Researchers can use this FOM to gauge the performance of a power device. We directly define this FOM as the objective function to be optimized by our algorithms. Our goal can be expressed mathematically as

$$\boldsymbol{x}^* = \arg\max \text{FOM}(\boldsymbol{x}) = \arg\max \frac{BV^2}{R_{\text{sp(on)}}} \tag{1}$$

where we wrote our input parameters in vector form $\boldsymbol{x} = \{x_1, x_2, \ldots, x_6\}^T = \{N_{\text{drift}}, L_{\text{drift.1}}, \ldots, L_{\text{JFET}}\}^T$. We perform a grid search, a Nelder-Mead (NM), a Powell, and a Bayesian Optimization (BO). We choose NM and Powell since they can optimize the objective in a design space without gradient information. BO algorithms can also find the global optimal solution without requiring gradient information. We selected these algorithms that do not need spatial gradient information because, in general, the calculation of gradient information in a completely unexplored unknown space requires additional computational resources, which increases the time required to find the optimal solution. We briefly explain the four algorithms in the following subsections:

1) THE GRID SEARCH METHOD

The most naïve optimization method is the grid search method, in which the FOM is calculated on a regular grid spanning several input parameters. Performing a grid search on a six-dimensional space is computationally prohibitive, so we only apply it on a two-dimensional space: N_{drift} ranging from 3×10^{16} cm^{-3} to 2.1×10^{17} cm^{-3} in steps of 10^{16} cm^{-3} and GP ranging from 5% to 95% in steps of 5% and another data point at 99%, not taking 100% to avoid numerical issues in the TCAD simulations. Therefore, the 2D grid search FOM is evaluated $19 \times 20 = 380$ times. We demonstrate the grid search result in the two-parameters optimization problem in section III-A.

2) THE NELDER-MEAD ALGORITHM

The NM algorithm uses a simplex, a polytype with a number of vertices equal to $n + 1$ (n is the dimension of the input space), to traverse the n-dimensional input space to find the optimal point $\boldsymbol{x}^*$. For example, the simplex in a 2-D space is a triangle (with $n + 1 = 3$ vertexes). The NM algorithm evaluates the objective function and optimizes it under four different operations: reflection, expansion, contraction, and shrinkage. This simplex will change its size and traverse the n-dimensional space until the algorithm reaches the stopping criterion. [32] provides a detailed flow chart of the NM algorithm.

3) THE POWELL ALGORITHM

The Powell algorithm starts from an initial data point $\boldsymbol{x_0}$ and executes a line search in the first direction, which is determined by changing the first input parameter (x_1). The optimal point in the first direction is $\boldsymbol{x_1}$. Next, the algorithm performs a line search in the second direction starting from $\boldsymbol{x_1}$, by changing the second input parameters (x_2). The Powell algorithm finds the optimal points in different directions and gradually approaches the final result. After running n line searches, the $(n+1)^{th}$ direction is determined by the direction from the data point $\boldsymbol{x_0}$ to the point $\boldsymbol{x_n}$. The line search process

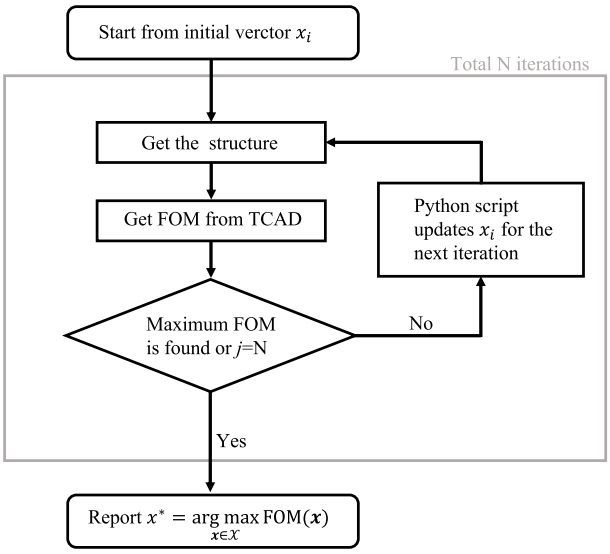

FIGURE 2. The optimization workflow. We use python to generate the updated structure using the NM, Powell, or BO algorithm. In the flow chart, i is the number of parameters in TCAD simulations, j means the j^{th} iteration in the optimization loop. For NM and Powell, an initial guess parameter set is provided at the start, for BO, a range for each of the input parameters is provided. For NM and Powell, a convergence criterion is specified while for BO, the number of iterations is fixed.

continues until the stopping criterion is reached. A detailed explanation can be found in [32].

4) BAYESIAN OPTIMIZATION

Bayesian Optimization needs bounds for all input variables and a number of iterations (N). BO has two critical components: the surrogate model and the acquisition function. The surrogate model is a Bayesian statistical model attempting to replicate the objective function. The acquisition function is used to decide where to sample the next data point. We use a Gaussian process regression-based surrogate model and the expected improvement (EI) as the acquisition function. Gaussian process regression has been applied successfully in various fields [33], [34]. The posterior probability distribution is updated by the measured result (likelihood) and the prior probability distribution (the distribution before the measurement). After updating the posterior distribution, the acquisition function is based on the ''new'' posterior probability distribution information to decide the next sampling point. For detailed information about BO, we refer to [35].

C. OPTIMIZATION FLOW

Fig. 2 shows the optimization flow chart. We start from a device with a given initial $\boldsymbol{x}$ (NM and Powell) or given bounds (BO). We calculate the device FOM using the commercial device simulator for each iteration. The NM and Powell convergence criterion is Error $< 10^{-4}$. For BO we run 20 iterations in the two parameters optimization case. After each iteration, the optimization algorithm generates a new vector $\boldsymbol{x}_{j+1} = \{x_{1,j+1}, x_{2,j+1}, \ldots, x_{6,j+1}\}^T$, and the commercial simulation software calculates the FOM for the next device.

III. RESULTS AND DISCUSSION

We present the results and the discussion in this section. In subsection A, we perform optimization of just two input parameters: the GP and N_{drift} while fixing the other four parameters to $L_{\mathrm{drift.1}} = 950$ nm, $L_{\mathrm{drift.2}} = 80$ nm, $L_{\mathrm{FOX}} = 800$ nm, and $L_{\mathrm{JFET}} = 380$ nm. We present the results of three different algorithms and compare the initial structure and the final structure. In subsection B, we optimize six parameters using the NM algorithm but find a relatively poor FOM. In subsection C, we use one-stage BO to determine the optimal parameters in the six-dimensional search space. In subsection D, we find more optimized six parameters using a three-stage implementation of the NM algorithm. In subsection E, we discuss the advantages and disadvantages of the NM and BO algorithm.

A. TWO-DIMENSIONAL OPTIMIZATION

Fig. 3 presents the two-dimensional GP and N_{drift} optimization process. We perform the Powell and NM optimization which are deterministic. We also apply the BO but we perform two separate BO optimizations since BO is stochastic. The progress of the optimization is illustrated through the color code, the deeper blue marker means closer to the initial condition, whereas the deeper red markers are closing in on the final result. We perform a grid search, calculating the FOM for 380 devices as outlined in subsection II-B-I) to outline the optimization landscape and use the result as a background. The contour plot reveals an optimal location on the ridge (light green) for $N_{\mathrm{drift}} = 1.20 \times 10^{17}$ cm^{-3}, $GP = 65.0$ %, and the optimized device has $R_{\mathrm{sp(on)}} = 5.42$ m$\Omega\times$ mm^2, $BV = 32.2$ V and FOM $= 191$ kW/mm^2.

The Powell and NM start from the same initial condition, located on $N_{\mathrm{drift}} = 5 \times 10^{16}$ cm^{-3} and $GP = 75$ %, and gradually migrate toward the optimum in Fig. 3(a) and (b). In Fig. 3(a), the Powell algorithm optimizes N_{drift} with fixed $GP = 75\%$. Once the optimal N_{drift} assuming a $GP = 75\%$ is found to be 1.3×10^{17} cm^{-3}, the Powell algorithm optimizes the GP with $N_{\mathrm{drift}} = 1.3 \times 10^{17}$ cm^{-3}. After finding the optimal GP in the optimal N_{drift}, the N_{drift} is re-optimized again and the Powell algorithm continues until convergence in the 108^{th} step. Fig. 3(a) shows two clear search directions and they intersect on the final optimal region. The final device of the Powell method has $N_{\mathrm{drift}} = 1.28 \times 10^{17}$ cm^{-3}, $GP = 73.8$ %, $R_{\mathrm{sp(on)}} = 5.16$ m$\Omega\times$ mm^2, $BV = 31.3$ V and FOM $= 190$ kW/mm^2.

Fig. 3 (c) and (d) show the results from the BO's first and second trials. The BO proceeds seemingly randomly, but both BO final results are in the optimal region of the contour plot. The NM, the Powell, and BOs take 114, 108, and 20 iterations, respectively. We list the final results by different methods in TABLE 2. All four algorithms can finally achieve an optimal device with similar performance. However, BO is the most data-efficient method since it takes the fewest steps to get a comparable result in the two-dimensional optimization problem.

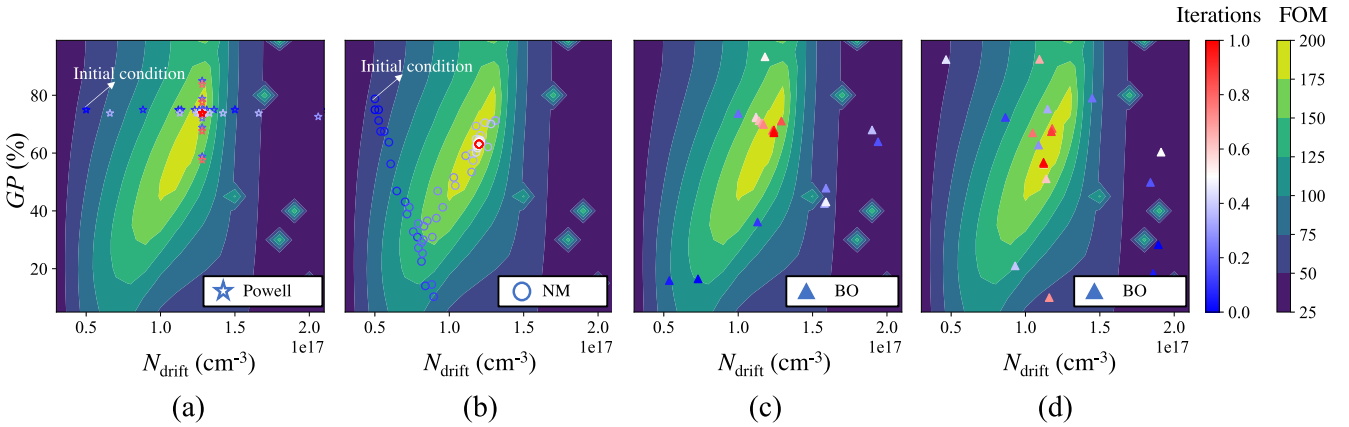

FIGURE 3. The contour plot and scatter plots for optimization of GP and N_{drift}. The contour plot in the background shows the grid search method result with 380 data points. Scatter plots indicate results from three different algorithms. (a) Powell (b) Nelder-Mead (c) A first Bayesian Optimization (d) A second Bayesian Optimization. All algorithms arrive at the top of the "ridge" following different paths. For NM and Powell, the initial device has $N_{drift} = 5 \times 10^{16}$ cm^{-3}, GP = 75%, and FOM = 58.89 kW/mm^2.

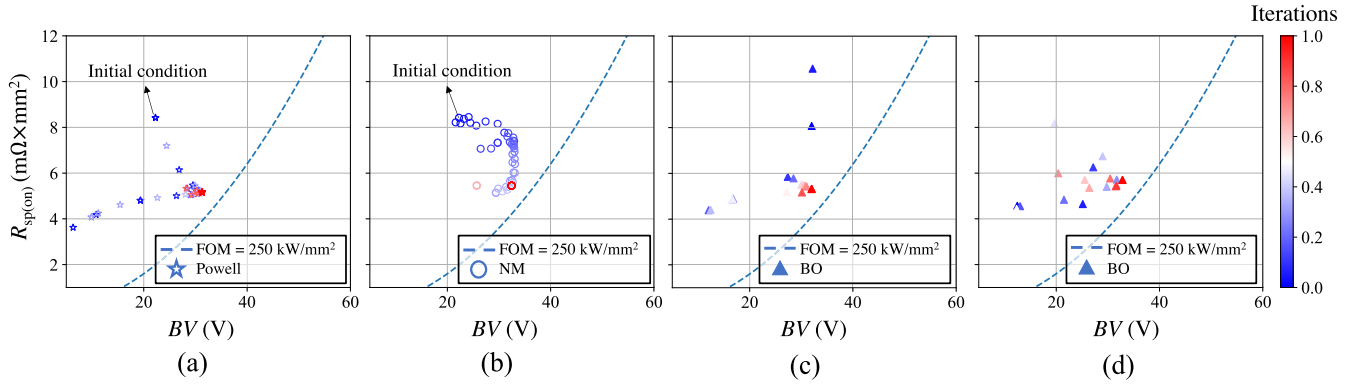

FIGURE 4. Optimization results from three different algorithms on the $R_{sp(on)}$ vs. BV plot. (a) Powell (b) Nelder-Mead (c) The first Bayesian Optimization (d) The second Bayesian Optimization. The colors show the normalized steps. Blue is the initial step, and red is the final step. For NM and Powell, the initial device has $R_{sp(on)}$ = 8.42, mΩ×mm^2, BV = 22.27 V, and FOM = 58.89 kW/mm^2.

TABLE 2. Six parameters in TCAD simulation as the inputs for the optimization problem. The initial values are for Nelder-Mead and Powell algorithms and the bounds are for Bayesian Optimization.

Algorithm	N_{drift} (cm^{-3})	GP (%)	$R_{sp(on)}$ (mΩ· mm^2)	BV (V)	FOM (kW/mm^2)
Grid search	1.20×10^{17}	65	5.42	32.2	191
NM	1.20×10^{17}	63.1	5.45	32.4	193
Powell	1.28×10^{17}	73.8	5.16	31.3	190
BO(first)	1.23×10^{17}	67.8	5.32	32	193
BO(second)	1.12×10^{17}	56.8	5.70	32.8	189

Fig. 4 shows the evolution of BV and $R_{sp(on)}$ during the optimization. The device evolves from the initial condition with BV = 22.27 V, $R_{sp(on)}$ = 8.42 mΩ× mm^2, I_{leak} = 2.48 × 10^{-15} A/μm, and FOM = 58.89 kW/mm^2 in Fig. 4(a) and 4(b). The dashed line shows the frontier for FOM = 250 kW/mm^2. Fig. 4(a) and 4(b) show the result from the Powell and NM algorithm, respectively. In Fig. 4(b), the initial condition is the first vertex of the simplex in the NM algorithm. The second and third vertices are calculated by changing N_{drift} and GP, respectively. These three vertices form a triangle which is the simplest shape of simplex in 2-D space. The next iteration is determined by calculating the reflection point in NM. The triangle moves by four different operations until the stopping criterion is reached in 114 steps. The optimization process forms a trajectory toward the frontier which is shown in Fig. 4(b). The final device of the NM optimization has $N_{drift} = 1.20 \times 10^{17}$ cm^{-3}, GP = 63.1 %, $R_{sp(on)}$ = 5.45 mΩ× mm^2, BV = 32.4 V and FOM = 193 kW/mm^2.

Fig. 4(c) and (d) show the evolution of the two BOs. After optimization with 20 iterations, the first BO yields N_{drift} = 1.23×10^{17} cm^{-3}, GP = 67.8 %, $R_{sp(on)}$ = 5.32 mΩ× mm^2, BV = 32.0 V and FOM = 193 kW/mm^2. The second BO yields N_{drift} = 1.12×10^{17} cm^{-3}, GP = 56.8 %, $R_{sp(on)}$ = 5.70 mΩ× mm^2, BV = 32.8 V and FOM = 189 kW/mm^2 after 20 iterations. These different results show the intrinsically stochastic property of the Gaussian process.

From Fig. 3 and 4, although the optimization paths for NM, Powell and BO algorithms differ, we observe that they all reveal the same optimum. However, the NM and Powell algorithms require more than one hundred iterations and

gradually improve the device every iteration, while BO only requires 20 iterations to achieve comparable performance. Assuming that each iteration takes 5 minutes to calculate the FOM, NM and Powell require more than 6 hours longer than BO to achieve the best result. In general, all three algorithms perform well in lower dimensional optimization problems.

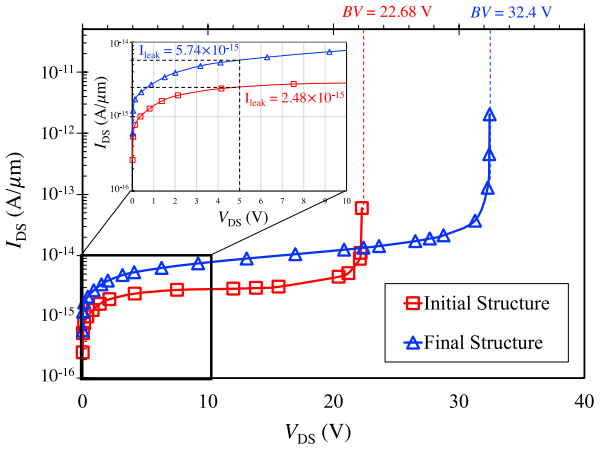

FIGURE 5. The breakdown curve of the initial and final devices from the NM optimization. The leakage current also can be extracted in this curve. The leakage current can maintain $I_{leak} < 10^{-13}$ A/μm during all steps of the NM optimization.

Fig. 5 shows the breakdown curves of devices before and after the NM optimization. We do not show the breakdown curve of the devices obtained using the other optimization methods but the curves look very similar. The breakdown voltage of the initial device is 22.68 V and improves to 32.4 V after NM optimization. The leakage current also can be extracted as the subplot shown. The subplot shows that the leakage currents of both devices is lower than 10^{-13} A/μm and we verify that no devices have a leakage current exceeding 10^{-13} A/μm during optimization.

Fig. 6 shows the electrical field and impact ionization distributions at breakdown conditions before and after the NM optimization. We define region I as the part of the drift region not under the FOX and region II as the part under the FOX. We observe that the electrical field on the surface is raised significantly after optimization. The electrical field in region I is less than 2.5×10^5 V/cm before NM optimization (Fig. 6(a)) but exceeds 2.5×10^5 V/cm throughout region I after optimization, as indicated by the green color in Fig. 6(a'). The impact ionization profile is concentrated on the drain side before NM optimization (Fig. 6(b)), and it becomes more spread out at breakdown after the NM optimization (Fig. 6(b')).

Fig. 7 shows the electrical field under the Si/SiO_2 interface before and after NM optimization of GP and N_{drift}. After optimizing GP and N_{drift}, the electrical field along the cutline C-C' is higher on average, indicative of the higher breakdown voltage. After optimization, there are two peaks (A and B) in the electrical field. Peak A arises from the poly gate corner on the step gate oxide structure. Peak B arises from the end of the poly gate on the SG-FOX (GP). Peak A occurs at X = 700 nm after optimization because we do not change the length of the FOX (L_{FOX}) during the two-parameter optimization. On the other hand, peak B shifts toward the source side since the GP was optimized from an initial value $GP = 75$ % to an optimized value $GP = 63.10$ %.

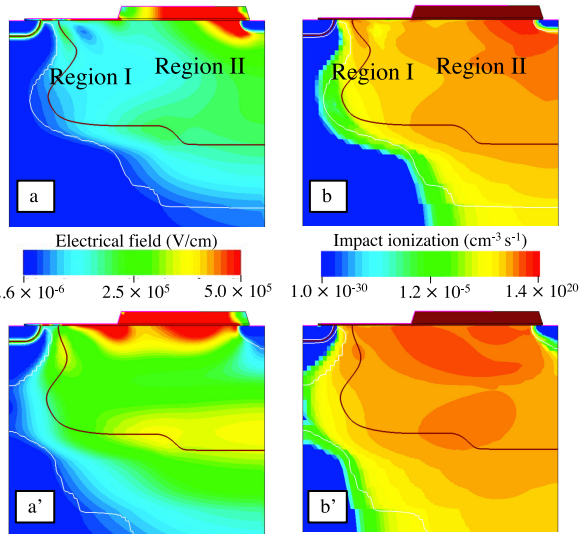

FIGURE 6. Comparison of the (a) electrical field and (b) impact ionization of before (a, b) and after (a', b') Nelder-Mead optimization for GP and N_{drift}.

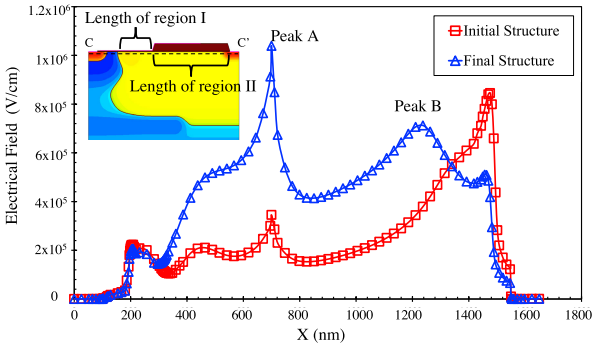

FIGURE 7. The electrical field distribution along the C-C' cutline under the surface before and after NM optimization. After the optimization, the electrical field on the surface is much closer to the RESURF condition. The high electrical field on the drain side (peak B) is shifted toward the source side because the GP is optimized to 63.10 %. Peak A comes from the poly metal gate corner on the step of field oxide.

B. OPTIMIZATION FOR SIX PARAMETERS USING ONE-STAGE NM

We now go back to the six parameters we identified in Table 1. We perform a NM optimization in this subsection which we refer to as a "one-stage" NM optimization. As we will see later, the one-stage NM does not reach a global optimum and in section D we will perform a "three-stage" NM optimization to get closer to the global minimum.

Fig. 8 shows the result from the optimization over all six parameters using the NM algorithm. We add the two-parameters optimization in Fig. 8 for comparison. The six-parameters optimized device has a FOM measuring 217 kW/mm^2 and is closer to the FOM = 250 kW/mm^2

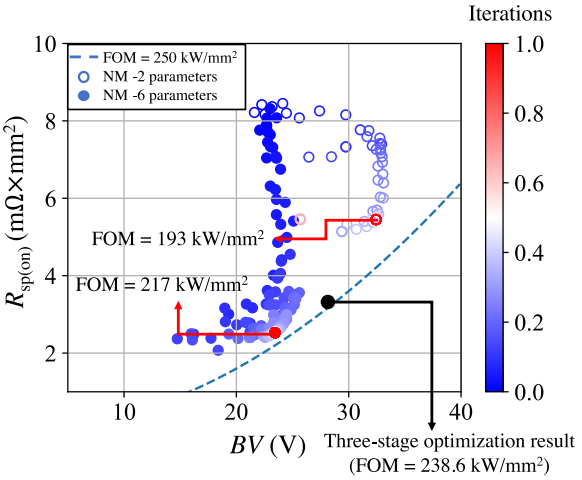

FIGURE 8. The solid dots show the result from the six parameters optimization using NM. The circles show the result from the two parameters optimization using NM from subsection A. The final result of three-stage NM optimization in subsection D is shown as the black dot as the reference. The result from the one-stage six parameters optimization is worse than the three-stage NM optimization, meaning the result of a one-stage six parameters NM optimization is not the global maximum.

frontier. The NM optimization for six parameters takes 357 iterations to converge. The final structure of the six parameters optimization has $N_{drift} = 5.96 \times 10^{16}$ cm^{-3}, $L_{drift.1} = 1025$ nm, $L_{drift.2} = 250$ nm, $GP = 63.1$ %, $L_{FOX} = 478$ nm, $L_{JFET} = 165$ nm and its performance is $R_{sp(on)} = 2.53$ mΩ× mm^2, $BV = 23.44$ V and FOM = 217 kW/mm^2. In the one-stage NM, the six parameters optimization result has a better performance than the two parameters optimization result but lower than the three-stage NM optimization result which we will explain in the following subsection D. We also show the result of the three-stage NM optimization, determined in section D, in Fig. 8.

Fig. 8 shows that in our case, the one-stage NM did not yield the global maximum in the six-dimensional space. Similarly, the Powell algorithm drove the result towards a local maximum and remained stuck there. The performance of one-stage NM optimization is worse than the three-stage NM optimization and one-stage BO optimization results which we will show in the following subsection C.

C. GLOBAL OPTIMIZATION BY BO

While for NM, a six-parameter optimization got stuck in a local maximum, BO can find the global maximum by optimizing up to 20 parameters simultaneously at an acceptable expense [35]. We use the bounds in TABLE 1 and perform a 100 iterations (N = 100) BO on all six parameters.

Fig. 9 shows the BO optimization result for six parameters. The one-stage BO returns a device with $R_{sp(on)} = 2.97$ mΩ× mm^2, $BV = 26.76$ V, and FOM = 241.38 kW/mm^2 ($N_{drift} = 1.03 \times 10^{17}$ cm^{-3}, $L_{drift.1} = 938$ nm, $L_{drift.2} = 199$ nm, $GP = 99$ %, $L_{JFET} = 220$ nm, $L_{FOX} = 560$ nm). The FOM obtained using BO is more than 11 % higher compared to the optimal device obtained by the one-stage NM in the previous subsection.

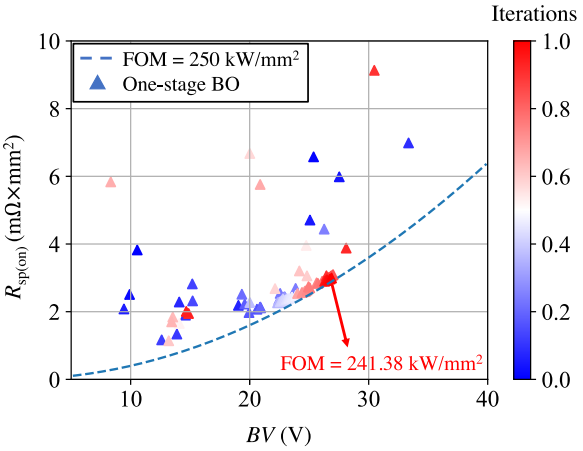

FIGURE 9. The result from BO with one hundred iterations. The data points are distributed randomly at beginning of optimization process.

D. OPTIMIZATION FOR SIX PARAMETERS USING THREE-STAGE NM

Fig. 10 shows the result of the three-stage NM optimization. The first stage is the optimization of N_{drift} and GP, as described in III-A. We use the blue dots and the blue color bar to present the data from the first stage optimization. The second stage optimizes the five parameters (N_{drift}, $L_{drift.1}$, $L_{drift.2}$, GP, and the ratio between the L_{JFET} and L_{FOX}). We optimize these five parameters but fix the half-pitch of the device to 1.65 μm in the second stage optimization. The results from the second stage optimization are shown in red dots and the red color bar. There are 256 iterations in the second stage of optimization. In the third stage, we optimize the GP, N_{drift}, and L_{FOX}, and the results are shown in green dots and the green color bar. The total length of the device will be changed after the third NM optimization. The third stage of NM optimization takes 161 iterations. The steps in each optimization stage are normalized and are presented in color (from deep to light colors). After three-stage NM optimization, the final device has $N_{drift} = 1.44 \times 10^{17}$ cm^{-3}, $L_{FOX} = 647$ nm, $GP = 76.85$ %, $R_{sp(on)} = 3.32$ mΩ× mm^2, $BV = 28.15$ V, and FOM = 238.59 kW/mm^2. The three-stage NM optimization takes 530 iterations to get the final structure.

In Fig. 8, we have identified a maximum located at $R_{sp(on)} = 2.53$ mΩ× mm^2, $BV = 23.44$ V and FOM = 217 kW/mm^2. The three-stage NM optimization path did not pass near this maximum, which prevented the algorithm from realizing the maximum in this six-dimensional design space. To avoid such getting stuck in a local maximum, designers have to carefully choose optimization parameters and repeat the optimization process when using methods like NM. However, since we usually do not know the location of local maximum in advance, methods like BO that can find other, more optimal, maximum offer an advantage.

E. COMPARISON BETWEEN THREE-STAGE NM AND ONE-STAGE BO

The result from the one-stage BO is comparable with the result from the three-stage NM, indicating that both the

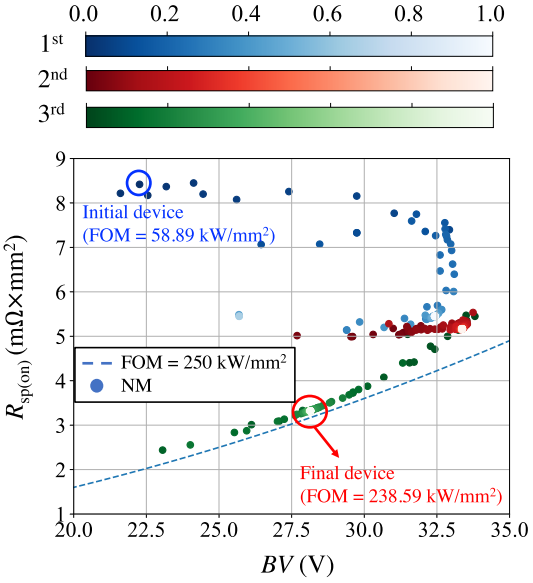

FIGURE 10. Three-stage NM optimization result. We optimize N_{drift} and GP in the first stage (Blues). In the second stage (Reds), we fix the total length of the device and optimize five parameters in TABLE 1. Finally, we optimize the L_{FOX}, GP, and N_{drift} in the third stage (Greens).

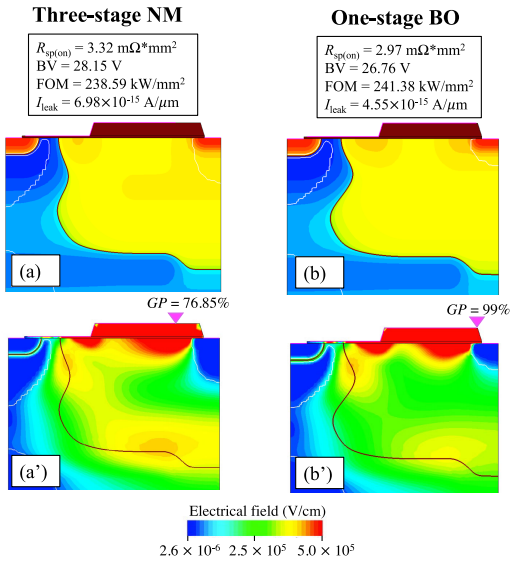

FIGURE 11. (a) The doping profile from three stage optimizations by NM. (a') the electrical field distribution. (b) the doping profile after six-parameters optimization using BO. (b') the electrical field distribution.

three-stage NM optimization and the BO are able to find the global maximum for our problem under study. The one-stage BO optimization for six parameters takes fewer iterations and has a higher FOM than the one-stage NM which we presented in subsection B and three-stage NM which we presented in subsection D.

Fig. 11 compares the devices from the one-stage BO and three-stage NM optimization. While both optimization methods realize a device with FOM ∼240 kW/mm^2, and the three-stage NM algorithm costs 530 iterations, the six-input optimizer by BO only takes 100 iterations. In our case, one device simulation approximately takes five minutes, meaning a difference of 35.83 hours different between the two methods.

However, the BO is not definitively the better method. One of the disadvantages of BO is that it is hard to set up reasonable bounds before executing the simulation. On the other hand, NM, and also Powell, do not need bounds. The setting of a suitable range of bounds for BO relies on expert knowledge. Another drawback of BO is the need to pre-set the number of iterations before beginning the BO loop, although recent research has addressed this issue with automatic stopping conditions [36]. Additionally, the establishment of bounds must account for potential numerical issues in TCAD simulations, making it a crucial consideration in selecting suitable bounds. Despite the various drawbacks listed above, the overall use of BO algorithm in device optimization process can still be more efficient than manual optimization or direct method optimizations, like NM and Powell method.

Another interesting point is that the BO and NM device configurations are significantly different as Fig. 11 showed, although both realize a FOM ≈ 240 kW/mm^2. The device structures from the algorithmic development may provide researchers or engineers with different ideas which are unintuitive. For example, we note that BO realizes a slightly higher FOM with a $GP = 99$ % while NM has a $GP = 76.85$ %. This means that unlike in the two-input optimization, for the six-input optimization there are multiple local maxima in the six-dimensional input space for the FOM. In our case, one with $GP \approx 77$ % and one with $GP \approx 99$ %. Direct methods, gradually evolving from an initial guess, will never reach an alternate optimum ($GP \approx 99$ %). Even human device engineers may not consider a completely different parameter space. Therefore, BO can not only accelerate the development of the LDMOS or other transistors but also may provide different design ideas never considered before.

Lastly, We have the flexibility to optimize different FOMs by changing the objective function. In this study, we only maximized FOM $= BV^2/R_{sp(on)}$. To optimize reliability, we may maximize or minimize other FOMs that are reliability-related, such as maximizing safe operating area and minimizing hot-carrier degradation. If we need to simultaneously optimize multiple FOMs, we must use multi-objective function device optimization [37] or other variants of BO. However, the reliability simulation for LDMOS is still an active developing topic of research [38]. Therefore, we are not yet able to automatically optimize the device using reliability as one of our FOMs.

Some further extended research can be explored, including process optimization using BO instead of the design of experiments (DOE) and utilizing this accelerated optimization algorithm to tackle previously intractable problems, such as identifying the fundamental physical limitations of different shapes of field oxides. This study has provided a novel approach to solving these previously unsolved problems, which are difficult to resolve through analytical methods.

IV. CONCLUSION

We have developed an optimization method that directly combines the different optimization algorithms and the physical-model-based TCAD simulations for a SG-FOX LDMOS. We defined the FOM $= BV^2/R_{sp(on)}$ as the objective function and used NM, Powell, and BO to optimize a SG-FOX LDMOS. We started with a two-parameter optimization to illustrate how the different methods reach their optimum. The two-parameter optimizations showed that the three algorithms identified similar optimized devices, but BO takes fewer iterations compared to Powell and NM. Powell and NM take 108 and 114 steps in the two-parameters optimization problem, respectively. Performing NM and BO on all six parameters significantly improves device performance. Using a three-stage NM optimization, a device with similar performance as the BO optimized device can be found. One-stage NM found a significantly inferior device compared to one-stage BO. Overall, the FOM was improved 4 times to FOM $\sim$240 kW/mm^2 by three-stage NM optimization or one-stage BO. One-stage BO reached the optimum in 100 iterations compared to 530 iterations for the three-stage NM.

BO is the most data-efficient method to achieve the best final structure for our SG-FOX LDMOS optimization. However, the need to set appropriate bounds before exploring the device is a disadvantage of Bayesian Optimization. Another inconvenience in the current BO implementation is that a pre-determined number of the iteration needs to be specified instead of a convergence criterion in its current implementation. NM or Powell are methods on the other hand that do not require bounds but only an initial device. Perhaps most remarkably, BO and three-stage NM yielded significantly different device designs realizing similar FOM. Overall, BO and NM are powerful tools for the design of new devices to accelerate time-consuming manual optimization.

REFERENCES

[1] B. J. Baliga, "The future of power semiconductor device technology," *Proc. IEEE*, vol. 89, no. 6, pp. 822–832, Jun. 2001, doi: 10.1109/5.931471.

[2] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 59–72, Jun. 2013, doi: 10.1109/JESTPE.2013.2271499.

[3] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, "The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 692–712, Mar. 2017, doi: 10.1109/TED.2017.2655149.

[4] A. N. Tallarico, S. Reggiani, R. Depetro, A. M. Torti, G. Croce, E. Sangiorgi, and C. Fiegna, "Hot-carrier degradation in power LDMOS: Selective LOCOS-versus STI-based architecture," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 219–226, Jan. 2018, doi: 10.1109/JEDS.2018.2792539.

[5] J. Cheng, S. Wu, W. Chen, H. Huang, and B. Yi, "A trench LDMOS improved by quasi vertical super junction and resistive field plate," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 682–689, Jul. 2019, doi: 10.1109/JEDS.2019.2928091.

[6] K. S. Nikhil, N. DasGupta, A. DasGupta, and A. Chakravorty, "SOI-LDMOS transistors with optimized partial n^+ buried layer for improved performance in power amplifier applications," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4931–4937, Nov. 2018, doi: 10.1109/TED.2018.2867656.

[7] M. Saremi, M. Saremi, H. Niazi, M. Saremi, and A. Y. Goharrizi, "SOI LDMOSFET with up and down extended stepped drift region," *J. Electron. Mater.*, vol. 46, no. 10, pp. 5570–5576, Jun. 2017, doi: 10.1007/s11664-017-5645-z.

[8] F. Giuliano, A. N. Tallarico, S. Reggiani, A. Gnudi, E. Sangiorgi, C. Fiegna, M. Rossetti, A. Molfese, S. Manzini, R. Depetro, and G. Croce, "TCAD predictions of hot-electron injection in *p*-type LDMOS transistors," in *Proc. 49th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Cracow, Poland, Sep. 2019, pp. 86–89, doi: 10.1109/ESSDERC.2019.8901703.

[9] X. Luo, B. Zhang, Z. Li, Y. Guo, X. Tang, and Y. Liu, "A novel 700-V SOI LDMOS with double-sided trench," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 422–424, May 2007, doi: 10.1109/LED.2007.894648.

[10] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Raleigh, NC, USA: Springer, 2007, ch. 1, p. 7.

[11] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 1979, pp. 238–240, doi: 10.1109/IEDM.1979.189589.

[12] X. Hu, W. Wang, Y. Ji, and Q. Hua, "The influence of the N^+ floating layer on the drift doping of RESURF LDMOS and its analytical model," *IEICE Electron. Exp.*, vol. 13, no. 20, pp. 1–6, Oct. 2016, doi: 10.1587/elex.13.20160852.

[13] H. D. Sunitha and N. Keshaveni, "Reduced surface field technology for LDMOS: A review," *Int. J. Emerg. Technol. Adv. Eng.*, vol. 4, no. 6, pp. 1–4, Jun. 2014.

[14] A. Saadat, M. L. van de Put, H. Edwards, and W. G. Vandenberghe, "Channel length optimization for planar LDMOS field-effect transistors for low-voltage power applications," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 711–715, Jul. 2020, doi: 10.1109/JEDS.2020.3008388.

[15] A. Saadat, M. L. van de Put, H. Edwards, and W. G. Vandenberghe, "Simulation study on the optimization and scaling behavior of LDMOS transistors for low-voltage power applications," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4990–4997, Nov. 2020, doi: 10.1109/TED.2020.3019479.

[16] J. Kim, S.-G. Kim, T. M. Roh, H. S. Park, J.-G. Koo, and D. Y. Kim, "Characteristics of *p*-channel SOI LDMOS transistor with tapered field oxides," *Electron. Telecommun. Res. Inst. J.*, vol. 21, no. 3, pp. 22–28, Sep. 1999, doi: 10.4218/etrij.99.0199.0304.

[17] A. Saadat, M. L. van de Put, H. Edwards, and W. G. Vandenberghe, "LDMOS drift region with field oxides: Figure-of-merit derivation and verification," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 361–366, 2022, doi: 10.1109/JEDS.2022.3169702.

[18] A. Parpia and C. A. T. Salama, "Optimization of RESURF LDMOS transistors: An analytical approach," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 789–796, Mar. 1990, doi: 10.1109/16.47787.

[19] S. Han, J. Choi, and S. Hong, "Acceleration of semiconductor device simulation with approximate solutions predicted by trained neural networks," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5483–5489, Nov. 2021, doi: 10.1109/TED.2021.3075192.

[20] S. B. Kutub, H. Jiang, N. Chen, W. Lee, C. Jui, and T. Wu, "Artificial neural network-based (ANN) approach for characteristics modeling and prediction in GaN-on-Si power devices," in *Proc. 32nd Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Sep. 2020, pp. 529–532, doi: 10.1109/ISPSD46842.2020.9170110.

[21] Y. Guo, J. Chen, J. Zhang, Q. Yao, Y. Dai, B. Guo, R. Xia, M. Zhang, M. Li, and J. Yao, "Application of machine learning method in the modeling and designing of semiconductor power devices," in *Proc. IEEE 16th Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Oct. 2022, pp. 1–4, doi: 10.1109/ICSICT55466.2022.9963153.

[22] C. Jeong, S. Myung, I. Huh, B. Choi, J. Kim, H. Jang, H. Lee, D. Park, K. Lee, W. Jang, J. Ryu, M. Cha, J. M. Choe, M. Shim, and D. S. Kim, "Bridging TCAD and AI: Its application to semiconductor design," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5364–5371, Nov. 2021, doi: 10.1109/TED.2021.3093844.

[23] J. Chen, M. B. Alawieh, Y. Lin, M. Zhang, J. Zhang, Y. Guo, and D. Z. Pan, "PowerNet: SOI lateral power device breakdown prediction with deep neural networks," *IEEE Access*, vol. 8, pp. 25372–25382, 2020, doi: 10.1109/ACCESS.2020.2970966.

[24] J. Chen, X. Guo, Y. Guo, J. Zhang, M. Zhang, Q. Yao, and J. Yao, "Deep neural network-based approach for breakdown voltage and specific on-resistance prediction of SOI LDMOS with field plate," *Jpn. J. Appl. Phys.*, vol. 60, no. 7, Jul. 2021, Art. no. 077002, doi: 10.35848/1347-4065/ac06da.

[25] S. Myung, J. Kim, Y. Jeon, W. Jang, I. Huh, J. Kim, S. Han, K.-H. Baek, J. Ryu, Y.-S. Kim, J. Doh, J.-H. Kim, C. Jeong, and D. S. Kim, "Real-time TCAD: A new paradigm for TCAD in the artificial intelligence era," in *Proc. SISPAD*, Nov. 2020, pp. 347–350, doi: 10.23919/SISPAD49475.2020.9241622.
[26] D.-G. Lin, S. L. Tu, Y.-C. See, and P. Tam, "A novel LDMOS structure with a step gate oxide," in *IEDM Tech. Dig.*, Dec. 1995, pp. 963–966, doi: 10.1109/IEDM.1995.499376.
[27] M. J. Kumar and R. Sithanandam, "Extended-p^+ stepped gate LDMOS for improved performance," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1719–1724, Jul. 2010, doi: 10.1109/TED.2010.2049209.
[28] *Sentaurus User Guide*, Synopsys, Mountain View, CA, USA, 2016.
[29] R. van Overstraeten and H. de Man, "Measurement of the ionization rates in diffused silicon $p - n$ junctions," *Solid-State Electron.*, vol. 13, no. 1, pp. 583–608, May 1970, doi: 10.1016/0038-1101(70)90139-5.
[30] S. Yuan, B. Duan, H. Cai, Z. Cao, and Y. Yang, "Novel LDMOS with assisted deplete-substrate layer consist of super junction under the drain," in *Proc. 29th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2017, pp. 279–282, doi: 10.23919/ISPSD.2017.7988951.
[31] M. Qiao, Y. Li, X. Zhou, Z. Li, and B. Zhang, "A 700-V junction-isolated triple RESURF LDMOS with n-type top layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 774–776, Jul. 2014, doi: 10.1109/LED.2014.2326185.
[32] M. J. Kochenderfer and T. A. Wheeler, *Algorithms for Optimization*. Cambridge, MA, USA: MIT Press, 2019, ch. 7.
[33] V. L. Deringer, A. P. Bartók, N. Bernstein, D. M. Wilkins, M. Ceriotti, and G. Csányi, "Gaussian process regression for materials and molecules," *Chem. Rev.*, vol. 121, no. 16, pp. 10073–10141, Aug. 2021, doi: 10.1021/acs.chemrev.1c00022.
[34] W. Dang, S. Liao, B. Yang, Z. Yin, M. Liu, L. Yin, and W. Zheng, "An encoder–decoder fusion battery life prediction method based on Gaussian process regression and improvement," *J. Energy Storage*, vol. 59, Mar. 2023, Art. no. 106469, doi: 10.1016/j.est.2022.106469.
[35] P. I. Frazier, "A tutorial on Bayesian optimization," 2018, *arXiv:1807.02811*.
[36] B. Kim and M. Shin, "Bayesian optimization of MOSFET devices using effective stopping condition," *IEEE Access*, vol. 9, pp. 108480–108494, 2021, doi: 10.1109/ACCESS.2021.3101812.
[37] S. Daulton, D. Eriksson, M. Balandat, and E. Bakshy, "Multi-objective Bayesian optimization over high-dimensional search spaces," in *Proc. 38th Conf. Uncertainty Artif. Intell.*, 2022, pp. 507–517.
[38] S. Reggiani, G. Barone, S. Poli, E. Gnani, A. Gnudi, G. Baccarani, M. Chuang, W. Tian, and R. Wise, "TCAD simulation of hot-carrier and thermal degradation in STI-LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 691–698, Feb. 2013, doi: 10.1109/TED.2012.2227321.

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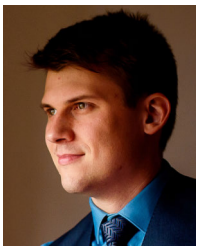

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