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RESEARCH ARTICLE

Improving Wireless Power Transfer Efficiency Considering Rectifier Input Impedance and Load Quality Factor

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ABSTRACT This paper presents a method to maximize power transfer efficiency (PTE) in wireless power transfer (WPT) systems with low-quality factors merely based on tuning the receiver-side components. The paper also suggests an algorithm to find the optimum components values considering the effect of input impedance of receiver-side rectifier at high-frequency (MHz) applications such as portable electronic devices. Existing methods often consider the input impedance of the full-bridge rectifier as a pure resistance at low frequencies. However, at high frequencies, the complex impedance of the rectifier should be taken into account since it impacts on the components optimum values to maximize PTE. Despite conventional maximizing PTE methods for series-series and series-parallel topologies, this paper shows that a series-parallel WPT system with low load quality factor requires adjusting the resonant capacitor in addition to resistive load. The validity of the proposed method is verified based on numerical simulations and experiment tests using a 100 mW cm-scale prototype of a resonant inductive link at 6.78 MHz with varying distance between coils. The test results show a PTE improvement up to 40% in a series-parallel WPT compared with the methods that only tune the load equivalent resistance.

INDEX TERMS Coupling coefficient, inductive link misalignment, load quality factor, power transfer efficiency, rectifier impedance, wireless power transfer.

I. INTRODUCTION

Proliferation of portable and wearable electronics, and recent advancement in electric vehicle technology rapidly increase the demand for wireless power transfer (WPT) systems as an effective contact-less method to deliver power to an electric load [1], [2], [3], [4]. The efficiency of a WPT system is highly sensitive to the coupling coefficient of its magnetically coupled coils which varies due to misalignment and distance between the coils [5], [6].

To maximize power transfer efficiency (PTE), a tuning circuit(s) is adopted at transmitter (Tx)- or receiver (Rx)-side that compensates the adverse effect of misalignment and/or variable distances between the coils [7]. Source frequency tuning; passive impedance matching by inserting a network of passive components; and active impedance matching at the receiving side rectifier are among PTE maximization methods that are used in various applications [8], [9], [10]. Source frequency tuning is confined with bandwidth to meet standards, therefore the fixed-frequency methods are preferable [11]. Using a tunable capacitor to control the zero-voltage switching angle in a WPT system [12], and tuning Tx and Rx sides compensation capacitors [13], are among the suggested methods to improve the efficiency. In [14], [15], and [16], an alternative method to maximize PTE is proposed for series-series (SS) WPT systems in which the equivalent load is tuned by adjusting the duty cycle of dc-dc converter in Rx-side. However, as the operation frequency is low (tens of kHz), considering the effect of rectifier input impedance on PTE is not required.

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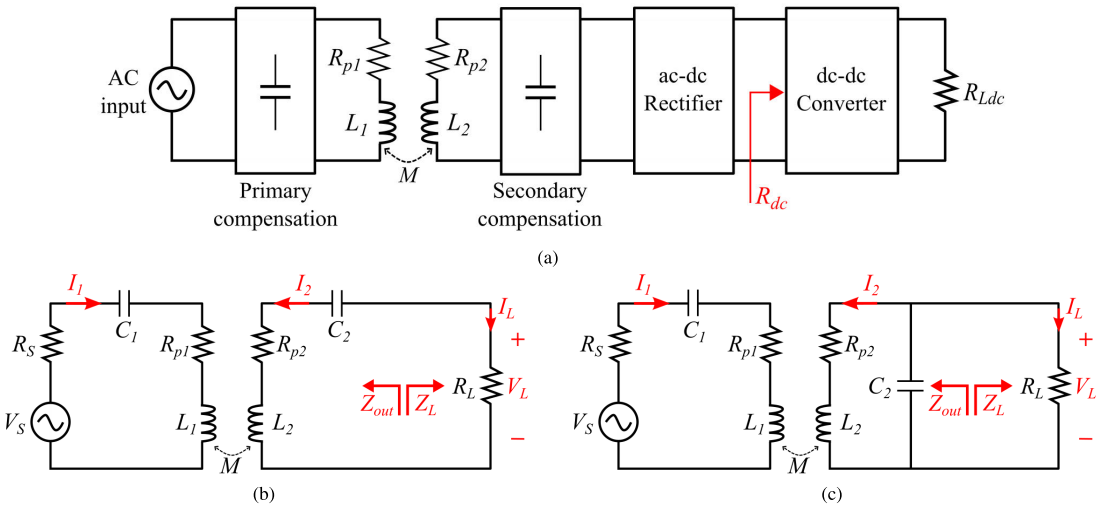

FIGURE 1. (a) Block diagram of a WPT system; (b) Equivalent circuit of SS topology; (c) Equivalent circuit of SP topology.

Using a tunable T-type impedance matching network at the Rx-side is also suggested to track the maximum efficiency [17]. However, an additional controller is required at the Tx-side to adjust the output voltage. The exiting methods that control both Tx and Rx-side components need an extra data link in addition to the power link. As the data link is omitted in single-side control circuits, they are superior solutions particularly for applications in which uncertainties exist at the end-user device, e.g. misalignment of the coil in wireless battery chargers [14], [15], [16], [17].

Most of existing methods assume that the input impedance of the receiver-side rectifier is a pure resistive element that is a valid assumption merely at low-frequency applications. For instance, in [18], two novel models for a WPT rectifier load with harmonics and parasitic components is presented to achieve high-performance transfer efficiencies. However, the operation frequency is 85kHz and therefore the reactance component of the rectifier is negligible. The impedance characteristics of the full-bridge rectifier at 6.78 MHz and their effects on WPT system are discussed in [19] and [20]. However, this investigation is performed assuming a high load quality factor that is defined as the ratio of resistive load to the impedance of compensating capacitance. It is shown that the load quality factor impacts on the efficiency of a WPT system. Existing maximizing PTE methods in series-parallel (SP) WPT systems usually assume a high load quality factor that is not necessarily a valid assumption particularly at high coupling coefficients.

This paper proposes a receiver-side PTE maximizing method for SS and SP WPT systems covering both high and low load quality factors which are not fully investigated in existing methods. It is shown that maximizing PTE under low load quality factor requires tuning the resonance tank in addition to a conventional resistive load matching at the receiver side. It also encounters the effect of Rx-side rectifier impedance at high-frequencies (6.78 MHz). The investigation shows that the full-bridge impedance impacts on calculating optimum components values at this range of frequencies. The proposed analytical and numerical methods are experimentally verified for both SS and SP topologies using prototypes of a cm-scale WPT system with variable distance between the coils, to investigate the effect of low load quality factor.

II. WIRELESS POWER TRANSFER TERMINOLOGY AND PRACTICAL CONSTRAINTS

Fig. 1(a) shows a WPT system diagram, including Tx/Rx coils (L_1, L_2) with parasitic resistances (R_{p1}, R_{p2}), and the mutual inductance $M = k\sqrt{L_1 L_2}$ where k is the coupling coefficient. To improve the power transfer efficiency, the resonant capacitors C_1 and C_2 are used to compensate L_1 and L_2 at the source frequency, ω, satisfying

$$\omega = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}. \tag{1}$$

Fig. 1(b) and (c) show the equivalent circuits of SS and SP topologies in which the ac-dc rectifier, dc-dc converter, and dc load are modeled with an equivalent resistance R_L. Using circuit theory under steady-state condition, the load voltage is:

$$V_L = \begin{cases} \dfrac{j\omega M R_L V_S}{Z_{11}Z_{22} + \omega^2 M^2} & \text{for SS} \\ \dfrac{j\omega M R_L V_S}{(Z_{11}Z_{22} + \omega^2 M^2)(1 + j\omega C_2 R_L)} & \text{for SP} \end{cases} \tag{2}$$

where V_S is the source voltage phasor and ω is the angular frequency of the ac source. Z_{11} and Z_{22} are the impedance of the Tx and Rx sides, given by:

$$Z_{11} = R_S + R_{p1} + j(\omega L_1 - \frac{1}{\omega C_1}) \tag{3}$$

$$Z_{22} = \begin{cases} R_L + R_{p2} + j(\omega L_2 - \dfrac{1}{\omega C_2}) & \text{for SS} \\ R_{p2} + j\omega L_2 + \dfrac{R_L}{1 + j\omega C_2 R_L} & \text{for SP} \end{cases} \tag{4}$$

Two common definitions for the efficiency of a WPT circuit are: i) Link energy efficiency (η_L) where defined as the ratio

TABLE 1. Study system parameters.

Symbol	Parameter Description	Value
L_1	Primary coil inductance	8.32 μH
L_2	Secondary coil inductance	3.1 μH
R_{p1}	Primary coil resistance	2.6 Ω
R_{p2}	Secondary coil resistance	1.9 Ω
C_1	Transmitting-side Resonant Capacitance	66 pF
C_2	Receiving-side Resonant Capacitance	178 pF
R_S	Source resistance	50 Ω
f	Operating frequency	6.78 MHz
k	Coupling coefficient	0.1-0.5
R_L	Equivalent load resistance for SS	20 Ω
	Equivalent load resistance for SP	1000 Ω

of the output power, P_L, to the input power to the link, P_{in}, i.e. $\eta_L = P_L/P_{in}$; and ii) Power Transfer Efficiency (PTE) defined as the ratio of P_L to the available source power P_{avs}, that is the maximum input power that can be delivered to the link [21], [22]. PTE and η_L may be interchangeably used, however, maximizing η_L does not lead to maximize P_L since $0 < P_{in} < P_{avs}$.

In high power applications (e.g. charging stations) the link energy efficiency is usually used as a design criterion. However, in low-power applications (e.g. in wearable electronics) source voltage amplitude can be of concern due to using low-voltage integrated circuit technology. Therefore, to secure a specific power delivered to the load at a permitted range of voltage, PTE is often used as the design optimization criterion. PTE can be defined in terms of S-parameters as: [22], [23]

$$\text{PTE} = |S_{21}|^2 = \frac{P_L}{P_{avs}} = \frac{4R_L}{R_S}\left(\frac{V_L}{V_S}\right)^2 \tag{5}$$

where S_{21} is transmission coefficient of WPT system equivalent circuit. Substituting for V_L from (2) into (5), PTE is obtained for SS and SP resonant circuits as given by:

$$\text{PTE} = \begin{cases} \dfrac{4\omega^2 M^2 R_S R_L}{\left|Z_{11}Z_{22} + \omega^2 M^2\right|^2} & \text{for SS} \\ \dfrac{4\omega^2 M^2 R_S R_L}{\left|Z_{11}Z_{22} + \omega^2 M^2\right|^2 |1 + j\omega C_2 R_L|^2} & \text{for SP.} \end{cases} \tag{6}$$

Fig. 2 shows the 3-dimensional (3D) PTE plots with respect to the change in k and f for both SS and SP circuits in which the simulation parameters are given in Table 1. The plots show that for k less than a specified quantity, so-called critical coupling coefficient (k_{crit}), the maximum PTE occurs at a fixed resonant frequency ($f = 6.78$ MHz) and it decreases as k is decreased. The region is labeled under-coupled on Figs. 2(a), and (b). The critical coupling coefficient can be obtained from the solution of $dPTE/dk = 0$ at $\omega = \omega_0$. For $k > k_{crit}$ the plot region is called over-coupled in which the frequency-splitting phenomenon occurs. This region has two maximum PTE points corresponding to different frequencies, below and above the resonant frequency [24]. These two

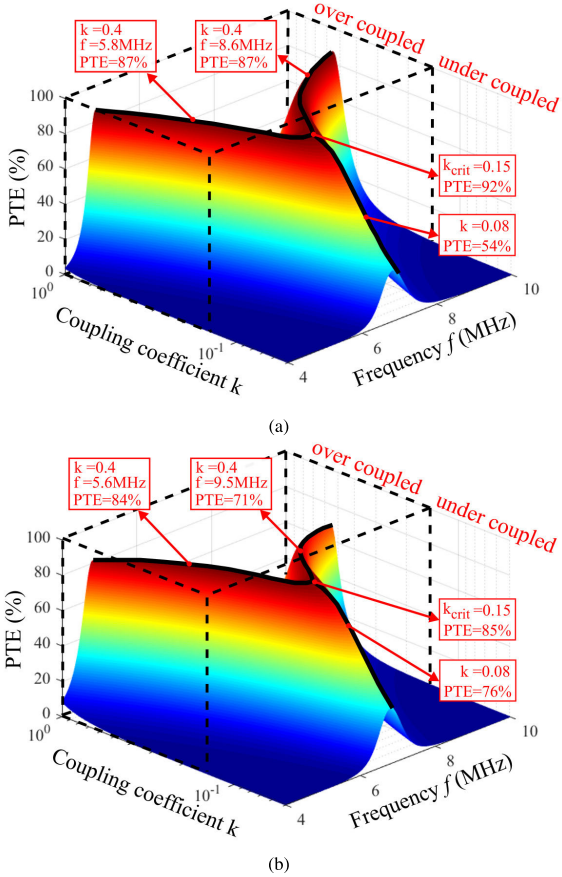

FIGURE 2. PTE versus k and f for (a) SS; and (b) SP circuits.

frequencies are functions of coupling coefficient. Within the over-coupled region, one needs a more complicated PTE optimization method that will be elaborated in the next section, verified by experimental and simulation test results.

III. PROPOSED METHOD TO IMPROVE PTE CONSIDERING RECTIFIER AND LOAD Q-FACTOR EFFECTS

The PTE optimum point is highly sensitive to coils misalignment and distance change. Existing PTE analysis methods for SP WPT systems assume a high load Q-factor, i.e. $Q_L^2 \gg 1$, where $Q_L \triangleq \omega C_2 R_L$. This assumption leads to a PTE maximum point tracking method that only needs tuning R_L. However, as k varies in a wide range and especially for high k, the load Q-factor does not necessarily remain high. Under this condition, conventional PTE analysis should be modified to encounter the low load Q-factor scenarios since PTE optimization is not achievable merely based on tuning R_L and adjusting C_2 at the receiver-side is also required. On the other hand, the bridge rectifier at low frequency WPT analysis is considered as a pure resistive equivalent circuit that is a function of dc-side load resistant (R_{dc}). However, at a high frequency WPT system, the rectifier input becomes a complex impedance, therefore, tuning C_2 is also required in addition to R_{dc} in order to maintain PTE at optimum point.

This section firstly extend the PTE analysis to a general case in which the load Q-factor is included in PTE analysis.

Then, a extended method is proposed and demonstrated that considers the effect of rectifier input impedance to maximize PTE.

A. IMPACT OF LOAD Q-FACTOR ON PTE MAXIMIZING ANALYSIS

Starting with SS circuit, Fig.1(b), and using (6) at the resonant frequency, the optimal load condition can be obtained from the solution of $d\text{PTE}/dR_L = 0$, that is

$$R_{Lopt} = R_{P2} + \frac{\omega^2 M^2}{R_{P1} + R_S}. \tag{7}$$

Thus, the optimized PTE can be achieved only by controlling the load (R_L) since $C_{2opt} = 1/(\omega^2 L_2)$ at the resonant frequency in SS circuit is independent of R_L.

To extend the analysis for SP circuit, the following parallel to series impedance transformation is used:

$$R'_L = \frac{R_L}{1+Q_L^2}, \quad C'_2 = C_2 \frac{1+Q_L^2}{Q_L^2} \tag{8}$$

where R'_L and C'_2 represents equivalent series components. Using this transformation and optimizing PTE in (6), yields:

$$R'_{Lopt} = \frac{R_L}{1+\omega^2 C_2^2 R_L^2} = R_{p2} + \frac{\omega^2 M^2}{R_{p1} + R_S}. \tag{9}$$

and

$$C'_{2opt} = \frac{1+\omega^2 C_2^2 R_L^2}{\omega^2 C_2 R_L^2} = \frac{1}{\omega^2 L_2}. \tag{10}$$

Finally, by solving (9) and (10) for R_L and C_2, the optimum values of components to maximize PTE in SP circuit are obtained as:

$$R_{Lopt} = \frac{(R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S})^2 + (\omega L_2)^2}{R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S}}, \tag{11}$$

$$C_{2opt} = \frac{L_2}{(R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S})^2 + (\omega L_2)^2}. \tag{12}$$

When $Q_L^2 \gg 1$, R'_L and C'_2 in (8) can be approximated as:

$$R'_L \approx \frac{R_L}{Q_L^2}, \quad |Err_{R_L}| = \frac{1}{Q_L^2} \tag{13}$$

$$C'_2 \approx C_2, \quad |Err_{C_2}| = \frac{1}{1+Q_L^2} \tag{14}$$

where Err_{R_L} and Err_{C_2} are the approximation errors for R_L and C_2, respectively. Using this approximation, the optimal values of R_L and C_2 become:

$$R_{Lopt} = \frac{1}{\omega^2 C_2^2 \left(R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S}\right)}, \tag{15}$$

$$C_{2opt} = \frac{1}{\omega^2 L_2}. \tag{16}$$

To investigate the influence of Q_L on R_{Lopt}, C_{2opt} and PTE, the approximated and exact quantities are compared

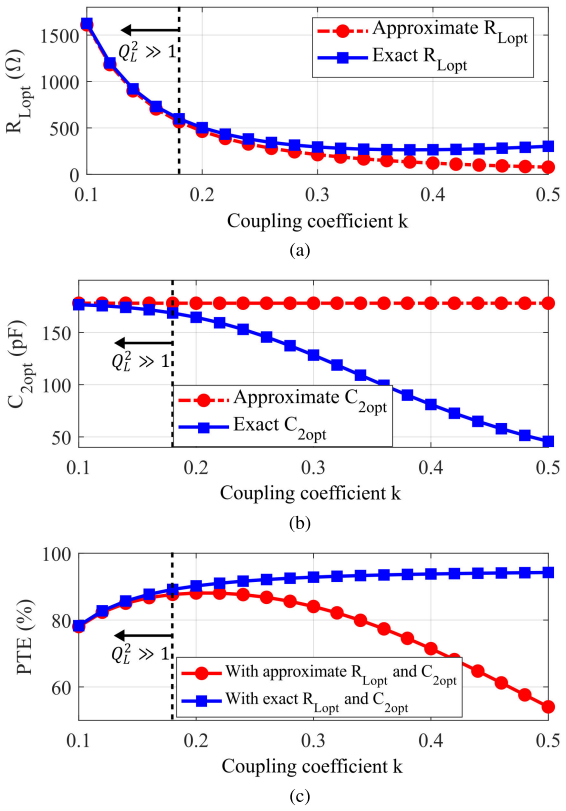

FIGURE 3. Comparing approximated and exact optimum quantities: (a) R_{Lopt}; (b) C_{2opt}; and (c) PTE.

as shown in Fig. 3 using the system parameters as listed in Table 1. Fig. 3(a) and (b) show that the approximated and exact parameters diverge as k increases. The divergence occurs when Q_L^2 is less than a specific value that is defined based on Err_{C_2} as:

$$Q_L^2 = \frac{1}{|Err_{C_2}|} - 1 \tag{17}$$

To quantify a threshold for $Q_L^2 \gg 1$ that approximated quantities can be used, it can be assumed $|Err_{C_2}| \leq 5\%$ that leads to:

$$Q_L^2 \geq 19 \tag{18}$$

where it corresponds to $k \leq 0.18$ and PTE can be maximized only by tuning R_L, as shown in Fig. 3(c).

The presented method of maximizing PTE based on circuit analysis of a WPT system can be extended to a receiving-side that includes a rectifying-bridge. Extending the analysis to circuits with rectifier bridge is explained using impedance matching concept in maximum power transformation theory, i.e. $Z_{out} = Z_L^*$ to obtain R_{Lopt} and C_{2opt}, where Z_{out} is the output impedance of the WPT system seen from the point of connection to the load in Fig. 1(b) and (c).

The proposed impedance matching method realizes Zero-Phase-Angle (ZPA) at the resonant frequency resulting in a circuit with pure resistive input impedance. However, to turn on the switches under Zero-Voltage-Switching (ZVS) condition, the input impedance should remains slightly inductive

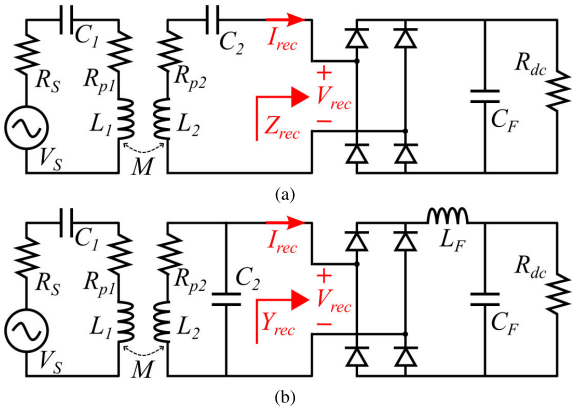

FIGURE 4. (a) SS; and (b) SP circuits with rectifier.

[12], [25]. Therefore, ZVS and ZPA techniques cannot be realized simultaneously, however, the realization of ZVS close to a ZPA condition can be practically performed by adjusting C_2.

B. PROPOSED ALGORITHM CONSIDERING THE EFFECT OF RECTIFIER

The last stage of the receiving-end circuit in a WPT system often includes a diode rectifier followed by a dc-dc converter for dc-side load matching. At low frequencies (kHz), the diode rectifier can be modeled with an equivalent resistance since the impedance of parasitic junction capacitance of diodes are negligible [14], [15]. However, at high frequencies (MHz) developing an analytical model for the rectifier diodes cannot be readily performed because of adding the effects of parasitic capacitances, which are voltage dependent and nonlinear [20], [26]. Thus, large-signal nonlinear circuit analysis techniques such as harmonic balance method can be used (e.g. by using advanced design system (ADS) software tools from Keysight Technologies). Based on this method the first harmonic of the rectifier input voltage and current are considered to find the equivalent impedance of the rectifier.

Explicit solution and analytical design of a WPT system including a rectifier cannot be readily performed as presented and explained for pure resistive load R_L. The reason is that C_{2opt} and R_{Lopt} depend on the amount of rectifier input impedance which in turn is a function of frequency and the amount of circuit parameters connected to the rectifier. Thus, the optimum parameters can be determined using iterative methods starting with an initial guess. Initially, a set of (C_{20}, R_{dc0}) is selected for circuit without rectifier, then, by using an iterative algorithm, the initial parameters gradually converge into the optimum values as listed in Table 4. Herein, a modified algorithm to find $R_{L_{opt}}$ and C_{2opt} is suggested for a WPT system including rectifier based on the following iterative method:

1) For a fixed V_S, select an initial R_{Lopt} and C_{2opt} as explained in circuit analysis without rectifier;
2) By sweeping R_{dc} and using the harmonic balance technique, the input impedance (admittance) of the rectifier in Fig. 4(a) for SS (Fig. 4(b) for SP) is obtained. The impedance and admittance are denoted by $Z_{rec} \triangleq R_{rec} + jX_{rec}$ for SS and $Y_{rec} \triangleq G_{rec} + jB_{rec}$ for SP circuit, respectively;
3) Select an R_{dc} from previous steps such that $R_{rec} = R_{Lopt}$ in SS ($G_{rec} = 1/R_{Lopt}$ in SP circuits). Then, for the selected R_{dc}, find the corresponding X_{rec} for SS (B_{rec} for SP) circuits from the impedance (admittance) function with respect to R_{dc};
4) Re-tune C_2 in the resonance tank to compensate the effect of X_{rec} for SS (B_{rec} for SP) on the total capacitance of the tank such that a new C_{2opt} is achieved for the circuit including rectifier;
5) Go to the step two and repeat the algorithm until C_{2opt} converges to a specific value that is the optimum capacitance.

To further investigate the proposed algorithm, it is applied to a case study including a full-bridge rectifier connected to a dc-load and its performance with respect to variation of k is investigated. Based on steps 3 and 4, the modified formulations for SS circuit are:

$$R_{rec_{opt}} = R_{P2} + \frac{\omega^2 M^2}{R_{P1} + R_S}, \; C_{2opt} = \frac{1}{\omega^2 L_2 + \omega X_{rec}} \tag{19}$$

and for SP circuit the optimum quantities are:

$$G_{rec_{opt}} = \frac{R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S}}{(R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S})^2 + (\omega L_2)^2} \tag{20}$$

$$C_{2opt} = \frac{L_2}{(R_{P2} + \frac{\omega^2 M^2}{R_{P1}+R_S})^2 + (\omega L_2)^2} - \frac{B_{rec}}{\omega}. \tag{21}$$

To complete this procedure for the case study, the specifications of coils are selected as given in Table 1 with $C_F = 20$ nF for SS ($L_F = 20\,\mu$H, $C_F = 1$ nF for SP) circuit. The Schottky diode BAT54 from Nexperia Inc. is selected for the rectifier and its SPICE model is used for simulation in ADS. Both SS and SP circuits are simulated for three different power levels, $P_{avs} = 25$, 100, and 250 mW, using Harmonic Balance toolbox in ADS software tool.

Fig. 5(a) and (b) show $(R_{rec},\ X_{rec})$ for SS and $(G_{rec},\ B_{rec})$ for SP circuit with respect to R_{dc}, respectively. R_{dc} axes are differently selected such that R_{rec} and G_{rec} in each plot overlaps with the optimum load conditions. In both SS and SP circuits, X_{rec} and B_{rec} are none zero and varies with transfer power levels and R_{dc}. This verifies that at Industrial, Scientific, and Medical (ISM) frequency band, the imaginary part of fundamental impedance/admittance of rectifiers must have been taken into account in WPT design optimization procedure. Furthermore, in SS circuit, R_{rec} almost varies linearly with respect to R_{dc} and in SP circuit, both G_{rec} and B_{rec} reciprocally vary with respect to R_{dc}.

The power conversion efficiency (PCE) of rectifier is also important to be investigated since it depends on the load variations. The PCE is defined as the ratio of the dc output power to the input power of the rectifier. To study the impact of load

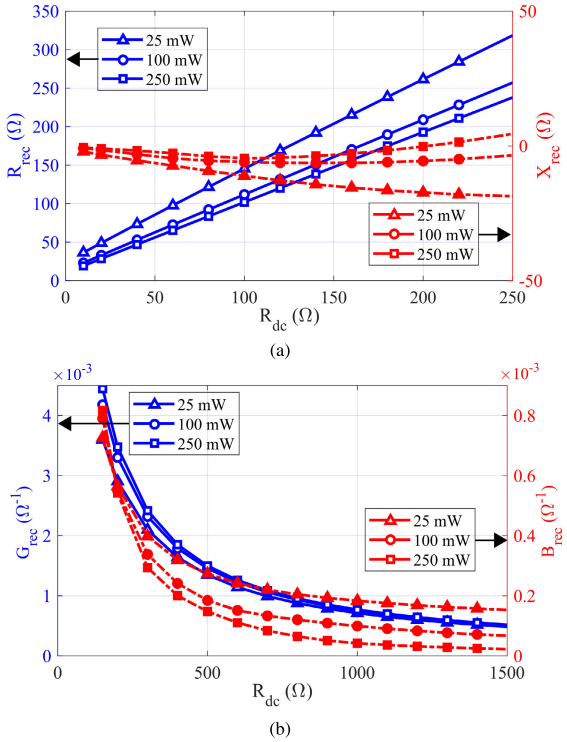

FIGURE 5. (a) (R_{rec}, X_{rec}) for SS compensation; and (b) (G_{rec}, B_{rec}) for SP compensation.

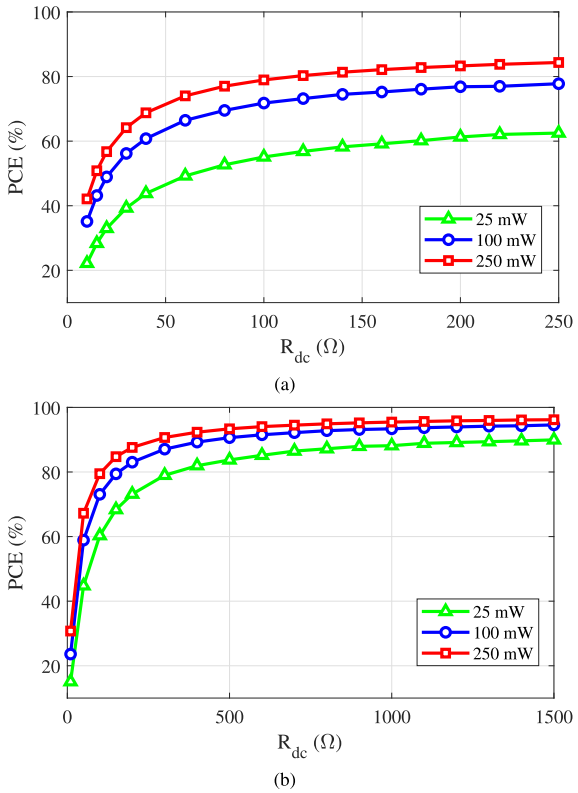

FIGURE 6. PCE versus dc load (R_{dc}) at different P_{avs}: (a) for SS compensation; and (b) for SP compensation.

changes on the PCE of the rectifier, both SS and SP circuits are simulated for three different power levels, $P_{avs} = 25$, 100, and 250 mW, using Harmonic Balance toolbox in ADS software tool. Figs. 6(a) and (b) show the PCE for SS and SP topologies in which the PCE increases as R_{dc} is increased. The PCE in both circuits also increases as the transferred power level is increased. However, the efficiency is highly sensitive to $R_{dc} < 50\ \Omega$. In SS topology, the PCE is less, compared with SP one. The reason is that the range of optimum load is less in SS (10 to 250 Ω) compared with 150 to 1500 Ω in SP. The smaller load causes a smaller voltage level at the rectifier input that is comparable with voltage drops across the rectifier diodes which in turn decreases the efficiency of the rectifier.

To evaluate the accuracy of the suggested method to design WPT systems with rectifier, SS and SP circuits are considered at $P_{avs} = 125$ mW (corresponding to $P_L \approx 100$ mW). Then, the results of the proposed algorithm with those of obtained based on a numerical optimization tool are compared (Table 2). Results of running the proposed algorithm show that R_{dc} and C_2 converge to optimum results at various k in less than 7 iterations. The optimized parameters are also calculated using numerical optimization in ADS software tool as presented in Table 2.

Comparing the R_{dc} and C_2 columns shows a close match between the results with a maximum error less than 2% and 5% for R_{dc} and C_2, respectively. The advantage of using the suggested algorithm compared with ADS optimization tool is that it can be also used when SPICE model of diode is unavailable as it works based on measured rectifier input impedance, as well.

TABLE 2. Proposed algorithm vs. numerical optimization.

		Proposed Alg.		Num. Optimization		Error (%)	
	k	$R_{dc}(\Omega)$	$C_2(pF)$	$R_{dc}(\Omega)$	$C_2(pF)$	$e_{R_{dc}}$	e_{C_2}
SS	0.2	26.7	180	26.6	179.7	0.4	0.2
	0.3	76.4	182.8	76.4	182.8	0.0	0.0
	0.4	148	175.1	148.3	175.1	-0.2	0.0
	0.5	251.3	138.6	251.6	138.3	-0.1	0.2
SP	0.1	1241	175.1	1237	175.1	0.3	0.0
	0.2	362	158.2	362	158.2	0.0	0.0
	0.3	195	108.9	195.5	109	-0.3	-0.1
	0.4	136	41.2	139	43.5	-2.2	-5.3
	0.5	147.5	27	145	28.4	1.7	-4.9

C. PRACTICAL CONSIDERATION OF IMPLEMENTATION

The proposed algorithm is established based on adjusting R_{dc} and C_2 at the receiver-side. In fact, the suggested algorithm is used to obtain the optimum values of R_{dc} and C_2 analytically with respect to each coupling coefficient corresponding to a coil distance. This analysis is useful for selection of the components and their range. In practice, a conventional perturb and observe (P&O) method can be employed to achieve optimum R_{dc} and C_2.

To adjust R_{dc}, the conventional method is using dc-dc converter in which by changing the converter duty cycle, the equivalent input resistance of the converter, i.e. R_{dc}, can

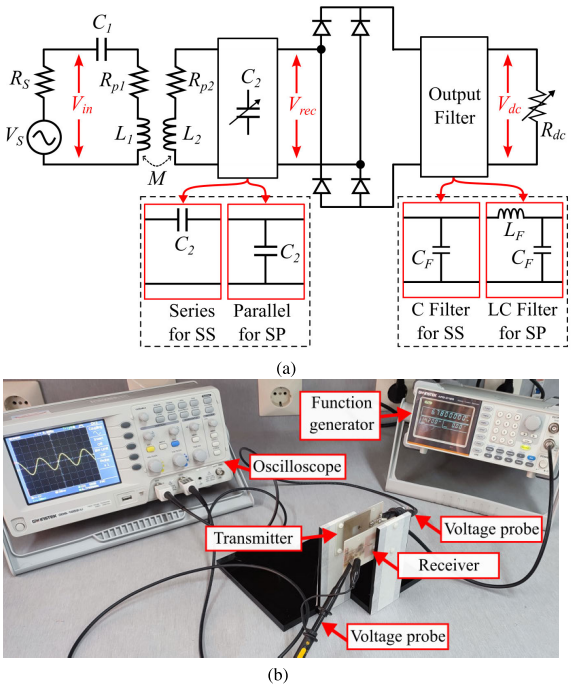

FIGURE 7. (a) Block diagram of the simulation and experiment test setup; and (b) Photo of the test setup.

be adjusted at the desired value [14], [15], [16]. To realize variable capacitance C_2, two different methods so-called *capacitor bank*, and *switch-controlled capacitor* (SCC) are suggested in literature [13], [27]. However, using SCC has some limitations in high-frequency applications. For low-power and high-frequency applications, a P&O algorithm that tracks the optimum C_2 by using a capacitor bank can be suggested as an appropriate method. Ultra-low power implementation of the close-loop control circuit requires an integrated-circuit design and fabrication that is beyond the scope of this work.

IV. EXPERIMENTAL VERIFICATION OF THE PROPOSED PTE MAXIMIZING METHOD

A. TEST SETUP AND METHOD

To verify the validity of the proposed method and its assumptions, an experiment test setup for WPT including Tx/Rx coils and a rectifier is developed. The test system is also numerically analyzed using a High Frequency Structure Simulation (HFSS) software tool from ANSYS Inc. for electromagnetic simulations. Fig. 7(a) shows the block diagram of the simulation and experiment test setup that presents the details of WPT circuit. This setup consists of two coupled coils; compensation capacitors; and a full bridge rectifier using high frequency BAT54 diodes from Nexperia Inc. The simulation of the circuit is initially performed in ADS software tool using parameter in Table. 1 to obtain the impedance of rectifier and PTE. In this simulation, corresponding to each coupling coefficient, the optimum C_2 and R_{dc} are calculated using the proposed algorithm.

Fig. 7(b) shows the photo of an experiment test setup consists of planar coils that are fabricated on a standard fiberglass

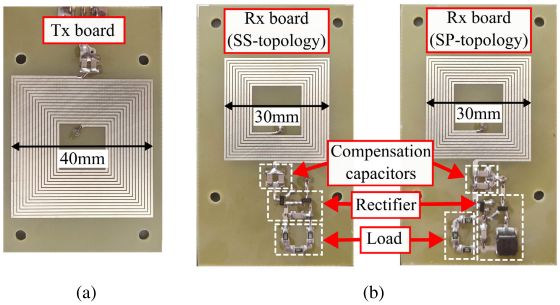

FIGURE 8. Photo of the fabricated Tx and Rx boards: (a) Tx board; and (b) SS- and SP-Topology Rx boards.

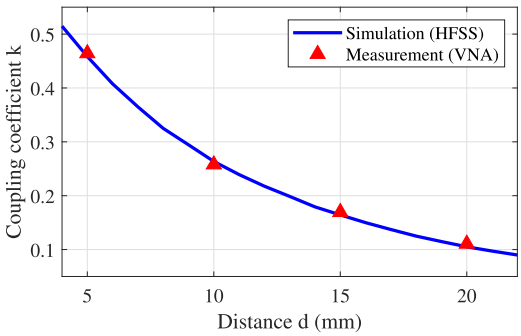

FIGURE 9. Coupling coefficient, k, versus coil distance, d.

TABLE 3. Coil parameters.

	$L_1(\mu H)$	$R_{p1}(\Omega)$	$L_2(\mu H)$	$R_{p2}(\Omega)$
HFSS	8.1	3.2	3.07	1.2
VNA	8.32	2.6	3.1	1.9

(FR-4) substrate. The sinusoidal source is a function generator (AFG-2125 Gw Instek) with $R_S = 50\ \Omega$ at $f = 6.78$MHz, adjusted at a constant effective voltage $V_S = 5.0\ V$ that corresponds to $P_{avs} = 125$ mW ($P_L \approx 100$ mW). The dc-side of the full-bridge rectifier is connected to an R_{dc} via a filter with $C_F = 20$ nF for SS and ($L_F = 20\ \mu$H, $C_F = 1$ nF) for SP circuit. In this test, the distance between the coils is increased from 4 mm to 22 mm using steps of 2 mm and corresponding to each step change, the optimum R_{dc} and C_2 are changed based on the proposed algorithm. Fig. 8 shows the photo of fabricated Tx-board that includes a 16 turns, 40mm × 40mm coil; and Rx-board that is a 10 turns, 30mm × 30mm coil.

To apply the proposed method and perform the test for various coupling coefficients, the coil parameters and variation of k with respect to distance are required. These parameters are obtain from modeling of the coils without other circuit components using HFSS software tool and verified by an experiment test using Vector Network Analyzer (VNA) at $f = 6.78$ MHz (VNA from Keysight Inc.), as given in Table 3. Comparing the measurement and simulation shows a close match with an error less than 2.7% for the inductance of coils. The variation of k with respect to the distance is also shown in Fig. 9 where the graph is obtained using HFSS software tool and the markers shows k based on measurements at four different distances using VNA.

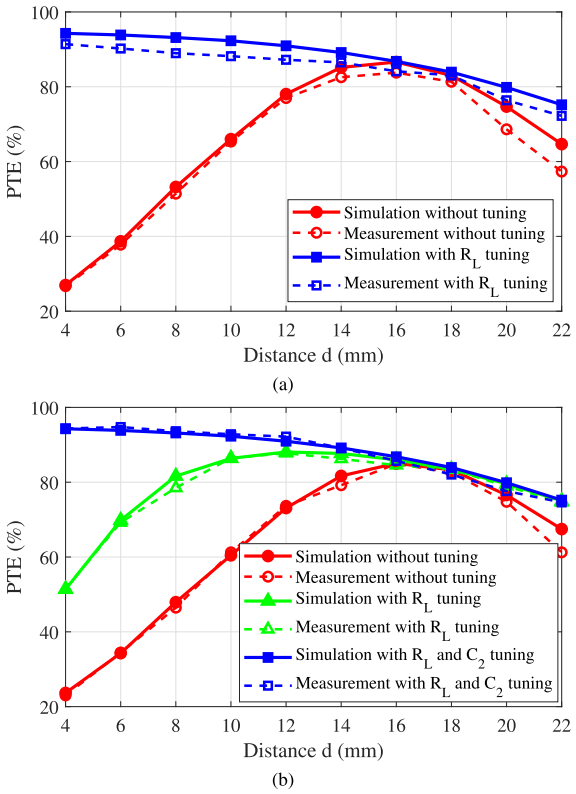

FIGURE 10. PTE in (a) SS, and (b) SP circuits without rectifiers.

B. RESULTS AND DISCUSSIONS

Fig. 10(a) shows the measured and calculated PTE for SS circuit without rectifier at various k, with/without tuning the pure resistive load, R_L. Variations of PTE graphs with respect to distance shows the necessity of tuning R_L to achieve optimum PTE as k varies. Close match between the calculated PTE from simulation with that of experimentally measured verifies the validity of the analysis and its assumptions.

Fig. 10(b) shows the test results for SP circuit without rectifier in which three scenarios including no tuning; only R_L; and (R_L, C_2) tuning are investigated. The results show that for all range of distances between the coils, optimum PTE can be achieved when both R_L and C_2 are tuned, simultaneously. Also, the two PTE curves corresponding to tuning R_L (Green Lines) and (R_L,C_2) (Blue Lines) beyond a specific distance coincide. The reason of this coincident can be explained based on Fig. 3 in which for $k < 0.18$ ($d > 15$ mm), the load quality factor Q_L will be significantly increased. Under this condition, the maximum PTE can be achieved by only tuning R_L based on (15) and (16).

The second test is performed for WPT system with rectifier at different distances considering the efficiency of diode rectifier by measuring V_{dc} instead of V_L. Fig. 11(a)-(d) depicts the input/output voltage waveforms of SS-WPT system (Fig. 7(a)) with rectifier corresponding to coil distances $d = 4,\ 8,\ 14$ and 18mm, respectively. Similarly, Fig. 12 shows the voltage waveforms for SP topology corresponding to $d = 4,\ 10,\ 16$ and 22mm, respectively. The optimum

TABLE 4. R_{dc} and C_2 test values and measured V_{dc}.

		SS topology			SP topology		
d (mm)	k	R_{dc} (Ω)	C_2 (pF)	V_{dc} (V)	R_{dc} (Ω)	C_2 (pF)	V_{dc} (V)
4	0.52	275	128	5.34	165	25	3.97
6	0.41	157	173	3.86	135	37	3.62
8	0.33	92	182	2.84	178	88	4.21
10	0.27	58	182	2.19	233	128	4.84
12	0.22	34	180	1.57	320	156	5.70
14	0.18	19.5	179	1.04	440	166	6.69
16	0.15	10	179	0.65	614	172	7.89
18	0.13	4.3	178	0.32	825	172	9.04
20	0.11	-	-	-	1130	175	10.3
22	0.09	-	-	-	1483	177	11.5

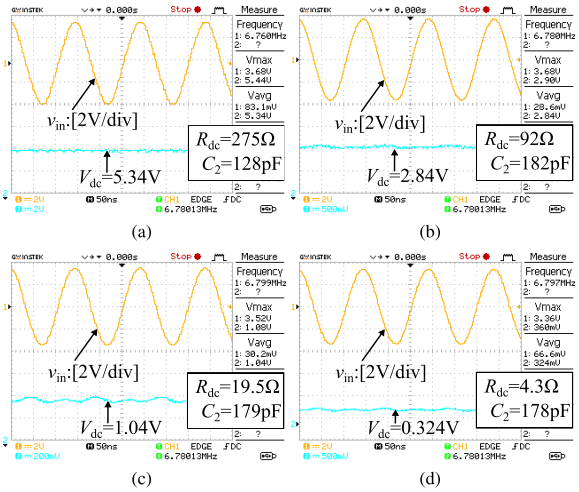

FIGURE 11. Experimental waveforms of SS-WPT system with optimum parameters corresponding to: (a) $d = 4mm$; (b) $d = 8mm$; (c) $d = 14mm$; and (d) $d = 18mm$.

R_{dc} and C_2 corresponding to each distance are obtained using the proposed algorithm as listed in Table 4. The measured rectifier output voltage is also given in Table 4 to calculate PTE at the fixed $P_{avs} = 125$ mW.

Fig. 13 shows the effect of coils distance on PTE in an experiment with diode rectifier. In this figure, the square markers show PTE based on simulation results for both SS and SP topologies (validated with experiment test results) in which R_{dc} and C_2 are selected based on the proposed algorithm. The graph with circle markers (red ones) shows PTE for a fixed R_{dc} and C_2. The gap between this graph and others confirms the need for parameter tuning particularly when the distance is changing.

To investigate the impact of rectifier input impedance on PTE, a simulation is added in which only R_{dc} is tuned (Fig. 13). Close matching between the square and triangle markers in Fig. 13(a) shows that the optimum PTE in SS topology is independent of C_2 because of the slight change of rectifier reactance in SS topology (Fig. 5(a)). However, Fig. 13(a) shows that PTE in SS topology drastically drops as distance increases. The reason is that $R_{dc\ opt}$ decreases as

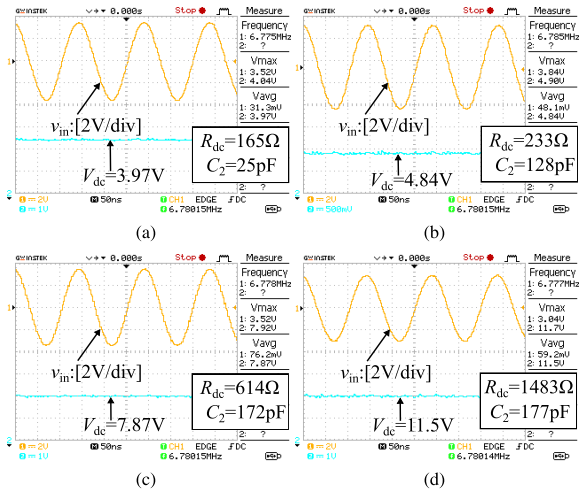

FIGURE 12. Experimental waveforms of SP-WPT system with optimum parameters corresponding to: (a) $d = 4mm$; (b) $d = 10mm$; (c) $d = 16mm$; and (d) $d = 22mm$.

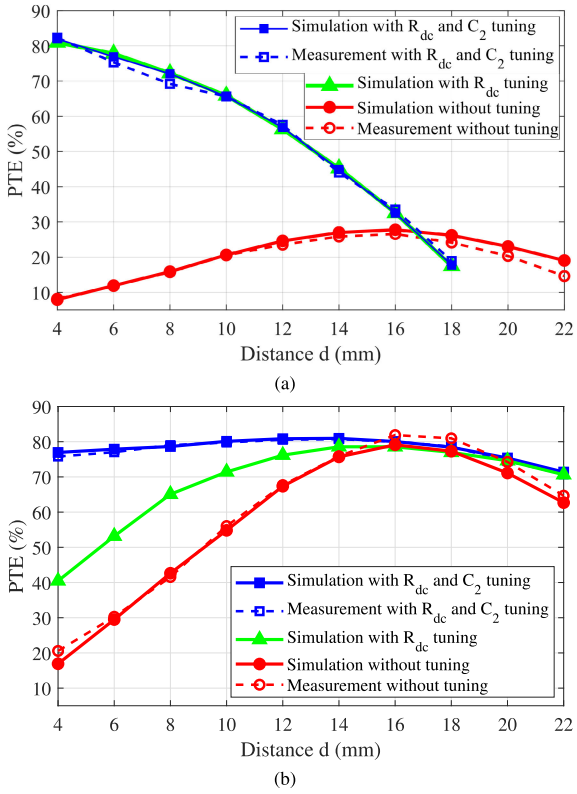

FIGURE 13. PTE in (a) SS; and (b) SP circuits with rectifiers.

distance is increased (Table 4) and it causes significant drop in PCE of the rectifier (Fig. 6(a)). As a result, the overall efficiency (PTE) is decreased. On the other hand, comparing PTE with/without tuning C_2 in Fig. 13(b) clearly shows the importance of tuning C_2 in addition to R_{dc} in SP topology. The figure shows that by tuning C_2, PTE can be improved up to 40% when C_2 is also compensated corresponding to the coil distance variation. Furthermore, considering input rectifier susceptance is required especially at high frequency WPT systems.

Fig. 13(b) shows the limitation of the proposed method in which for $d > 20\,mm$ (in this WPT system), PTE is decreased less than 75%. This limitation holds for all other approach as well since coils currents are increased that in turn increase the power losses in a WPT system. Thus, although the proposed method properly works for $4 < d < 20\,mm$ with PTE > 75%, it is inefficient for very weakly coupled WPT systems with large coil distances, similar to other existing methods.

V. CONCLUSION

A maximizing PTE method for WPT systems based on tuning receiver-side components is proposed and demonstrated that considers the effect of load quality factor and full-bridge input impedance at 6.78 MHz. The simulation and experiment test results of a cm-scale WPT prototype validate the accuracy and effectiveness of the proposed method for both SS- and SP-WPT systems. The test results show that using the proposed tuning method for a 100 mW WPT system can improve PTE up to 40% in SP topology. The suggested method based on tuning the receiver-side components enables the development of an efficient method for more complex configurations in future studies such as multi-receiver WPT systems.

REFERENCES

[1] K. Matsuura, D. Kobuchi, Y. Narusue, and H. Morikawa, "Communication-less receiver-side resonant frequency tuning for magnetically coupled wireless power transfer systems," *IEEE Access*, vol. 11, pp. 23544–23556, 2023.
[2] Z. Zhang, H. Pang, A. Georgiadis, and C. Cecati, "Wireless power transfer—An overview," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1044–1058, Feb. 2019.
[3] I. A. Mashhadi, M. Pahlevani, S. Hor, H. Pahlevani, and E. Adib, "A new wireless power-transfer circuit for retinal prosthesis," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6425–6439, Jul. 2019.
[4] A. Mahesh, B. Chokkalingam, and L. Mihet-Popa, "Inductive wireless power transfer charging for electric vehicles—A review," *IEEE Access*, vol. 9, pp. 137667–137713, 2021.
[5] Y. Gong, Y. Otomo, and H. Igarashi, "Neural network for both metal object detection and coil misalignment prediction in wireless power transfer," *IEEE Trans. Magn.*, vol. 58, no. 9, pp. 1–4, Sep. 2022.
[6] Y. Li, J. Zhao, Q. Yang, L. Liu, J. Ma, and X. Zhang, "A novel coil with high misalignment tolerance for wireless power transfer," *IEEE Trans. Magn.*, vol. 55, no. 6, pp. 1–4, Jun. 2019.
[7] W. Li, W. Mei, Q. Yuan, Y. Song, Z. Dongye, and L. Diao, "Detuned resonant capacitors selection for improved misalignment tolerance of LCC-S compensated wireless power transfer system," *IEEE Access*, vol. 10, pp. 49474–49484, 2022.
[8] A. Koran and K. Badran, "Adaptive frequency control of a sensorless-receiver inductive wireless power transfer system based on mixed-compensation topology," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 978–990, Jan. 2021.
[9] K. Zhang, W. Gao, R. Shi, Z. Yan, B. Song, and A. P. Hu, "An impedance matching network tuning method for constant current output under mutual inductance and load variation of IPT system," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11108–11118, Oct. 2020.
[10] P. Pérez-Nicoli and F. Silveira, "Maximum efficiency tracking in inductive power transmission using both matching networks and adjustable AC–DC converters," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3452–3462, Jul. 2018.
[11] N. Soltani, M. ElAnsary, J. Xu, J. S. Filho, and R. Genov, "Safety-optimized inductive powering of implantable medical devices: Tutorial and comprehensive design guide," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 6, pp. 1354–1367, Dec. 2021.
[12] U. D. Kavimandan, S. M. Mahajan, and C. W. Van Neste, "Analysis and demonstration of a dynamic ZVS angle control using a tuning capacitor in a wireless power transfer system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1876–1890, Apr. 2021.

[13] J. Zhang, J. Zhao, Y. Zhang, and F. Deng, "A wireless power transfer system with dual switch-controlled capacitors for efficiency optimization," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6091–6101, Jun. 2020.
[14] K. Zhang, T. Ye, Z. Yan, B. Song, and A. P. Hu, "Obtaining maximum efficiency of inductive power-transfer system by impedance matching based on boost converter," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 2, pp. 488–496, Jun. 2020.
[15] X. Dai, X. Li, Y. Li, and A. P. Hu, "Maximum efficiency tracking for wireless power transfer systems with dynamic coupling coefficient estimation," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5005–5015, Jun. 2018.
[16] W. X. Zhong and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4025–4034, Jul. 2015.
[17] Y. Liu and H. Feng, "Maximum efficiency tracking control method for WPT system based on dynamic coupling coefficient identification and impedance matching network," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3633–3643, Dec. 2020.
[18] Y. Yang, "Precise modeling of nonlinear rectifier loads in wireless power transfer systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 3574–3585, Mar. 2023.
[19] M. Fu, Z. Tang, M. Liu, C. Ma, and X. Zhu, "Full-bridge rectifier input reactance compensation in megahertz wireless power transfer systems," in *Proc. IEEE PELS Workshop Emerg. Technologies: Wireless Power (WoW)*, Jun. 2015, pp. 1–5.
[20] M. Fu, Z. Tang, and C. Ma, "Analysis and optimized design of compensation capacitors for a megahertz WPT system using full-bridge rectifier," *IEEE Trans. Ind. Informat.*, vol. 15, no. 1, pp. 95–104, Jan. 2019.
[21] S. Liu, R. Mai, L. Zhou, Y. Li, J. Hu, Z. He, Z. Yan, and S. Wang, "Dynamic improvement of inductive power transfer systems with maximum energy efficiency tracking using model predictive control: Analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12752–12764, Dec. 2020.
[22] J. D. Heebl, E. M. Thomas, R. P. Penno, and A. Grbic, "Comprehensive analysis and measurement of frequency-tuned and impedance-tuned wireless non-radiative power-transfer systems," *IEEE Antennas Propag. Mag.*, vol. 56, no. 4, pp. 44–60, Aug. 2014.
[23] A. P. Sample, D. T. Meyer, and J. R. Smith, "Analysis, experimental results, and range adaptation of magnetically coupled resonators for wireless power transfer," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 544–554, Feb. 2011.
[24] X. Liu, X. Yuan, C. Xia, and X. Wu, "Analysis and utilization of the frequency splitting phenomenon in wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3840–3851, Apr. 2021.
[25] D. Li, X. Wu, C. An, J. Gao, and W. Gao, "Implementation of ZVS for double-sided LCC inductive coupled wireless power transfer system under constant current/constant voltage operation mode," *IEEE Access*, vol. 11, pp. 29726–29743, 2023.
[26] J. Ou, S. Y. Zheng, A. S. Andrenko, Y. Li, and H. Tan, "Novel time-domain Schottky diode modeling for microwave rectifier designs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1234–1244, Apr. 2018.
[27] H. Lyu and A. Babakhani, "A 13.56-MHz -25-dBm-sensitivity inductive power receiver system-on-a-chip with a self-adaptive successive approximation resonance compensation front-end for ultra-low-power medical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 1, pp. 80–90, Feb. 2021.

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