RESEARCH ARTICLE

Battery Integrated Three-Port Soft-Switched DC–DC PSFB Converter for SPV Applications

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ABSTRACT This paper proposes a three-port soft-switched DC-DC converter integrating solar photovoltaic (SPV) source, battery energy storage system (BESS), and DC load. The proposed converter modifies the basic phase-shifted full bridge (PSFB) DC-DC converter topology with the addition of a link inductor to create a three-port converter structure and it uses a secondary passive clamp circuit to minimize the unwanted circulating current loss suffered by the conventional PSFB converters. The load port is isolated from the SPV and BESS port through a high frequency transformer. All semiconductor switches and diodes of the converter change their switching states under soft conditions. The proposed converter uses closed loop controller for maximum photovoltaic power extraction, charge/discharge control of BESS and load voltage regulation. Detailed steady-state operation of the converter with design guidelines of power and control circuits are presented in this work. Finally, real-time performance of the converter under different solar irradiance and load conditions is successfully validated through laboratory testing of a hardware prototype.

INDEX TERMS Maximum power point tracking (MPPT), phase-shifted full bridge (PSFB) converter, three-port converter (TPC), soft-switching, zero-voltage switching (ZVS), zero-current switching (ZCS).

I. INTRODUCTION

Serious environmental concern owing to uncontrolled use of fossil fuel and steep rise in its pricing over the years have led to rapid installations of solar photovoltaic (SPV) power stations for unpolluted and free of cost electricity generation. However, the electrical power generated by SPV sources being inconsistent and strong weather dependent, energy storage systems are usually integrated to maintain power supply continuity to local load and/or grid. Conventionally, SPV arrays are connected to the DC bus through an isolated DC-DC converter with maximum power point tracking (MPPT) controller and the battery energy storage systems (BESS) are integrated to the SPV system [1], [2], [3], [4], [5], [6] through bidirectional DC-DC converters as shown in Fig.1(a). However, an economical and efficient SPV system demands for integration of SPV source,

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BESS and the load to a single converter [7], [8], [9], [10], [11], [12], [13] as shown in Fig.1(b).

Many configurations of three-port converters (TPC) integrating SPV source, BESS and the load are reported in recent literatures [14], [15], [16], [17], [18]. The papers [14] and [15] have proposed high step-up non-isolated TPCs with all switches operating under ZVS conditions. The SPV-battery integrated isolated TPC proposed by [16] suffers from the problem of partial hard-switched transition of the secondary side active switches. Although the SPV-battery integrated isolated TPC [17] achieved ZCS transition of all active switches, it suffers from the problem of large conduction loss due to passive mode current circulation through the transformer. Conventional phase-shifted full bridge (PSFB) DC-DC converters enjoy the advantages arising out of ZVS transition of switching devices, but suffer from the problem of large conduction loss due to circulation of passive mode freewheeling current. Several solutions either using passive clamping networks [19], [20], [21], [22], [23], [24] and/or active clamping networks [25], [26], [27], [28] have

been suggested by the researchers to diminish the circulating current.

Considering the merits and limitations of previous topologies, this work modified the basic PSFB converter topology with the addition of a link inductor to create a TPC structure. In the proposed TPC, a simple passive clamp circuit comprising of a diode and two capacitors have been used in the rectifier side, in a similar fashion described in [29] and [30] to completely reset the passive mode circulating current. This enables lagging leg switches of the TPC to operate under ZCS conditions, whereas the leading leg switches operate under ZVS conditions as experienced in conventional PSFB converters. The proposed TPC, integrating SPV source, BESS and the load, provides the features of load port isolation through high frequency transformer, improved power density, less component count, good utilisation of active and passive components, soft-switched transition of semiconductor devices, minimised circulating current loss and high efficiency. The proposed TPC uses simple closed loop control circuitry for MPPT of SPV source, charge/discharge control of BESS and load voltage regulation.
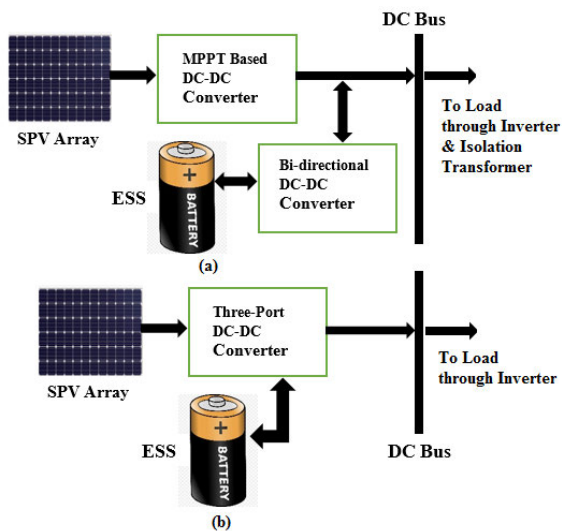

FIGURE 2. Structure of proposed three-port converter.

TABLE 1. Nomenclature.

Symbol	Quantity
$Q_1 - Q_4$	Semiconductor active switches
V_{PV}	Solar Photovoltaic source voltage
V_{BAT}	Battery source voltage
L_S	Link Inductor
$D_1 - D_4$	Anti-parallel body diodes of Semiconductor switches
C_1, C_3	Snubber Capacitor of switch Q_1 and Q_3
$D_5 - D_8$	Full Bridge Rectifier diodes
D_9, D_{10}	Passive auxiliary clamping circuit diodes
C_C	Clamping capacitor
n	Transformer turns ratio
L_{lk}	Transformer leakage inductance
L_O	Filter inductor
V_O	Load voltage
I_O	Load current
V_{CC}	Voltage across clamping capacitor
I_S	Current through link inductor
V_{Rec}	Full-bridge rectifier output voltage
V_{C1}	Voltage across snubber capacitor C_1
V_{pri}	Transformer primary voltage
i_{PRI}	Transformer primary current
i_{CC}	Current through clamping capacitor
i_{D3}	Antiparallel body diode current of Q_3
ω_{rl}	Angular resonant frequency
i_{Q3}	Current through switch Q_3
i_{Q1}	Current through switch Q_1
N_1	No of turn in transformer primary winding
N_2	No of turn in transformer secondary winding
V_F	forward voltage drop of semiconductor
k	Duty cycle loss factor
D	Duty ratio
D_{min}	Minimum duty ratio
D_{max}	Maximum duty ratio
f_s	Switching frequency
ΔI_{LS}	Link inductor current ripple
V^*	MPPT controller generated reference voltage
φ	Phase-shift in diagonal PWM gate pulse

The paper has been organized in five sections. After brief introduction in section I, structure of the proposed converter with steady-state operation in different modes have been described in section II. Section III and section IV discusses the design guideline of power and control circuitry respectively. Simulation and experimental results are presented in section V and performance comparison with existing topologies are described in section VI. Finally, section VII represents the conclusion.

FIGURE 1. a) Conventional hybrid structure, b) Three–port converter structure.

II. PROPOSED THREE-PORT PSFB CONVERTER

The architecture of proposed three-port converter is shown in Fig.2. It uses a modified PSFB structure of four semiconductor switches ($Q_1 - Q_4$) with series-connected SPV source
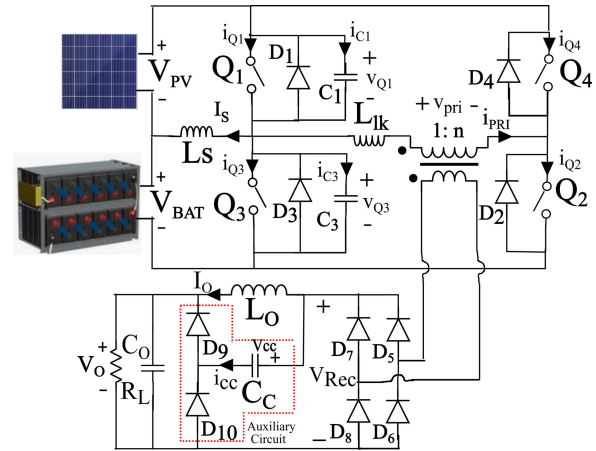
(V_{PV}) and BESS (V_{BAT}) across the D.C. bus. The junction of V_{PV} and V_{BAT} is connected to the mid-point of the leading leg through a link inductor (L_S). The anti-parallel diodes ($D_1 - D_4$) across the switches ($Q_1 - Q_4$) are their integral body diodes and C_1, C_3 are the snubber capacitors. The secondary circuit is formed with a diode bridge ($D_5 - D_8$), L-C filter and an auxiliary clamping network with two diodes (D_9 and D_{10}) and a clamping capacitor (C_C) to minimize the passive mode
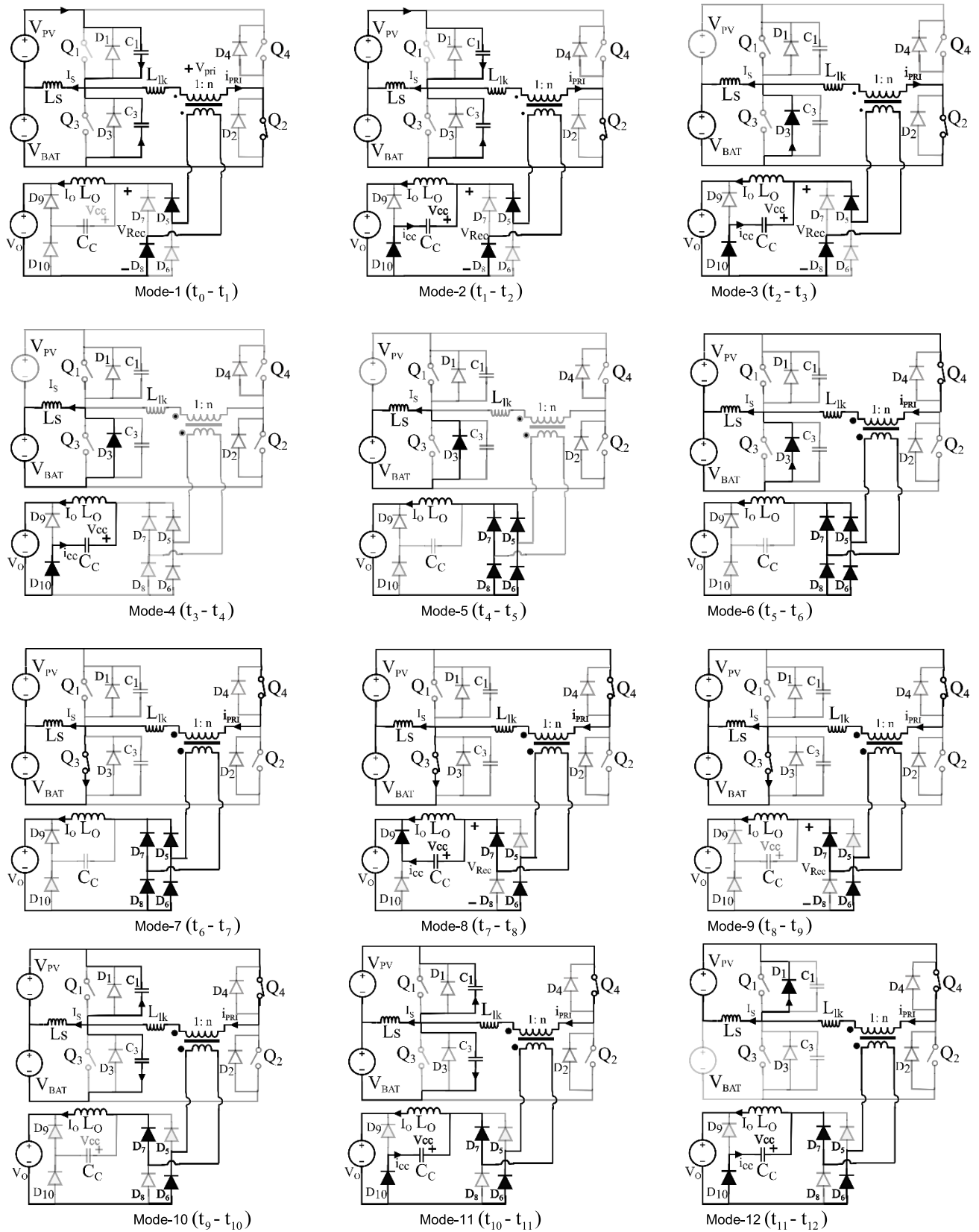
FIGURE 3. Topological stages of proposed PSFB converter.

Mode-13 (t_{12} - t_{13})   Mode-14 (t_{13} - t_{14})   Mode-15 (t_{14} - t_{15})

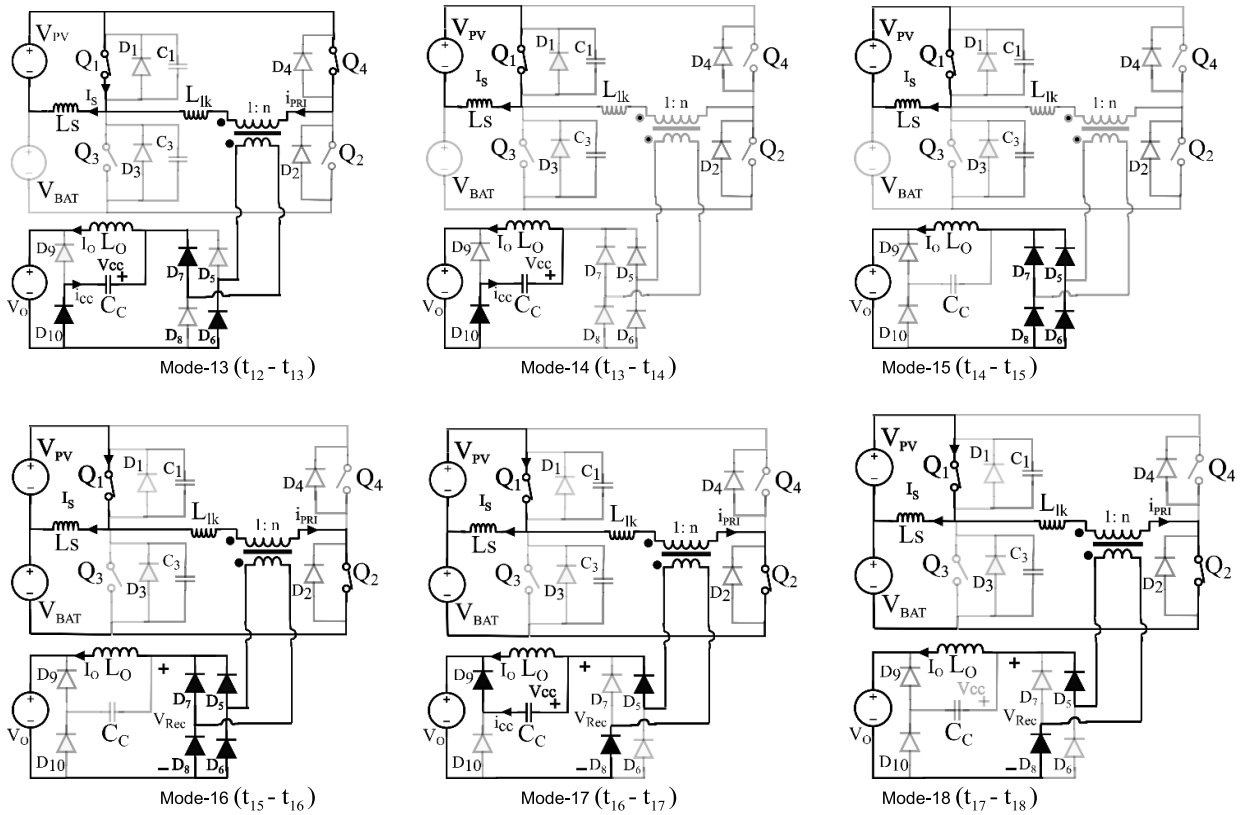Mode-16 (t_{15} - t_{16})   Mode-17 (t_{16} - t_{17})   Mode-18 (t_{17} - t_{18})

FIGURE 3. *(Continued.)* Topological stages of proposed PSFB converter.

circulating current [19]. The primary and secondary circuits are linked through a high frequency transformer with turns ratio 1:n.

The leading leg switches are operated by complementary gate pulses with a dead time to enable ZVS transition of the switches, whereas the dead time between lagging leg complementary gate pulses is to avoid the dead short-circuit of the D.C. bus. The load voltage has been regulated by phase-shift control of leading and lagging switch gate pulses and conventional pulse width modulation (PWM) control algorithm has been used to deliver/extract energy to/from the battery and thus extracting maximum power from the SPV source.

Steady-state converter operation is explained with following assumptions.

i) Ideal behavior of active and passive components.
ii) Transformer leakage inductance (L_{lk}) is very small in comparison to the magnetizing inductance.
iii) Constant currents (I_S and I_O) are maintained by large link inductor (L_S) and filter inductor (L_O) respectively.
iv) The clamping capacitor (C_C) is much larger than the snubber capacitors (C_1 and C_3).
v) Constant load voltage (V_O) is maintained by large filter capacitor.

In active state of the converter, assuming the diagonal switches, Q_1 and Q_2 are in conduction and the primary is impressed with dc bus voltage ($V_{PV} + V_{BAT}$). The secondary

rectified voltage feeds the load through filter inductor (L_O) and the load current (I_O) is reflected to the primary as nI_O. The link inductor (L_S) now gets energized from V_{PV} through Q_1. The snubber capacitor (C_3) is now charged to ($V_{PV} + V_{BAT}$) and the clamping capacitor (C_C) is assumed to be charged to a voltage (V_{CC}), which will be determined in later section. Converter operation is started with the turn-off of Q_1 and a switching cycle is completed in eighteen modes. The equivalent circuits and typical time domain waveforms in each mode are shown in Fig.3. and Fig.4. respectively.

Mode 1 ($t_0 - t_1$): As Q_1 is turned off, C_1 charges and C_3 discharges linearly by the current ($nI_O + I_S$). Thus, transformer primary voltage (V_{pri}) decreases linearly from ($V_{PV} + V_{BAT}$) and secondary rectified voltage (V_{Rec}) decreases accordingly. The important voltage equations are given by,

$$v_{C1}(t) = \frac{I_S + nI_O}{C_1 + C_3}(t - t_0) \tag{1}$$

$$v_{C3}(t) = V_{PV} + V_{BAT} - \frac{I_S + nI_O}{C_1 + C_3}(t - t_0) \tag{2}$$

$$v_{pri}(t) = V_{PV} + V_{BAT} - \frac{I_S + nI_O}{C_1 + C_3}(t - t_0) \tag{3}$$

$$V_{Rec}(t) = n \cdot v_{pri}(t) \tag{4}$$

As V_{Rec} is reduced to V_{CC}, the diode (D_{10}) starts conduction. This mode is ended here and its duration is given below.

$$T_1 = t_1 - t_0 = (C_1 + C_3)\frac{n \cdot (V_{PV} + V_{BAT}) - V_{CC}}{nI_s + n^2 I_O} \tag{5}$$

Mode 2 ($t_1 - t_2$): As D_{10} starts conduction, the rectifier voltage is clamped to V_{CC} and transformer primary voltage continues to decrease as before. This mode ends, when C_1 is charged to ($V_{PV} + V_{BAT}$) and C_3 gets completely discharged. This mode's duration is given below.

$$T_2 = t_2 - t_1 = \frac{(V_{PV} + V_{BAT})(C_1 + C_3)}{I_S + nI_O} - T_1 \quad (6)$$

Mode 3 ($t_2 - t_3$): As C_3 gets completely discharged, the anti-parallel body diode (D_3) provides the conducting path for the transformer primary current and link inductor current. The BESS now gets energized by the stored energy of L_S. As the rectifier voltage is clamped to V_{CC}, the reflected secondary voltage (V_{CC}/n) is now impressed across the primary. Thus, the primary and secondary winding currents start decreasing linearly from nI_O and I_O respectively. The clamping capacitor (C_C) now supplies the balance load current. During this mode, Q_3 is turned on under ZV-ZCS condition, since nearly zero voltage (only diode drop) is applied across it. The governing equations are given below.

$$i_{PRI}(t) = nI_O - \frac{V_{CC}}{nL_{lk}}(t - t_2) \quad (7)$$

$$i_{CC}(t) = \frac{1}{n}i_{PRI}(t) - I_O \quad (8)$$

$$i_{D3} = I_S + i_{PRI}(t) \quad (9)$$

As the primary and secondary winding currents are linearly reduced to zero, the rectifier diodes (D_5 and D_8) are commutated softly and current through Q_2 is linearly reduced to zero. This mode ends here and its duration is given below.

$$T_3 = t_3 - t_2 = \frac{n^2 L_{lk} I_O}{V_{CC}} \quad (10)$$

At t_3, the clamping capacitor voltage is given by,

$$V_{CC}(t_3) = 2\left(\frac{V_{BAT}}{n} - V_O\right)\cos\omega_{r1} T_3 \quad (11)$$

Mode 4 ($t_3 - t_4$): During this mode, C_C supplies the load current (I_O) through D_{10} and the BESS continually gets energized by the stored energy of L_S. As the current through Q_2 is reduced to zero, it can now be turned off under ZCS condition. The clamping capacitor voltage is given by,

$$V_{CC}(t) = v_{CC}(t_3) - \frac{I_O}{C_C}(t - t_3) \quad (12)$$

With complete discharge of clamping capacitor, this mode gets ended with the duration given below.

$$T_4 = t_4 - t_3 = \frac{V_{CC}(t_3)C_C}{I_O} \quad (13)$$

Mode 5 ($t_4 - t_5$): The filter inductor (L_O) now supplies the load current (I_O) through the parallel paths formed by the rectifier diodes. Thus, each rectifier diode conducts half of the load current. As the switch (Q_4) is turned, this passive mode gets over.

Mode 6 ($t_5 - t_6$): With the turn-on of Q_4, the DC bus voltage ($V_{PV} + V_{BAT}$) is impressed across the leakage inductor (L_{lk}),
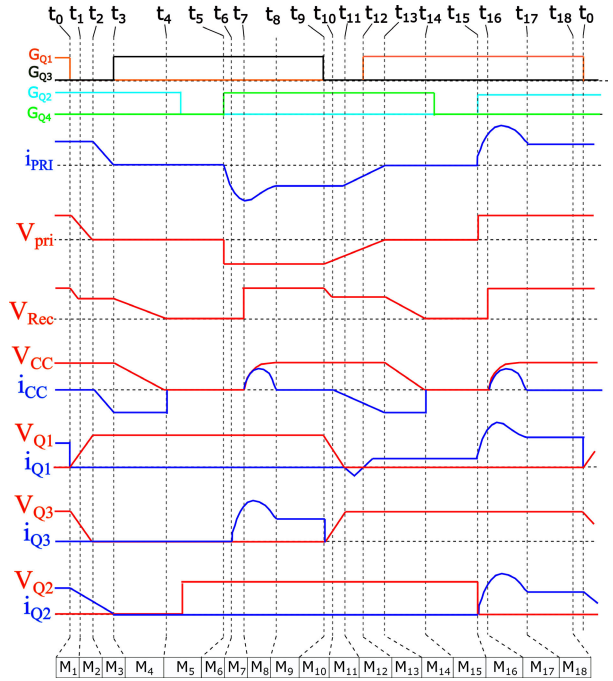

FIGURE 4. Key waveforms of proposed converter.

as the transformer secondary is short circuited by the rectifier diodes. Now, the primary winding current (i_{PRI}) starts increasing linearly from zero in opposite direction through Q_4 and D_3. Thus, the switch (Q_4) turns on with ZCS. With the increase in primary winding current (i_{PRI}), the secondary current increases in the same fashion. Thus, current through the rectifier diodes (D_6 and D_7) increases linearly from $I_O/2$ and the current through the diodes (D_5 and D_8) decreases accordingly. The governing equations are given below.

$$i_{PRI}(t) = -\frac{V_{PV} + V_{BAT}}{L_{lk}}(t - t_5) \quad (14)$$

$$i_{D3}(t) = I_S - i_{PRI}(t) \quad (15)$$

As the primary winding current is linearly reached to I_S, the diode (D_3) commutates softly. This marks the end of this mode, duration of which is given by,

$$T_6 = t_6 - t_5 = \frac{I_S \cdot L_{lk}}{V_{PV} + V_{BAT}} \quad (16)$$

Mode 7 ($t_6 - t_7$): At t_6, the switch (Q_3) starts conduction with zero current, as the excess primary winding current ($i_{PRI} - I_S$) starts flowing through Q_3. During this mode, the primary winding current and the rectifier diode currents change in the same fashion as before. The important current equations are given by,

$$i_{Q3}(t) = \frac{V_{PV} + V_{BAT}}{L_{lk}}(t - t_6) - I_S \quad (17)$$

As the secondary current is reached I_O, the diodes (D_5 and D_8) commute softly. The mode ends here with duration given below.

$$T_7 = t_7 - t_6 = \frac{nI_O L_{lk}}{(V_{PV} + V_{BAT})} \quad (18)$$

Mode 8 ($t_7 - t_8$): After t_7, the dc bus voltage ($V_{PV} + V_{BAT}$) is impressed across the primary and rectifier voltage (V_{Rec}) becomes almost equal to $n(V_{PV} + V_{BAT})$, as the leakage inductance is negligible in comparison to the magnetizing inductance. The clamping capacitor (C_C) now starts getting charged resonantly with the reflected leakage inductance ($n^2 L_{lk}$) through D_9 and the load. Thus, the primary winding current (i_{PRI}) increases resonantly above $n I_O$. The governing equations are given below.

$$i_{PRI}(t) = n I_O + \frac{n(V_{PV} + V_{BAT}) - V_O}{\sqrt{L_{lk}/C_C}} \sin \omega_{r1}(t - t_7) \tag{19}$$

$$V_{CC}(t) = \{n(V_{PV} + V_{BAT}) - V_O\}\{1 - \cos \omega_{r1}(t - t_7)\} \tag{20}$$

$$V_{Rec}(t) = V_O + V_{CC}(t) \tag{21}$$

where,

$$\omega_{r1} = \frac{n}{\sqrt{L_{lk} C_C}} \tag{22}$$

After half resonance period of $n^2 L_{lk}$ and C_C, the charging current of the clamping capacitor (C_C) is reduced to zero and the diode (D_9) is commutated softly. This is the end of this mode. Duration of this mode is given by,

$$T_8 = t_8 - t_7 = \frac{\pi}{\omega_{r1}} \tag{23}$$

At t_8, the primary current is reduced to $n I_O$ and C_C is charged to its peak voltage (V_{CC}) given by,

$$V_{CC} = V_{CC}(t_8) = 2\{n(V_{PV} + V_{BAT}) - V_O\} \tag{24}$$

Mode 9 ($t_8 - t_9$): In this mode, the secondary rectified voltage $n(V_{PV} + V_{BAT})$ supplies the load current (I_O) and also energizes the filter inductor (L_O). The BESS (V_{BAT}) continues to get energized by the link inductor current (I_S) as before. The switch (Q_4) conducts the primary current ($n I_O$) and Q_3 conducts the current ($n I_O - I_S$). This is the active or powering mode, which gets over with the turn-off of Q_3.

Mode 10 ($t_9 - t_{10}$): As Q_3 is turned off, C_3 gets charged linearly from zero and C_1 discharges from ($V_{PV} + V_{BAT}$) by the current ($n I_O - I_S$). Thus, Q_3 turns off under ZVS condition. The transformer primary voltage (V_{pri}) now decreases linearly from ($V_{PV} + V_{BAT}$) and accordingly, the secondary rectified voltage (V_{Rec}) from $n(V_{PV} + V_{BAT})$. The important voltage equations are given by,

$$v_{C1}(t) = V_{PV} + V_{BAT} - \frac{n I_O - I_S}{C_1 + C_3}(t - t_9) \tag{25}$$

$$v_{C3}(t) = \frac{n I_O - I_S}{C_1 + C_3}(t - t_9) \tag{26}$$

$$v_{pri}(t) = -v_{C1}(t) \tag{27}$$

$$V_{Rec}(t) = n \cdot V_{pri}(t) \tag{28}$$

As, the rectifier voltage is decreased to V_{CC}, D_{10} gets forward biased and starts conduction. The mode ends here with duration given below.

$$T_{10} = t_{10} - t_9 = \frac{(C_1 + C_3)[n(V_{PV} + V_{BAT}) - V_{CC}]}{n I_s + n^2 I_O} \tag{29}$$

Mode 11 ($t_{10} - t_{11}$): At t_{10}, the rectifier voltage (V_{Rec}) is clamped to V_{CC}. However, the transformer primary voltage decreases linearly as before. As C_3 is charged to ($V_{PV} + V_{BAT}$) and C_1 discharges completely, this mode gets over with a duration given by,

$$T_{11} = t_{11} - t_{10} = \frac{(V_{PV} + V_{BAT})(C_1 + C_3)}{I_S + n I_O} - T_{10} \tag{30}$$

Mode 12 ($t_{11} - t_{12}$): As C_1 gets discharged, the current ($n I_O - I_S$) is conducted through the anti-parallel body diode (D_1) of Q_1. The SPV voltage (V_{PV}) is now impressed across L_S through D_1 and hence L_S starts getting energized from V_{PV}. The reflected secondary voltage (V_{CC}/n) is now impressed across transformer primary and hence the primary current (i_{PRI}) decreases linearly from $n I_O$. As D_1 is in conduction, Q_1 can now be turned on under ZVS conduction. The governing voltage and current equations are given by,

$$i_{PRI}(t) = n I_O - \frac{V_{CC}}{n L_{lk}}(t - t_{11}) \tag{31}$$

$$i_{CC}(t) = I_O - \frac{i_{PRI}(t)}{n}(t - t_{11}) \tag{32}$$

$$i_{D1} = i_{PRI}(t) - I_S \tag{33}$$

As the primary current is reduced to I_S, D_1 is commutated softly. This marks the end of this mode, duration of which is given by.

$$T_{12} = t_{12} - t_{11} = \frac{n L_{lk}(n I_O - I_S)}{V_{CC}} \tag{34}$$

Mode 13 ($t_{12} - t_{13}$): In this mode, the primary current (i_{PRI}) continues to decrease and L_S gets energized through Q_1, as before. The important current equations are given by,

$$i_{PRI}(t) = I_S - \frac{V_{CC}}{n L_{lk}}(t - t_{12}) \tag{35}$$

$$i_{Q1} = I_S - i_{PRI}(t) \tag{36}$$

As the primary current is linearly reduced to zero, the rectifier diodes (D_6 and D_7) are commutated softly. The mode ends here with duration given below.

$$T_{13} = t_{13} - t_{12} = \frac{n^2 L_{lk} I_O}{V_{CC}} \tag{37}$$

At t_{13}, the clamping capacitor voltage (V_{CC}) is given below.

$$V_{CC}(t) = 2(\frac{V_{PV}}{n} - V_O) \cos \omega_{r1}(t - t_{12}) \tag{38}$$

Mode 14 ($t_{13} - t_{14}$): In this mode, C_C supplies the entire load current (I_O) through D_{10} and L_S gets energized from V_{PV} as before. The switch (Q_4) can now be turned off under ZCS condition, as its current has already been reduced to zero. The clamping capacitor voltage (V_{CC}) is given by,

$$V_{CC}(t) = V_{CC}(t_3) - \frac{I_O}{C_C}(t - t_{13}) \tag{39}$$

As C_C is completely discharged, the rectifier diodes ($D_5 - D_8$) get forward biased and the mode is ended with following duration.

$$T_{14} = t_{14} - t_{13} = \frac{V_{CC}(t_{13})C_C}{I_O} \quad (40)$$

Mode 15 ($t_{14} - t_{15}$): During this mode, the filter inductor (L_O) supplies the load current (I_O) through rectifier diodes ($D_5 - D_8$). Each rectifier diode conducts half of the load current. This is the second passive mode, which gets over with turn-on of Q_2 at t_{15}.

Mode 16 ($t_{15} - t_{16}$): As Q_2 is turned on and transformer secondary is short circuited by rectifier diodes, the dc bus voltage ($V_{PV} + V_{BAT}$) is impressed across the leakage inductor (L_{lk}) and its current (i_{PRI}) starts increasing linearly from zero. Thus, Q_2 turns on under ZCS condition. As, the primary winding current increases, the current through D_5 and D_8 increases from $I_O/2$ and the currents through D_6 and D_7 decreases accordingly. The governing equations are given by,

$$i_{PRI}(t) = \frac{V_{PV} + V_{BAT}}{L_{lk}}(t - t_{15}) \quad (41)$$

$$i_{Q1}(t) = I_S + i_{PRI}(t) \quad (42)$$

As i_{PRI} becomes equal to the reflected load current (I_O/n), the diodes (D_6 and D_7) recover softly. This mode ends here after a duration given below.

$$T_{16} = t_{16} - t_{15} = \frac{I_S \cdot L_{lk}}{V_{PV} + V_{BAT}} \quad (43)$$

Mode 17 ($t_{16} - t_{17}$): Almost the entire dc bus voltage ($V_{PV} + V_{BAT}$) is now impressed across transformer primary. The clamping capacitor (C_C) gets charged in resonance with the reflected leakage inductance (n^2L_{lk}) through D_9 and the load. The important current and voltage equations are given by,

$$i_{PRI}(t) = nI_O + \frac{n(V_{PV} + V_{BAT}) - V_O}{\sqrt{L_{lk}/C_C}} \sin \omega_{r1}(t - t_{16}) \quad (44)$$

$$V_{CC}(t) = \{n(V_{PV} + V_{BAT}) - V_O\}\{1 - \cos \omega_{r1}(t - t_{16})\} \quad (45)$$

$$V_{Rec}(t) = V_O + V_{CC}(t) \quad (46)$$

After half resonance period, C_C is charged to V_{CC} again and primary winding current is minimised to nI_O. Duration of this mode is given by,

$$T_{17} = t_{17} - t_{16} = \frac{\pi}{\omega_{r1}} \quad (47)$$

Mode 18 ($t_{17} - t_{18}$): During this mode, the secondary rectified voltage $n(V_{PV} + V_{BAT})$ supplies the load current (I_O) and also energizes the filter inductor (L_O). The link inductor (L_S) gets energized from the source (V_{PV}). This is the second active or powering mode of the converter.

This mode is ended with the turn-off of Q_1 and operation of the next cycle is repeated.

TABLE 2. Specifications and major components.

Element	Specifications
Source 1 (SPV Source)	V_{OC} = 140 V, V_{MP} = 100 V – 110 V, I_{MP} = 1.5 A, I_{SC} = 1.6 A, P_{MP} = 165 W
Source 2 (Battery bank)	V_{BAT} = 48 V
Rated output	V_O = 48 V, I_O = 3 A
Switching frequency	f_S = 100 kHz
Capacitors Inductors	C_{CC} = 2.2 nF , $C_1 = C_3$ = 1 nF, C_O = 10 μF L_S = 650 μH, L_m = 13.6 μH, L_O = 175 μH.
Active Switch	Q_1 and Q_3 - STF26N60N (600 V, 20 A) Q_2 and Q_4 - G4PC50UD (600 V, 27 A)
Power Diode	($D_5 - D_{10}$)- MUR1560 (600 V, 15 A)

III. DESIGN GUIDELINES

This section provides concise design guidelines towards selection of passive and active elements of the converter with specifications detailed in Table 2. The design exercise is based on the converter dynamic equations, stated in section II.

A. ISOLATION TRANFORMER

The transformer turns-ratio (n) has been fixed in accordance with the traditional method [30] as below.

$$n = \frac{N_2}{N_1} = \frac{V_O + 2V_F}{2 \cdot k \cdot D \cdot (V_{PV} + V_{BAT} - 2V_F)} \quad (48)$$

Here, V_F represents the forward voltage drop of semiconductor devices and k is the factor accounting for duty cycle loss due to leakage inductance. Considering V_F and *k* to be 1 V and 0.95 respectively and the maximum permissible duty ratio (*D*) corresponding to the minimum PV voltage of 100 V is considered to be 0.45, the transformer turns-ratio (*n*) is obtained to be 0.85. The minimum duty ratio (D_{min}) corresponding to maximum PV voltage (140V) is also obtained to be 0.35.

B. LINK INDUCTOR (L_S)

At the input of the TPC, the leading leg switches (Q_1 and Q_3) with their anti-parallel integral body diodes and the link inductor (L_S) formed a bidirectional buck-boost converter structure between the input ports (V_{PV} and V_{BAT}). Hence, the link inductor (L_S) has been selected in conventional way from the following relation.

$$L_S = \frac{V_{PV} \cdot D_{max}}{\Delta I_{LS} \cdot f_S} \quad (49)$$

Here, an input inductor of 650 μH has been selected for the buck-boost converter such that it operates little above boundary conduction mode.

C. CLAMPING CAPACITOR (C_C)

In the active or powering mode with diagonal switches in conduction, the clamping capacitor (C_C) of the converter gets resonantly charged to peak voltage (V_{CC}) expressed in equation (24). As the leading leg switch (Q_1 or Q_3) is turned off to terminate the active mode, the reflected clamping capacitor voltage is impressed across transformer primary and reset the leakage current. This helps in minimizing the unwanted passive mode conduction loss and consequently ZCS turn-on of the lagging leg switch (Q_2 or Q_4). This operational sequence is possible if the clamping capacitor (C_C) can supply the load current (I_O) for the duration from turn-off of the leading leg switch to at least until the leakage current is reset. In the design analysis, the clamping capacitor (C_C) is selected based on an overestimated consideration that C_C solely supplies the load power during the period mentioned above satisfying following condition.

$$\frac{1}{2} C_C \cdot V_{CC}^2 \geq V_O \cdot I_O (T_{11} + T_{12} + T_{13}) \tag{50}$$

It is estimated from equations (24), (30), (34), (37) and (50) that, the clamping capacitor (C_C) should be larger than 1 nF. However, a large C_C increases the current stress of the semiconductor switches and diodes, as evident from equation (19). Therefore, to get an optimum performance a 2.2 nF polyester capacitor has been selected for C_C with a safe margin.

D. SNUBBER CAPACITOR (C_1 AND C_3)

The primary role of the snubber capacitors (C_1 and C_3) is to reduce the turn-off dv/dt of the leading leg switches (Q_1 and Q_3). Although, large snubber capacitors improve switching performance due to reduced turn-off dv/dt, but requires large charging/discharging time at turn-off of the leading switch. If charging and discharging of outgoing switch snubber capacitor and complementary incoming switch snubber capacitor respectively is not completed within the dead time, then the incoming switch suffers from large current spike due to hard-switched turn-on. The time ($T_1 + T_2$) required for charging/discharging of the snubber capacitors are obtained from equation (6) as below.

$$T_1 + T_2 = \frac{(V_{PV} + V_{BAT})(C_1 + C_3)}{I_S + nI_O} \tag{51}$$

It is evident from equation (51) that apart from snubber capacitors, charging/discharging time ($T_1 + T_2$) also depends on converter load condition. The variation of charging/ discharging time ($T_1 + T_2$) for different snubber capacitors under different load conditions are plotted in Fig. 5. In the design analysis, considering maximum switch duty ratio of 0.45 and keeping a safe margin of 0.2 μs, the maximum permissible limit of ($T_1 + T_2$) has been set to 0.3 μs. If the charging/discharging time ($T_1 + T_2$) of the snubber capacitors exceeds 0.3 μs, then the lagging leg switch may suffer from hard-switched turn-on and large current stress. Thus, an optimum solution with the selection of 1nF polyester capacitors have been made for the snubber capacitors (C_1 and C_3), such
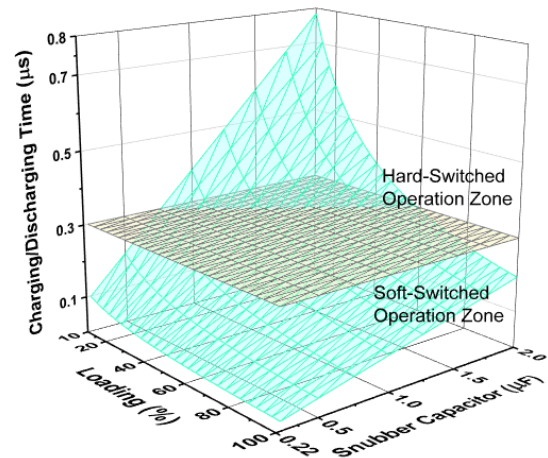

FIGURE 5. Charge/discharge requirement of snubber capacitors under different loading conditions.

that soft-switched turn-on of the lagging leg switch can be achieved for wide range from full load to 20% loading and simultaneously, the turn-off dv/dt of the leading leg switch is also within acceptable limit.

E. SEMICONDUCTOR DEVICES

The voltage stress of the switches is equal to ($V_{PV} + V_{BAT}$) and their current stress as computed from equation (19) is calculated to be 6 A. As the leading leg switches (Q_1 and Q_3) change their switching states under ZVS condition, they have been realized with MOSFETs (STF26NM60N, 600 V, 20 A). The parasitic body capacitors of the MOSFETs have been effectively used in the ZVS transitions. However, IGBTs (IRG4PC50UD, 600 V, 27 A) have been selected for the lagging leg switches (Q_2 and Q_4), since they operate under ZCS condition. Thus, the lagging leg switches (IGBTs) are also saved from unwanted tail currents [31].

The peak current and maximum voltage stress of the rectifier diodes are found to be 5.4 A and 256 V respectively. Hence, ultrafast schottky diodes (RHRP1560) with current and voltage rating of 15 A and 600 V respectively have been selected here.

IV. CONTROL SCHEME

The control circuitry of proposed three-port converter, as shown in Fig. 6, has two closed loops. The input loop uses the input voltage controller (IVCON) for MPPT control of SPV source and the output loop has output voltage controller (OVCON) for load voltage control. Voltage (V_{PV}) and current (i_{PV}) signals of SPV source are sensed by the MPPT controller and then following incremental conductance algorithm [32], [33], [34] a reference voltage signal (V^*) corresponding to the maximum power point (MPP) is generated. The error signal obtained by comparing the SPV voltage (V_{PV}) to V^* is fed to IVCON block, which in turn generates appropriate PWM signals corresponding to MPP of SPV source. The OVCON block primarily regulates the
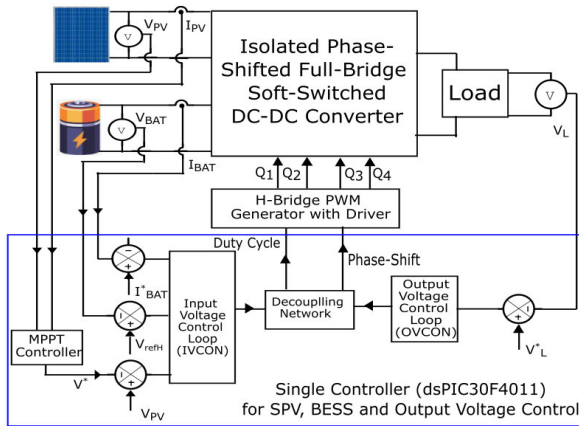
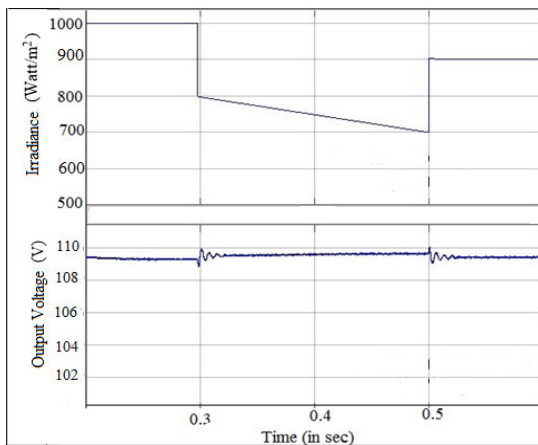**FIGURE 6.** Overall control scheme of proposed converter.

FIGURE 8. Experimental setup.

FIGURE 7. Irradiance and output voltage variation of the converter.

FIGURE 9. MPPT tracking by three-port PSFB Converter.

output voltage by proper control of the phase shift (φ) among the PWM gate signals of PSFB switches.

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed three-port converter with TYPE-II compensators in the input and output voltage controllers has been simulated in MATLAB Simulink. The important results in terms of dynamic response of the MPPT controller are presented in this section. Fig. 7 shows the converter output voltage against variation in solar irradiance, which is changed abruptly from 1000 W/m² to 800 W/m², followed by linear decrease to 700 W/m² and finally stepped up to 900 W/m². It is observed that, the SPV voltage is returned to the steady state with a small overshoot of 1.5 V and within a settling time of few milliseconds.

A. EXPERIMENTAL RESULTS

A laboratory scale prototype of proposed three-port converter with specifications detailed in Table 1 has been developed for real time experimentation and performance verification. Fig. 8 shows the experimental setup with solar emulator (ITECHIT6514C) as 110 V/165 W SPV source, battery emulator (ITECH IT6433) as 48V BESS and DC electronic
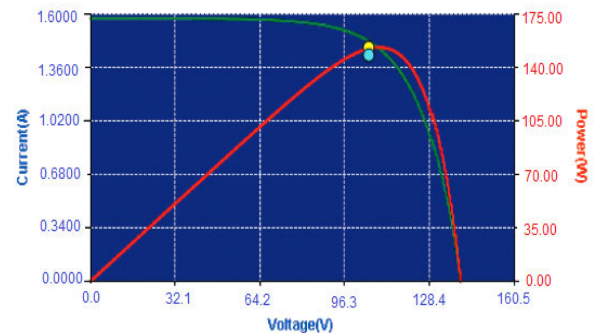
load (ITECH IT8512B) at output port. The proposed converter uses dsPIC30f4011 microcontroller for incremental conductance based MPPT control, developed in Microchip MPLAB software using C30 compiler. Controller generated phase shifted gate pulses of switching frequency 100 kHz are fed to the switches through dual channel gate drivers (Texas Instruments UCC21520). Important test results captured under different conditions of solar irradiance and load variation are presented here. The SPV emulator observations recorded during laboratory testing of the converter at a solar irradiance of 1000 W/m² are summarized in Table 3 and the corresponding operating point on the I-V and P-V characteristics are shown in Fig. 9. It is observed that, the converter is drawing SPV power with 96.6% MPPT efficiency.

Switching voltage and current waveforms of different semiconductor devices, as captured by digital storage oscilloscope (DSO) are also presented in this section. Fig. 10 shows the gate pulses of Q_1 and Q_2 along with the voltage and current waveforms of leading leg switch (Q_1). It is observed that, Q_1 turns on with zero voltage across it and it is turned off under ZVS condition. Similarly, ZVS turn-on and ZVS turn-off of another leading leg switch (Q_3) is also evident from Fig. 11. The switching gate pulses of Q_3 and Q_4 along with voltage and current waveforms of lagging leg switch (Q_4) as produced in Fig. 12 shows that at turn-on its current starts from zero and it is reduced to zero before withdrawal of the gate pulse. Thus, ZCS transitions of Q_4 at both the switching instants are clearly established. Fig. 13 showing phase-shifted
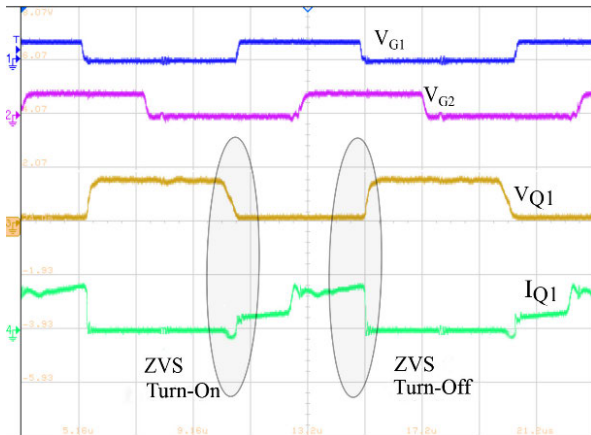
FIGURE 10. ZVS transition of leading leg switch (Q_1): Experimental waveforms of Q_1, Q_2 gate pulses (scale: 20V/div) Q_1 voltage (scale: 150V/div) and Q_1 current (scale: 5 A/div).
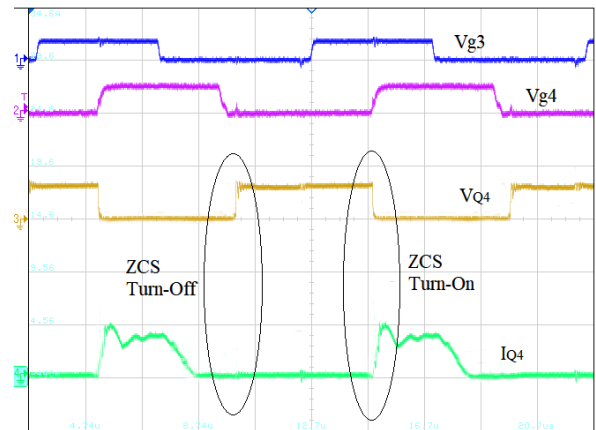

FIGURE 12. ZVS transition of lagging leg switch (Q_4): Experimental waveforms of Q_3, Q_4 gate pulses (scale: 20V/div), Q_4 voltage (scale: 150V/div) and Q_4 current (scale: 5A/div).
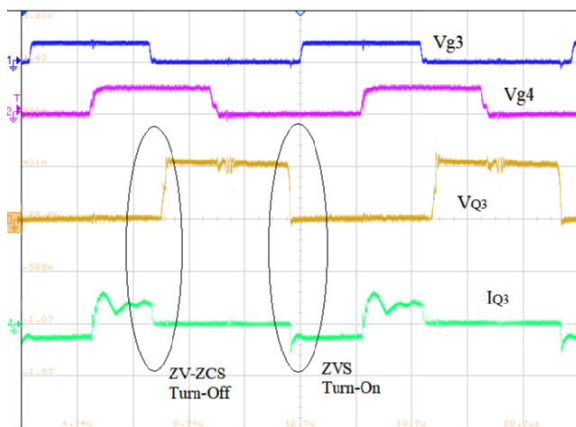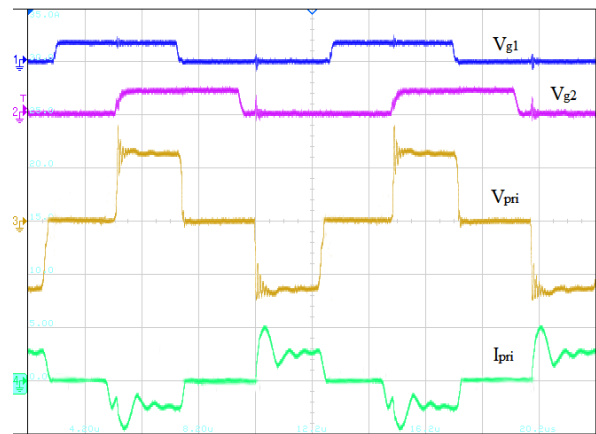

FIGURE 11. ZVS transition of leading leg switch (Q_3): Experimental waveforms of Q_3, Q_4 gate pulses (scale: 20V/div), Q_3 voltage (scale: 100V/div) and Q_3 current (scale: 5 A/div).

FIGURE 13. Circulating current minimization of transformer: Experimental waveforms of Q_1, Q_2 gate pulses (scale: 20V/div), primary voltage (scale: 100V/div) and primary current (scale: 5A/div).

TABLE 3. SPV emulator captured experimental results.

Element	Specifications	
Rated parameters	MPP Voltage:	110 V
	MPP Power:	165 W
Experimental Results	MPP Voltage:	109.2 V
	Extracted Power:	159.43 W
	MPPT Efficiency:	96.6%

gate pulses to diagonal switches (Q_1 and Q_2) along with voltage and current waveforms at transformer primary clearly verifies successful minimization of passive mode circulating current, thereby validating the predicted analysis.

VI. COMPARISON

This section presents performance comparative analysis of the proposed topology with two non-isolated [14], [15] and four isolated [16], [17], [35], [36] TPC structures of previous literatures. The comparison is drawn from the viewpoint of load port isolation, active and passive component count, component utilisation, transition behaviour of active switches, circulating current loss and control circuit complexity. The comparison parameters are summarised in Table 4. Amongst the five isolated TPC structures, converter [16] has minimum count of active and passive components with good utilisation of the components. But, this converter suffers from the problems of hard-switched transition of the secondary switches, large circulating current loss and requirement of complex control circuitry. All semiconductor switches of the converters [35], [36] operate under ZVS conditions and they use a use comparatively simple control circuitry. Large count of active and passive components and large circulating current loss are the primary disadvantages of these TPCs. The converter [17] is better than the above structures in terms of less component count, soft-switching behaviour and minimised circulating current loss, but requires complex control circuitry than other versions. The converter structure proposed in this work has avoided most of the limitations suffered by TPCs of earlier literatures. The proposed topology provides load port isolation, less component count, good utilisation of active and

TABLE 4. Comparison between three port onverters.

Converter Features \ Reference Converters	[14]	[15]	[16]	[17]	[35]	[36]	Proposed topology
Load port isolation	Non-isolated	Non-isolated	Isolated	Isolated	Isolated	Isolated	Isolated
Semiconductor component count	4 MOSFETs and 5 Diodes	5 MOSFETs	5 MOSFETs and 1 Diode	3 MOSFETs and 3 Diodes	18 MOSFETs	12 MOSFETs	4 MOSFETs and 6 Diodes
Passive component count	4 inductors and 2 capacitors	4 capacitors	1 inductor and 3 capacitors	3 inductor and 5 capacitors	6 inductor and 2 capacitors	4 inductors and 2 capacitors	2 inductors and 1 capacitor
Active and passive component utilization	Good	Weak	Good	Moderate	Weak	Moderate	Good
Switching transition of active switches	ZVS transition of all switches	ZVS transition of all switches	ZVS transition of primary switches. Hard-switched transition of secondary switches	ZCS transition of all switches	ZVS transition of all switches	ZVS transition of all switches	ZVS transition of leading leg switches. ZCS transition of lagging leg switches
Circulating current loss	-	-	High	Minimized	High	Very high	Minimized
Control circuit complexity	Simple	Medium	High	High	Medium	Medium	Simple

passive components, soft transition of semiconductor devices, minimised circulating current loss and requirement of simple control circuitry.

VII. CONCLUSION

A battery integrated isolated three-port converter is presented in this work for wide applications in SPV power systems. The proposed converter uses a modified of PSFB structure with following features.

1. The converter integrates a SPV source, battery energy storage, and DC load.
2. The load port is electrically isolated from the SPV source and battery port.
3. All semiconductor switches of the converter are operated under ZVS or ZCS conditions for wide load variation.
4. The power diodes of the converter recover softly.
5. The converter is operated at high switching frequency improving its power density.
6. Circulating current loss of this converter has been minimized using a secondary passive clamping circuit.

Real time Performance of the proposed TPC has been successfully validated by testing a 144W laboratory-scale hardware prototype operating at 100 kHz switching frequency. Close agreements between recorded experimental results and theoretical predictions have been clearly observed.

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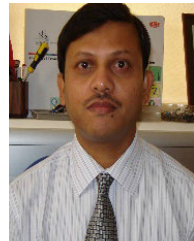
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