IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 9 May 2023, accepted 7 June 2023, date of publication 16 June 2023, date of current version 21 June 2023.

*Digital Object Identifier 10.1109/ACCESS.2023.3286976*

RESEARCH ARTICLE

# Curing Process on Passivation Layer for Backside-Illuminated CMOS Image Sensor Application

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This work was supported in part by the Ministry of Trade, Industry, and Energy (MOTIE) and the Korea Evaluation Institute of Industrial Technology (KEIT) through the Korea Semiconductor Research Consortium (KSRC) Support Program for the Development of Future Semiconductor Devices under Grant 20010574 and Grant RS-2023-00234828; in part by the National Research Foundation of Korea (NRF) through the Korea Government [Ministry of Science and ICT (MSIT)] under Grant NRF-2020M3F3A2A02082436; and in part by the Brain Korea 21 Fostering Outstanding Universities for Research (BK21 FOUR) Program.

**ABSTRACT** We fabricated Al/$Al_2O_3$/$SiO_2$/Si and Al/$HfO_2$/Si structures to optimize the passivation layer of a backside-illuminated (BSI) complementary metal oxide semiconductor (CMOS) image sensor (CIS), with the key properties of the newly developed high-*k* passivation layer analyzed via border traps, interface traps, and fixed charges. In the first experiment using $Al_2O_3$/$SiO_2$ bilayer-based structures, different thicknesses of $SiO_2$ were applied from 0 to 15 nm. The improvement in their properties was confirmed by applying forming gas annealing (FGA), a type of post-treatment, to all experimental systems. The first experiment results indicated that both the $SiO_2$ layer and FGA were effective for chemical passivation. However, a tradeoff occurred in the degree of improvement of the interface trap density ($D_{it}$) and fixed-charge density ($Q_f$) according to the $SiO_2$ layer thickness. Subsequently, in the second experiment using $HfO_2$ single-layer-based structures, FGA improved the border trap to a relatively poor extent compared to the first experiment. Nevertheless, FGA improved the electrical characteristics of the $HfO_2$ films without any side effects and results in optimal $D_{it}$ and $|Q_f/q|$ values of $2.59 \times 10^{11}$ $eV^{-1}$ $cm^{-2}$ and $1.00 \times 10^{12}$ $cm^{-2}$, respectively, demonstrating its potential for the passivation layer in BSI CIS applications.

**INDEX TERMS** Plasma-enhanced atomic layer deposition, forming gas annealing, CMOS image sensor, surface passivation, $SiO_2$, $HfO_2$.

## I. INTRODUCTION

Complementary metal oxide semiconductor (CMOS) image sensors (CISs), used in various fields, such as autonomous vehicles, intelligent monitoring systems, and mobile devices [1], [2], [3], have steadily increased in popularity. CIS development has mainly focused on pixels, i.e., the basic units of CISs; pixel size was gradually reduced to enhance the resolution by increasing the number of pixels in the same area [4]. However, the benefits of reducing the size were offset by side effects, such as (1) light reflection and cross-talk [5] and (2) reduction of the full-well capacitor [6].

Thus, a backside-illuminated (BSI) structure was introduced to address the critical issues encountered in scaled pixels [7]. However, thinning the substrate in the BSI structure can cause many defects on its surface, which increases its fatal dark-current [7], [8], [9]. In these systems, the passivation layer is in direct contact with the rough surfaces of the substrate [7]. Therefore, to ensure the stable utilization of the BSI structure, it is crucial to improve the interface characteristics between the passivation layer and substrate through appropriate treatments. A high-*k* passivation layer can be

The associate editor coordinating the review of this manuscript and approving it for publication was Chaitanya U. Kshirsagar.

introduced to increase the full-well capacitance [10] and provide an additional solution for the dark-current issue. This solution is attributed to the field-effect passivation caused by the fixed charge present inside the high-k material [11], [12]. However, the field-effect passivation is insufficient for overcoming the dark-current problem. Therefore, chemical passivation should be considered together to limit the effects of interfacial traps [13].

Atomic layer deposition (ALD) is one of the most attractive methods for depositing high-*k* materials because it can optimize chemical defects while maintaining high uniformity [14], [15]. ALD is advantageous for BSI structures because it can be performed at low temperatures [7]. However, the deposition rate is too low to deposit a thick passivation layer. Therefore, plasma-enhanced ALD (PEALD) is utilized to increase the deposition rate at low temperatures [16], [17]. However, in the PEALD process, the interface quality may deteriorate because of plasma-induced damage [17], [18], which can be rectified using various treatments, as shown in our previous study [19]. However, further improvements to this process are required.

In this study, we applied two approaches to improve upon the results of a previous study [19]: adding a thermal $SiO_2$ layer (first experiment) and replacing $Al_2O_3$ with $HfO_2$ (second experiment). Although $SiO_2$ has a lower permittivity ($\sim$3.9) and refractive index ($\sim$1.4) than $Al_2O_3$ [20], [21], $SiO_2$ has the advantage of forming a stable bonding structure because of its good compatibility with the Si substrate. Conversely, $HfO_2$ has a higher permittivity ($\sim$25) and refractive index ($\sim$1.93) than $Al_2O_3$ [20], [22]; therefore, it may also be advantageous for CIS applications.

In the first experiment, improvements resulting from the $SiO_2$ layer and forming gas annealing (FGA) were confirmed for the $Al_2O_3/SiO_2$ bilayer-based samples. FGA was applied in all experiments as a post-treatment process. However, when the $SiO_2$ layer became thinner, the resulting chemical passivation was insufficient, owing to the many traps at the $Al_2O_3/SiO_2$ interface. Furthermore, the fixed charge was canceled when the $SiO_2$ layer became thicker, resulting in weakened field-effect passivation. In contrast, in the second experiment, the FGA process resulted in stable development for the $HfO_2$ single-layer-based samples, sufficiently decreasing the interface trap density ($D_{it}$), approximately 98% lower than the lowest $D_{it}$ reported in a previous study [19]. The improved fixed charge density ($Q_f$), which was not ideal, was deemed sufficient for field-effect passivation [11].

## II. SAMPLE PREPARATION AND EXPERIMENTAL DETAILS

Metal-insulator-semiconductor (MIS) capacitors were fabricated as shown in **Fig. 1**. **Table 1** lists the process condition splits of the MIS capacitors.

In the first experiment, thermal $SiO_2$ was grown on a p-type Si substrate [18 $\Omega \cdot$ cm, (100)] to improve the interface quality. $Al_2O_3$ films were then deposited by PEALD using a trimethyl aluminum (TMA, $Al(CH_3)_3$) precursor with $O_2$ plasma and an ALD reactor (Plus 200 system, Quros) at a substrate temperature of 300 °C [19], [23], maintaining the same process conditions as before. Furthermore, during the deposition, the Ar purge and $O_2$ flow rates were 500 and 100 sccm, respectively, and the chamber pressure was 0.4 mTorr [19], [23]. The $SiO_2$ films had various thicknesses ($T_{SiO2}$ = 0, 5, 10, and 15 nm), whereas the thickness of the $Al_2O_3$ films was fixed at 30 nm. Top Al electrodes with a thickness of 500 nm and diameter of 300 $\mu$m were deposited using an e-beam evaporator with a shadow mask. The MIS capacitors were annealed using FGA in $N_2$ 95% + $H_2$ 5% ambient conditions in a tube furnace at 400 °C for 30 min to improve the still unstable bonding between $Al_2O_3$ and $SiO_2$.

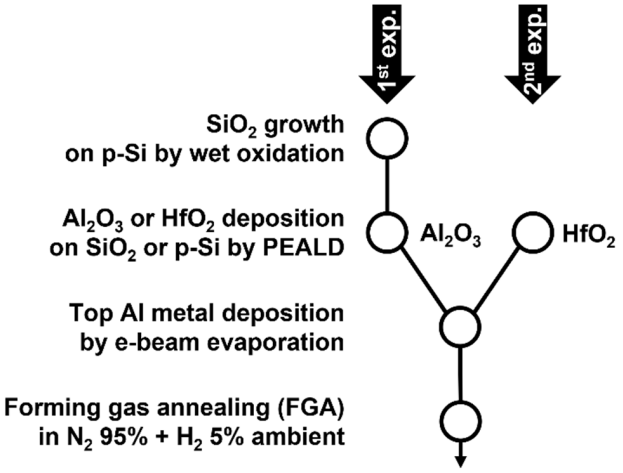


**FIGURE 1.** Process flows of the $Al/Al_2O_3/SiO_2/Si$ and $Al/HfO_2/Si$ structures.

**TABLE 1.** $Al_2O_3/SiO_2$ and $HfO_2$ samples with various treatments.

| Samples | $SiO_2$ Thickness ($T_{SiO2}$) | High-*k* | FGA |
|---|---|---|---|
| S1_$T_{SiO2}$_as_dep | 0 [19]/5/10/15 nm | $Al_2O_3$ | X |
| S1_$T_{SiO2}$+FGA | 0/5/10/15 nm | $Al_2O_3$ | O |
| S2_as_dep | 0 nm | $HfO_2$ | X |
| S2+FGA | 0 nm | $HfO_2$ | O |

In the second experiment, in the absence of $SiO_2$, $Al_2O_3$ was replaced with $HfO_2$ in the structure used in the first experiment. $HfO_2$ films were deposited on a p-type Si substrate used in the first experiment by PEALD using a tetrakis-ethyl-methylamino hafnium (TEMAHf, $Hf[N(CH_3)C_2H_5]_4$) precursor with $O_2$ plasma at a substrate temperature of 280 °C [24]. The thickness of the $HfO_2$ film was fixed at 20 nm. The absence of $SiO_2$ can be advantageous for high-*k* materials. However, the resulting unstable bonding properties of $HfO_2$ must be addressed. Therefore, the MIS capacitors were annealed using FGA, as in the first experiment. The other process conditions were the same as those in the first experiment.

In both experiments, the capacitance-voltage (C-V) curves were measured using an Agilent B1500A semiconductor characterization system at a multifrequency range of 1 kHz to 1 MHz, with all measurements conducted at room temperature under dark conditions.

The number of border traps was estimated from the frequency dispersion of the C-V curves in the accumulation region [25], and the oxide-trapped charge was calculated from the C-V hysteresis curves [26]:

$$D = \frac{C_{High} - C_{Low}}{C_{High}} \times \frac{100}{log\left(f_{High}\right) - log(f_{Low})} [\%/dec] \quad (1)$$

where $D$ is the frequency dispersion and $C_{High}$ and $C_{Low}$ are the capacitance values in the accumulation region at $f_{High}$ (1 MHz) and $f_{Low}$ (1 kHz), respectively.

$$N_{trapped} = \frac{C_{ox} \times \Delta V_{FB}}{q} [cm^{-2}] \quad (2)$$

Here, $N_{trapped}$ is the number of oxide-trapped charges, $q = 1.6 \times 10^{-19}$ $[C]$, $C_{ox}$ is the capacitance measured in the accumulation region, and $\Delta V_{FB}$ is the flat-band voltage ($V_{FB}$) difference between forward- and reverse-direction scans. $V_{FB}$ was extracted using the $[(C_{ox}/C)^2 - 1] - V$ curve [27].

The interface trap density ($D_{it}$) [28] and fixed charge density ($Q_f$) [29] were calculated from the C-V curves.

$$D_{it} = \frac{2.5}{q} \left[ \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 \left(C_{ox} - C_m\right)^2} \right]_{max} [eV^{-1}cm^{-2}] \quad (3)$$

Here, $C_m$ and $G_m$ are the measured capacitance and conductance at the given frequency $\omega$, respectively.

$$Q_f = \left(\Phi_{MS} - V_{FB}\right) C_{ox} [C/cm^2] \quad (4)$$

Here, $\Phi_{MS}$ is the work function difference between Al and Si.

In the first experiment, transmission electron microscopy (TEM; JEOL JEM-2200FS) was used to confirm the effect of the interfacial layer (IL) on the $SiO_2$ layer, morphology, and thickness of the $Al_2O_3/SiO_2$ films.

## III. RESULTS AND DISCUSSION

### A. [EXP. 1] EFFECTS OF FGA ON THE $Al_2O_3/SiO_2$ BILAYERS WITH DIFFERENT $SiO_2$ THICKNESSES

The thicknesses of the IL of all S1 samples were measured using TEM images, as shown in Figs. 2(a) and 2(b). In the absence of a $SiO_2$ layer, an interfacial layer was formed after FGA (see Fig. 2(a)). However, it was difficult to visually confirm the difference before and after FGA (see Fig. 2(b)), which may have occurred via the $SiO_2$ layer suppressing the formation of the IL [30]. Typically, a thin IL formed after annealing is insufficient to passivate the surface, making it difficult to estimate the side effects owing to incomplete bonding. Moreover, even with a sufficiently thick $SiO_2$ layer, as shown in Fig. 2(b), it is necessary to analyze the electrical properties to determine the passivation ability of $SiO_2$ and the effects of bonding between $Al_2O_3$ and $SiO_2$. Therefore, we electrically analyzed the effects of the presence and absence of $SiO_2$ on border traps, interface traps, and fixed charges.

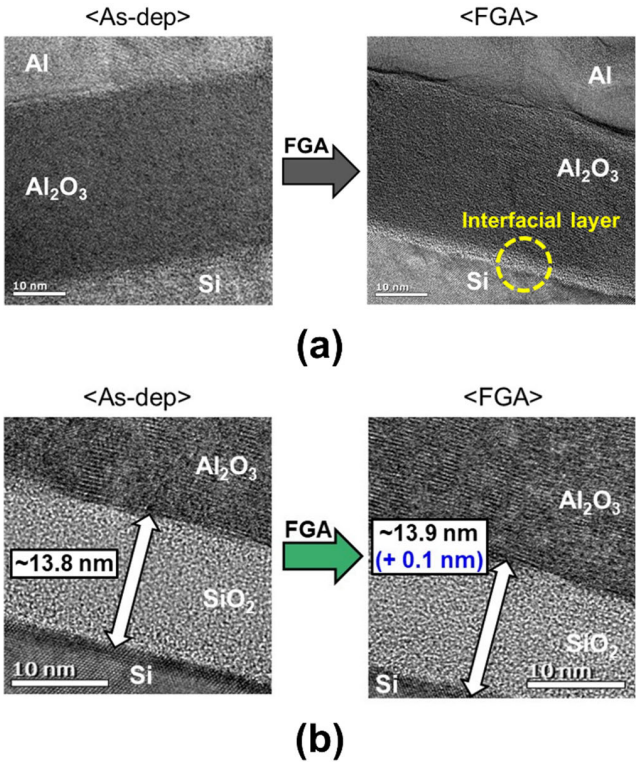


**FIGURE 2.** Cross-sectional TEM images of (a) $Al/Al_2O_3/Si$ and (b) $Al/Al_2O_3/SiO_2/Si$ structures before (left) and after (right) the FGA.

Unlike interface traps, border traps rely on a low tunneling probability to exchange charges with the Si substrate. However, they also cause leakage and noise problems; therefore, they should be minimized, such as interface traps [31], [32], [33]. The multifrequency characteristics and C-V hysteresis of the S1 samples used to estimate the number of border traps are illustrated in Fig. 3.

When comparing the C-V curves of the S1_5 nm_as_dep and S1_10 nm_as_dep samples shown in Fig. 3(a), the former showed a much larger frequency dispersion in the accumulation region than the latter. In addition, considering the frequency dispersion in the accumulation for all samples shown in Fig. 3(b), the sample with a 5 nm $SiO_2$ layer exhibited the strongest frequency dispersion. These results suggested that many traps exist at the $Al_2O_3/SiO_2$ interface, and these traps act predominantly as border traps when the traps are close to the $SiO_2/Si$ interface owing to the thin $SiO_2$ layer [31], [34], [35], [36], [37]. On the other hand, as the $SiO_2$ layer thickens, the traps at the $Al_2O_3/SiO_2$ interface move away from the $SiO_2/Si$ interface, reducing the border trap effects and decreasing the frequency dispersion. If there is no risk of unstable bonding between $Al_2O_3$ and $SiO_2$ or if such instability can be disregarded, any defects such as contamination present in the bulk of $Al_2O_3$ or $SiO_2$ can serve as border traps. In this respect, the results of weak frequency

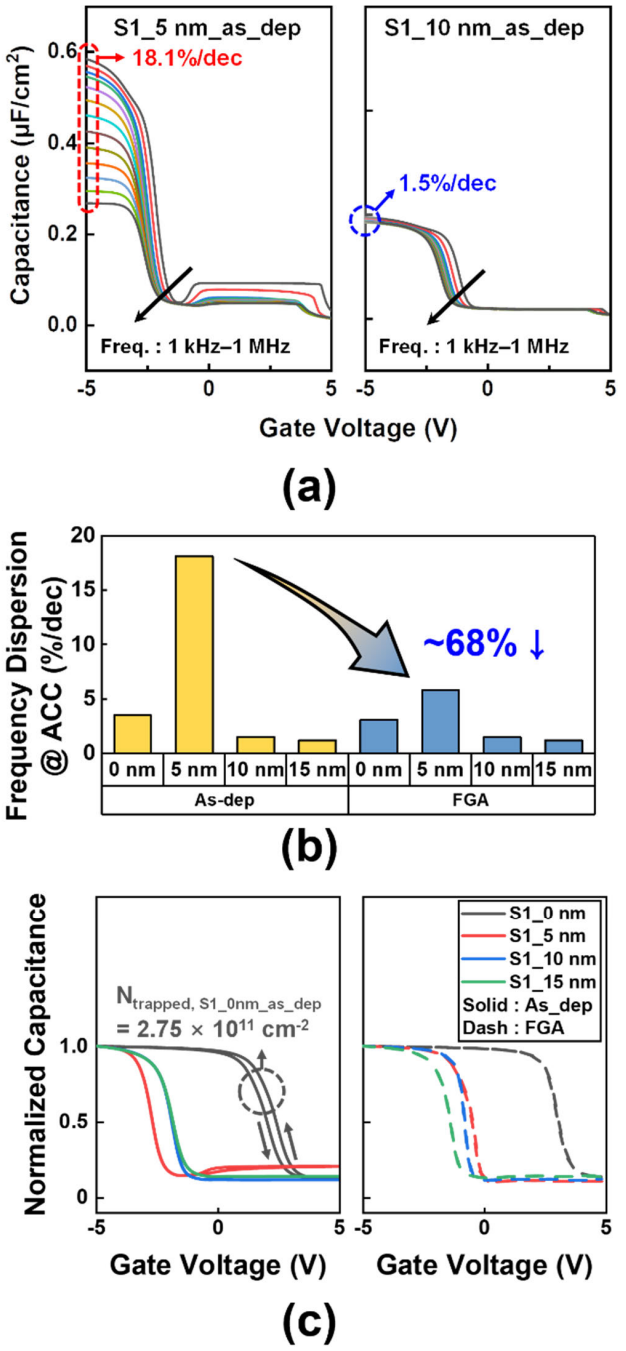


**FIGURE 3.** (a) C-V curves of the S1_5 nm_as_dep and S1_10 nm_as_dep samples measured at multiple frequencies of 1 kHz to 1 MHz, (b) frequency dispersion of the C-V curves in the accumulation region, and (c) C-V hysteresis for the as-deposited (left) and FGA-treated (right) S1 samples.

dispersion in the remaining samples, except those with a 5 nm $SiO_2$ layer, show that both PEALD and thermal oxidation processes for depositing $Al_2O_3$ and $SiO_2$, respectively, were stable in terms of border traps. Comparing the remaining samples, except those with a 5 nm $SiO_2$ layer, it can be confirmed that $SiO_2$ forms a more stable bond and has fewer bulk traps than $Al_2O_3$.

After FGA, meanwhile, the decrease in the border trap effect was significant only in S1_5 nm_FGA. These results indicate that the FGA curing effects for the $Al_2O_3/SiO_2$ interface are greater than that for the oxide bulk, or the rest of the as-deposited samples, except for S1_5 nm_as_dep, had border traps so low that FGA could no longer improve them.

In Fig. 3(c), $N_{trapped}$ of S1_0 nm_as_dep obtained from the C-V hysteresis data is $2.75 \times 10^{11}$ $cm^{-2}$, which are not confirmed in Fig. 3(b). In contrast, the as-deposited samples with the $SiO_2$ layer showed near-hysteresis-free characteristics, indicating that the border trap of the sample with the $SiO_2$ layer had a lower time constant than that of the sample without the $SiO_2$ layer [36]. The dominant criterion for determining this difference is whether the border trap is located inside a single oxide layer or at the interface between two layers. After FGA, the border trap of the sample without the $SiO_2$ layer was improved, as evidenced by the absence of C-V hysteresis.

Fig. 4(a) shows the $D_{it}$ values of the sample extracted under flat-band conditions. Considering deep depletion is a trap-dominated region [38], it is reasonable to place the gate bias of each plot within this region. Compared to the as-deposited samples, $D_{it}$ was reduced by approximately 70% owing to the presence of $SiO_2$. Furthermore, all samples significantly reduced $D_{it}$ by more than 95% after FGA. As a result, the lowest levels of $D_{it}$ of $3.98 \times 10^{11}$ and $3.85 \times 10^{11}$ $eV^{-1}cm^{-2}$ were achieved in the S1_10 nm + FGA and S1_15 nm + FGA samples, respectively. The conductance method was used for additional analysis, as shown in Fig. 4(b). Unlike in the case of the S1_5 nm_as_dep sample, the peak with $\partial(G_P/\omega)/\partial\omega = 0$ does not exist within the frequency range of measurement in the FGA-treated samples with a $SiO_2$ layer, indicating that the trapping effect of the $SiO_2$-included samples decreased to a negligible value after FGA [38]. In addition, the time constant of the trap, obtained from the $\omega$ value at the peak, was estimated to be higher for the S1_5 nm + FGA sample than for the FGA-treated samples with the $SiO_2$ layer. A high time constant is a property of border traps [37], suggesting that the relatively large number of border traps in the S1_5 nm + FGA samples affected the high $D_{it}$ value of this system.

Fig. 5 shows the number of fixed charges for each sample. Compared to the as-deposited samples, the sample with the $SiO_2$ layer had a negative $Q_f$ value owing to interstitial oxygen point defects and Al vacancies [39]. In contrast, the sample without the $SiO_2$ layer had a positive $Q_f$ value, owing to oxygen vacancies [40]. The negative shift in $Q_f$ in all samples after FGA can be interpreted as a result of reduced oxygen vacancies or dangling bonds owing to charge injection [41]. When comparing the samples containing the $SiO_2$ layer, the tendency for $Q_f$ to shift to a greater extent as the $SiO_2$ thickness decreases indicates that the curing effect at the $Al_2O_3/SiO_2$ interface far from the $SiO_2$/Si interface can be neglected.

As a result, because the $SiO_2$ layer canceled the $Q_f$ values, the fixed charge decreased in the S1_10 nm + FGA

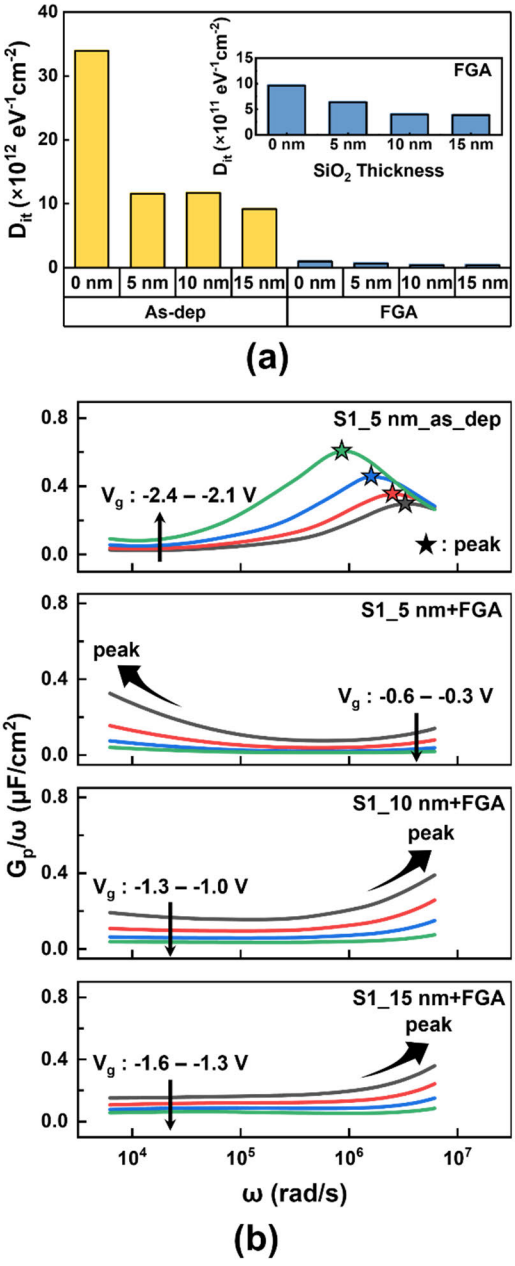


**FIGURE 4.** (a) Interface trap density ($D_{it}$) measured under flat-band conditions for the as-deposited (left) and FGA-treated (right) S1 samples. The inset graph shows a magnified view of $D_{it}$ for the FGA-treated S1 samples. (b) $G_P/\omega$ vs. $\omega$ curves of the S1_5 nm_as_dep and S1_5/10/15 nm + FGA samples. The gate bias range of each plot was set to include a deep depletion region [38].

and S1_15 nm + FGA samples with the lowest $D_{it}$ values. In contrast, the S1_0 nm + FGA sample has the largest number of fixed charges, but its relatively high $D_{it}$ value may negatively affect this system. Given these results, the tradeoff between $D_{it}$ and $Q_f$ according to the $SiO_2$ thickness should be further investigated to utilize $SiO_2$ layers, and the interfacial characteristics of the $Al_2O_3$ single layer must be improved.

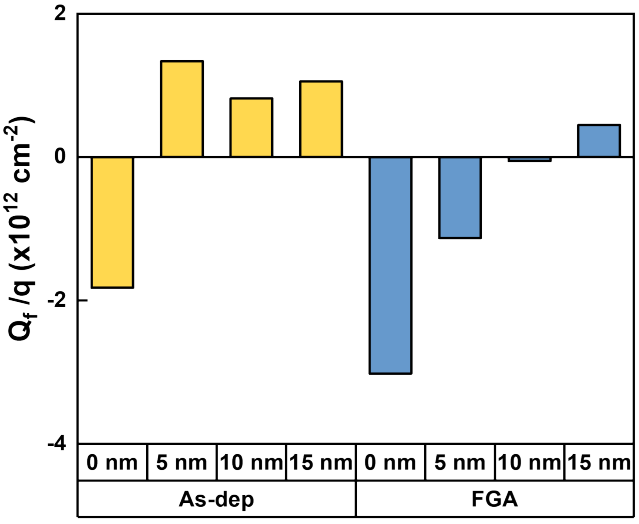


**FIGURE 5.** Fixed charge density ($Q_f/q$) for the as-deposited (left) and FGA-treated (right) S1 samples.

### B. [EXP. 2] EFFECTS OF FGA ON THE $HfO_2$ SINGLE LAYERS

When comparing the multifrequency C–V curves (Fig. 6(a)) and C-V hysteresis loops (Fig. 6(b)) of the S2_as_dep and S2 + FGA samples, the frequency dispersions in the accumulation region of each curve were 17%/dec and 14.8%/dec, respectively. The $N_{trapped}$ value of 1.68 × 10$^{12}$ cm$^{-2}$ in the as-deposited sample decreased to 9.51 × 10$^{11}$ cm$^{-2}$ (43% reduction) after FGA. As a result, the border traps improved after FGA, but more border traps remained compared to the first experiment. These results suggest the need for continued monitoring on the side effects of unmitigated border traps; if additional improvements are needed, the FGA process conditions should be changed or other treatments should be considered. Conversely, comparing the depletion region of the two multifrequency curves, FGA appears to be very effective in improving the interface traps [42].

Figs. 7(a) and 7(b) show $D_{it}$ and $Q_f$ for all samples, respectively. After FGA, $D_{it}$ decreased significantly by 96.8%; consequently, the S2 + FGA sample achieved the lowest level of $D_{it}$ throughout all experiments. In contrast, the variation in $Q_f$ was relatively large for the S2_as_dep sample, mainly owing to plasma damage. Nevertheless, as the variations were alleviated, $Q_f$ remained at a similar level and decreased after FGA, as in the first experiment following FGA. On the other hand, compared with the S1_0 nm + FGA sample, which had the most fixed charges in the first experiment, the sign of $Q_f$ was the opposite. It means that the doping types of the pixel substrates of the two samples that can be applied to the CIS are opposite [12], [13]. In other words, the S2 + FGA sample can still be effectively applied to the CIS passivation layer.

The measurement results of $D_{it}$ and $Q_f$ in all the experiments are summarized in Table 2. For the $Al_2O_3/SiO_2$ bilayer-based sample, both the $SiO_2$ layer and FGA effectively improved the interface. However, concerns remain regarding the effect of the $SiO_2$ layer on the high permittivity of the passivation layer. In addition, tradeoff characteristics

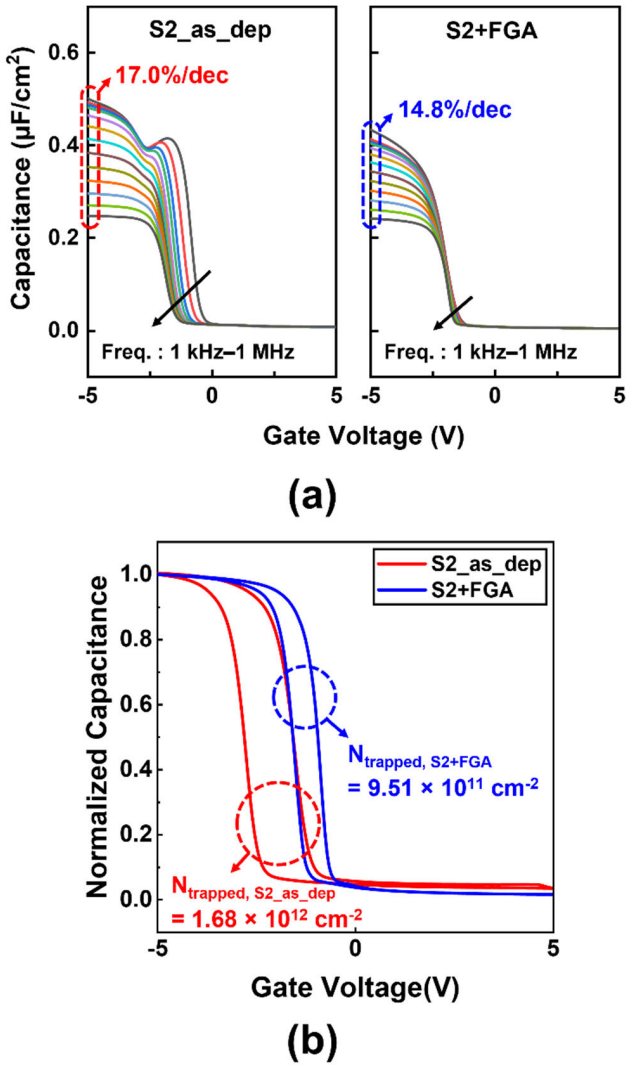


**FIGURE 6.** (a) C-V curves measured at multi-frequency of 1 kHz–1 MHz and (b) C-V hysteresis for as-deposited (left) and FGA-treated (right) S2 samples.

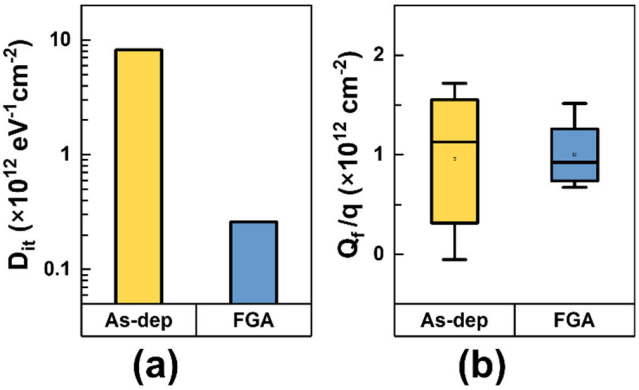


**FIGURE 7.** (a) Interface trap density ($D_{it}$) and (b) fixed charge density ($Q_f/q$) for as-deposited (left) and FGA-treated (right) S2 samples. For $Q_f/q$, sample variation was also reflected.

may arise depending on the $SiO_2$ thickness. In contrast, the $HfO_2$ single-layer-based sample was the only sample that simultaneously optimized the $D_{it}$ and $Q_f$.

**TABLE 2.** $D_{it}$ and $Q_f$ values for the FGA-treated S1 and S2 samples. The three best cases (blue) and remaining cases (red) are displayed.

| Samples | $D_{it}$ ($\times 10^{11}$ $eV^{-1}cm^{-2}$) | $\lvert Q_f/q \rvert$ ($\times 10^{12}$ $cm^{-2}$) |
|---|---|---|
| S1_0 nm+FGA | 9.63 | 3.02 |
| S1_5 nm+FGA | 6.35 | 1.13 |
| S1_10 nm+FGA | 3.98 | 0.06 |
| S1_15 nm+FGA | 3.85 | 0.45 |
| S2+FGA | 2.59 | 1.00 |

## IV. CONCLUSION

In this study, to address the inadequate enhancement of the interface quality observed in a prior study that utilized a single layer of $Al_2O_3$ for BSI CIS applications, structural modifications were implemented along with additional post-treatment methods, such as FGA. $Al_2O_3/SiO_2$ bilayer-based and $HfO_2$ single-layer-based structures were fabricated, and their electrical properties, such as the border traps, interface traps, and fixed charges, were investigated. The structure with 10- and 15-nm $SiO_2$ layers achieved the lowest levels of $D_{it}$. In addition, $D_{it}$ improved after FGA treatment in all S1 samples. However, optimization was not simultaneously achieved because of the tradeoff between $D_{it}$ and $Q_f$ according to the $SiO_2$ thickness. When using an $HfO_2$ single layer, FGA was less effective in improving the border traps than for the first investigated structure; therefore, the effects of the traps on the leakage current and noise should be considered for these CIS systems. Nevertheless, FGA improved the $D_{it}$, $Q_f$, and border trap characteristics of all samples without side effects. In particular, the plasma-induced damage in PEALD was alleviated by FGA, reducing the variation in the fixed charge. As a result, the FGA-treated $HfO_2$ sample exhibited a $D_{it}$ value of $2.59 \times 10^{11}$ $eV^{-1}cm^{-2}$ and $|Q_f/q|$ value of $1.00 \times 10^{12}$ $cm^{-2}$. To summarize our findings, the structure that yielded the best results in our experiments can be universally implemented to enhance performance while addressing defect-induced variation that may occur in various processes.

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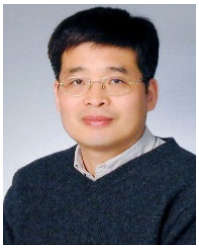

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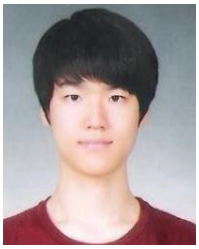

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