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RESEARCH ARTICLE

Strained Si Nanosheet pFET Based on SiC Strain Relaxed Buffer Layer for High Performance and Low Power Logic Applications

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ABSTRACT The application of SiC-based strain-relaxed buffers (SRB) technology in gate-all-around (GAA) pMOS nanosheet transistors (NS-FETs) fabrication has been systematically investigated. TCAD simulation results show that SiC SRB can effectively enhance the p-channel stress, up to 3.8Gpa has been achieved without S/D parasitic RC degradation. Furthermore, introducing a wide-bandgap SiC layer underneath NS-FET can help suppress the bottom parasitic transistor. The SiC SRB technology presents a integrated and streamlined approach for addressing the major performance bottlenecks of NS-FETs and is a potential solution for developing future NS-FET based high-performance and low-power logic applications.

INDEX TERMS Gate-all-around (GAA), nanosheet (NS-FET), S/D stressor, stress enhancement, strain relaxed buffer.

I. INTRODUCTION

With the continuous scaling of CMOS technology, the gate length of transistors is approaching sub-15nm region for the 3nm node and beyond. At this size, even FinFET technology struggles to provide adequate gate control to minimize short-channel effects [1]. In order to meet the ever increasing demand of modern high-performance and low-power SoCs, stacked nanosheet GAA FETs (NS-FETs) have emerged as the most promising alternative to replace FinFETs, owing to their superior electrostatics control and relatively smooth transition from existing FinFET technologies [2]. Being a revolutionary device structure, NS-FET inevitably introduces its unique challenges. First, the primary surface orientation for NS-FET has switched to (100), which leads to decreased hole mobility when compared to FinFET counterparts. To compensate for the performance degradation of pFET, much higher stress needs to be introduced to the channel using SiGe source/drain (S/D) stressors. However, the epitaxial quality of these stressors is already challenged by the discontinuous initial interface. Second, the area efficiency of NS-FET is often considered advantageous since it can theoretically be improved by adding more stacked nanosheets. In practice, the benefit is severely limited by bulky S/D stressors, as the low-lying nanosheets are hampered by high access resistance [3]. Third, there is a parasitic fin transistor at the bottom of the NS-FET structure which, if left untreated, becomes a significant leakage path and increases parasitic RC [4]. A lot of work has been carried out to address these shortcomings to bring NS-FETs into mass production. While potential process solutions, such as bottom dielectric isolation (BDI), have been proposed [5]. Implementing a separate solution for each challenge increases the complexity of process integration and manufacturing cost. Therefore, a more integrated solution is preferred.

Stress can also be introduced through the epitaxial growth of Si channels on a strain-relaxed buffer (SRB) virtual substrate. Unlike other common stress techniques utilized in

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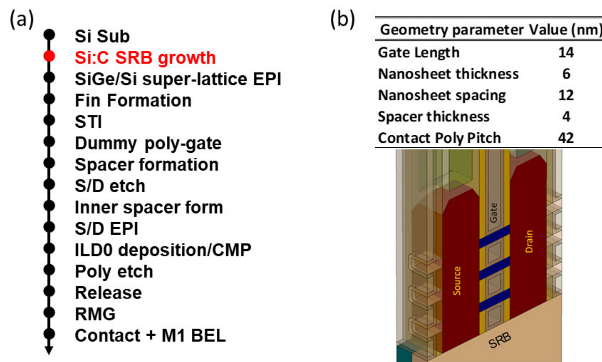

FIGURE 1. (a)Detailed integration flow of proposed SiC SRB-based NS-FET. (b)Target device parameters and simulated device structure.

CMOS technologies, the stress introduced by SRB does not decrease as transistor size shrinks [6]. The lattice spacing of substitutional carbon based SRB (SiC) is smaller than that of silicon. Therefore, using an epitaxially grown SiC layer as a SRB offers an alternative approach to introduce highly desirable compressive stress in the nanosheet pFET. In addition, the use of a SiC layer as an SRB can provide an additional isolation benefit due to the larger band offset of SiC [7]. Although SiC SRB has been proposed for FinFET applications, the effect of the SiC SRB on NS-FETs has not been systematically investigated [8].

In this work, the effect of SiC SRB layers as a virtual substrate for NS-FET application has been systematically investigated using TCAD simulations. The proposed integration scheme utilizes a strain buffer layer to alleviate the conflicting needs between high-stress and bottom sheet access resistance. In addition, the carbon element in the parasitic fin structure can suppress parasitic transistor leakage by reducing the junction depth and introducing a larger barrier for isolation.

II. SiC SRB FOR NS-FET INTEGRATION

A. INTEGRATION FLOW

Channel stress engineering through SRB is typically achieved by epitaxial growth of the channel material directly over the SRB virtual substrate. The fabrication of the SRB virtual substrate can be done directly on the Si substrate or by replacing the existing fin after the STI [6], [9]. Implanting SRB into NS-FETs is more complicated as the stacking Si nanosheet channels are not in direct contact with the substrate. With the replacement fin scheme, the epitaxial quality of the superlattice structure is a concern, therefore, it is preferred that SRB epitaxy is grown directly on the Si substrate. The proposed SRB NS-FET flow is illustrated in Figure 1(a), where a fully relaxed SiC layer was epitaxially grown on the Si substrate. The upper limit of carbon concentration in SRB is set to 4% to take into consideration the capability of current fabrication techniques [10]. After SRB formation step, NS-FET was fabricated following the generic NS-FETs process steps reported by previous works [2], [11].

B. SIMULATION METHODOLOGY

Sentaurus Process was selected to perform the 3D process simulation using the aforementioned integration flow. Figure 1(b) shows the geometry parameter and schematic view of the final structure of a three-layer Si GAA NS-FET with SiC SRB generated by process simulation. The target structure dimension was based on the ITRS road map for the 3nm node. The gate length of 14 nm, NS width of 33 nm, NS thickness of 6 nm, and gate pitch of 42 nm was assumed. To accurately simulate the epitaxial growth process on complex 3D structures, Lattice Kinetic Monte Carlo (LKMC) model was employed in key epitaxial steps, including SRB layer growth, SiGe/Si multi-layer growth, and the $Si_{0.6}Ge_{0.4}$ S/D stressor growth(pFETs). Stress equilibrium calculations were also performed after each step for the accurate evaluation of stress relaxation effects.

After process simulation, Sentaurus Device was used for device performance evaluation. The accuracy of the TCAD simulation depends on the appropriate physical model selection and physical parameters calibration. In this study, the drift-diffusion transport (DD) model was used in combination with the Poisson equation and quantum correction models to perform self-consistent computation. The selection of mobility model in DD module includes low-field ballistic mobility, auto-orientation inversion and accumulation layer mobility (IALMob), and high field saturation velocity. The recombination effect was accounted for by utilizing the Dynamic Nonlocal Path Band-to-Band (BTBT), Shockley-Read-Hall (SRH), and Anger recombination models. The strain impact on devices was calculated using the multi-valley electron and hole mobility model that considers the mass anisotropy and valley/band energy change with orientation and stress. A variety of physical parameters, such as doping profile, ballistic coefficient, and surface roughness scattering factor, were carefully calibrated to match reported NS-FET experimental results [2].

III. RESULTS AND DISCUSSION

A. STRESS ENHANCEMENT PRINCIPLE

In NS-FETs, Si nanosheet channels are formed by selectively removing the SiGe sacrificial layers from epitaxially grown SiGe/Si multi-layer heterostructure. As the thickness of each layer is within the range of a few nanometers, less than the corresponding critical thickness, the lattice spacing of both Si channel layers and SiGe sacrificial layers matches that of the substrate, resulting in a strained multi-layer heterostructure [12]. Figure 2(a) shows the initial longitudinal stress (S_{ZZ}) distribution of the resulting multi-layer heterostructure. When a silicon substrate was used, there is no stress in the Si channel layer due to the same lattice parameters, and only the SiGe sacrificial layer is compressed. However, if the SiGe/Si superlattice was epitaxially grown on a fully relaxed SiC SRB, both Si and SiGe layers are now compressed as they conform to the smaller lattice spacing of the underlying SiC alloy. The stress of the top three Si layers has reached 2GPa with a 3% SiC SRB.

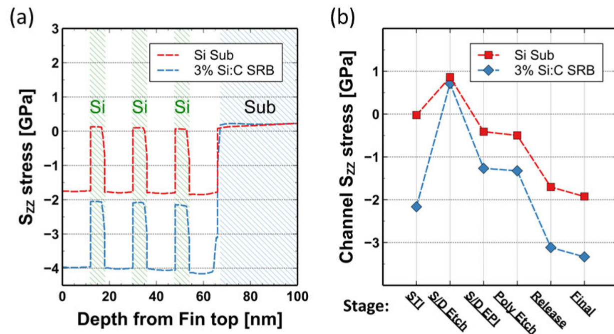

FIGURE 2. **(a)Longitudinal Stress distribution of superlattice cross-section, Si layer is pre-stressed to 2GPa with 3% SiC Sub (b)The average channel stress evolution between process stages, the initial stress obtained from SiC SRB was lost after S/D etch but regained after S/D SiGe EPI.**

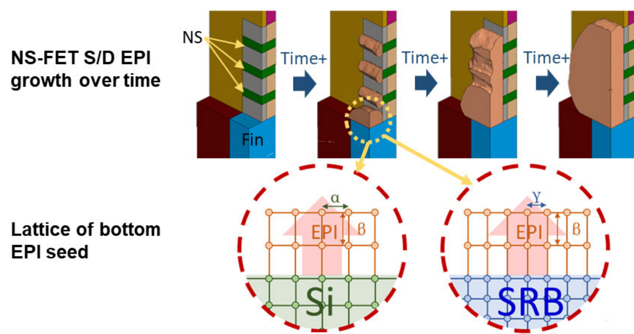

FIGURE 3. **During S/D SiGe epitaxy process, the bottom seed surface grown out of the SiC SRB layer has a smaller lattice spacing than one on the Si sub, thus providing a stress boost to the nanosheet channels.**

Figure 2(b) shows stage-to-stage channel stress evolution extracted during NS-FET fabrication, both with and without SiC SRB. It can be observed that both conditions exhibit tensile stress after the S/D trench etch process due to the fragmentation of the fin structure and the emergence of the free surface. At this point, the nanosheets and sacrificial layers can extend elastically along the channel direction. Due to the short gate length of NS-FET, the majority of the residual stress introduced by the SRB is lost, which shows good agreement with X-ray nano diffraction measurement results reported in literature [13].

However, after the subsequent S/D SiGe EPI step, the SRB condition was 0.35GPa higher than the baseline. The stress difference between the two conditions widened after the channel release and was maintained throughout the rest of the processes. resulting in a significant increase of 1.41 GPa. A closer examination of the S/D SiGe EPI step reveals a considerable difference between the two conditions. Epitaxial growth of S/D on NS-FET is known for its challenge of discrete initial seed surface. The situation is even more complex in structures with the SRB layer, as there are two different materials for SiGe epitaxy seed: the silicon in the nanosheet channels and the SiC in the parasitic Fin. The SiC SRB has a smaller lattice spacing (γ) than the Si layer (α), and the epitaxy of the SiGe material on top of the SiC

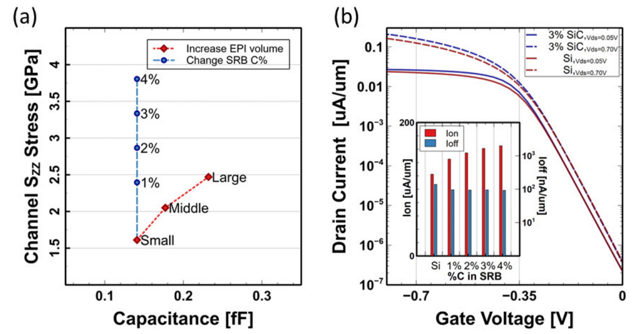

FIGURE 4. **(a)Stress-capacitance comparison between SiC SRB carbon concentration modulation method and conventional S/D SiGe EPI volume enlarging method.(b)Comparison of IdVg curve with Si Sub SiC SRB. The effect of SiC SRB carbon concentration on Ion/Ioff is summarized in the insert.**

results in a larger lattice mismatch and higher compressive stress, as shown in Figure 3. When the highly stressed bottom seed begins to merge with the seed grown out of the nanosheets during epitaxial growth, the extrusion from the highly stressed bottom seed is transmitted through the less stressed channel seed, increasing the stress in nanosheets.

B. PERFORMANCE BOOSTER WITHOUT RC PENALTIES

One advantage of SRB technology is that the stress effect can be modified by adjusting the composition of the SRB layer. Simulations were performed for different SRB carbon doping concentrations using a fixed S/D SiGe EPI condition. The effect of S/D stressor volume on stress was also simulated on conventional Si substrates for comparison. The results are plotted in Figure 4(a), which shows the extracted final channel stresses versus the total device capacitance. The data indicate that increasing carbon concentration is an effective method for boosting final stress. Up to 3.8GPa final stress is achieved when 4% SiC SRB is combined with "Small" sized S/D SiGe EPI while maintaining the total capacitance. In contrast, with conventional Si substrates, the stress-boosting method of enlarging S/D SiGe EPI stressor volume ("Middle" and "Large") comes with a heavy capacitance penalty. With enhanced channel stresses, the overall device performance gain of SiC SRB technology is present in Figure 4(b). Compared to conventional Si substrates, SiC SRB offers up to 35% increase in transistor driving current while maintaining nearly the same Ioff level. Such electrical benefits are similar to those of the previous FinFET study [8]. This suggests that SiC SRB technology can be effectively adapted to NS-FETs, despite the structural differences between the two device architectures.

C. PARASITIC CHANNEL LEAKAGE CONTROL

In FinFET technology, a Punch-through stop (PTS) layer is typically introduced at the bottom of the fin structure through angled implantation to suppress the parasitic transistor. However, its effectiveness in NS-FET has yet to be established, as the shadowing effect of the NS-FET structure is expected to be much worse than that of the FinFET structure [14]. In this

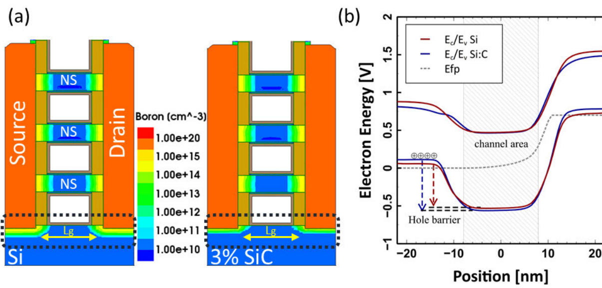

FIGURE 5. (a) Comparing the boron distribution in the bottom parasitic transistor (highlighted), the boron diffusion into the parasitic fin structure is significantly reduced when using SiC SRB. (b) Comparison of band alignment of parasitic FinFET transistor at off-state with (blue) and without (Red) SiC SRB. The valence band offset in SiC SRB is larger than Si, resulting higher hole barrier.

regard, the incorporation of SiC SRBs brings two additional benefits. Firstly, The addition of carbon to silicon is known to reduce transient diffusion (TED) [15]. Consequently, there is less boron diffusing out of the source-drain region into the underlying parasitic fin structure, as shown in Figure 5(a). The shorter S/D extension leads to an increase in the equivalent gate length of the parasitic FinFET transistor, resulting in better gate control during off-state. Secondly, by replacing Si with SiC alloy in the parasitic fin structure, the valence band offset in the parasitic FinFET transistor is broadened, as shown in Figure 5(b) [16]. This further suppresses the tunneling effect and reduces leakage. While some of the leakage benefits gained from the parasitic channel are offset by increased leakage in the NS channel due to excessive bandgap narrowing caused by high NS channel stress, the overall leakage control is much better than that of Si-based devices, as shown by the electrical results [8].

IV. CONCLUSION

By implementing a SiC strain-relaxed Buffer into nanosheet pFET fabrication, the stress effect of SiGe S/D stressors can be significantly enhanced. Up to 3.8Gpa channel stress can be achieved without increasing S/D epitaxy volume. Moreover, SiC SRB brings additional benefits in terms of bottom parasitic channel control and enables a new flexible method of channel stress adjustment without parasitic RC penalties, which may be a crucial performance enhancer for future NS-FETs.

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