RESEARCH ARTICLE

A Control Stage for Parallel-Connected Interlinking Converters in Hybrid AC–DC Microgrids

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ABSTRACT Having two or more interlinking converters connected in parallel in hybrid microgrids has some benefits, like modularity, flexibility, and redundancy. However, the parallelization of the inverters leads to circulating currents that can cause system malfunctions. This work uses a method for suppressing low-frequency circulating currents in interlinking converters by controlling the zero-sequence component of the phase currents, showing that the control structure is valid for interlinking converters. The proposed control scheme has been applied to two parallel interlinking inverters of 5 kW and 2.5 kW, respectively. The interlinking inverters are connected to the grid, and they control the voltage in the DC bus of the hybrid microgrid. To validate the concept, simulation and experimental results are shown.

INDEX TERMS Circulating currents, hybrid microgrid, interlinking converters, parallel inverters.

I. INTRODUCTION

In the coming years, the electrical grid will evolve from the current highly centralized model to a more distributed one with many microgrids. A microgrid is a local grid composed of distributed generators (DGs), energy storage systems, and dispersed loads that may operate in both grid-connected and islanded modes [1]. The micro-grid concept allows energy generation and consumption points to be close to each other, decreasing distribution losses. Microgrids have other benefits, such as improving local reliability, compensating for voltage sags, or working as uninterruptible power supplies [2].

A. MICROGRID TOPOLOGIES

Microgrids can be divided into three main groups: AC, DC, and hybrid microgrids. AC microgrids are the most widely used since they allow the integration of distributed generators

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into the current power grid with minimal modifications, the voltage levels can be modified by means of low-frequency transformers, and protection circuits are extensively developed for AC systems [3], [4]. However, it is necessary to synchronize the generation systems, and the circulation of reactive power increases transmission losses. Regarding DC microgrids, they are interesting due to the increase in DC loads, such as LED luminaires, the growing fleet of electric vehicles, DC renewable energy generators, and energy storage systems [5]. Among its advantages, it may be highlighted that there is no reactive power in the system, and synchronization systems are not needed. In addition, rectification stages to connect DC loads can be avoided, being necessary only for small DC-DC converters. However, this configuration requires an intensive modification of the distribution grid, which increases costs drastically, and the design of appropriate protections for these systems is a challenge [6]. As an alternative, hybrid microgrids combine the advantages of AC and DC architectures. In this kind of microgrid, DC and AC buses are connected to the same distribution grid, facilitating

the integration of distributed generation systems, storage systems, and both DC and AC loads, avoiding unnecessary conversion processes [7], [8].

Fig. 1 shows several topologies of microgrids: radial, ring, and meshed. In a radial configuration, power is distributed from the grid connection point to the loads located along the branch lines. This is a simple, cheap, and easy-to-implement configuration in which the control and protection functions are located at the grid connection point. However, as a drawback, if one of the lines is disconnected for any reason, all downstream lines will lose their power supply [9]. Besides, they are not very flexible since new loads require new wiring to be installed unless the system is initially oversized. In a ring configuration, all nodes are interconnected in such a way that they form a closed geometric loop in which power can be distributed in either direction to any point of the microgrid [10]. This configuration offers higher performance and reliability than a radial system. In case of breakdown or maintenance, the different parts of the system can be properly isolated, ensuring that most of the loads continue to receive power. A ring system is somewhat more difficult to implement than a radial system, and the cost of these systems may be a major drawback [11]. The meshed configuration is similar to a ring connection but also includes redundant lines that allow the power flow to be rerouted in case of a mainline failure. Compared to the radial and ring configurations, the meshed structure is the most difficult to implement since it includes many interconnection alternatives among nodes, increasing complexity.
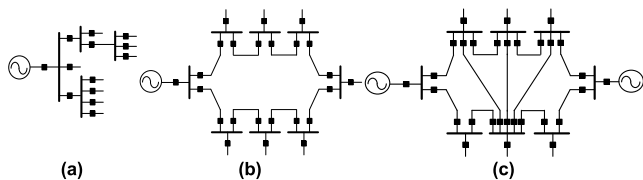

FIGURE 1. Microgrid topologies: (a) radial, (b) ring, (c) meshed.

B. GRID-FEEDING, GRID-FORMING, AND GRID-SUPPORTING INVERTERS

In a decentralized system, inverters can perform multiple roles. Based on their operating principle, the inverters can be classified as grid-feeding, grid-supporting, and grid-forming [12]. An inverter working as grid-feeding is a current source that injects active power into a stable grid [13]. These converters cannot regulate the amplitude and frequency of the grid voltages, and they are limited to supplying the available power to the main grid or the connected loads in the case of isolated operation. These converters use synchronization algorithms for the current injection to the grid. Grid-supporting power converters act as synchronous generators that regulate voltage and frequency according to the delivered active and reactive power. The usual control schemes are based on droop control techniques that allow the operation of a grid-supporting converter with grid-forming or

other grid-supporting inverters [14]. The usual application of grid-supporting converters is in weak grid connections and isolated systems. Grid-forming power converters act practically as ideal voltage sources that establish the voltage and frequency of a grid or microgrid. They are typically used in isolated systems and require droop control techniques to adequately distribute the active and reactive power in the parallel operation of several grid-forming converters. The methods proposed in this work focus on grid-feeding inverters, without prejudice that their application can be extrapolated to grid-supporting and grid-forming inverters.

C. MICROGRID CONFIGURATION UNDER STUDY

Due to increased environmental awareness or even the lower cost of self-production of energy, it is becoming increasingly common to have renewable energy generation available locally, such as photovoltaic generation systems. In locations such as office buildings, industrial parks, or even residential neighborhoods with self-production of energy, hybrid microgrids are considered interesting since they allow significant energy savings by managing both AC and DC loads and sources in independent buses. Hybrid microgrids suppress the double conversion from DC to AC and AC to DC, thus avoiding the associated energy losses that occur in a conventional grid [7]. The power deficits or surpluses of the DC and AC buses can be managed through so-called interlinking converters.

Fig. 2 shows the schematic of a hybrid microgrid in a ring configuration. The microgrid is composed of an AC bus (in red) to which AC generation and consumption systems are connected. This AC bus is connected to the distribution grid through the point of common coupling (PCC). The microgrid also has a DC bus (in blue) interconnected with the AC bus through interlinking converters (IC). DC generators and loads are connected to the DC bus.
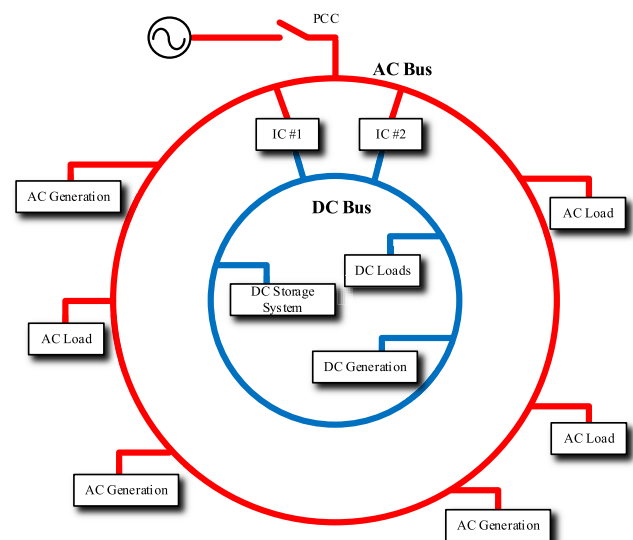

FIGURE 2. Hybrid microgrid based on ring topology with AC and DC buses connected through interlinking converters (IC).

A ring microgrid offers robustness, allowing power to flow in both directions. Besides, suppose the interlinking converters are connected in parallel. In that case, a modular system is obtained, in which additional inverters can be added if the rated power to be transmitted between the AC and DC buses is increased. The additional inverters can be rated at the same power, but in general, the power of inverters could be different to avoid unnecessary costs. Parallelization of the inverters also provides a redundant system since, in the event of failure of one of the inverters, the power flow between the AC and DC buses is maintained. In addition, parallel connection of converters has several advantages, such as low current ripple, modularity, better thermal management, higher power capacity, redundancy, and easy maintenance [15]. However, circulating currents appear when converters operate in parallel, which can produce undesirable effects on the whole system or even damage inverters [16].

Some works studied methods to reduce circulating currents in the past. Reference [17] studies the high-frequency circulation currents and proposed a method for compensating the carrier signals' phase errors with regard to the magnitude of the zero-sequence circulating currents. In the present work phase errors are avoided by synchronizing the switches of the IGBTs, so it is not needed an algorithm that uses additional computational resources. Reference [18] proposes a method for reducing circulating currents based on the virtual impedance concept. This technique is interesting when the parallel inverters are placed over a long distance without communication among units. However, the reduction of the circulating current is not as good as that obtained with the technique proposed in [19], where there is a short distance and communication among inverters. In reference [19], the authors propose the reduction of the low-frequency circulating currents by controlling the homopolar component of the phase currents.

The circulating currents that appear in interlinking converters connected in parallel in a hybrid microgrid have been studied in this work. With regard to reference [19], the main contributions of this paper are: i) the proposed method for avoiding low-frequency circulating currents is applied to the specific case of interlinking converters, ii) the interlinking converters work as grid-feeding and the DC voltage is controlled, whereas an ideal DC voltage was considered in [19], and iii) the high-frequency components are also reduced by synchronizing the switching control signals between the inverters.

The laboratory setup was initially composed of a 5 kW three-phase inverter, whose power has been increased by 50% by connecting a 2.5 kW inverter in parallel. Experimental and simulation results have been obtained in an easily manageable power range in the laboratory, demonstrating that circulating currents in hybrid microgrids can be avoided using the proposed techniques without affecting the performance of the DC voltage control loop.

II. MODEL OF THE SYSTEM

Fig. 3 represents the single-line diagram of the two interlinking inverters connected in parallel. Inverter #1 has a nominal power of 5 kW, and the nominal power of inverter #2 is 2.5 kW. The grid filter of both converters consists of LCL filters with inductances L_{f1} and L_{f2} of different values, capacitors C_{f1} and C_{f2} with damping resistors R_{d1} and R_{d2}, and a three-phase inductance L_g common to both converters. The coupling term M_g of the three-phase inductor L_g has been considered in this model. The inductor resistances have been represented by r_{f1}, r_{f2}, and r_g. The LCL filter has been designed considering the procedure described in [20].

As the microgrid works in grid connection mode, the amplitude and frequency of the voltage on the AC bus are set by the grid to 230 V phase-phase and 50 Hz, while the voltage on the DC bus will be regulated by the interlinking converter over the entire operating range of 400 V- 600 V.
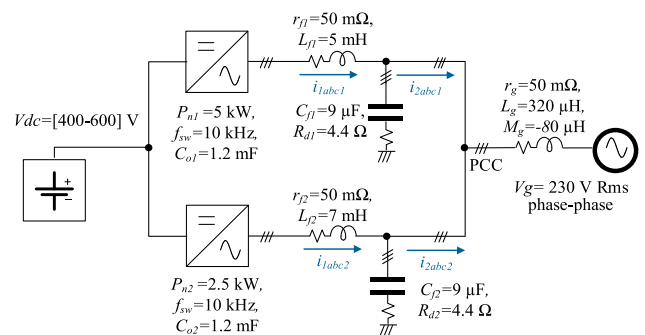
FIGURE 3. One-line diagram of the parallel ICs of the hybrid microgrid.

A. SMALL SIGNAL MODEL EQUATIONS

The interlinking converters have been modeled on a synchronous reference frame (SRF), being the grid voltage aligned with the d-axis. With this method, the active power managed by the ICs is controlled with a d-axis current control loop, and the reactive power can be controlled with the q-axis component. As proposed in [19], the o- component is used to suppress the circulating currents since the homopolar component of the phase currents agrees with the circulating currents.

The SRF small signal model is expressed in (1)-(23). The model has been obtained following the procedure described in [19], but particularized for a system composed of two parallel inverters. The state X and the output Y vectors are defined in (3). The input vector U contains the control variables and the disturbances, which are the duty cycle applied to the switches of each branch of the inverters and the grid voltage. The matrices A, B, C, and D of the small signal model are expressed in (5)-(8), being (9)-(23) submatrices that simplify A, B, C, D. In the following equations i_{1di}, i_{1qi}, i_{2di}, i_{2qi}, and i_{o1} are the currents in both sides of the LCL filter in the SRF, being $i = 1,2$ each one of inverters #1 and #2. Variables v_{cd1}, v_{cq1}, v_{cd2}, and v_{cq2} define the voltage

$$\frac{d}{dt}X = A \cdot X + B \cdot U \tag{1}$$

$$Y = C \cdot X + D \cdot U \tag{2}$$

$$X = Y = \begin{bmatrix} \hat{i}_{1d1} & \hat{i}_{1q1} & \hat{i}_{2d1} & \hat{i}_{2q1} & \hat{i}_{o1} & \hat{v}_{cd1} & \hat{v}_{cq1} & \hat{i}_{1d2} & \hat{i}_{1q2} & \hat{i}_{2d2} & \hat{i}_{2q2} & \hat{v}_{cd2} & \hat{v}_{cq2} & \hat{v}_{dc} \end{bmatrix}^T \tag{3}$$

$$U = \begin{bmatrix} \hat{d}_{d1} & \hat{d}_{q1} & \hat{d}_{o1} & \hat{d}_{d2} & \hat{d}_{q2} & \hat{v}_{gd} & \hat{v}_{gq} & \hat{v}_{go} \end{bmatrix}^T \tag{4}$$

$$A = \begin{bmatrix} A_{\hat{i}12dq\_i12dq} & 0 & A_{\hat{i}12dq\_vcdq} & 0 & 0 & A_{\hat{i}12dq\_vdc} \\ 0 & A_{\hat{i}o\_io} & 0 & 0 & 0 & A_{\hat{i}o\_vdc} \\ A_{\hat{v}cdq\_i12dq} & 0 & A_{\hat{v}cdq\_vcdq} & 0 & 0 & 0 \\ 0 & 0 & 0 & A_{\hat{i}12dq\_i12dq} & A_{\hat{i}12dq\_vcdq} & A_{\hat{i}12dq\_vdc} \\ 0 & 0 & 0 & A_{\hat{v}cdq\_i12dq} & A_{\hat{v}cdq\_vcdq} & 0 \\ A_{\hat{v}dc\_i12dq} & A_{\hat{v}dc\_io} & 0 & A_{\hat{v}dc\_i12dq} & 0 & A_{\hat{v}dc\_vdc} \end{bmatrix} \tag{5}$$

$$B = \begin{bmatrix} B_{\hat{i}12dq\_ddq} & 0 & 0 & 0 \\ 0 & B_{\hat{i}o\_do1} & 0 & 0 \\ 0 & 0 & B_{\hat{i}12dq\_ddq} & B_{\hat{i}12dq\_vgdqo} \\ 0 & 0 & 0 & 0 \\ B_{\hat{v}dc\_ddq} & B_{\hat{v}dc\_do} & B_{\hat{v}dc\_ddq} & 0 \end{bmatrix} \tag{6}$$

$$C = I \tag{7}$$

$$D = 0 \tag{8}$$

$$A_{\hat{i}12dq\_i12dq} = \begin{bmatrix} \dfrac{-(R_{di} + r_{fi})}{L_{fi}} & \omega & \dfrac{R_{di}}{L_{fi}} & 0 \\[2ex] -\omega & \dfrac{-(R_{di} + r_{fi})}{L_{fi}} & 0 & \dfrac{R_{di}}{L_{fi}} \\[2ex] \dfrac{R_{di}}{\frac{c_1+c_2}{c_i}(L_g - M_g)} & 0 & \dfrac{\left(R_{di} + \frac{c_1+c_2}{c_i} r_g\right)}{\frac{c_1+c_2}{c_i}(L_g - M_g)} & \omega \\[2ex] 0 & \dfrac{R_{di}}{\frac{c_1+c_2}{c_i}(L_g - M_g)} & -\omega & \dfrac{-\left(R_{di} + \frac{c_1+c_2}{c_i} r_g\right)}{\frac{c_1+c_2}{c_i}(L_g - M_g)} \end{bmatrix}, \quad i = 1, 2 \tag{9}$$

$$A_{\hat{i}o\_io} = -\frac{r_{fi}}{L_{f1} + L_{f2}} \tag{10}$$

$$A_{\hat{i}12dq\_vcdq} = \begin{bmatrix} -\dfrac{1}{L_{fi}} & 0 \\[2ex] 0 & -\dfrac{1}{L_{fi}} \\[2ex] \dfrac{1}{\frac{c_1+c_2}{c_i}(L_g - M_g)} & 0 \\[2ex] 0 & \dfrac{1}{\frac{c_1+c_2}{c_i}(L_g - M_g)} \end{bmatrix}, \quad i = 1, 2 \tag{11}$$

$$A_{\hat{i}12dq\_vdc} = \begin{bmatrix} \dfrac{Fm \cdot Ddi}{L_{fi}} \\[2ex] \dfrac{Fm \cdot Dqi}{L_{fi}} \\[2ex] 0 \\ 0 \end{bmatrix}, \quad i = 1, 2 \tag{12}$$

$$A_{\hat{i}o\_vdc} = \frac{Fm \cdot D_{o1}}{L_{f1} + L_{f2}} \tag{13}$$

in the filter capacitors. The grid voltage in the synchronous reference frame is expressed as V_{gd}, V_{gq}, and V_{go}. The transistors (IGBT) duty cycles have been defined as d_{d1}, d_{q1}, d_{o1}, d_{d2}, and d_{q2}. Fm is the modulator gain, and c_i stands for the load factor of inverters #1 and #2, while I_{dc} is the DC current of the inverter. Equations (1)–(13), as shown at the previous page and (14)–(23), as shown at the bottom of the page. TABLE 1 summarizes the equations of the variables at the operating point. These expressions have been obtained considering the control objectives: the load sharing between both inverters, null reactive power, and the suppression of circulating currents. The operating point has been calculated neglecting the filter capacitors, so currents on both sides of the filter capacitors are considered the same.

TABLE 1. Variables in the operating point.

Variable	Expression
V_{gd}	V_{gRMS} (phase-phase)
V_{gq}	0
V_{go}	0
I_{di}	$\dfrac{I_{dc\_nom}}{2Fm \cdot D_{di}} c_i, i = 1,2$
I_{qi}	0
I_{oi}	0
D_{di}	$\dfrac{V_{gd}}{Fm \cdot V_{dc}}$
D_{qi}	$\dfrac{\omega I_{di}\left(L_{fi} + \dfrac{c_1 + c_2}{c_i}(L_g - M_g)\right)}{Fm \cdot Vdc}, i = 1,2$
D_{ol}	0

III. CONTROL SCHEME

Fig. 4 shows the proposed control structure. Both inverters have a current control loop on the d- axis, which regulates the active power, and another on the q- axis, which regulates the reactive power. As the inverters have been modeled in the SRF, coupling terms between the d- and q- currents of the inverters appear. The decoupling terms expressed in (24)-(25) have been employed to eliminate the effect of these

$$A_{\hat{v}cdq\_i12dq} = \begin{bmatrix} \dfrac{1}{C_{fi}} & 0 & -\dfrac{1}{C_{fi}} & 0 \\ 0 & \dfrac{1}{C_{fi}} & 0 & -\dfrac{1}{C_{fi}} \end{bmatrix}, \quad i = 1, 2 \tag{14}$$

$$A_{\hat{v}cdq\_vcdq} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \tag{15}$$

$$A_{\hat{v}dc\_i12dq} = \begin{bmatrix} -\dfrac{Fm \cdot D_{di}}{C_{o1} + C_{o2}} & -\dfrac{Fm \cdot D_{qi}}{C_{o1} + C_{o2}} & 0 & 0 \end{bmatrix}, \quad i = 1, 2 \tag{16}$$

$$A_{\hat{v}dc\_io} = -\dfrac{Fm \cdot D_{o1}}{C_{o1} + C_{o2}} \tag{17}$$

$$A_{\hat{v}dc\_vdc} = -\dfrac{-\dfrac{Idc}{Vdc}}{C_{o1} + C_{o2}} \tag{18}$$

$$B_{\hat{i}12dq\_ddq} = \begin{bmatrix} \dfrac{Fm \cdot Vdc}{L_{fi}} & 0 \\ 0 & \dfrac{Fm \cdot Vdc}{L_{fi}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad i = 1, 2 \tag{19}$$

$$B_{\hat{i}o\_do1} = \dfrac{Fm \cdot Vdc}{L_{f1} + L_{f2}} \tag{20}$$

$$B_{\hat{i}12dq\_vgdqo} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \dfrac{-1}{\frac{c_1+c_2}{c_i}(L_g - M_g)} & 0 & 0 \\ 0 & \dfrac{-1}{\frac{c_1+c_2}{c_i}(L_g - M_g)} & 0 \end{bmatrix}, \quad i = 1, 2 \tag{21}$$

$$B_{\hat{v}dc\_ddq} = \begin{bmatrix} -\dfrac{Fm \cdot I_{di}}{C_{o1} + C_{o2}} & -\dfrac{Fm \cdot I_{qi}}{C_{o1} + C_{o2}} \end{bmatrix}, \quad i = 1, 2 \tag{22}$$

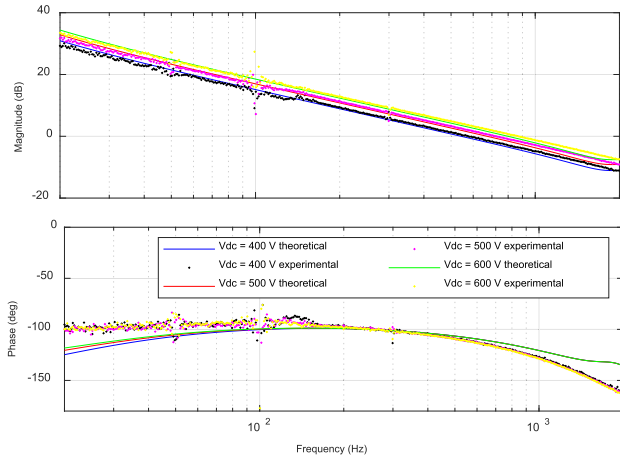$$B_{\hat{v}dc\_do} = -\dfrac{Fm \cdot I_{o1}}{C_{o1} + C_{o2}} \tag{23}$$

FIGURE 4. Scheme of the proposed control stage.

coupling terms.

$$k_{qdi} = -\frac{\omega(L_{fi} + \frac{c_1+c_2}{c_i}(L_g - M_g))}{Fm \cdot V_{dc}}, \quad i = 1, 2 \quad (24)$$

$$k_{dqi} = \frac{\omega(L_{fi} + \frac{c_1+c_2}{c_i}(L_g - M_g))}{Fm \cdot V_{dc}}, \quad i = 1, 2 \quad (25)$$

Besides the active and reactive current control loops, the second inverter has a third current control loop that regulates the *o*- axis component of the currents, allowing the cancellation of the circulating current between both inverters. When two inverters are connected in parallel, it is only necessary to regulate the zero-sequence current of one of the inverters, being null the zero-sequence duty cycle of the other. It is worth pointing out that conventional two-dimensional spatial vector modulation (2D-SVM) only operates in the $\alpha\beta$ plane, so this type of modulator cannot regulate the o-component. For this reason, the use of a three-dimensional SVM (3D-SVM) was proposed in [19] to properly regulate the *o*-component of currents. Fig. 4 shows the voltage control loop that calculates the current reference in the *d*- axis of both inverters, considering the relationship between their nominal power. The rated power of inverter #1 is 5 kW, and that of inverter #2 is 2.5 kW. To equally share the total power, the reference of the second inverter should be half of that of the first inverter.

A. STABILITY STUDY OF THE SYSTEM
The expressions of the current control loop gains in the *d*-, *q*-, and *o*- axes are defined in (26)-(28). In these equations, R_s stands for the current sensor gain that has a unitary value, $G_i(s)$ is the regulator for the *d*- and *q*- currents, $G_{io}(s)$ is the current regulator for the *o*- axis, $D(s)$ represents a delay equivalent to a switching period calculated from the second-order Padé approximant, and $FPB(s)$ is a low-pass

antialiasing filter. This filter is composed of a second-order Rauch filter and a first-order RC filter, both with a cut-off frequency of 10 kHz. The transfer functions of the duty cycle to the current in each axis have been calculated from the state space equations (1)-(23) using MATLAB^{TM} (R2018b). Note that *Fm* has a value of 0.5 V/V.

$$T_{idi}(s) = R_s \cdot G_i(s) \cdot D(s) \cdot FPB(s) \cdot \frac{\hat{i}_{i1di}(s)}{\hat{d}_{di}(s)}, \quad i = 1, 2 \quad (26)$$

$$T_{iqi}(s) = R_s \cdot G_i(s) \cdot D(s) \cdot FPB(s) \cdot \frac{\hat{i}_{i1qi}(s)}{\hat{d}_{qi}(s)}, \quad i = 1, 2 \quad (27)$$

$$T_{ioi}(s) = R_s \cdot G_{io}(s) \cdot D(s) \cdot FPB(s) \cdot \frac{\hat{i}_{i1oi}(s)}{\hat{d}_{oi}(s)}, \quad i = 1, 2 \quad (28)$$

Equation (29) shows the expression of the current regulators on the *d*- and *q*- axes. As the current control loops in both axes are similar, they have been used controllers that have the same expression. The regulator on the *o*- axis is expressed in (34). The current regulator in the *o*- axis is made up of a proportional integral regulator and resonants at 50 Hz (31), 150 Hz (32), and 450 Hz (33), implemented through second-order generalized integrators (SOGIs). The SOGIs allow increasing the gain of the control loops at the frequency of the most significant harmonics of the circulating currents.

$$G_i(s) = PI_i(s) = 0.1 + \frac{10}{s} \quad (29)$$

$$PI_o(s) = 0.2 + \frac{10}{s} \quad (30)$$

$$R_{50}(s) = \frac{4 \cdot 10 \cdot s}{s^2 + 10s + (2\tau\omega)^2} \quad (31)$$

$$R_{150}(s) = \frac{4 \cdot \frac{10}{3}s}{s^2 + \frac{10}{3}s + (2\tau 3\omega)^2} \quad (32)$$

$$R_{450}(s) = \frac{0.5 \cdot \frac{10}{9}s}{s^2 + \frac{10}{9}s + (2\tau 9\omega)^2} \quad (33)$$

$$G_{io}(s) = PI_o(s) + R_{50}(s) + R_{150}(s) + R_{450}(s) \quad (34)$$

Figures 5-7 represent the Bode (dB, deg) diagrams of the current loops defined in (26)-(28). The bode plots have been obtained within a voltage range from 400 V to 600 V. Both the theoretical and the experimental bode plots are represented in these figures. The calculation of the current control loop gains has been performed employing Matlab R2018b, and the measurements of the control loops have been obtained using the frequency response analyzer FRA5097 from NF Corporation.

These figures show that the system dynamics is sensitive to Vdc variations, being the system stable in all the Vdc range. Some stability parameters like the values of crossover frequency (fc), the gain margin (GM), and the phase margin (PM) for each of the loops have been summarized in TABLE 2.

FIGURE 5. Bode plot of the control loop gain of the current in channel d-for DC bus voltages from 400 V to 600 V.
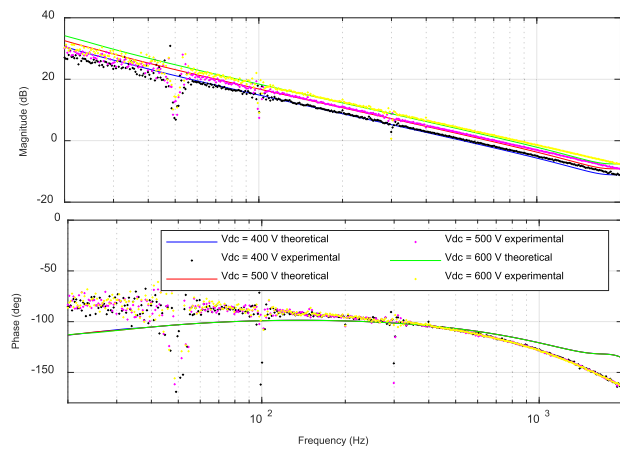

FIGURE 6. Bode plot of the control loop gain of the current in channel q-for DC bus voltages from 400 V to 600 V.
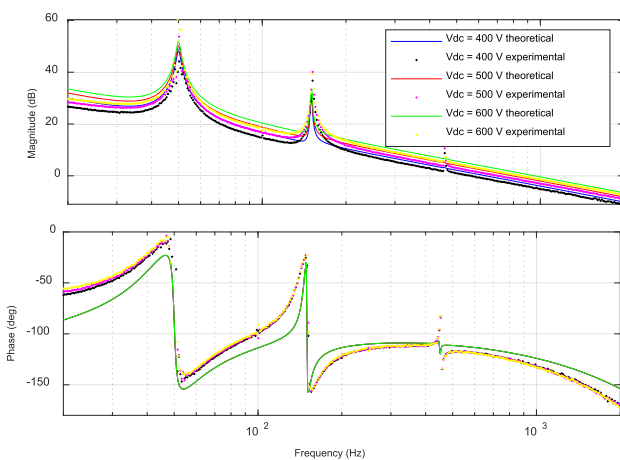

FIGURE 7. Bode plot of the control loop gain of the current in channel o-for DC bus voltages from 400 V to 600 V.

The voltage control loop gain follows (35). In this equation, β represents a unitary voltage sensor gain, $PI_v(s)$ stands for a

TABLE 2. Stability of current and voltage control loops.

	Parameter	400 V	500 V	600 V
$T_{id}(j\omega)$	Crossover frequency	550 Hz	680 Hz	800 Hz
	Gain Margin	11 dB	9.1 dB	7.5 dB
	Phase Margin	53°	49°	44°
$T_{iq}(j\omega)$	Crossover frequency	550 Hz	680 Hz	800 Hz
	Gain Margin	11 dB	9.1 dB	7.5 dB
	Phase Margin	53°	49°	44 °
$T_{io}(j\omega)$	Crossover frequency	640 Hz	800 Hz	950 Hz
	Gain Margin	9.2 dB	7.2 dB	5.6 dB
	Phase Margin	54°	47°	40°
$T_v(j\omega)$	Crossover frequency	14.6 Hz	12 Hz	10.2 Hz
	Gain Margin	19 dB	21.2 dB	23 dB
	Phase Margin	76°	74°	74°
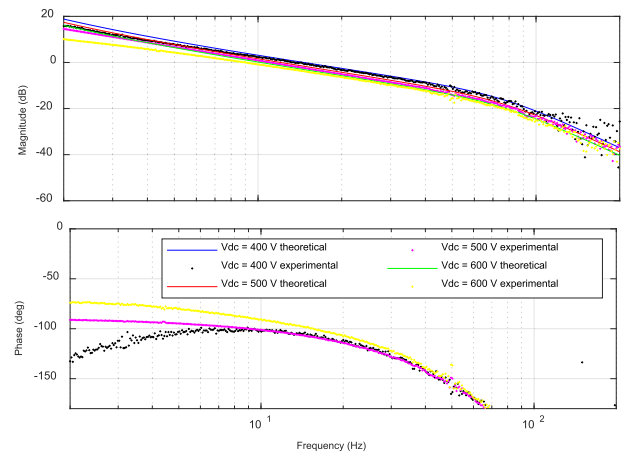
FIGURE 8. Bode plot of the control loop gain of the voltage in the DC bus for voltages from 400 V to 600 V.

proportional-integral regulator, and FPB(s) is a second-order low-pass filter that has a cut-off frequency of 80 Hz.

$$T_{vi}(s) = \beta \cdot PI_v(s) \cdot FPB(s) \cdot (c_1 + c_2) \cdot \frac{\hat{i}_{1di}(s)}{\hat{i}_{dref}(s)} \cdot \frac{\hat{v}_o(s)}{\hat{i}_{1di}(s)}$$

$$= \beta \cdot PI_v(s) \cdot FPB(s) \cdot (c_1 + c_2) \cdot \frac{\hat{v}_o(s)}{\hat{i}_{dref}(s)} \qquad (35)$$

The integral proportional regulator of the voltage regulation loop is expressed in (36).

$$PI_v(s) = -0.2 - \frac{2}{s} \qquad (36)$$

Figure 8 represents the system's theoretical and experimental voltage control loop gains, obtained in the voltage range from 400 V to 600 V.

TABLE 2 shows the measured stability parameters. Note that the crossover frequency of the current loops ranges from 550 Hz to 950 Hz, and the crossover frequency of the DC voltage loop ranges from 10.2 Hz to 14.6 Hz, with proper stability margins.
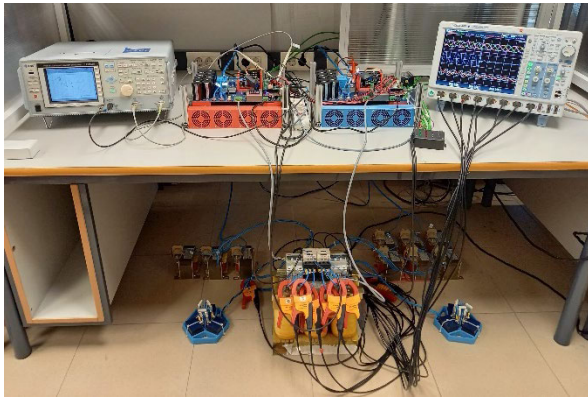
FIGURE 9. Experimental setup.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results are presented in this section. The simulation results have been obtained employing PSIM^{TM} software, while the experimental results have been performed with the setup pictured in Fig. 9. As expressed above, the two inverter modules connected in parallel have been connected to the AC bus and the DC bus of a hybrid microgrid. In the experimental setup, the AC bus has been powered by a bidirectional power supply Cinergia GL & EL-50 that has emulated the AC grid operating at 230 V RMS phase-phase and 50 Hz. A bidirectional GSS Regatron power supply has been used to emulate the DC bus of the hybrid microgrid working in a voltage range between 400 V and 600 V.

The inverters have been controlled using a dual-core Texas Instruments TMS320F28379D microcontroller. Each inverter has been controlled by its own DSP. The first core of the DSP establishes a Modbus communication system with a Graphical User Interface (GUI), and the second core is responsible for inverter control. The switching control signals of both inverters have been synchronized to avoid high-frequency circulating currents. The microcontrollers have been programmed in C using the Code Composer Studio v.5 suite.

A. SIMULATION RESULTS

1) LOW-FREQUENCY CIRCULATING CURRENTS

Simulation results of the control of circulating currents in hybrid microgrid interlinking converters in grid connection mode have been obtained with PSIM to validate the control scheme described in the previous section.

Figs. 10 (a), (b), and (c) show the phase currents, circulating currents, and the DC voltage before and after the activation of the circulating current (*o*- channel) control loop. The reference of the voltage control loop has been set to 400 V, 500 V, and 600 V, respectively. In all three cases, results are shown with the inverters working at the nominal power of the system, so inverter #1 is working at 5 kW and inverter #2 at 2.5 kW.

The graphic at the top of Fig. 10 (a), (b), and (c) depicts the phase currents of inverter #1. The second graphic depicts the
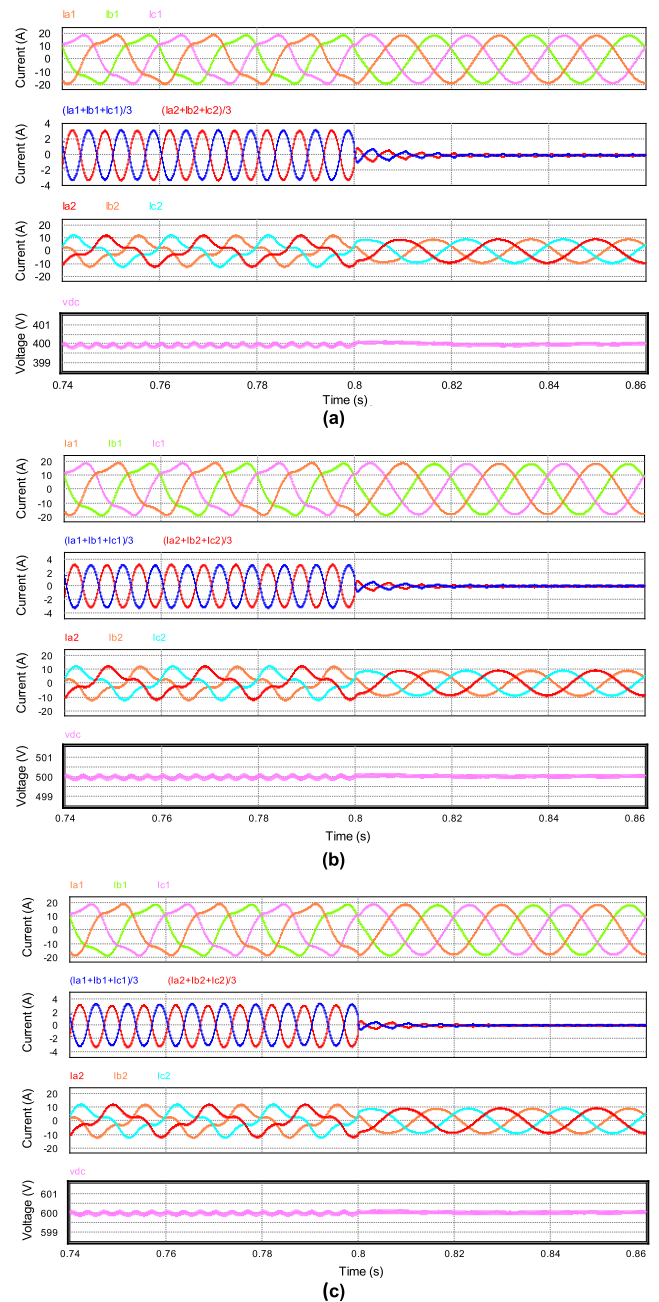
FIGURE 10. Simulation circulating currents, phase-currents, and DC-bus voltage before and after the activation of the circulating current control loop with DC voltage regulation at (a) 400 V, (b) 500 V, (c) 600 V.

circulating currents expressed as $(i_a + i_b + i_c)/3$, which are the zero-sequence currents of each inverter; the third graphic shows the phase currents of inverter #2, and the graphic at the bottom shows the DC bus voltage.

Before the activation of the zero-sequence current control loop, the circulating current of each inverter has a high amplitude of approximately 3.3 A (36% with regard to the fundamental component of the phase currents of inverter #2), obtaining a high distortion in the phase currents with a 33% THD value. Moreover, a 300 Hz ripple of approximately
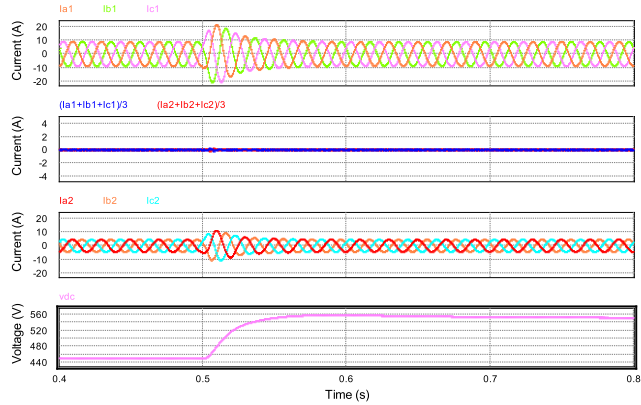
FIGURE 11. Simulation circulating currents, phase-currents, and DC-bus voltage with a voltage step from 450 to 550 V.
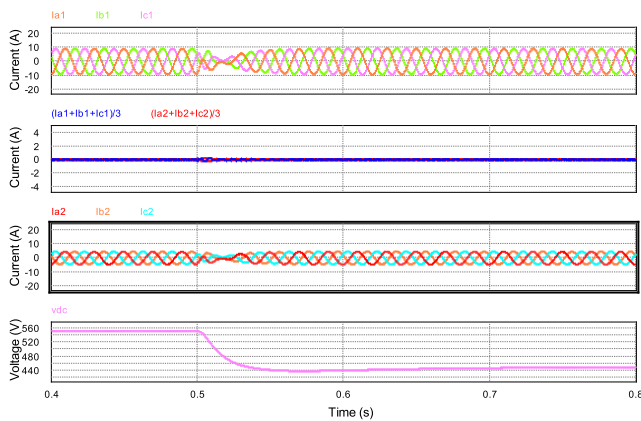
FIGURE 12. Simulation circulating currents, phase-currents, and DC-bus voltage with a voltage step from 550 to 450 V.
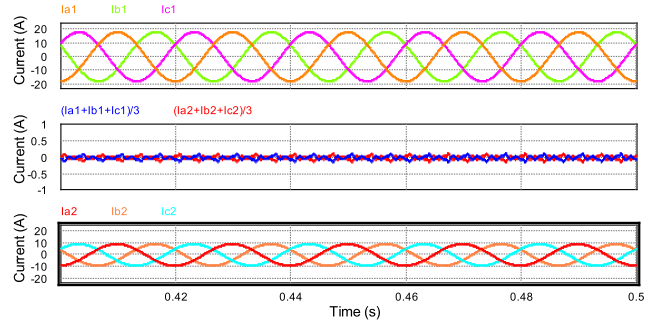

FIGURE 13. Simulation circulating currents and phase-currents with the carrier signals synchronized. $L_{f1} = 5$ mH, $L_{f2} = 7$ mH.
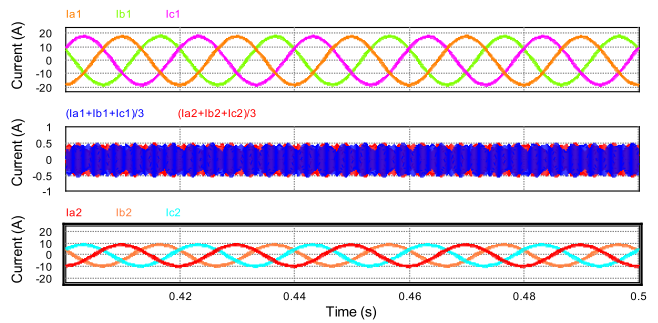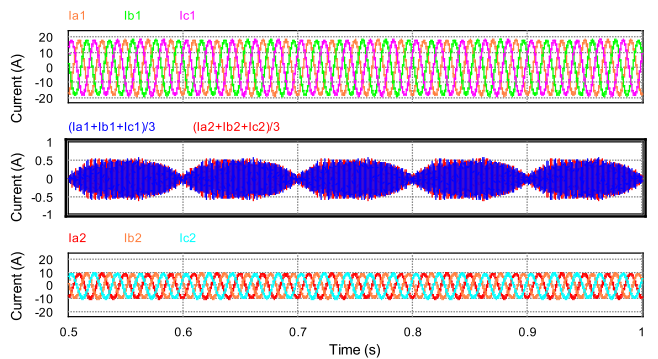

FIGURE 14. Simulation circulating currents and phase-currents with a 180° phase delay in the carrier signals. $L_{f1} = 5$ mH, $L_{f2} = 7$ mH.

FIGURE 15. Simulation circulating currents and phase-currents with a 0.1% difference in the carrier signals frequency. $L_{f1} = 5$ mH, $L_{f2} = 7$ mH.

50 mV appears in the DC bus voltage. By activating the zero-sequence control, the circulating currents are reduced, and the distortion of the phase currents and the 300 Hz ripple of the DC voltage disappear.

The control stage's performance has also been analyzed with DC voltage steps. In this case, the zero-sequence control loop is activated, being the circulating currents practically null in all the simulation time. To test whether sudden transients affect the performance of the zero-sequence current loop, Fig. 11 shows the system's behavior with a voltage step from 450 V to 550 V, where the voltage settling time is about 40 ms. Fig. 12 shows results for a step from 550 V to 450 V. In this case, the settling time is slightly longer, approximately 50 ms. In both cases, the circulating current remains correctly regulated to zero, although in the first instants of the transient, a slight variation can be seen that quickly disappears.

2) HIGH-FREQUENCY CIRCULATING CURRENTS

In the previous section, the performance of the zero-sequence current control loop has been analyzed. Results have been obtained by synchronizing the switches of the IGBTs in both inverters so that high-frequency circulating currents do not

appear. In this section, simulation results with mismatches in the carrier signals of the modulators have been obtained to analyze the influence of high-frequency circulating currents in this application.

Figs. 13, 14, and 15 show the results of the circulating currents with the same parameters as in the previous section. Inverter #1 works at 5 kW with 2D-SVM, inverter #2 operates at 2.5 kW with 3D-SVM, and the inductance values are $L_{f1} = 5$ mH, and $L_{f2} = 7$ mH. The zero-sequence current control loop is active in all cases.

Fig. 13 shows results with the carrier signals of the modulators synchronized, so high-frequency circulating currents do not appear. Fig. 14 shows the same waveforms in the same conditions but with a phase difference of 180° in the carrier
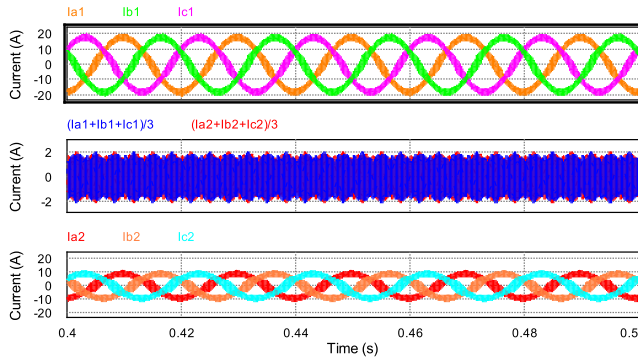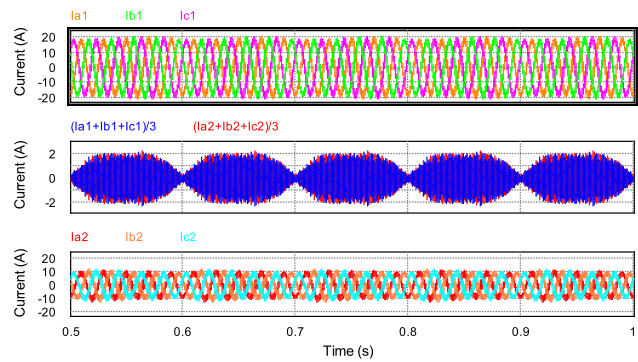
FIGURE 16. Simulation circulating currents and phase-currents with a 180° phase delay in the carrier signals. L_{f1} = 1 mH, L_{f2} = 2 mH.

FIGURE 17. Simulation circulating currents and phase-currents with a 0.1% difference in the carrier signals frequency. L_{f1} = 1 mH, L_{f2} = 2 mH.
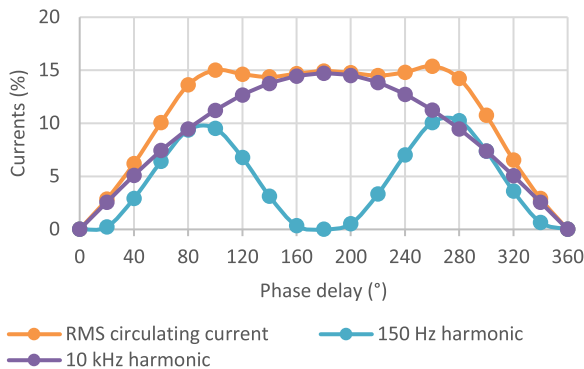

FIGURE 18. Evolution of the circulating currents with regard to the phase delay between the carrier signals.

signal of the modulator of inverter #2. In this case, high-frequency circulating currents with an RMS value of 320 mA appear. It is 5% with regard to the phase current of inverter #2.

The quartz crystal clocks of the DSPs have some frequency tolerance. For example, the quartz crystal of the TMS320F28379D is an ATS100B-E with a frequency stability of ±50 ppm, so it is a 0.01% error in the switching frequency of the inverters. Fig. 15 shows the circulating currents having a switching frequency of 10.01 kHz in the second inverter; it is a 0.1% increment. An increment of 0.1% instead of 0.01% has been considered in these results in order
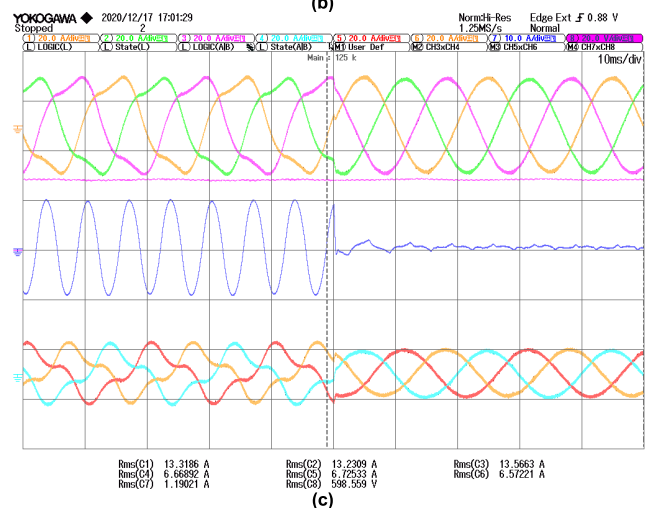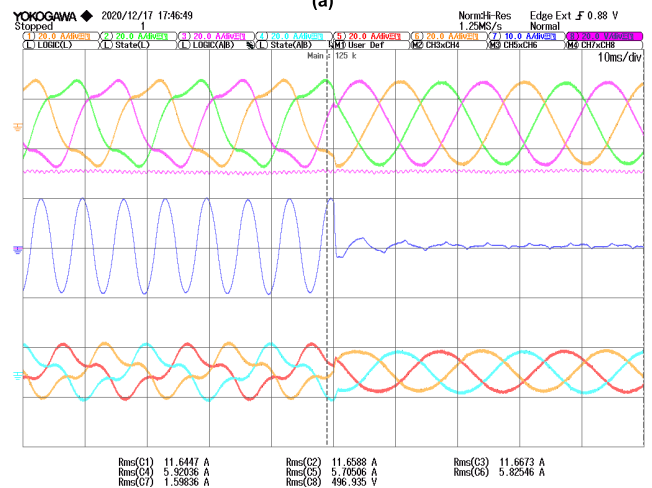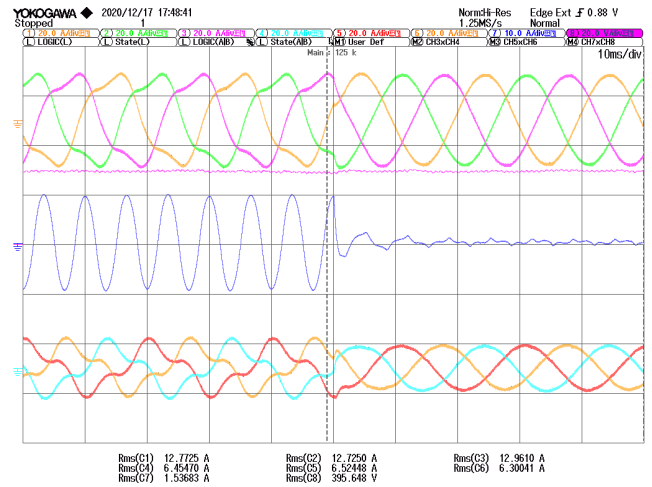
FIGURE 19. Experimental circulating current (center blue), phase-currents (top #inv1 bottom #inv2, and DC-bus voltage (center pink) before and after the activation of the circulating current control loop with voltage regulation in the DC bus at (a) 400 V, (b) 500 V, (c) 600 V.

to improve the visualization of the signals. The RMS value of the circulating currents is 231 mA (3.6% with regard to
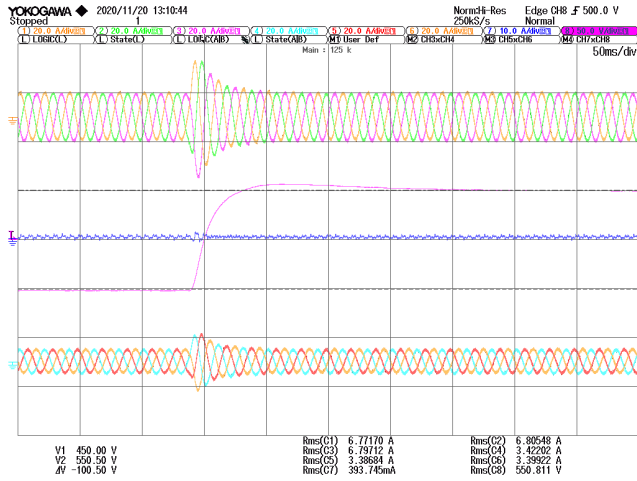
FIGURE 20. Experimental circulating current (center blue), phase-currents (top #inv1, bottom #inv2), and DC-bus voltage (center pink) with a voltage step of 450 to 550 V.
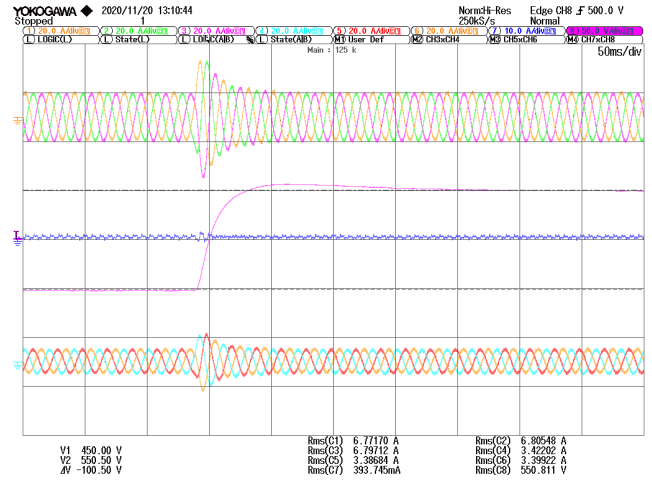

FIGURE 21. Experimental circulating current (center blue), phase-currents (top #inv1, bottom #inv2), and DC-bus voltage (center pink) with a voltage step of 550 to 450 V.

the phase current of inverter #2) and is not affected by the frequency tolerance of the carrier signals.

Similar results to Figs. 14 and 15 have been obtained in Figs. 16 and 17, respectively, but with a smaller LCL filter. Results in Figs. 14 and 15 have been obtained with the inductances available in the laboratory for the experimental results. The new filter has been calculated considering a 30% ripple in the L_f inductor, which is a common practice in industrial applications. In this case, the inductances would have the values $L_{f1} = 1$ mH and $L_{f2} = 2$ mH. The RMS value of the circulating currents in Fig. 16, where a 180° phase delay in the carrier signals has been considered, is 1.62 A (25% with regard to the phase current of inverter #2). In Fig. 17, in which a 0.1% frequency difference in the carrier signals has been considered, the RMS value of the circulating current is 1.16 A, which is 18% with regard to the RMS value of the phase currents of inverter #2.

Finally, Fig. 18 shows the effects of phase delay in the carrier signals of the modulators. Fig. 18 shows that the 150 Hz component of the circulating currents is higher when the phase delay is 90° and 270° being its value of approximately 10% with regard to the fundamental component of the phase currents. However, the 10 kHz component of the circulating currents is greater at 180° with a 15% value with regard to the fundamental component of the phase currents, where the 150 Hz component is null. At 0° and 360°, when the carrier signals are synchronized, both the 150 Hz and the 10 kHz components are null.

B. EXPERIMENTAL RESULTS

Fig. 19(a), (b), and (c) show experimental results of the phase currents, the circulating currents, and the DC bus voltage (in pink, channel 8 of the oscilloscope). The circulating currents are represented as the sum of $i_a + i_b + i_c$, three times the value of the circulating currents. The voltage in the DC bus is set at the three operating points described above 400 V, 500 V,

and 600 V. In all cases, results are shown for 100% of the nominal power of the system before and after the activation of the zero-sequence current control loop. It is observed that in all the cases, the DC voltage remains stable and that the circulation current is highly reduced when the zero-sequence current control loop is activated. High-frequency circulating currents do not appear due to the synchronization of the carrier signals between the inverters.

The performance of the regulation loops to voltage steps from 450 V to 550 V and from 550 V to 450 V has also been measured. The results obtained are shown in Fig. 20 and Fig. 21. The settling time for the 450 V to 550 V step is approximately 150 ms, while the settling time for the 550 V to 450 V voltage step is approximately 200 ms.

V. CONCLUSION
This work has contributed to the parallel connection of inter-linking inverters between the AC and DC buses of a hybrid microgrid. Despite its benefits, the parallelization of inverters causes the appearance of circulating currents. To avoid low-frequency circulating currents, a current control loop that regulates the zero-sequence component of the phase currents has been implemented in this work. The control scheme has been applied to a system composed of one 5 kW and one 2.5 kW interlinking inverters, emulating an eventual 50% power increase in the system. They have been obtained simulation and experimental results that show the effectiveness of zero-sequence current control loop for canceling low-frequency circulating currents in this application, as well as confirming that there are no interactions with the DC bus voltage control loop in a wide regulation range. Moreover, simulation results have been obtained showing the effects of the frequency and phase difference of the carrier signals of the modulators in the circulating currents. With these mismatches, a 150 Hz component appears in the circulating currents that can be suppressed with the zero-sequence

current control loop. However, the components that are near the switching frequency cannot be controlled with the zero-sequence current control loop, so it is necessary to synchronize the switches of the IGBTs in both inverters.

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