

RESEARCH ARTICLE

A 0.57 mW@1 FPS In-Column Analog CNN Processor Integrated Into CMOS Image Sensor

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ABSTRACT This article presents a high-performance, low-power analog convolutional neural network (CNN) circuit integrated into a CMOS image sensor (CIS) for face detection applications. The main block of the proposed in-column analog CNN circuits is an analog multiplication-and-accumulation (MAC) circuit consisting of an operational transconductance amplifier-based switched capacitor circuit enabling the programmable weight function. With the proposed MAC, a 3-layer analog CNN processor is implemented into the column-parallel readout circuit in conventional CIS. Furthermore, for low-power CNN operations, we use a low-resolution analog-to-digital converter with the proposed nonlinear quantization method resulting in an increase in the accuracy of face detection from 92.8% to 98.75% at 120 frame rates with 2.8 V/1.5 V supply voltage. A prototype sensor with 160 × 120 effective image resolution was fabricated using a 110 nm CMOS image sensor process. The measurement results showed that the maximum power consumption was 0.57 mW and 4.02 mW at 1 and 120 frame rates, respectively.

INDEX TERMS CMOS image sensor, convolutional neural networks, face detection, multiplication-and-accumulation, nonlinear quantization.

I. INTRODUCTION

Recently, with the advancement of machine learning, various deep neural network (DNN)-based applications have been widely used in the Internet of Things (IoT) applications [1]. The system architecture of conventional DNN converts image information from external high-performance CMOS image sensors (CIS) into digital output to perform DNN tasks on neural processing units (NPU) [2]. Operating two chips requires a large memory area to transmit extensive image data to the external NPU chip, resulting in decreased operation speed and increased power consumption. To overcome such issues from two-chip solutions, simple image processors adjacent to image sensors with switched-current-based

multiplication-and-accumulation (MAC) and in-column convolutional neural network (CNN) processors in CIS have been proposed [3], [4], [5]. The switched-current-based MAC converts the voltage scale of the pixel into a current and performs a convolution operation. However, since the error in the current mirror circuit can lead to variations in the weight values, a high-performance current mirror is required. In addition, frame per second (FPS) operation is low (=1 FPS in [3]). The in-column CNN processor in CIS showed a fast data-processing time (120 FPS in [4]). However, a the switched-capacitor-based AMAC consisting of passive devices without an operational transconductance amplifier (OTA) was used, the weights could not be changed, resulting in low face detection accuracy due to a fixed weight. Furthermore, the functions of the algorithms are limited [4], [5].

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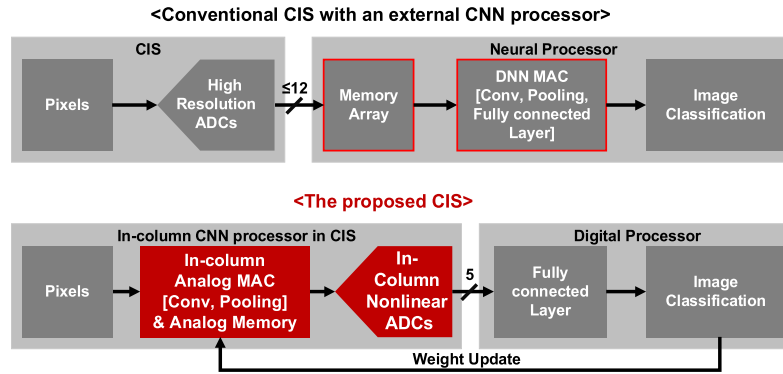


FIGURE 1. Conventional CIS with CNN system and the proposed CIS system.

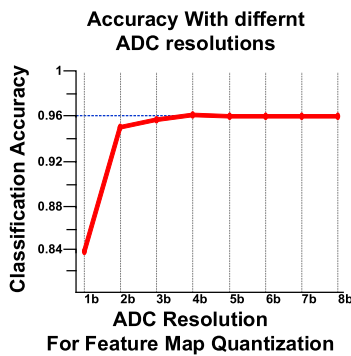


FIGURE 2. Accuracy of the proposed CIS by ADC resolution.

Therefore, we present an in-column CNN processor in a CIS capable of weight update and high-speed operation (=120 FPS) with the proposed switched-capacitor-based analog MAC with an OTA. In addition, for low-power operation within a limited area, a nonlinear quantization technique was proposed for a low-resolution analog-to-digital converter (ADC) to improve the accuracy of face detection. Fig. 1 shows a conventional CIS with a CNN system and the proposed CIS system. The conventional system performs CNN algorithms in the digital domain after converting analog voltages representing extensive image data from the pixel array to digital code with a high-performance ADC. On the other hand, the proposed CIS has an in-column CNN processor structure with two integrated convolution layers for low-power operation and high face detection accuracy. The proposed CIS consists of an analog MAC circuit and memory block to perform a convolution operation. The algorithm of the proposed analog CNN processor consists of a 2×2 convolution layer (stride = 1) and a 2×2 pooling layer (stride = 2). Fig. 2 shows the trend of face-detection accuracy with different ADC resolutions of the proposed CIS. The feature maps were quantized with different ADC resolutions ranging from one to eight bits. After performing classification, the accuracy tendency according to the different quantized ADC bits can be calculated. From the results, we found that ADCs with four or more bits had similar image classification accuracies of

approximately 96%. We think the reason why the accuracy is saturated at ADC resolution above a certain level is that in the case of face detection, classification is performed by learning key elements such as eyes and nose from a human face. Therefore, unlike CNN systems using conventional CIS that require a high-resolution ADC (≥ 12 bits), the ADC resolution for quantizing feature map images in the proposed in-column CNN can be lowered (ADC resolution: 5 bits in this paper).

Furthermore, with the proposed analog MAC with an OTA-based switched capacitor circuit, a weight update was possible, resulting in an approximately 2.62% improvement in the face detection accuracy from 92.8% to 95.42%. In addition, the proposed nonlinear quantization technique has a face-detection accuracy of 97.50% and power consumption of 4.02 mW at 120 FPS, 5b-resolution ADC.

This article is organized as follows. Section II describes the operation of the proposed analog MAC and nonlinear quantization. Section III presents the measurement results with a prototype sensor. Finally, Section IV presents the conclusions of this paper.

II. THE PROPOSED ANALOG CNN PROCESSOR IN CIS SYSTEM

A. OVERALL SYSTEM ARCHITECTURE

Fig. 3 shows the proposed analog CNN processor architecture; it receives 160×120 image data as input and consists of 2×2 convolutional layers (numerical = 1) and 2×2 pooling layers (numerical = 2). The outputted 5-bit 40×30 feature map data is a fully connected layer processed by the software. Fig. 4 shows the proposed CIS architecture integrated with an in-column analog CNN processor. The CIS consists of a 160×120 pixel array and a source follower and uses a rolling-shutter reading method. For analog CNN processing, there were three layers using the proposed analog MAC circuit and a nonlinear single-slope analog-to-digital (SSADC) in each column. Fig. 5 shows the two operation modes of the proposed CIS: CIS and CNN modes. For example, the proposed CIS may operate in either CIS mode or CNN mode, depending on the operation of an analog convolution

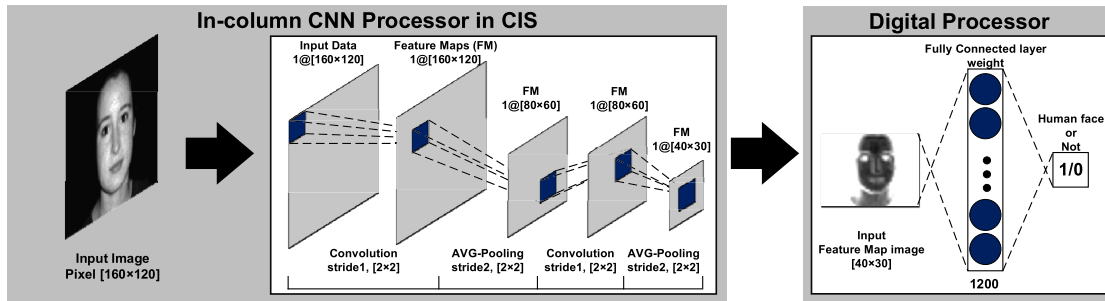


FIGURE 3. The proposed analog convolutional neural network algorithm.

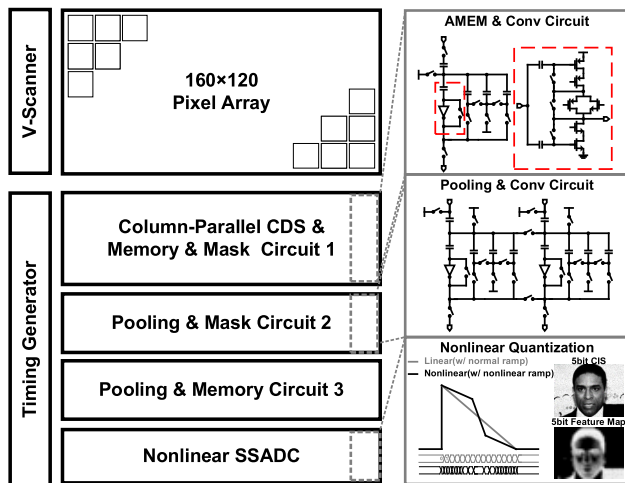


FIGURE 4. The proposed CIS system architecture.

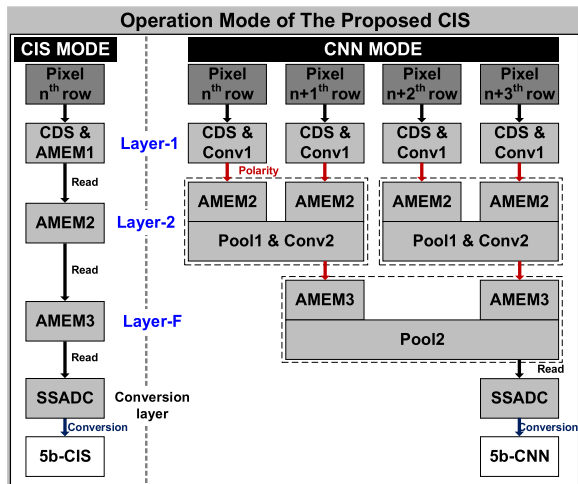


FIGURE 5. Operation mode of the proposed CIS.

processor. In this model, two convolutional layers were implemented with three analog layers. In CIS mode, a pixel voltage of 160×120 is input to the analog convolution processor, and the first layer (Layer-1) performs and stores a pixel's correlated double sampling (CDS). After that, Layer-1 and the final layer (Layer-F) convert the pixel voltage data of the

final 160×120 into a 5-bit CIS image through SSADC using the read and storage process. In CNN mode, a pixel voltage of 160×120 is input into the analog convolution processor as in CIS mode. Layer-1 performs CDS and first convolutional weight (with 2×2 convolutional mask) operations. Then, the second layer (Layer-2) accumulates the output of Layer-1 in analog memories and applies average-pooling and the second convolutional weight (with 2×2 convolutional mask) operations. After pooling, 80×60 feature map data were stored in Layer-2, and the 2×2 convolution 2-layer weight was calculated and stored. Polarity and pooling are performed in the same process as in Layer-2, and the final input data of 160×120 pixels are compressed and output as 40×30 feature map data. Finally, in Layer-F, Layer-2 values are accumulated in analog memories, and the second average pooling is performed. The 40×30 feature map converted a 5-bit CNN image into a nonlinear lamp signal at the SSADC. The proposed CIS can retrain the algorithm models by obtaining noisy images from the CIS mode output data. Based on the retraining results, weight updates were performed to improve the model accuracy by 2.62%, from 92.8% to 95.42%.

B. THE PROPOSED ANALOG MAC CIRCUIT

Fig. 6 shows the proposed analog MAC circuit and its timing diagram for the CDS and convolution weight operations. The proposed analog MAC circuit with an auto-zeroing operation was implemented in a column pitch ($12.8 \mu\text{m}$ in this paper) with an amplitude of approximately 50 dB. OTA operates the Reset and Redistribution phases using auto-zeroing (AZ) signals. In the reset phase, AZ is logic 'Low', and the input transistors M1 and M6 are connected to the drain nodes of the current source (M2 and M5) to sample the OTA logical current bias (auto-zeroing voltage) to the C_{AZ} at negative feedback. In the redistribution phase, the OTA operates with an AZ high signal. M1 and M6 use the bias sampled from the C_{AZ} , and the AZb switch is connected to become the OTA of the cascode inverter structure. M3 and M4 are used to set the bias voltages V_{G1} and V_{G6} when a static current with V_{SG3} and V_{SG4} flows during the reset phase (called the floating current source [6]). After resetting, M3 and M4 are bypassed. OTA uses a negative feedback structure to allow programmable weight values to be used during analog MAC

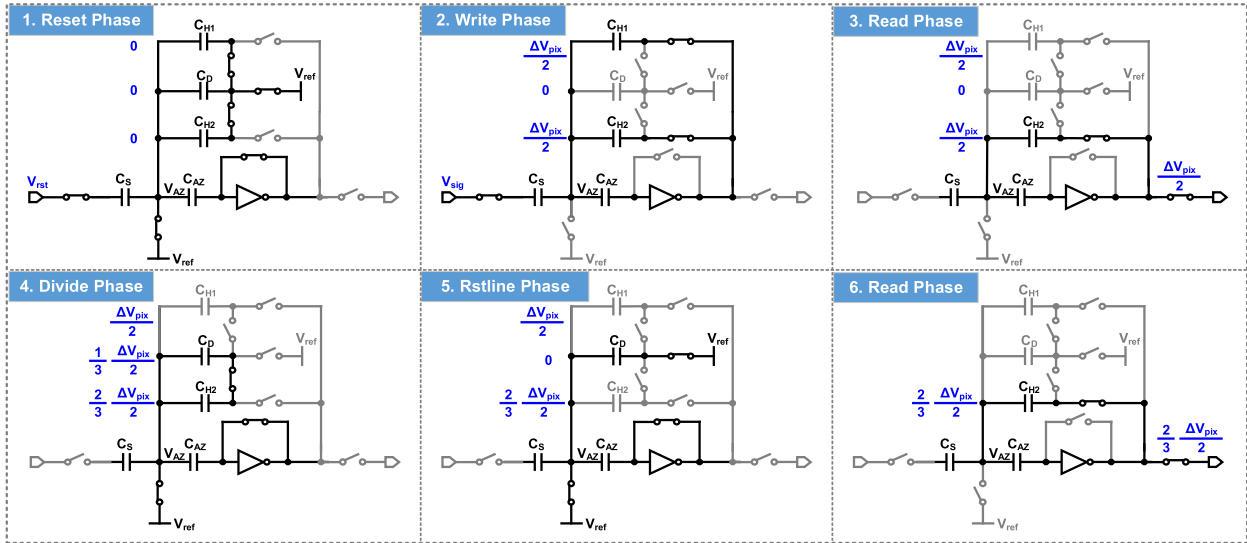


FIGURE 8. The proposed analog MAC convolution weight operations.

$$Q_{W2} = C_S (V_{FM} + V_{ref} - V_{ref}) + 2C_H (V_{out} - V_{ref})$$

$$V_{out} = V_{H1,2} = -\frac{C_S}{2C_H} (V_{FM}) + V_{ref} \quad (4)$$

The non-inverted sampling of the proposed analog MAC follows (5). First, when the V_{FM} is input, the initial charging in the write phase of the analog MAC and reset phase of the OTA follow Q_{WR2} . Second, the polarity phase of the analog MAC reset the C_S and changes the charge to Q_{RL2} . Finally, the output voltage, V_{out} was sampled using the non-inverted V_{FM} .

$$Q_{WR2} = C_S (V_{FM} + V_{ref} - V_{ref})$$

$$Q_{RL2} = C_S (V_{ref} - V_{ref}) + 2C_H (V_{out} - V_{ref})$$

$$V_{out} = V_{H1,2} = +\frac{C_S}{2C_H} (V_{FM}) + V_{ref} \quad (5)$$

Fig. 10 shows the proposed analog CNN architecture. The processes shown in Figs. 8 and 9 can implement the size and polarity of the convolution mask. The masks for M and $M+1$, as shown in Fig. 7, were implemented. The CNN of the proposed CIS has a 2×2 mask (stride = 1) structure, and receives data from one row at a time. Before reading the Pixel N row data, the weight of mask $N-1$ row is implemented with $N-1$ row data stored in the conv1 layer. The data of the M and $M+1$ columns are received and accumulated by the MUX. After performing the $N-1$ row of a mask, the conv1 layer performs the N row of the pixel with CDS and weight. The calculated 2-row data (one row of the feature map) are accumulated in the conv2 layer for the pooling operation. If two rows of feature maps accumulate in the conv2 layer by repeating the previous process, 2×2 pooling (stride = 2) is operated by connecting the $M+1$ column with switches, S_{ML} and S_{MR} . The convolution and pooling processes of the conv2 and convF layers are identical. Finally, the 4-row pixel

data were compressed into 1-row feature map data using the analog CNN.

Furthermore, the proposed analog CNN operates with a 2×2 average pooling (stride = 2). First, the 2-row feature map data operating in the conv1 and conv2 layers were accumulated in the conv2 and convF layers. Second, average pooling is performed by connecting the M and $M+1$ columns using a binning switch (S_{Bin}). The V_{FM} stored in $C_{H1,2}$ is distributed as an average voltage. The average pooling operation process of the proposed analog MAC follows (6).

$$Q_{P,M} = 2C_H (V_{FM,M}) + 2C_H (V_{FM,M+1})$$

$$Q_{P,M+1} = 4C_H (V_{out} - V_{ref})$$

$$V_{out} = V_{H1,2} = \frac{1}{2} (V_{FM,M} + V_{FM,M+1}) + V_{ref} \quad (6)$$

The 160×120 input data were compressed and output as 40×30 feature map data by operating with an average pooling layer. One hundred and sixty columns of ADC are required to perform CIS, and only 40 columns of ADC are required to perform CNN. As a result, the power consumption of CIS mode is 4.54 mW, while that of CNN mode is 4.02 mW, 11% less power consumption at 120 FPS.

D. NONLINEAR QUANTIZATION TO IMPROVE ACCURACY

Fig. 11 shows the process and image of the SSADC depending on the mode of the proposed CIS. In the CIS mode, the pixel voltage after performing CDS is input to the SSADC comparator input node V_{LF} and the ramp signal is input to V_{ramp} to output a 5b CIS image. The feature map (FM) calculated by the analog CNN was input to the V_{LF} in the CNN mode. A 5-bit CNN image is output by applying the CNN offset signal shown in Fig. 12, which is capable of negative calculation. Based on the output 5-bit feature map data, face detection achieved an accuracy of 92.8%. The random noise generated when implemented in hardware was reduced by

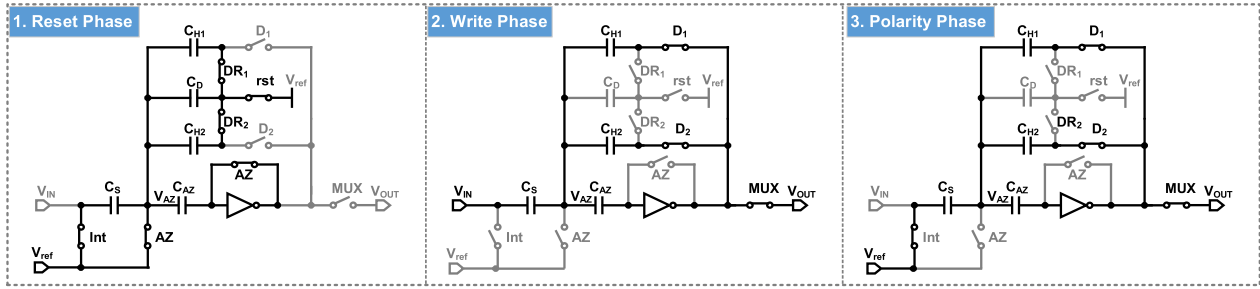


FIGURE 9. The proposed analog MAC convolution weight polarity operations.

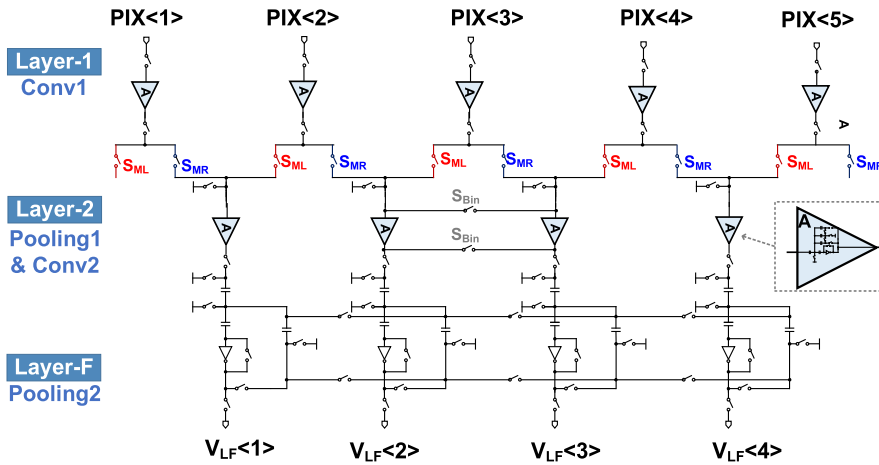


FIGURE 10. The proposed analog CNN architecture.

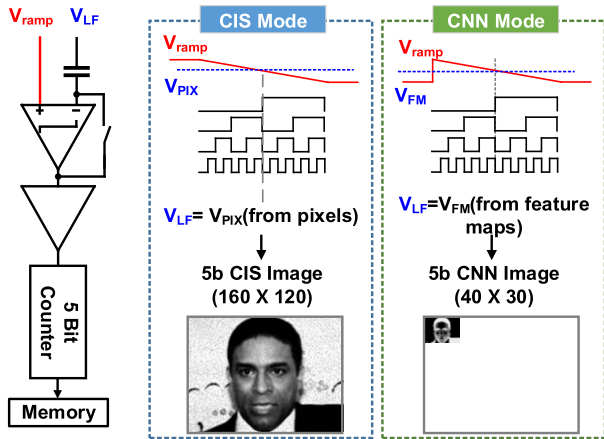


FIGURE 11. Data conversion operations of the proposed CIS.

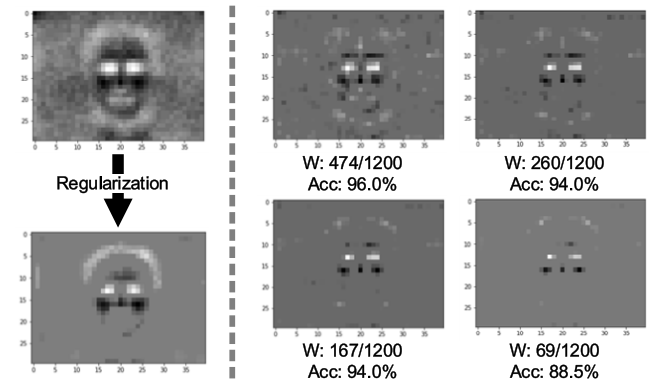


FIGURE 12. Image classification accuracy and weight changes according to regularization lambda.

3.2% compared to the results of existing software models. To compensate for the reduced accuracy, software retraining was conducted with noise-containing data, and because of the weight update and regularization of the fully connected layers, the accuracy was improved by 95.42%.

Fig. 12 shows the weight and image classification accuracy change depending on the regularization lambda of the fully connected layer. Normalization makes the low-critical

weight of the fully connected layer zero and allows only the high-critical weight to perform the classification. As lambda increased, the weight and accuracy decreased, but a critical feature map could be identified. As a result, classification accuracy improves for features such as eyes, nose, cheekbones, and hair. The feature map data to be calculated by weight were 0–3 and 20–31 5-bit codes, which were the minimum and maximum data conversion values, respectively. These are close to the minimum and maximum codes of the

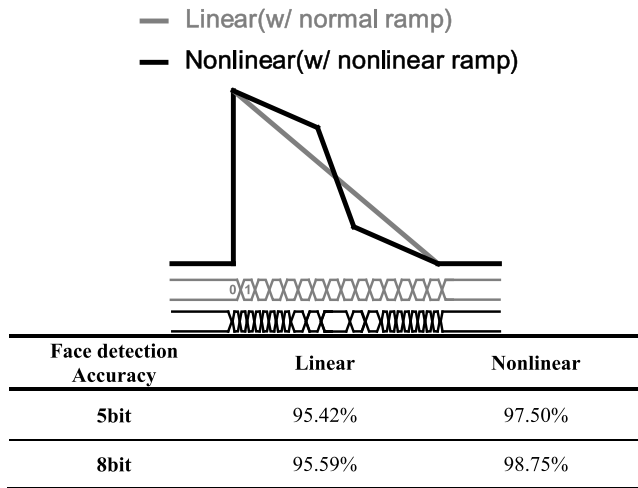


FIGURE 13. Comparison to the accuracy of face detection with linear and nonlinear signals.

feature map, and are the start and end of the CNN ramp signal, respectively. Therefore, the importance of performing a CNN is low because the other codes are weighted to zero.

Fig. 13 shows a comparison of the accuracies of the linear and nonlinear signals. The proposed CIS can apply a double gain slope for highly critical values (= codes 0–1, 26–31 based on a normal 5-bit ramp), resulting in the same effect as using a high-resolution ADC. In the ADC of the proposed CIS, noise can be reduced compared with the conventional SSADC because the ADC quantization noise is smaller than the thermal noise [7], [8]. The low-critical value is a 5-bit ADC obtained by applying a gain slope of 1 and 0.5, which improves the face-detection accuracy by 2.08%, from 95.42% to 97.5%. The proposed enhancement technique demonstrates improved performance because the higher the bit resolution, the higher is the resolution usage effect. In the 8-bit resolution SSADC, nonlinear quantization techniques were applied for a 3.18% improvement from 95.59% to 98.75%. Using the proposed technique, the proposed CIS achieves high face-detection accuracy even in low-resolution ADC and reduces the ADC area and power.

III. IMPLEMENTATION RESULTS

Fig. 14 shows the layout and summary of the CIS with the proposed integrated analog CNN processor. The proposed CIS was designed with a 110 nm 1P4M CIS process at $3.3 \times 3.6 \text{ mm}^2$. A pixel is an active pixel sensor with a 4-tr structure that uses a rolling shutter readout method with an image resolution of 160×120 . The total power consumption is 4.02 mW at 120 frames/s and a global clock of 20 MHz.

Fig. 15 shows the power consumption depending on the mode of the proposed CIS. As shown in Fig. 5, CIS and CNN have different readout operations. The proposed CIS uses an analog CNN processor as the CDS and analog memory to output $160 \times 1,205$ bits of output data and 4.54 mW at 120 FPS. Meanwhile, the CNN mode of the proposed CIS outputs 160×120 input data as 40×30 5-bit output data, as it

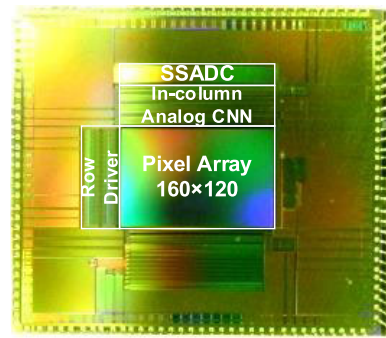


FIGURE 14. Chip photograph.

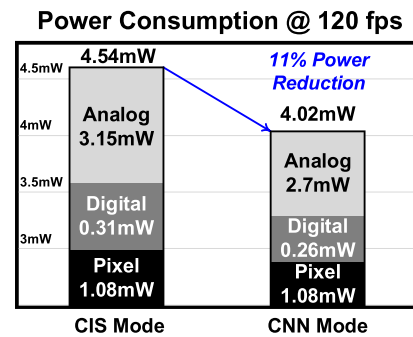


FIGURE 15. Measured power consumption reduction.

can compress pixel 4-row data into 1-row data with an analog CNN operation. Since only a 40-column ADC was used in the 160-column ADC, the power consumption decreased by 11% to 4.02 mW.

Fig. 16 shows the measurement environment and the system block of the proposed CIS. The proposed CIS was measured using field-programmable gate array (FPGA) boards, LED displays projecting test images, a host PC, and PC software. The TEST image was input from the laptop LED display, and the proposed CIS could output different images in the CIS and CNN modes. Either the CIS or CNN modes operate with only one ramp generator, similar to a normal CIS. In this paper, the ramp signal was generated using an external digital-to-analog converter (DAC) on an FPGA board. However, a bi-directional gamma curve for nonlinear characteristics can be implemented by modifying the counter circuit to almost the same area by changing the counter clock frequency [8]. The output images are transmitted in the order of FPGA, host PC, and software PC, and image classification and retraining are performed. In addition, the weight and nonlinear ramp signals trained through a Host PC and FPGA can be adjusted externally. Images (input dataset) with 160×120 resolution consisting of 600 human faces and 600 non-face objects were used in the experiment. Furthermore, the entire data set was divided into a 4:1 ratio to form a training set and a test set. Using the proposed analog CNN circuits and nonlinear ADC, the feature map images were quantized. The final fully connected layer classifies and estimates the

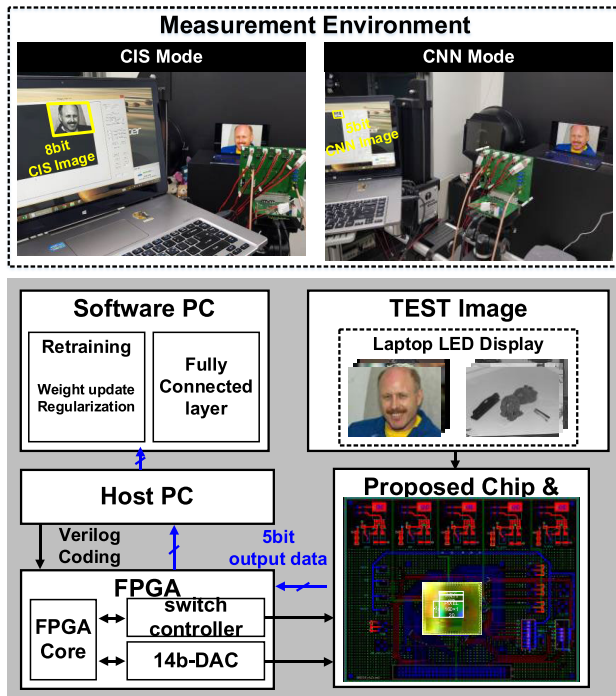


FIGURE 16. Measurement environment & system.

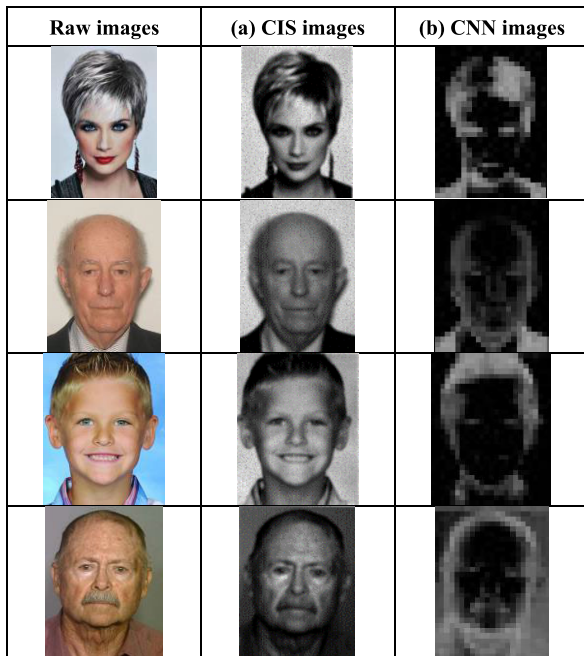


FIGURE 17. Measured images of (a) CIS mode and (b) CNN mode of the proposed CIS.

accuracy. The proposed CIS achieved 97.50% face-detection accuracy at a 5-bit resolution and 98.75% at an 8-bit resolution. Fig. 17 shows the measured images with the CIS and CNN modes, respectively. It should be noted that the CIS mode is used to control the focus before capturing images and collecting data for retraining.

TABLE 1. Performance comparison table for CIS-integrated FD.

	ISCAS' 19 [3]	Sensors' 20 [4]	ISSCC' 22[5]	This Work
Technology	65nm	110nm	180nm	110nm
Supply [V]	Analog: 2.5, 1.2 Digital: 0.77~1.1	3.3	0.8	2.8
Pixel readout	4T-APS	4T-APS	4T-PWM	4T-APS
Pixel Size[μm^2]	7 \times 7	3.2 \times 3.2	7.6 \times 7.6	3.2 \times 3.2
Pixel resolution	320 \times 240	160 \times 120	126 \times 126	160 \times 120
Maximum frame rate [FPS]	1	120	250	120
Chip Area [mm²]	3.6 \times 4.4	2.93 \times 2.61	2.18 \times 2.46	3.3 \times 2.6
Algorithm	FD & FR: Analog-digital hybrid CNN	FD: Analog-CNN	FD: Analog-digital CNN	FD: Analog-CNN
Accuracy [%]	1.5b ^a :96.18	8b ^a :89.33	8b ^a :93	5b ^a :97.50 8b ^a :98.75
Total Power [mW]	@1FPS: 0.62	@120FPS: 1.12	@250FPS: 0.135	@120FPS: 4.02

^a ADC resolution.

^b Estimated power consumption for FD; power consumption is reduced by about 20% with the reduction of every 10 FPS in [9]

Table 1 shows a performance comparison table of CIS integrated with face-detection algorithms. A conventional CIS [4] integrated with face detection is designed in a column for integration and fast data processing, and its constraints achieve a low face-detection accuracy of 2 \times 2 convolution layer (stride = 2) and fixed-weight 8-bit resolution ADC. The additional out-of-array processor design [3] achieves 96.18% accuracy at 0.62 mW through current convolution and digital operations but has a one FPS slower data processing performance. In the case of [5] using 4T-pulse width modulation (PWM) for fast data-processing speed and low power consumption, it has 0.135 mW power consumption at 250 FPS and achieves 93% face-detection accuracy. However, it is difficult to use the 4T-PWM reading method in typical mobile applications. The proposed CIS had a 4.02 mW power consumption at 120 FPS through an in-column design using a general 4T-APS. Analog CNN processors with weight-updateable and nonlinear quantization achieved a face-detection accuracy of 98.75% at an 8-bit resolution SSADC. The proposed CIS has the lowest power consumption of 0.57 mW among the methods that achieved \geq 95% face-detection accuracy and a fast data-processing speed of 120 FPS.

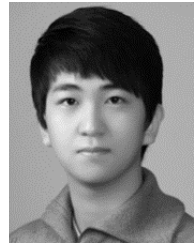
IV. CONCLUSION

This article proposes a CIS integrated with an in-column analog CNN processor with a power consumption of 4.02 mW and 98.75% face-detection accuracy at 120 FPS operation. The proposed analog MAC circuit with integrated analog memory, convolution and pooling operations, low-resolution ADC usage, and weight update is possible. The proposed CIS

can achieve high face-detection accuracy with weight updates and the proposed nonlinear quantization techniques, even if the face-detection accuracy is reduced by the random noise generated in the hardware implementation. The proposed CNN architecture can be implemented as an in-column CNN processor with a 160×120 image resolution, which can be effective for a variety of face-detection mobile applications.

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