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APPLIED RESEARCH

Control Strategy for a Bidirectional Wireless Power Transfer System With Vehicle to Home Functionality

MANUELE BERTOLUZZO, ABHAY KUMAR, AND AMRITANSH SAGAR, (Senior Member, IEEE)
Department of Industrial Engineering, University of Padova, 35131 Padua, Italy
Corresponding author: Manuele Bertoluzzo (manuele.bertoluzzo@unipd.it)

ABSTRACT The advancements in the charging strategy of electric vehicles will have inevitable effects on the electric grid in the coming future. Electric vehicle battery chargers are able to perform the bidirectional power transfer according to the vehicle-to-grid concept and will offer valuable services to the distribution grid or to the domestic grid of the vehicle owner. The wireless power transfer battery chargers offer the opportunity for a more safe and user-friendly approach to electric vehicles for people who are not confident with technological apparatuses. Bidirectional wireless power transfer chargers capable of vehicle to grid services are the natural evolution of the above-mentioned concepts. This paper faces the topic of developing the control strategy for such a battery charger, focusing on the needs of the power conversion stages involved in the functioning of a charger enabled for vehicle to home operation. At first, the separation of the control strategy into two levels is explained, and then the interaction between the algorithms of the internal and external level is introduced. In implementing the control algorithms, it was decided to design controllers as simple as possible. This made it possible to adopt techniques well known in the scientific community for their design and to contain the computational resources needed for their implementation. Despite the simplicity of the controllers, the introduction and the management of the interactions between the various algorithms led to the development of an overall control strategy that at the same time respects the voltage and current limits set by the grid and the battery and also avoids exceeding the maximum operating conditions of the static converters that constitute the system. The algorithms and the relevant controllers are developed one by one in the continuous time domain, using techniques based on the analysis of Bode diagrams of the transfer functions involved in the operation of the system. In designing the controllers, the effects of their subsequent implementation in a discrete time domain are considered together with the effects of the transmission delay originated by the data exchange between the two sections of the system. The discretization of the controllers has been performed using the Tustin method. The performance of all the algorithms has been separately verified in the discrete time domain using simulations developed in the Matlab/Simulink environment. Finally, the functioning of the complete control strategy has been successfully checked in the same environment.

INDEX TERMS Electric vehicle, vehicle to home, wireless power transfer, bidirectional power transfer.

I. INTRODUCTION

According to the current trends of technological advancement, electric vehicles (EVs) are proposed as a solution for future transport that promises energy saving and a contribution to reducing greenhouse gases. Indeed, the Global EV outlook 2021 reports that the target sales of light-duty vehicles will rise from 3 million in 2020 to 25 million in 2030 [1]. In this background, EVs create a power demand problem for the grid system. Fortunately, this issue can be

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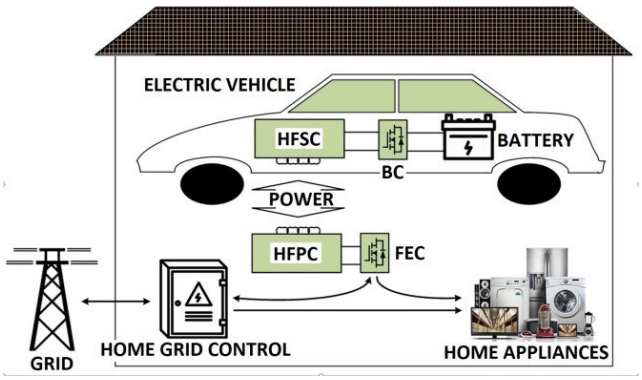

FIGURE 1. BWV2H in the home grid.

overcome by EVs themselves, by exploiting their batteries as energy sources that back up the grid [2], [3].

The conventional battery chargers perform the energy transfer through the plug and socket pair. Plug-in charging has to deal with electrical insulation issues, is uncomfortable in bad weather conditions, such as rain, snow, or ice, and may be viewed with suspicion by people unfamiliar with electrical devices. Nowadays, wireless power transfer (WPT) technology offers an alternative solution for EVs charging. Compared to its wired counterpart, WPT technology has many benefits, such as inherent isolation and prevention from shock, fewer issues due to moisture and dirt, enhanced flexibility, reduced maintenance, and higher user-friendliness [4], [5].

The two main disadvantages of WPT battery chargers lie in their lower efficiency with respect to the conventional ones, and in the electromagnetic emission in the vicinity of the coupling coils [6]. However, both of these issues are not very serious, especially for static applications, such as the one considered in this paper. With a careful design of the coils, the average efficiency during battery charging easily exceeds 90% [7] whilst the chassis of the car operates as an inherent shield against electromagnetic fields [8].

It is well known that generally vehicles are parked for most of the day. This condition gives the opportunity of charging the batteries when the power demand from the grid is low, performing the so-called power shaving. If the battery chargers are enabled to manage a bidirectional power flow, the EVs can be considered both as a load or as an energy source for the grid [9]. Indeed, they can give back the stored energy during peak demand, provided that the battery state of charge is restored before the EVs are used [10], [11], [12], [13]. EVs can support the grid by mitigating the fluctuation of available power inherent to renewable energy sources or regulating the grid frequency [14], [15], [16]. Besides the advantages for the grid, this use of the EVs batteries can generate some economic income for the owners. This power exchange strategy is known as vehicle to grid (V2G) [17], [18].

V2G strategy can be adopted at a smaller scale to counterbalance and settle household needs via smart EV battery charging. This particular application of V2G is denoted as vehicle to home (V2H) [19], [20], [21], [22]. A typical V2H arrangement is shown in Fig. 1. V2H approach helps to shave the daily variable load demand of home appliances, for example, by charging the EV battery during the night, when the domestic power demand is lower. During the day, the stored energy can be injected into the domestic grid whenever the energy demand increases [23], [24], [25], [26].

This paper aims to fully describe the control strategy for a bidirectional wireless battery charger with V2H capability (BWV2H) [2]. The strategy is designed in order to fulfill the requirements of the grid about the maximum exchanged power, and of the battery about the charging and discharging currents and voltages. At the same time, the voltages of the dc buses of the two sections of the BWV2H are prevented from exceeding their designed operating voltages. The overall strategy encompasses eleven different control algorithms organized in two levels that operate in a coordinated manner. The internal level consists of four algorithms that directly interface with the individual static converters that form the BWV2H. The external level encompasses seven algorithms that generate the references for the algorithms of the internal level and are responsible for the consistent operations of the primary and secondary sections of BWV2H. These seven algorithms are divided into three groups: three of them are always enabled, two are enabled only during battery charging, and two operate only during battery discharge.

Each algorithm relies on a simple PI type controller but their accurately designed interactions allow to obtain the correct functioning of the system in all its operating conditions, with a seamless transition from one condition to the other and without the need to resort to more complex solutions. The sizing procedure of each controller is described in detail so that the readers are put in the conditions to design the control system of their own BWV2H starting from its parameters.

In the literature there are numerous papers dealing with this topic, but most of them are focused on a single aspect of the problem, generally the management of the WPT sub-system, while neglecting the need to manage also the interactions with the grid and with the EV battery. Furthermore, very sophisticated control algorithms are often presented without providing the readers with sufficient information to reproduce the published results in their own prototypes. For example, in [27] and [28], the power exchange between the EV battery and another battery installed in the house is considered, but the interaction with the grid and the relevant issues are completely neglected. In the same way there is no description of any control algorithm. Like the previous paper, [11] studies only the power transfer between the dc buses of the BWV2H. It does not handle battery and grid limitations and does not explain regulator sizing. Moreover, it even seems that only one microprocessor is used for controlling both the sections of the system. Paper [29] deals only with the power exchange between the two sections of the BWV2H, in this case using a predictive controller. However, the interface with the grid is not considered and explanations about the generation of the

power reference are not given. Grid interfacing is not covered in [30] either, moreover, the proposed control algorithm does not pass seamlessly from the constant current to the constant voltage battery charging. Paper [31] considers also the topic of interfacing the primary side dc bus with the grid, but limited to the requirement of maintaining a constant dc voltage, without taking in account the grid power limitation. In the same way, the secondary section control algorithm manages the transferred power but entrust to an outer control loop, not considered in the paper, the management of the battery charging. In [32] the issue of exchanging power with the grid is faced and the control of the proposed matrix converter is detailed, however the interaction with the battery is not considered in detail. Like the previous paper, [33] is mainly focused on the active and reactive power exchange with the grid, but there is a lack of detail about the management of the battery charge and the design of the relevant controller.

The BWV2H considered in this paper [2] has been designed by following as closely as possible the indications of the SAE J2954 report [34], which considers only unidirectional WPT systems. The power rating and the requirements of the interface with the grid have been derived from the Italian technical rules (CEI 0-21) [35].

In detail, paper is organized as follows. Section II describes the circuital scheme and the operating principles of the static converters that make up the BWV2H. Section III explains the overall control strategy of the battery charger, defines the functions of the different control algorithms, and analyzes the mechanisms and the consequences of their interactions. Section IV illustrates in detail the development of the individual control algorithms, providing for each of them the block diagram of the complete control loop and the results of preliminary simulations carried out to verify their correct functioning. Section V is dedicated to verifying the functioning of the complete control strategy. It considers both battery charging and discharging and provides a detailed description of the different modes of operation of the BWV2H during these two processes. Section VI concludes the paper. Appendix A gives a list of the abbreviations used through the paper. Appendix B illustrates the flow charts of the control strategy during battery charging and discharging. Appendix C reports the closed loop transfer functions (TFs) of the control loops described in Section IV.

II. CIRCUITAL SCHEME OF THE BWV2H

Fig. 2 shows the circuital scheme of the BWV2H. In the scheme and through the full paper, uppercase letters indicate constant quantities or quantities that vary slowly with respect to the grid frequency, peak amplitudes of alternating quantities, or average values of continuous quantities. Lowercase letters indicate alternating or variable quantities at or above grid frequency.

The BWV2H is interfaced to the domestic grid by means of the front-end converter (FEC) equipped with an inductive input filter denoted as L_G. The FEC absorbs the current i_G from the domestic grid. The phase of i_G with respect to grid voltage v_G is adjusted in order to define the direction of the active power flow and the amount of the reactive power exchanged with the grid, if any. At the output of the FEC the capacitor C_{DCP} sustains the dc bus of the primary section. The continuous voltage V_{DCP}, which can be considered nearly constant, is applied to the input of the high-frequency primary converter (HFPC).

The HFPC generates the quasi-square wave voltage v_{HFP} at the nominal supply frequency of 85 kHz [34], and controls the first harmonic amplitude V_{HFP} of this voltage by adjusting the phase delay between the gate commands of its two legs, according to the phase shift control technique [36]. The HFPC supplies the primary coil and its compensation network, consisting of the capacitor C_P connected in series to the coil and resonating with the coil's self-inductance [34], [37].

Thanks to resonance, the current i_P flowing in the primary coil is practically sinusoidal. It generates a variable magnetic induction flux that links the secondary coil and induces an alternating voltage across its terminals. The induced voltage is the mean by which the power P_{PS} is transferred from the primary to the secondary section of the BWV2H. The series resonant capacitor C_S compensates for the voltage drop originated by the flow of the current i_S through the secondary coil's self-inductance L_S. Consequently, the first harmonic of the voltage v_{HFS} applied across the input of the high-frequency secondary converter (HFSC) is ideally equal to the induced voltage. During the charging operation, the switches T_9-T_{12} of HFSC are not driven, and the current i_S flows through the freewheeling diodes. The alternating component of the rectified current I_{DCS} flows in the capacitor C_{DCS}. The average component of I_{DCS}, denoted as I_{BC}, is suitably conditioned by the bidirectional chopper (BC) and originates the current I_B that charges the battery. The capacitor C_{DCS} is sized so that the dc bus voltage V_{DCS} of the secondary section of the BWV2H can be considered constant. In the hypothesis that i_S flows for the whole supply period alternatively across the pairs of diodes D_9-D_{12} and D_{10}-D_{11}, from the constant value of V_{DCS} it derives that v_{HFS} actually have a square waveform.

In order to reverse the direction of the power flow, i.e. to transfer the power P_{SP} from the EV battery to the grid, it is sufficient to adjust the current references provided to the control loops of FEC and BC and to mutually exchange the control strategies of HFPC and HFSC. In this way, the HFPC behaves as a high frequency diode rectifier whilst the HFSC operates as a high frequency inverter.

III. CONTROL STRATEGY OF THE BWV2H

A. CONTROL ALGORITHMS OF THE INTERNAL AND EXTERNAL LEVEL

The control strategy developed for the BWV2H relies on a number of control algorithms that cooperate to maintain the system in the required operating conditions. The names and the characteristics of the algorithms are summarized

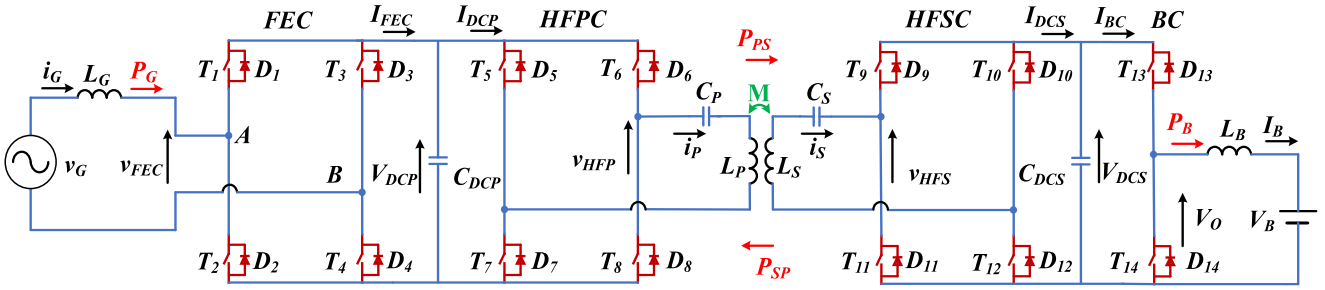

FIGURE 2. Circuital scheme of the BWV2H.

TABLE 1. Control Algorithms of the BWV2H.

Action carried out	Name	Controlled quantity	Manipulated quantity	Level	Active	Controller's TF	Subsection
Grid current control	AL_i_G_B	i_G	v_{FEC}	Internal	Both	$C_{iG,VFEC}(s)$	IV.B.1
Secondary coil current control	AL_I_S_C	I_S	v_{HFP}	Internal	Charge	$C_{IS,VHFP}(s)$	IV.B.2
Primary coil current control	AL_I_P_D	I_P	v_{HFS}	Internal	Discharge	$C_{IP,VHFS}(s)$	IV.B.3
Battery current control	AL_I_B_B	I_B	V_O	Internal	Both	$C_{IB,VO}(s)$	IV.B.4
V_{DCP} voltage regulation	AL_V_{DCP}_B	V_{DCP}	P_G (i_G)	External	Both	$C_{VDCP,PG}(s)$	IV.C.1
V_{DCP} voltage regulation	AL_V_{DCP}_C	V_{DCP}	P_{PS} (I_S)	External	Charge	$C_{VDCP,PPS}(s)$	IV.C.2
V_{DCP} voltage regulation	AL_V_{DCP}_D	V_{DCP}	P_{SP} (I_P)	External	Discharge	$C_{VDCP,PSP}(s)$	IV.C.3
V_{DCS} voltage regulation	AL_V_{DCS}_B	V_{DCS}	P_B (I_B)	External	Both	$C_{VDCS,PB}(s)$	IV.C.4
V_{DCS} voltage regulation	AL_V_{DCS}_C	V_{DCS}	P_{PS} (I_S)	External	Charge	$C_{VDCS,PPS}(s)$	IV.C.5
V_{DCS} voltage regulation	AL_V_{DCS}_D	V_{DCS}	P_{SP} (I_P)	External	Discharge	$C_{VDCS,PSP}(s)$	IV.C.6
V_B voltage regulation	AL_V_B_B	V_B	P_B (I_B)	External	Both	$C_{VB,PB}(s)$	IV.C.7

in Tab. 1. Each algorithm is denoted as "AL_X_Y", where "AL" stands for "algorithm", "X" denotes the controlled quantity and "Y" specifies when the algorithm is enabled, i.e. during the charge of the battery ("C"), during its discharge ("D"), or during both the operations ("B"). Each control algorithm controls a quantity by manipulating another one. The TF of the controller designed for each algorithm are denoted as $C_{X,Z}(s)$, where X specifies the controlled quantity and Z the manipulated one. Their names are listed in the second last column of Tab. 1. The algorithms are organized in two levels, i.e., internal and external. The quantities manipulated by the algorithms of the external level are indirectly used as references for quantities controlled by the algorithms of the internal level. The algorithms of the external level control the voltages of the two dc busses and of the battery. To this end, they generate the references for the power P_{PS} and P_{SP}, exchanged between the two sections of the BWV2H, for the power P_B, which is injected into the battery, and for the power P_G, which is absorbed from the grid. The algorithms of the internal level are designed to control the currents i_G, I_B, and the amplitudes I_P and I_S of the currents i_P and i_S. For this reason, the power references generated by the external level are manipulated exploiting simple relationships to convert them into the current references required by the algorithms of the internal level. These current references are listed within parentheses in Tab. 1.

The internal level algorithms compute the references for the voltages v_{FEC}, v_{HFP}, v_{HFS}, and V_O that must be generated by the static converters that compose the BWV2H. The gate commands for the static switches of the converters are obtained from the respective voltage references by means of the conventional techniques of PWM or phase shift.

In the external level there are seven algorithms. The always-on algorithms AL_V_B_B, AL_V_{DCS}_B,and AL_V_{DCP}_B are dedicated respectively to controlling the voltages across the battery and the capacitors C_{DCS} and C_{DCP}. The first two algorithms manipulate the power P_B exchanged with the battery while the third one manipulates the power P_G absorbed by the grid. Algorithms AL_V_{DCS}_C and AL_V_{DCP}_C are active during battery charging. They control the voltages across the capacitors C_{DCS} and C_{DCP} at a constant value by acting on P_{SP} through the amplitude I_S of i_S. The algorithms AL_V_{DCS}_D and AL_V_{DCP}_D are active during battery discharging and control the same voltages V_{DCS} and V_{DCP}, but this time acting on P_{SP} through I_P. The action of the algorithms activated during battery charging or discharging overlaps that of the two always-on algorithms that generate the references for P_B and P_G. For example, during the battery charging, both AL_V_{DCS}_B and AL_V_{DCS}_C control V_{DCS} by manipulating P_B and P_{PS} through I_B and I_S.

In a real application, a battery management system controls the battery voltage during the charge and monitors it during the discharge. However, in order to complete the design of the control strategy of the BWV2H and to simulate its operation

in all the working conditions, in the following discussion the functions of the battery management system are assigned to AL_V_B_B. By manipulating I_B, it takes care that the battery is initially charged at the constant current and then at the constant voltage specified by the manufacturer. Moreover, it takes care that the battery is discharged without exceeding the maximum current and the minimum voltage.

The implementation of the internal level algorithms requires to transduce and acquire the currents i_G, i_P, i_S, and I_B. In addition, the grid voltage v_G must be transduced to allow controlling the phase of the current i_G. The external level algorithms require the transduction and acquisitions of the voltages V_B, V_{DCS}, V_{DCP}. The signals obtained from the circuitry that transduces I_B, i_g, v_g, V_B, V_{DCS}, and V_{DCP} are processed by an analog low pass filter (LPF). Finally, they are acquired by the micro controllers that implement the control strategy.

The subsections related to the design of the different controllers are listed in the last column of Tab. 1.

B. INTERACTIONS BETWEEN THE CONTROL ALGORITHMS OF THE BWV2H

The functioning of the BWV2H requires to simultaneously satisfy specifications relevant to its primary and secondary sections, such as those about to the voltages across C_{DCP} and C_{DCS}. At the same time, the operating limits imposed by the grid and the battery must be respected. Consequently, it is not possible to entrust the control of the system to algorithms that operate independently. For this reason, the algorithms reported in Tab. 1 interact with each other to obtain the desired overall behavior.

Two types of interactions are exploited in designing the control strategy. In the first type of interaction, two algorithms control the same quantity but generate the references for two different quantities. This is the case, for example, of AL_V_{DCS}_C and AL_V_{DCS}_B that control V_{DCS} during battery charging. AL_V_{DCS}_C brings V_{DCS} towards a reference value $V_{DCS,ref,high}$ generating the reference for the transferred power P_{PS}, which in turn depends on I_S. Instead, AL_V_{DCS}_B brings V_{DCS} towards a lower value $V_{DCS,ref,low}$ generating the reference for the power P_B from which $I_{B,ref}$ is derived. The interaction between the two algorithms ensures that in steady state V_{DCS} is always between the lower and upper references and that both I_S and I_B are controlled.

The second type of interaction occurs when two algorithms control different quantities but generate the reference for the same one. This happens, for example, in the case of AL_V_{DCS}_B and AL_V_B_B. AL_V_{DCS}_B controls V_{DCS} while AL_V_B_B controls V_B, but both of them compute the reference $P_{B,ref}$ for the power P_B injected in the battery. The lower of the two references is sent to AL_I_B_B of the internal level, so as to avoid both the battery overload and the excessive discharge of C_{DCS}. As can be deduced from the two examples, it may happen that the same control algorithm, such as AL_V_{DCS}_B, has two interactions of different types with two other algorithms.

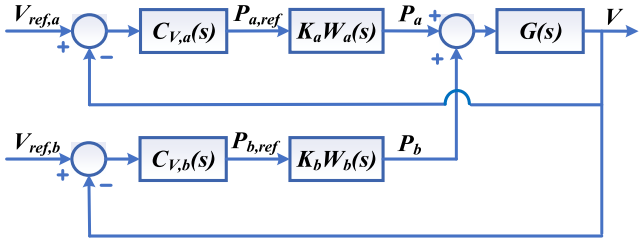

FIGURE 3. Block diagram of interaction of first type between two control loops.

From the description given above, it derives that the actions of the various algorithms are closely coordinated without requiring to exchange a large amount of data between them. Indeed, as it will be explained in subsections IV-B2 and IV-C2, during battery charging only the error on the amplitude I_S and the reference for P_{PS} are exchanged between the two sections of the BWV2H. During discharging the exchanged variables are the reference for P_{PS} and the error on I_P. This feature is very appreciable in WPT systems since the control algorithms are implemented by different microprocessors, installed on the two sections of the system which are electrically and physically separated. The data exchange is then carried out by means of suitable communication systems. These additional devices are not required in the case of other types of battery chargers since, even in the insulated ones, the entire control strategy can be implemented by a single microprocessor.

The approach based on the two levels and on the interactions allows to design independently the algorithms, provided that their passbands are compatible. The implementation of the second type of interaction simply requires to select between the two references provided at the output of the interacting algorithms. Instead, in order to implement effectively an interaction of the first type, the two interacting algorithms must be properly designed, as it will be explained in the next subsection.

C. INTERACTIONS OF THE FIRST TYPE

Interaction of the first type between two algorithms of the external level can be represented as in Fig. 3. One single voltage, denoted as V, is controlled by two separate control loops that manipulate two different power, denoted as P_a and P_b. P_a and P_b are injected or extracted from a capacitor that constitutes the controlled plant G(s). The two controllers $C_{V,a}(s)$ and $C_{V,b}(s)$ try to force V to follow the references $V_{ref,a}$ and $V_{ref,b}$, respectively, and generate the references $P_{a,ref}$ and $P_{b,ref}$. The power references are processed by closed control loops that generate the actual power P_a and P_b. The power control loops are represented by their steady state gain, denoted as K_a and K_b, followed by the TFs $W_a(s)$ and $W_b(s)$, which have unitary gain and account for the poles and the zeros of the control loops.

By defining the quantity

$$\Delta V_{ref} \triangleq V_{ref,a} - V_{ref,b}, \tag{1}$$

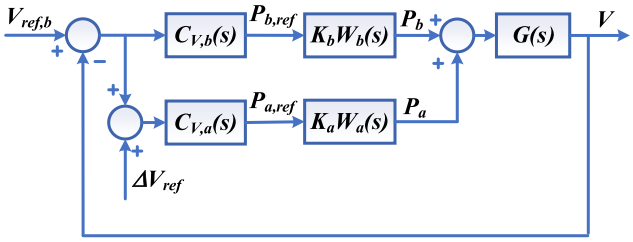

FIGURE 4. Redrawn block diagram of interaction of first type.

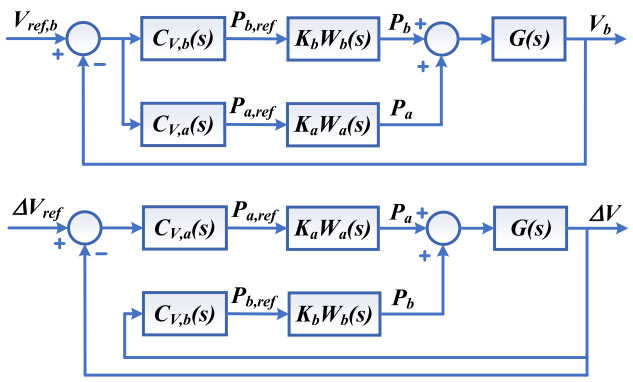

FIGURE 5. Independents loops equivalent to an interaction of the first type.

the diagram of Fig. 3 can be redrawn as in Fig. 4. Then it is modified as in Fig. 5, where the two inputs $V_{ref,b}$ and ΔV_{ref} are processed by two independent loops. The sum of the two quantities V_b and ΔV generated by the independent loops gives V.

It can be reasonably assumed that the joint action of the controllers $C_{V,a}(s)$ and $C_{V,b}(s)$ brings V_b to the reference value $V_{b,ref}$ since, as shown in the upper half of Fig. 5, they work together to achieve this result.

In order to determine the outcome of the control action of the other loop, the TF from ΔV_{ref} to ΔV must be computed. At first, the TF from P_a to ΔV of the inner loop of the block diagram of Fig. 5 is worked out as

$$G_{P_a,\Delta V}(s) = \frac{G(s)}{1 + G(s)\, C_{V,b}(s)\, K_b W_b(s)}. \tag{2}$$

Then, the complete TF from P_a to ΔV is derived as

$$G_{\Delta V_{ref},\Delta V}(s) = \frac{G_{P_a,\Delta V}(s)\, C_{V,a}(s)\, K_a W_a(s)}{1 + G_{P_a,\Delta V}(s)\, C_{V,a}(s)\, K_a W_a(s)}, \tag{3}$$

which, by using (2) and after some manipulations, gives

$$G_{\Delta V_{ref},\Delta V}(s) = \frac{C_{V,a}(s)\, K_a W_a(s)}{1/G(s) + C_{V,a}(s)\, K_a W_a(s) + C_{V,b}(s)\, K_b W_b(s)}. \tag{4}$$

By approximating $W_a(s)$ and $W_b(s)$ with TFs of the first order, (4) can be rewritten as

$$G_{\Delta V_{ref},\Delta V}(s) = \frac{C_{V,a}(s)\, K_a \frac{1}{1+s\tau_a}}{1/G(s) + C_{V,a}(s)\, K_a \frac{1}{1+s\tau_a} + C_{V,b}(s)\, K_b \frac{1}{1+s\tau_b}}, \tag{5}$$

and applying the final value theorem, the response ΔV to a step reference of amplitude ΔV_{ref} is

$$\Delta V = \lim_{s\to 0} s \frac{\Delta V_{ref}}{s} \frac{C_{V,a}(s)\, K_a}{1/G(s) + C_{V,a}(s)\, K_a + C_{V,b}(s)\, K_b}. \tag{6}$$

Equation (6) shows that ΔV does not depend on the time constants of the control loops $W_a(s)$ and $W_b(s)$ but on their gains K_a and K_b, on the controllers $C_{V,a}(s)$ and $C_{V,b}(s)$, and on G(s).

Considering that G(s) has an integral action, and hence

$$\lim_{s\to 0} \frac{1}{G(s)} = 0, \tag{7}$$

if $C_{V,a}(s)$ and $C_{V,b}(s)$ are both of proportional type with gains $K_{P,a}$ and $K_{P,b}$, (6) gives

$$\Delta V = \Delta V_{ref} \frac{K_{P,a} K_a}{K_{P,a} K_a + K_{P,b} K_b}. \tag{8}$$

Equation (8) shows that ΔV reaches a constant value different from ΔV_{ref}. Consequently, at steady state P_a is different from zero and, given that ΔV is constant, by the lower half of Fig. 5 it must be $P_b = -P_a$.

Analysis of the lower half of Fig. 5 and the use of (8), at steady state gives

$$P_a = (\Delta V_{ref} - \Delta V) K_{P,a} = \Delta V_{ref} K_{P,a} \frac{K_{P,b} K_b}{K_{P,a} K_a + K_{P,b} K_b}. \tag{9}$$

This condition is not enough to operate effectively the BWV2H because the power P_a transferred through its sections is defined by the gains of the controller whilst it should be limited only by and the capabilities of the battery and of the grid.

The use of proportional integral (PI) controllers gets rid of this limitation. The TF between the error e(t) at the input of a PI controller and the manipulated quantity y(t) at its output is given by (10) in terms of the proportional gain K_P and the integral time constant τ_I

$$C(s) \triangleq \frac{Y(s)}{E(s)} = K_P \left(\frac{1 + s\tau_I}{s\tau_I} \right). \tag{10}$$

In this case, instead of (8), (11) is derived

$$\Delta V = \Delta V_{ref} \frac{K_{P,a} K_a \tau_b}{K_{P,a} K_a \tau_b + K_{P,b} K_b \tau_a}, \tag{11}$$

where τ_a and τ_b are the time constants of the PI controllers $C_{V,a}(s)$ and $C_{V,b}(s)$, and $K_{P,a}$ and $K_{P,b}$ are their gains.

Also in this case a steady state error remains, however, thanks to the integral action of $C_{V,a}(s)$, P_a increases while

$C_{V,b}(s)$ maintains the relation $P_b = -P_a$. This relation assures that, when P_a is clamped at its extreme value compatible with the operations of the BWV2H, P_b is limited as well. This inherent power limitation happens even if the roles of P_a and P_b are exchanged.

IV. CONTROL ALGORITHMS DESIGN

A. DESIGN AND DISCRETIZATION OF THE BWV2H CONTROLLERS

As a general approach, the controllers of the algorithms of the internal and external levels are based on the PI architecture and are designed by imposing the phase margin M_ϕ and the passband angular frequency ω_{PB} of the control loop.

From (10) it derives that the controller's time constant must satisfy the condition

$$atan\left(\omega_{PB}\tau_I\right) - \frac{\pi}{2} = -arg\left[Sys\left(j\omega_{PB}\right)\right] - \pi + M_\phi, \quad (12)$$

where the left-hand terms give the phase at the passband angular frequency of the TF of the PI. On the right-hand side, $\arg[Sys(j\omega_{PB})]$ is the phase of the system to be controlled and the sum $(-\pi + M_\phi)$ is the required phase of the controlled open loop system at $\omega = \omega_{PB}$. From (12), the time constant τ_I is worked out as

$$\tau_I = \frac{1}{\omega_{PB}} tan\left(-\frac{\pi}{2} - arg\left[Sys\left(j\omega_{PB}\right)\right] + M_\phi\right). \quad (13)$$

The assumption, usually taken, that the passband of the closed-loop TF corresponds to the cut-off frequency of the open-loop TF, leads to the relation

$$K_P \left|\frac{1 + j\omega_{PB}\tau_I}{j\omega_{PB}\tau_I}\right| \left|Sys\left(j\omega_{PB}\right)\right| = 1, \quad (14)$$

where the operator $|\cdot|$ denotes the magnitude of its argument.

By substituting (13) into (14) it is possible to work out τ_I and K_P as functions of the system TF and of the required ω_{PB} and M_ϕ. Finally, the integral gain K_I of the controller is expressed as

$$K_I = \frac{K_P}{\tau_I}. \quad (15)$$

The controllers are designed in the continuous-time domain according to (13) and (14), but bearing in mind that they will be implemented in a discrete-time system with sampling period T. To this end, a block representing the sampling delay has been inserted in series to the system to be controlled before designing the controller. This block, which in the discrete-time domain is represented by the "z^{-1}" operator, in the continuous-time domain is modelled using

$$SD\left(s\right) = \frac{1 - s\frac{T}{2}}{1 + s\frac{T}{2}}, \quad (16)$$

derived by inversion of the Tustin discretization method by which the "s" and the "z^{-1}" operators are linked according to

$$s \Rightarrow \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}}, \quad (17)$$

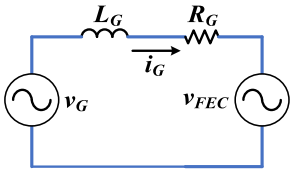

FIGURE 6. Equivalent scheme of the system to be controlled.

After computing K_P and K_I, the controller is discretized using the Tustin method obtaining (18), which links the present value of the controller's output to its previous sample and to the present and previous samples of the error signal.

$$Y\left(k\right) = Y\left(k-1\right) + K_{e(k)}e\left(k\right) + K_{e(k-1)}e\left(k-1\right). \quad (18)$$

The gains $K_{e(k)}$ and $K_{e(k-1)}$ are given by the equations

$$K_{e(k)} = \left(K_I\frac{T}{2} + K_P\right) \quad (19)$$

$$K_{e(k-1)} = \left(K_I\frac{T}{2} - K_P\right). \quad (20)$$

B. INTERNAL LEVEL ALGORITHMS

1) AL_I_G_B: CONTROL OF THE GRID CURRENT

AL_i_G_B acquires the reference $i_{G,ref}$, generated by AL_V_{DCP}_B, computes the reference for the voltage v_{FEC} to be generated at FEC input, and finally generates the gate commands for the FEC as a function of $v_{FEC,ref}$ and of the measured dc voltage V_{DCP}.

The system to be controlled consists of the filter inductance L_G placed at the FEC input and its serially connected parasitic resistance R_G. The grid voltage v_G acts as an external disturbance. The scheme of the controlled system is shown in Fig. 6. Its TF is

$$G_{iG}\left(s\right) = \frac{1}{sL_G + R_G} \quad (21)$$

and the block diagram of the relevant control loop is shown in Fig. 7.

The controller $C_{iG,VFEC}(s)$ processes the error on i_G and generates $v_{FEC,ref}$. Within one sampling delay the voltage reference is converted into the command signals for the power switches of the FEC and v_{FEC} is generated at its input. In the feedback path, the first order TF, given by (22) and having a cutoff frequency of 10 kHz, is inserted to represent the LPF that attenuates the high-frequency components of the signal coming from the transducer of i_G.

$$LPF\left(s\right) = \frac{1}{s\tau_{LPF} + 1}. \quad (22)$$

The supply frequency of the coupled coils is standardized at 85 kHz [34]. Nevertheless, the outputs of the control algorithms are updated once every four supply periods of the HFPC in order to allow the microcontroller enough processing time. Hence, the output of the discretized version of $C_{iG,VFEC}(s)$ is updated every 45 μs. For reasons related to the simplicity of the implementation of the control loops and to

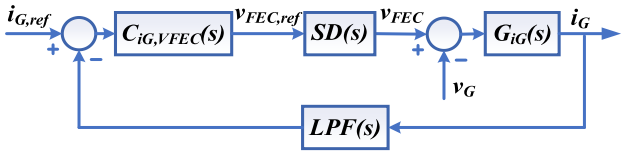

FIGURE 7. Block diagram of the control loop of AL_i_G_B.

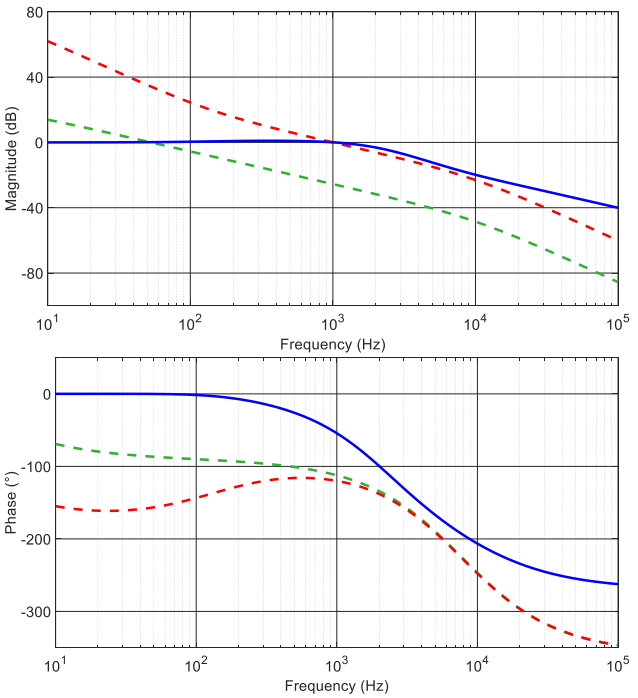

FIGURE 8. Bode diagrams relevant to AL_i_G_B. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

TABLE 2. Specifications of the BWV2H.

Parameters	Symbol	Value
Grid power	P_G	3300 W
Grid Peak Voltage	V_G	358 V
Grid Current	i_G	22.6 A
Battery Maximum voltage	$V_{B,M}$	120 V
Battery Minimum voltage	$V_{B,m}$	65 V
Battery current (charging)	$I_{B,C}$	37.4 A
Battery current (discharging)	$I_{B,D}$	50 A
Grid side inductance	L_G	3 mH
DC Primary Capacitor	C_{DCP}	1.21 mF
Primary & Secondary Inductance	$L_P = L_S$	220 µH
Primary & Secondary Capacitor	$C_P = C_S$	15.9 nF
DC Secondary Capacitor	C_{DCS}	540 µF
Battery side inductor	L_B	260 µH
Battery nominal charging current	$I_{B,C,N}$	37.4 A
Battery series resistance	$R_{B,ESR}$	0.1 Ω

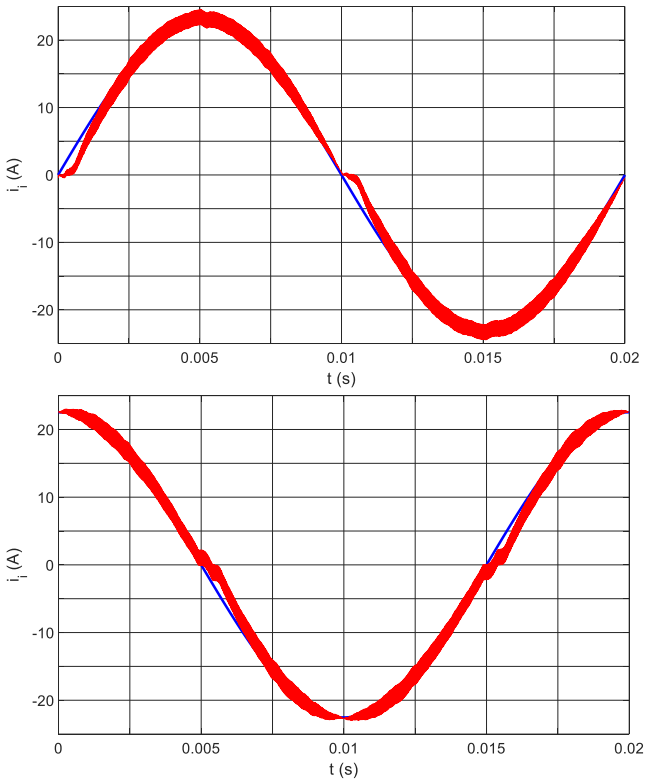

FIGURE 9. AL_i_G_B resposes. Top: $i_{G,ref}$ (blue) and i_G (red) with $i_{G,ref}$ in phase to v_G. Bottom: $i_{G,ref}$ (blue) and i_G (red) with $i_{G,ref}$ leading v_G of $\pi/2$ rad.

the reduction of the power losses, the switches of the FEC commutate with the same period, i.e., at 21.25 kHz. Given the sampling frequency above 20 kHz and the requirement of generating a sinusoidal current at 50 Hz, it is reasonable to set the passband ω_{PB} of the control loop to 1 kHz and the phase margin M_ϕ to 70°. This selection of M_ϕ gives a quick response, but causes an overshoot when a stepwise reference is applied. However, it must be remembered that $i_{G,ref}$ is sinusoidal, so this problem does not arise in the considered application.

The PI controller $C_{iG,VFEC}(s)$ has been designed by applying the procedure reported in the subsection IV-A to the system constituted by the cascade of $G_{iG}(s)$, SD(s), and LPF(s). The closed loop TF obtained from the block diagram of Fig. 7 is reported by (A1) in Appendix C.

Considering a BWV2H having the parameters reported in Tab. 2 [2], the uncontrolled system has the magnitude and phase Bode diagrams plotted with the dashed green line in Fig. 8. The Bode diagrams of the open-loop controlled system are drawn with the dashed red line, while that of the closed-loop controlled system is shown by the solid blue line. The analysis of the diagrams confirms that $C_{iG,VFEC}(s)$ successes in imposing the required bandwidth and phase margin.

The controller has been discretized according to (16)-(19) and inserted in a circuital model developed using Simulink version 10.5 with the toolbox Simscape Electrical version 7.7, running in the Matlab 9.12 environment. In this simulation, and in all the other considered in this Section, the maximum integration step has been set to 0.1 μs.

In order to limit the ripple of the current i_G, the power switches of the FEC are controlled using the bipolar technique. Fig. 9 shows two examples of i_G waveforms obtained

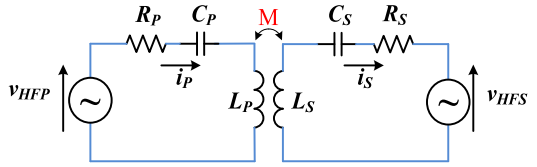

FIGURE 10. Equivalent circuit of the coupled coils.

from the circuital simulation. The top half of Fig. 9 considers the situation where $i_{G,ref}$ is in phase with v_G while the bottom half refers to the condition where $i_{G,ref}$ leads v_G by $\pi/2$ rad. In both cases, i_G follows its reference accurately and L_G demonstrates its effectiveness in containing the current ripple. Distortions in the current waveforms around the zeros of i_G are due to the dead times, equal to 1μs, inserted in the power switches commutations.

2) AL_I_S_C: CONTROL OF THE AMPLITUDE OF THE SECONDARY COIL CURRENT DURING BATTERY CHARGING

When the power flows from the grid to the battery, HFPC acts as an inverter, and its gate commands are generated by AL_I_S_C. Instead, HFSC is not controlled and operates as a diode rectifier. Thanks to the series resonance, the first harmonic components of the HFPC output voltage v_{HFP} is about equal to the voltage induced across the primary coil. Consequently, the amplitude of v_{HFP} is proportional to that of the current i_S flowing in the secondary coil. Based on this condition, during the battery charging, AL_I_S_C manipulates v_{HFP} to control I_S.

The TF from the first harmonic of v_{HFP} to i_S is obtained by solving the mesh equations of the equivalent circuit of the coupled coils sketched in Fig. 10. Considering the primary and the secondary sections, the following expressions are derived.

$$\begin{aligned} V_{HFP}(s) &= \left(R_P + \frac{1}{sC_P} + sL_P\right) I_P(s) + sMI_S(s) \\ sMI_P(s) &= \left(R_S + \frac{1}{sC_S} + sL_S\right) I_S(s), \end{aligned} \tag{23}$$

obtained by using the complex variable "s" instead of "jω" in representing the reactive components of the circuit.

From (23), the link between $V_{HFP}(s)$ and $I_S(s)$ is written as

$$V_{HFP}(s) = \frac{\left(R_P + \frac{1}{sC_P} + sL_P\right)\left(R_S + \frac{1}{sC_S} + sL_S\right) + s^2M^2}{sM} I_S(s). \tag{24}$$

With some simple manipulations, from (24) the TF from $V_{HFP}(s)$ to $I_S(s)$ is obtained as

$$G_{v_{HFP},i_S}(s) = \frac{MC_SC_Ps^3}{D_4s^4 + D_3s^3 + D_2s^2 + D_1s + 1}. \tag{25}$$

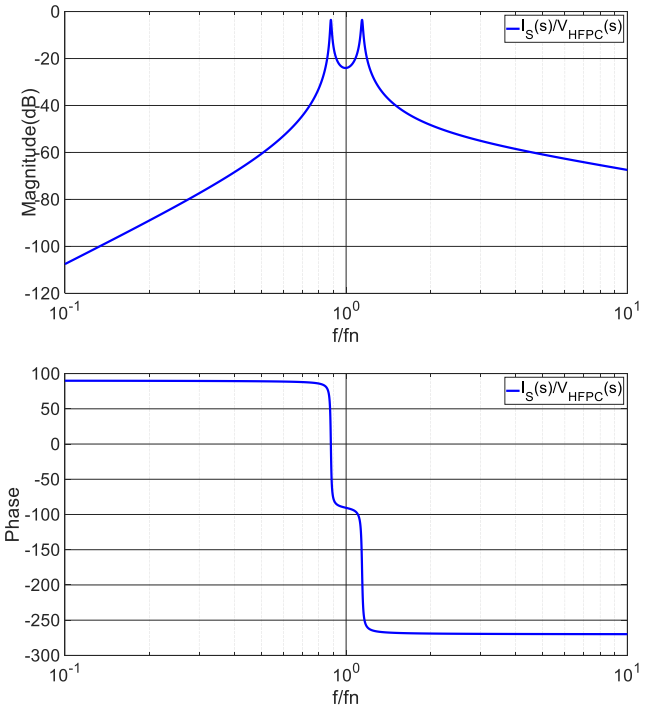

FIGURE 11. Bode diagrams of $G_{vHFP,iS}(s)$.

The coefficients of the denominator of $G_{vHFP,iS}(s)$ are equal to

$$\begin{aligned} D_4 &= C_SC_PL_SL_P + C_SC_PM^2 \\ D_3 &= C_SC_PL_SR_P + C_SC_PL_PR_S \\ D_2 &= C_SL_S + C_PL_P + C_SC_PR_SR_P \\ D_1 &= C_SR_S + C_PR_P \end{aligned} \tag{26}$$

The Bode diagrams of $G_{vHFP,iS}(s)$ are plotted in Fig. 11.

Generally speaking, it is reasonable to assume that the sampling and processing frequency of AL_i_S_C is at most equal to the supply frequency of the coils. In the considered application, it is even a submultiple. Consequently, it is not possible to control the actual waveform of i_S but only its amplitude I_S, relying on the filtering effect of the compensation network to enforce the current to maintain an almost sinusoidal waveform.

On the other hand, v_{HFP} cannot be freely manipulated. Instead, only the amplitude V_{HFP} of its first harmonic component is directly affected by the phase shift technique applied to HFPC. Then, the TF $G_{vHFP,iS}(s)$ is not useful in designing the controller of AL_I_S_C and must be substituted for by the TF from V_{HFP} to I_S. It can be demonstrated [38] that, if the bandwidth of the variations of V_{HFP} is much smaller than the supply frequency and the amplitude Bode diagram of $G_{vHFP,iS}(s)$ is smooth enough around the supply frequency, as it happens in the considered case, then the TF that links V_{HFP} to I_S can be approximated by the gain of $G_{vHFP,iS}(s)$ computed at the supply frequency ω_{HF}, i.e. by

$$K_{V_{HFP},I_S} = \frac{1}{\omega_{HF}M}, \tag{27}$$

with the parameters of Tab. 2, it results $K_{VHFP,IS} = 0.083$.

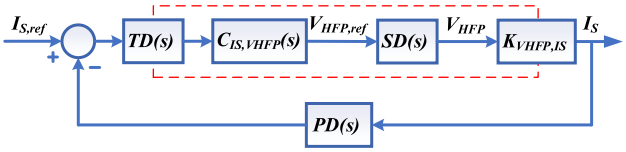

FIGURE 12. Block diagram of control loop of AL_I_S_C.

When designing the controller of I_S, it must be remembered that the computation of $I_{S,ref}$ and the transduction of I_S are performed in the secondary section of the BWV2H, whilst the manipulated voltage v_{HFP} is related to the primary section. It is therefore necessary to set up a communication channel between the two sections. A viable solution is to employ a pair of radio transceivers operating on the industrial, scientific and medical (ISM) band. It is reasonable to assume a refresh period of the transmitted data of 1 ms.

The block diagram of the control loop of I_S is shown in Fig. 12. The blocks within the dashed red rectangle are located on the primary section of the BWV2H whilst the others are on the secondary section. The blocks crossed by the rectangle interface the two sections: $K_{VHFP,IS}$ approximates the TF from V_{HFP} to I_S whilst TD(s) represents the delay due to data transmission. Its TF is equal to (16) but the delay is T_D instead of T. The blocks SD(s) and $C_{IS,VHFP}(s)$ represent the microprocessor delay and the controller, respectively. Like in the previous subsection, SD(s) is computed supposing that the sampling frequency of the microcontroller is one fourth of the HFPC switching frequency. The amplitude I_S is obtained by processing the signal coming from the transduction of i_S using an analog peak detector with a bandwidth of 10 kHz [38]. It is represented by the PD(s) block in the feedback path of the diagram of Fig. 12. Its TF is equal to (22) but with the time constant τ_{PD} instead of τ_{LPF}.

The Bode diagrams of the open-loop system without the controller, obtained using the parameters from Tab. 2, are plotted with the dashed green line in Fig. 13. Initially, $C_{IS,VHFP}(s)$ has been designed as a PI controller, sizing its gains in order to obtain a control loop with a bandwidth of 50 Hz and a phase margin of 80°. However, the obtained closed-loop gain at high frequencies was not effectively attenuated, and undue oscillations occurred in the system response. To prevent this issue, the controller architecture has been modified by inserting an additional pole at a frequency of 2 kHz. The pole has been considered part of the forward path of the system to be controlled, and the gains of $C_{IS,VHFP}(s)$ have been computed again to maintain the same bandwidth and phase margin. The Bode diagrams of the open-loop and closed-loop systems with the enhanced controller are shown in Fig. 13 using the dashed red line and the solid blue line, respectively.

Once computed $V_{HFP,ref}$, the phase shift angle between the gate commands of the legs of the HFPC is obtained as [36]

$$\alpha = 2arcsin\left(\frac{\pi}{4}\frac{V_{HFPC,ref}}{V_{DCP}}\right). \tag{28}$$

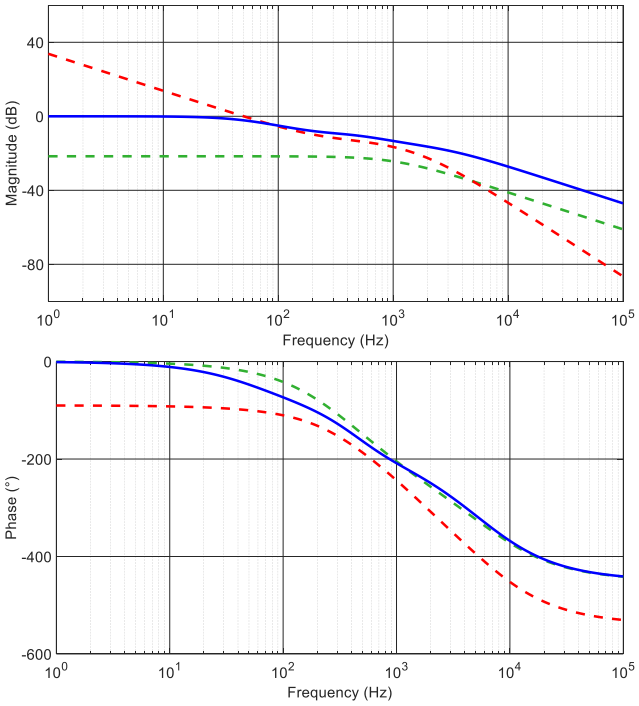

FIGURE 13. Bode diagrams relevant to AL_I_S_C. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

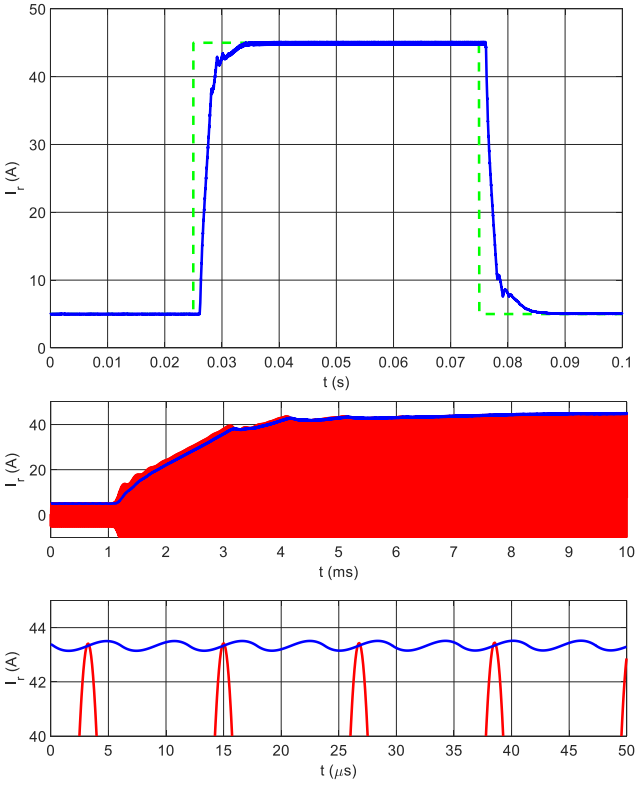

FIGURE 14. AL_I_S_C responses. Top: $I_{S,ref}$ (dashed green) and I_S (blue). Bottom: i_S (red) and I_S (blue) during transient and their magnifications.

The discrete version of the controller has been inserted into a simulation along with a circuital model of the HFPC and of the coupled coils to check the performance of the control

algorithm. The response to an $I_{S,ref}$ step from 1A to 15 A has been simulated, obtaining the plots reported in Fig. 14. The solid blue line represents I_S obtained at the output of PD(s). It can be seen that the control loop reaches the steady state in about 30 ms without any overshoot, even if a small oscillation is superimposed on the response. The bottom half of Fig. 14 shows the waveforms of i_S and I_S up to 10 ms after the reference step. Because of its high frequency, at the time scale of the figure, i_S appears as a solid red area with I_S following its envelope. It is worth highlighting that the peak detector operates accurately only at steady state and if i_S is sinusoidal. During the transient, these conditions are not satisfied and this explains why, in the first 5 ms after the reference step, the correspondence between I_S and the actual amplitude of i_S is not perfect. The magnification of the figure, which is relevant to the steady state condition, shows that I_S tracks the amplitude of i_S accurately even if some oscillation at twice the supply frequency can be found.

3) AL_I_P_D: CONTROL OF THE AMPLITUDE OF THE PRYMARY COIL CURRENT DURING BATTERY DISCHARGING

When the power flows from the battery to the grid, the functions of the two power converters are exchanged. AL_I_P_D generates the gate commands for HFSC while the power switches of HFPC are not commanded. In this case, the reference $I_{P,ref}$ and the transduction of I_P are performed in the primary section of the BWV2H, whilst the manipulated voltage v_{HFS} is generated in the secondary section. Hence, like in the previous subsection, the use of the radio transceiver and the relevant refresh period of 1ms must be considered in designing the controller. From the symmetry of Fig. 10 and of (24)-(26) it derives that the TF $G_{vHFS,iP}(s)$ from the voltage v_{HFS} to the current i_P is the same as $G_{vHFP,iS}(s)$, given by (25). Consequently, the gain $K_{VHFS,IP}$ from the amplitude of v_{HFS} to the amplitude of i_P is equal to $K_{VHFP,IS}$, given by (27).

Given these symmetries, the design procedure of $C_{IP,VHFS}(s)$ is the same as that described for $C_{IS,VHFP}(s)$ in the previous subsections. The results obtained from the simulation of this control loop are reported in Fig. 15. It clearly appears that the responses are quite similar to those relevant to AL_I_S_C.

4) AL_I_B_B: CONTROL OF THE BATTERY CURRENT

The battery current control loop has the structure shown in Fig. 16. It is the same reported in Fig. 7 and relevant to the control loop of i_G. In this case, the battery plays the role of the grid and the BC acts as the FEC. AL_I_B_B controls the battery current I_B both during the charging and discharging of the battery and acts on the gate commands of the switches of the BC to manipulate its average output voltage V_O. The reference current $I_{B,ref}$ is provided by selecting the one with the smallest magnitude between the outputs of the interacting algorithms AL_V_B_B and AL_V_{DCS}_B.

The system $G_{IB}(s)$ to be controlled consists of the L_B filter inductor placed at the output of the BC and of the battery parasitic series resistance $R_{B,ESR}$. The battery voltage acts as a disturbance. The inductor has the twofold function of attenuating the high-frequency harmonics of I_B, and of decoupling the square wave voltage v_O from the slowly variable battery voltage V_B. In the feedback path, the LPF is inserted to attenuate the high-frequency components of the signal taken from the battery current transducer.

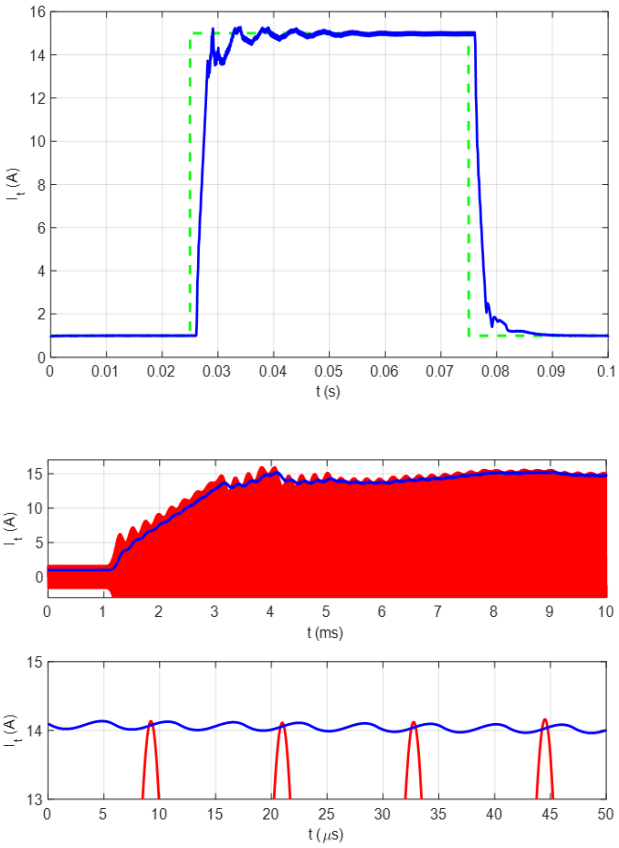

FIGURE 15. AL_I_P_D responses. Top: $I_{P,ref}$ (dashed green) and I_P (blue). Bottom: i_P (red) and I_P (blue) during transient and their magnifications.

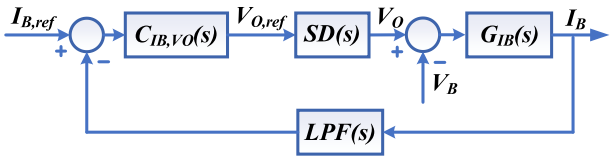

FIGURE 16. Block diagram of the control loop of AL_I_B_B.

To verify the operation of the BC in all operating conditions and to reduce the simulation time, the battery was modeled using the capacitor C_{eq} and its series resistance $R_{B,ESR}$. The capacity of 6.8 F has been selected for C_{eq} by imposing that the voltage across its terminals changes from the minimum battery voltage $V_{B,m}$ to the maximum battery voltage $V_{B,M}$ in 10 s when the charging current is at the nominal value $I_{B,C,N}$.

The controller was designed imposing a bandwidth of 1 kHz and adjusting the phase margin around 70° until a satisfactory response is obtained. Fig. 17 shows the Bode diagrams of the system without the controller, of the system

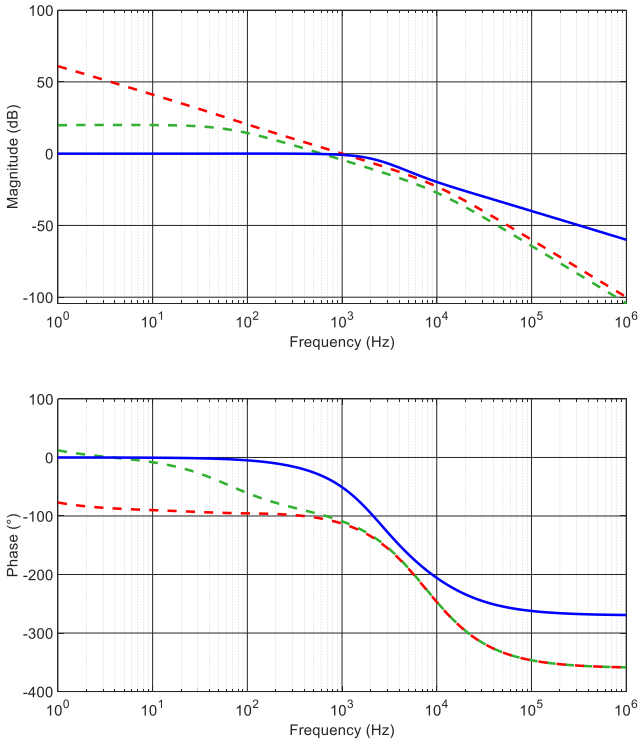

FIGURE 17. Bode diagrams relevant to AL_I_B_B. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

with the controller, and of the closed-loop system with the controller using the dashed red line, the dashed green line, and the solid blue line, respectively.

The discretization of the controller has been performed assuming that the sampling frequency of the control algorithm is equal to the switching frequency of the BC, set to 1/4 of the supply frequency of the coils.

As shown in Fig. 2, the BC is constituted by the two switches T_{13} and T_{14}. It operates as a buck chopper during the battery charging and as a boost chopped during discharging. The duty cycle of T_{13} is obtained from the controller output $V_{O,ref}$ using the relation [36]

$$\delta_{BC} = \frac{V_{O,ref}}{V_{DCS}} \tag{29}$$

The discrete controller and a circuital model of the BC have been simulated to test the performance of the control loop. A square wave reference with an amplitude of 30 A and a frequency of 20 Hz has been used as $I_{B,ref}$ in order to check AL_I_B_B both during the charge and the discharge of the battery. At this stage of development of the control algorithms, V_{DCS} is not controlled because AL_V_{DCS}_B, AL_V_{DCS}_C, and AL_V_{DCS}_D are not yet available. For this reason, AL_I_B_B has been checked inserting in the circuital model of the BC a voltage generator instead of the capacitor C_{DCS}.

The simulation results are reported in Fig. 18. The dashed green line represents the reference current whilst the solid

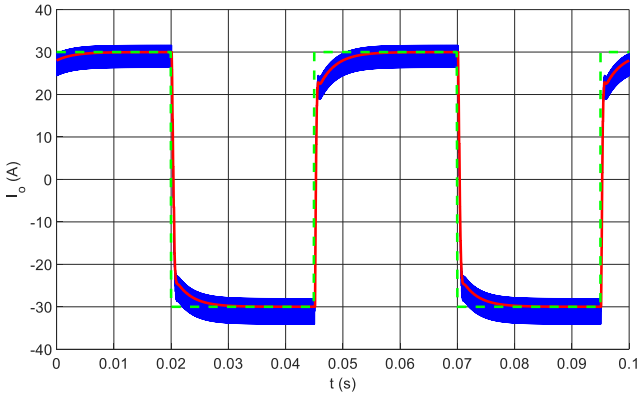

FIGURE 18. AL_I_B_B responses. $I_{B,ref}$ (dashed green), I_B (blue), and I_B at the output of the LPF (red solid).

blue line shows the battery current. It appears as a thick band because of the high frequency ripple generated by the power switches commutations. The solid red line is the feedback signal found at the output of the LPF. The overall response of the control loop is quite satisfactory as the battery current follows the reference accurately, without oscillations or overshoot.

C. EXTERNAL LEVEL ALGORITHMS

1) AL_V_{DCP}_B: CONTROL OF V_{DCP} VOLTAGE THROUGH P_G

a: GENERATION OF $P_{G,ref}$

The FEC has the two tasks of controlling the average voltage V_{DCP} across the terminals of C_{DCP} to a value that allows the HFPC to operate correctly and of managing the power exchanged with the grid. This latter task is performed following the indications of CEI 0-21 [35], which requires adjusting the ratio of active to reactive power according to grid conditions. This issue is not considered in this paper, however, AL_V_{DCP}_B and AL_i_G_B, which manipulates and controls the grid current, respectively, are able to manage both active and reactive power. The two tasks of AL_V_{DCP}_B are easily integrated by designing an algorithm that manipulates directly the active and reactive power P_G and Q_G exchanged with the grid rather than the current i_G. The grid current reference $i_{G,ref}$ is then obtained by processing the active power reference $P_{G,ref}$ and, possibly, the reactive power reference $Q_{G,ref}$.

According to Tab. 1, AL_V_{DCP}_B has an interaction of the first type with AL_V_{DCP}_C during battery charging and another interaction of the first type with AL_V_{DCP}_D during battery discharging. During the charging process, AL_V_{DCP}_C tries to bring V_{DCP} to the lower reference value $V_{DCP,ref,low}$. To this end, it generates a reference for the power P_{PS} absorbed from C_{DCP} and transferred to the secondary side of BWV2H. At the same time, AL_V_{DCP}_B tries to bring V_{DCP} to the higher reference value $V_{DCP,ref,high}$ by generating the reference for the grid power P_G injected in C_{DCP}. On the contrary, while discharging the battery, AL_V_{DCP}_D tries to bring V_{DCP} to the higher reference value $V_{DCP,ref,high}$ by generating the reference for the power P_{SP} drawn from the battery and injected in C_{DCP}. At the same time, AL_V_{DCP}_B tries to bring V_{DCP} to the lower reference

value $V_{DCP,ref,low}$ by generating the reference for the power P_G drawn from C_{DCP} and injected in the grid.

In this paper, $P_{G,ref}$ is limited to the maximum value specified in [35] and used to design the BWV2H. However, it is perfectly compatible with the operation of the designed control algorithms to assume that an even higher management level exists that assigns the available domestic grid power to the various home appliances [39], [40]. Then, during battery charging, $P_{G,reg}$ could be lower than the power limit specified in [35]. In the same way, during battery discharging, $P_{G,ref}$ can be adjusted to the actual requirements of the domestic grid, for example to comply with the efficient use of PV panels or storage batteries, but in any case without exceeding the maximum discharge power of the battery.

Being the current references for the algorithms of the internal level derived from the power references, the interactions of AL_V_{DCP}_B with AL_V_{DCP}_C and AL_V_{DCP}_D ensure that in steady state V_{DCP} is always between its lower and higher references and that the current i_G and the amplitudes I_P and I_S do not exceed their maximum values.

The assumption that the power P_{SP} is transferred from the battery and injected into C_{DCP} entails that the losses in the power converters and in the coupled coils have been neglected. The same approach is also applied in manipulating the power references to obtain the current references. This approximation does not affect the functioning of the system since it is compensated by the feedback control loops implemented in all the algorithms. More in details, the power losses due to the voltage drops across the coils' parasitic resistances and across the power switches and diodes are compensated by the controllers relevant to the algorithms of the internal level. They perform this compensation automatically by requiring the power converters to generate voltages a little higher than those needed in ideal conditions. The losses of the cores of the coupled coils, that cause the induced voltage to be lower than the expected one, are automatically compensated as well. In this case, the external level algorithms generate $I_{P,ref}$ and $I_{S,ref}$ a little higher than those expected in ideal conditions. It is worth to highlight that near the end of the battery charge, the current I_B reduces gradually to zero so that the voltage error caused by $R_{B,ESR}$ reduces to zero as well. During battery discharge, the voltage across the battery terminals is lower than its no-load voltage so that also in this case the end-of-discharge voltage is not exceeded despite the voltage error caused by $R_{B,ESR}$. A detailed analysis of the power losses in a WPT system can be found in [41].

Given that AL_V_{DCP}_B generates a reference for P_G, it results convenient to model the controlled system by highlighting this quantity. The first step is to express the relationship between the voltage across a capacitor and its stored energy in terms of Laplace transforms. By considering that the energy stored in the capacitor corresponds to the integral of the injected power, this relationship is given by

$$\frac{P(s)}{s} = \frac{1}{2} C V^2(s), \tag{30}$$

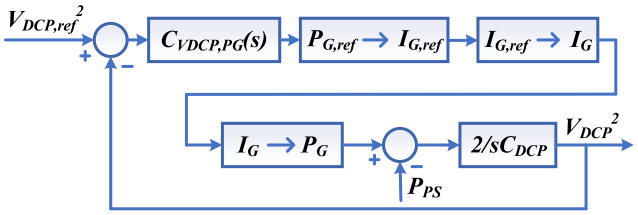

FIGURE 19. Ideal block diagram of control loop of AL_V_{DCP}_B.

where $V^2(s)$ is the L-transform of the capacitor squared voltage. From (30) it derives that the state variable used in modelling the system is V_{DCP}^2 instead of V_{DCP} and that it is convenient to control the square of the voltage across C_{DCP} rather than the voltage itself.

The ideal scheme of the voltage control loop is represented in Fig. 19. Like in the previous cases, the controller $C_{VDCP,PG}(s)$ is of the PI type. The integral action would not be strictly necessary if the purpose of the controller was only to charge an insulated capacitor at the desired voltage. In this case, however, the capacitor supplies the HFPC (or the FEC, during battery discharging). Consequently, $C_{VDCP,PG}(s)$ must require the injection of power into C_{DCP} even when the voltage error is null to compensate for the power P_{PS} absorbed by the HFPC.

The block denoted as $P_{G,ref} \rightarrow I_{G,ref}$ represents the conversion between the active power reference generated by the controller and the reference $I_{G,ref}$ for the amplitude of the grid current. It is approximated by the relation

$$I_{G,ref} = \frac{2P_{G,ref}}{V_{G,N}}, \tag{31}$$

obtained by assuming that the grid voltage is sinusoidal and with the nominal amplitude $V_{G,N}$, that the grid current is in phase with the voltage, and that the efficiency of the FEC is equal to one. The reference $I_{G,ref}$ will be further manipulated to work out the grid current reference $i_{G,ref}$ to be provided to AL_i_G_B, described in subsection IV-B1.

The block denoted as $I_{G,ref} \rightarrow I_G$ models the non-idealities introduced by the control algorithm AL_i_G_B in modulating the amplitude of i_G. The amplitude Bode diagram of the control loop of i_G, shown in Fig. 8, is flat up to 1 kHz. On the other hand, in the following paragraphs it will be shown that the bandwidth of the loop controlled by $C_{VDCP,PG}(s)$ is much smaller. Consequently, the effects of the block $I_{G,ref} \rightarrow I_G$ can be disregarded and it can be considered as an unitary gain. The block $I_G \rightarrow P_G$ represents the conversion between the actual amplitude of the grid current and the power entering into to the dc bus of the FEC. By disregarding the FEC losses, it is approximated by reversing (31). The power P_{PS} constitutes a disturbance for the system. It is subtracted from P_G to obtain the net power injected in the capacitor. The last block in the forward path of Fig. 19 comes from (30) and represents the capacitor C_{DCP}.

In implementing the control system, it must be remembered that the transduced quantity is V_{DCP} instead of V_{DCP}^2

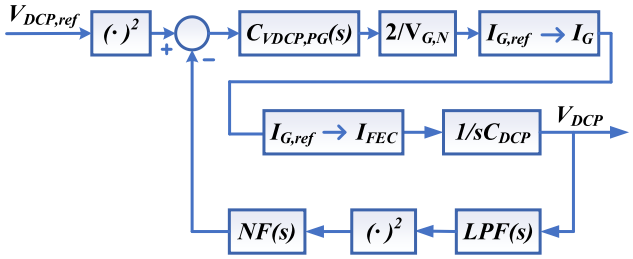

FIGURE 20. Realistic block diagram of control loop of AL_V_{DCP}_B.

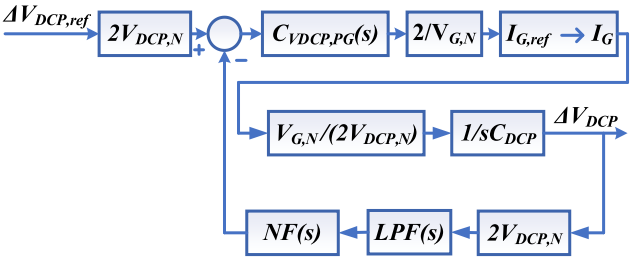

FIGURE 21. Linearized block diagram of the control loop of AL_V_{DCP}_B.

and that C_{DCP} is actually charged by a current. Consequently, the block diagram of Fig. 20 gives a more realistic representation of the physical implementation of the control loop of V_{DCP}. In the figure, the block $P_{G,ref} \rightarrow I_{G,ref}$ has been substituted for by the gain coming from (31). The block $I_G \rightarrow I_{FEC}$ represents the relation between the grid current and the current that actually enters into the dc bus of the FEC. In order to simplify the diagram, the disturbance current I_{DCP}, which accounts for the power P_{PS}, is not shown. The blocks $(\cdot)^2$ represent the square operator. The microprocessor implements them while processing the samples of $V_{DCP,ref}$ and of the voltage acquired at the output of the LPF.

The capacitor C_{DCP} has the function of absorbing the oscillating components of the power exchanged with the grid in order to charge or discharge the battery with a constant power. For this reason, at steady state, V_{DCP} oscillates at twice the grid frequency around its reference value and can be approximated as

$$V_{DCP}(t) \approx V_{DCP,ref} + \Delta v_{DCP} sin(2\omega_G t). \tag{32}$$

The quantity processed by the controller $C_{VDCP,PG}(s)$ is V^2_{DCP} that, following from (32), is approximated with the expression

$$V^2_{DCP}(t) \approx V^2_{DCP,ref} + \frac{\Delta v_{DCP}{}^2}{2} + 2V_{DCP,ref}\Delta v_{DCP} sin(2\omega_G t) - \frac{\Delta v_{DCP}{}^2 cos(4\omega_G t)}{2}, \tag{33}$$

obtained using the relation

$$sin(2\omega_G t)^2 = \frac{1}{2} - \frac{cos(4\omega_G t)}{2}. \tag{34}$$

which comes from the half-angle formula.

In (33) a term with angular frequency $2\omega_G$, corresponding to 100 Hz, and one with angular frequency $4\omega_G$, corresponding to 200 Hz, appear.

The controller $C_{VDCP,PG}(s)$ should not attempt to eliminate the oscillations of V^2_{DCP}, otherwise a distortion in the waveform of i_G would be introduced. Hence, either the components at frequencies of 100 Hz and 200 Hz are left outside the bandwidth of the V_{DCP} control loop, or they are attenuated before being processed by the controller. In designing the control loop, an intermediate solution has been selected: the bandwidth ω_B has been set to $2\pi \cdot 20$ rad/s with a the phase margin of 80°, and a notch filter, denoted as NF(s) in Fig. 20, has been inserted in the feedback path of the loop. The notch filter has the TF

$$NF(s) = \frac{s^2 + \omega_0^2}{s^2 + s\omega_B + \omega_0^2}, \tag{35}$$

with a bandwidth $\omega_B = 2\pi \cdot 40$ rad/s and a center frequency $\omega_0 = 2\pi \cdot 100$ rad/s. Being inserted after the square operator $(\cdot)^2$, the notch filter operates both on the 100 Hz and the 200 Hz components of V^2_{DCP}.

The presence of the operator $(\cdot)^2$ makes the diagram of Fig. 20 not linear and, consequently, the controller $C_{VDCP,PG}(s)$ cannot be designed using the conventional approach. Then, the diagram has been linearized around the nominal working point $V_{DCP} = V_{DCP,N}$ by expressing V_{DCP} in the form

$$V^2_{DCP} \approx V^2_{DCP,N} + 2V_{DCP,N}\Delta V_{DCP}, \tag{36}$$

where ΔV_{DCP} is the variation of V_{DCP} with respect to $V_{DCP,N}$. Using (36) and a similar expression for $V^2_{DCP,ref}$, the diagram of Fig. 20 has been redrawn as in Fig. 21. The block $I_G \rightarrow I_{FEC}$ has been replaced by

$$I_{DCP} = \frac{V_{G,N}}{2V_{DCP,N}} I_G, \tag{37}$$

obtained neglecting the losses of the FEC and in the hypothesis that the current i_G is in phase with the voltage v_G and that the voltage V_{DCP} remains close to its nominal value.

The $C_{VDCP,PG}(s)$ controller was designed on the basis of Fig. 21 using the same technique described in subsection IV-A. The Bode diagrams for V_{DCP} control loop are shown in Fig. 22 where, as in the previous figures, the dotted green line represents the diagram of the open-loop system without the controller; the dashed red line refers to the open-loop controlled system, and the solid blue line shows the Bode diagrams of the closed-loop controlled system.

b: GENERATION OF $i_{G,ref}$

The power reference $P_{G,ref}$ computed by $C_{VDCP,PG}(s)$ is further manipulated to work out the grid current reference $i_{G,ref}$ for AL_i_G_B.

In static converters connected to the three-phase grid, the power control algorithm is often developed on the basis of the theory of instantaneous power [42]. The application of this theory requires a prior transformation of the three-phase voltages from the frame a,b,c to the stationary frame α, β, γ

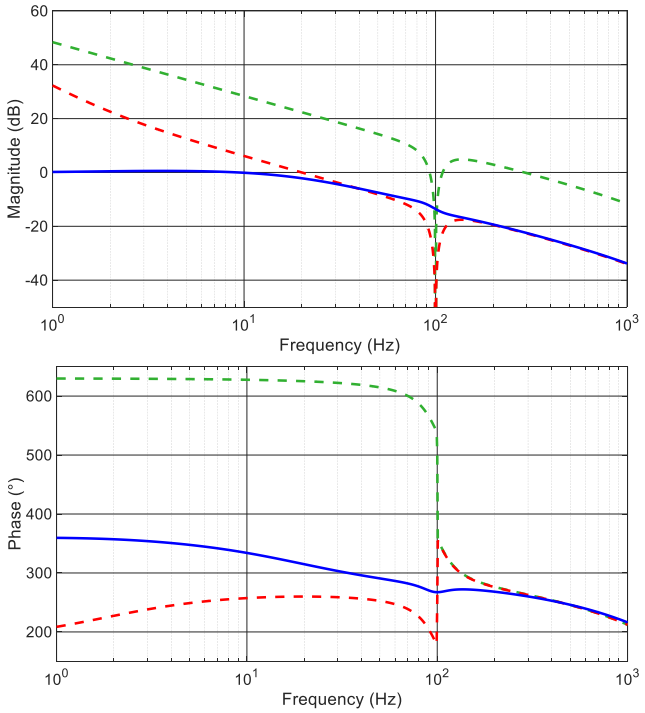

FIGURE 22. Bode diagrams relevant to AL_V_{DCP}_B. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

by means of the Clarke matrix. Eventually, a further transformation to the synchronous frame d,q,0 is performed by means of the Park matrix.

In a three-phase system without neutral, or when the sum of the phase currents is identically zero, the theory of instantaneous power defines the real instantaneous power p and the imaginary instantaneous power q as

$$\begin{aligned} p &\triangleq \frac{3}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \\ q &\triangleq \frac{3}{2}\left(v_\alpha i_\beta - v_\beta i_\alpha\right) = \frac{3}{2}\left(v_d i_q - v_q i_d\right) \end{aligned} \tag{38}$$

where i_α, i_β, i_d, and i_q are the current components in the stationary and in the synchronous reference frames.

In a three-phase system with symmetrical voltages and balanced currents, the real instantaneous power corresponds to the active power whilst the imaginary instantaneous power corresponds to the opposite of the reactive power. From this property it derives that, if the references $P_{G,ref}$ and $Q_{G,ref}$ for the active and the reactive power are given, by inversion of (38) it is possible to work out the corresponding references for the currents in the stationary and/or in the synchronous frames by means of

$$\begin{aligned} i_\alpha &= \frac{2}{3}\frac{P_{G,ref}\,v_\alpha + Q_{G,ref}\,v_\beta}{v_\alpha^2 + v_\beta^2}, \quad & i_d &= \frac{2}{3}\frac{P_{G,ref}\,v_d + Q_{G,ref}\,v_q}{v_d^2 + v_q^2} \\ i_\beta &= \frac{2}{3}\frac{P_{G,ref}\,v_\beta - Q_{G,ref}\,v_\alpha}{v_\alpha^2 + v_\beta^2}, \quad & i_q &= \frac{2}{3}\frac{P_{G,ref}\,v_q - Q_{G,ref}\,v_d}{v_d^2 + v_q^2} \end{aligned} \tag{39}$$

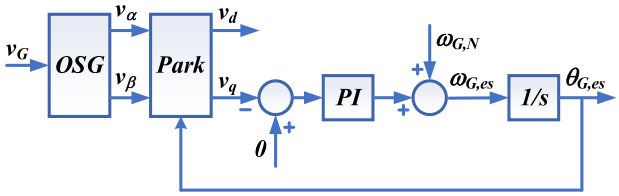

FIGURE 23. Block diagram of a Park-PLL.

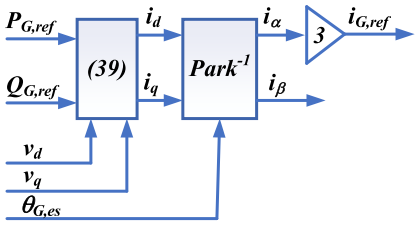

FIGURE 24. Block diagram for the generation of $i_{G,ref}$.

In single-phase systems, like the BWV2H, the Clarke transformation cannot be applied because only one phase voltage is available. Nevertheless, v_α and v_β are computed exploiting the properties by which $v_\alpha = v_G$ and v_β has the same waveform as v_G but lags it by 90°. The subsequent Park transformation requires to know the instantaneous phase θ_G of v_G. It is obtained by means of a PLL that works out the voltage components v_d and v_q as a side-product of the computation, as shown in the diagram of Fig. 23. The filter at the PLL input performs the orthogonal signal generation (OSG) by which v_β is obtained from v_G. Different kinds of OSG algorithms are available. In simulating the BWV2H the one described in [43] has been adopted.

Once v_d, v_q, and θ_G are obtained from the PLL, the active power reference $P_{G,ref}$ coming from $C_{VDCP,PG}(s)$, and, possibly, the reactive power reference $Q_{G,ref}$ generated by a suitable external control loop, are processed according to the block diagram of Fig. 24 to work out $i_{G,ref}$. The instantaneous power theory used to derive $i_{G,ref}$ is based on three phase systems, but in the BWV2H the full power must be exchanged through a single phase. For this reason the gain 3 is inserted between i_α and $i_{G,ref}$.

2) AL_V_{DCP}_C: CONTROL OF V_{DCP} VOLTAGE THROUGH P_{PS}

AL_V_{DCP}_C is enabled during process of battery charging and tries to bring V_{DCP} to the lower reference value $V_{DCP,ref,low}$ by absorbing from C_{DCP} the power P_{PS} transferred to the secondary side of BWV2H. In the same way as it happens with AL_V_{DCP}_B, the power reference $P_{PS,ref}$ generated by the controller $C_{VDCP,PPS}(s)$ is converted into a reference for I_S and forwarded to AL_I_S_C, described in subsection IV-B2. As explained in subsection IV-C1.a, it results convenient to use V_{DCP}^2 instead of V_{DCP} in modelling the system and in designing its controller. According to this approach, the block diagram of Fig. 25 is obtained, where the blocks within the dashed rectangle are located

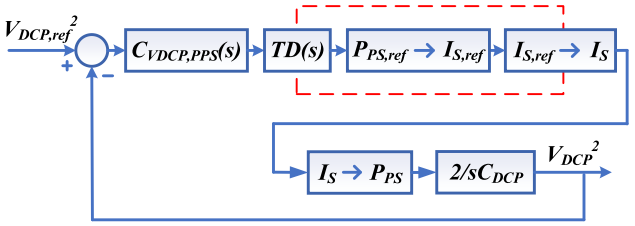

FIGURE 25. Ideal block diagram of control loop of AL_V_{DCP}_C.

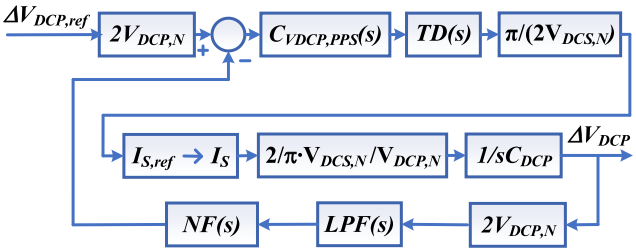

FIGURE 26. Linearized block diagram of the control loop of AL_V_{DCP}_C.

on the secondary section of the BWV2H. The diagram is similar to that of Fig. 19, with the differences that the block TD(s) has been added to account for the delay due to the radio transmission of $P_{PS,ref}$ to the secondary section of the BWV2H. The disturbance power P_G injected in the capacitor C_{DCP} is not represented to simplify the diagram.

AL_V_{DCP}_C has an interaction of the second type with AL_V_{DCS}_C. It is managed in the secondary side of the BWV2H by selecting the smaller between the power reference received via radio from AL_V_{DCP}_C and that one generated by AL_V_{DCS}_C. The selected power reference is converted into a current amplitude reference by the block $P_{PS,ref} \rightarrow I_{S,ref}$ according to the relation

$$I_{s,ref} = \frac{\pi}{2} \frac{P_{PS,ref}}{V_{DCS,N}}. \tag{40}$$

It has been obtained by neglecting the losses of the HFSC in performing the current rectification and supposing i_S sinusoidal and V_{DCS} at its nominal value $V_{DCS,N}$. The gain $\pi/2$ accounts for the ratio between the amplitude of the current flowing in the secondary coil and the average value of its rectified version I_{DCS}.

Within AL_I_S_C, the amplitude reference $I_{s,ref}$ is transmitted back to the primary section trough the radio connection, as shown in Fig. 12, and processed by $C_{IS,VHFP}(s)$, designed in subsection IV-B2. In Fig. 25, the whole control loop of I_S is represented by the block $I_{S,ref} \rightarrow I_S$. The current i_S discharges the capacitor C_{DCP} with the power P_{PS}, as modeled by the block $I_S \rightarrow P_{PS}$, whose TF can be approximated as a gain given by inversion of (40).

Following the same considerations of subsection IV-C1, the block diagram of Fig. 25 has been linearized around the nominal working point and redrawn as in Fig. 26. With respect to Fig. 25, the low pass filter and the notch filter have been added in the feedback path, as in Fig. 21. Obviously,

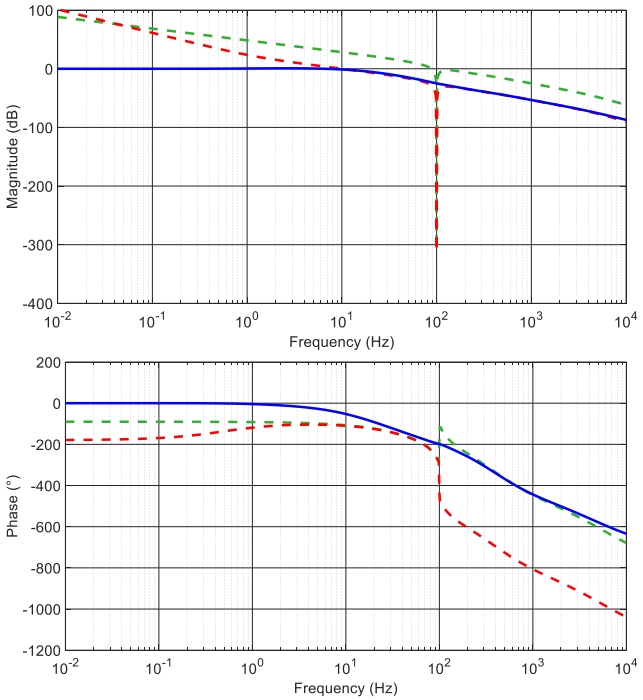

FIGURE 27. Bode diagrams relevant to AL_V_{DCP}_C. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

they are implemented only once in the control firmware of BWV2H and the output of NF(s) is forwarded to all the control loops that need it. The block $2/\pi \cdot V_{DCS,N}/V_{DCP,N}$ accounts for the block $I_S \rightarrow P_{PS}$ and for the division by $V_{DCP,N}$ that converts the power P_{PS} in the current I_{DCP}.

In designing the controller $C_{VDCP,PPS}(s)$, the block $I_{S,ref} \rightarrow I_S$ has been approximated by a first order low pass filter with a cutoff frequency of 100 Hz, according to the Bode diagrams of Fig. 13. A PI controller resulted enough to satisfy the control specifications, which consist of a cutoff frequency of 10 Hz and a phase margin of 70°. Fig. 27 shows the Bode diagrams of the open-loop uncontrolled system, of the open-loop system with the PI controller, and of the closed-loop controlled system.

The algorithms AL_V_{DCP}_C and AL_V_{DCP}_B have been simulated together to check their interaction. The power reference $P_{PS,ref}$ computed by AL_V_{DCP}_C has been used in the simulation, without considering the second type of interaction with AL_V_{DCS}_C because it is not yet available. For this reason, the voltage across C_{DCS} has been kept constant by substituting the capacitor with a constant voltage generator set to $V_{DCS,N}$.

The simulation results are reported in Fig. 28. The top half of the figure shows the voltage V_{DCP} with the blue line and its lower and higher references with the dashed red lines. It has been hypothesized that the initial value of V_{DCP} is equal to the nominal peak grid voltage, i.e. about 325 V, so that at the beginning of the simulation, the capacitor is charged and V_{DCP} approaches the final value in about 0.5 s. The voltage

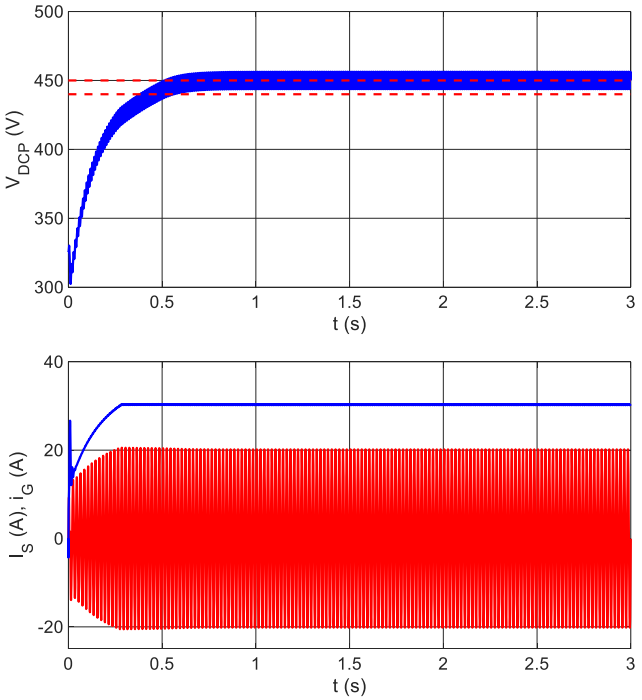

FIGURE 28. Top: Voltage V_{DCP} (blue), $V_{DCP,ref,high}$ (dashed red), and $V_{DCP,ref,low}$ (dashed red). Bottom: I_S (blue) and i_G (red).

plot appears as a thick solid band because V_{DCP} oscillates around the final value at twice the grid frequency. In the bottom half of the figure the blue line and the red line show the behavior of I_S and of i_G. Like V_{DCP}, i_G appears as a solid red surface because its oscillations cannot be resolved at the time scale of the figure. In the first phase of the capacitor charging, the amplitudes of both currents grow until I_S reaches its maximum value. At this point, the effect of i_G on the V_{DCP} voltage temporarily prevails over that of i_S so that the voltage reaches the upper reference. Then, the amplitude of i_G stabilizes to keep the voltage constant. Under these conditions, there is a continuous flow of maximum power from the grid to the receiving section of the BWV2H, as foreseen by the analysis carried out in subsection III-C.

3) AL_V_{DCP}_D: CONTROL OF V_{DCP} VOLTAGE THROUGH P_{SP}

AL_V_{DCP}_D is enabled during battery discharging and tries to bring V_{DCP} voltage to it higher reference $V_{DCP,ref,high}$ by injecting in C_{DCP} the power P_{SP} transferred to the primary side of BWV2H. In this case, the power reference $P_{SP,ref}$ generated by AL_V_{DCP}_D is converted into a reference for I_P and forwarded to AL_I_P_D, described in subsection IV-B3. Like for AL_V_{DCP}_C, the variable actually controlled is V_{DCP}^2 so that the block diagram of the control loop must be linearized to design the controller, as shown in Fig. 29.

The diagram is a little simpler than the one relevant to AL_V_{DCP}_C because the controlled variable V_{DCP} and the manipulated one, which is actually I_P, both pertain to the same section of the BWV2H. Hence, the block $2/\pi \cdot V_{DCS,N}/V_{DCP,N}$ of Fig. 26 simplifies to $2/\pi$, which accounts

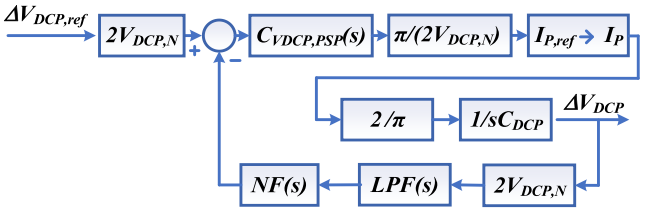

FIGURE 29. Linearized block diagram of the control loop of AL_V_{DCP}_D.

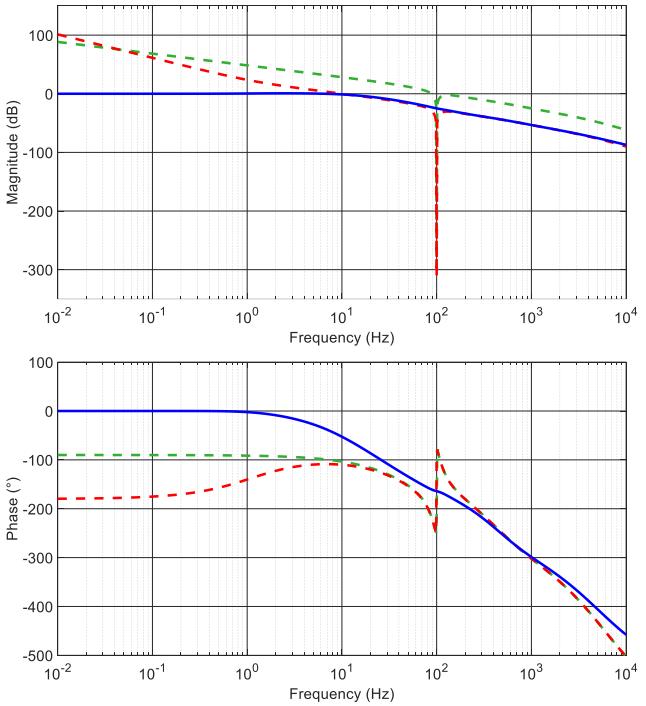

FIGURE 30. Bode diagrams relevant to AL_V_{DCP}_D. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

for the ratio between the amplitude I_P of the current flowing in the primary coil and the average value I_{DCP} of its rectified version, which discharges the capacitor C_{DCP}. For the same reason, no radio transmission is required, and the block TD(s) does not appear in the diagram. Nevertheless, it is worth to highlight that the control loop of I_P, represented by the block $I_{P,ref} \rightarrow I_P$, encompasses a transmission delay block because the primary coil current is controlled by means of the HFSC, which pertains to the secondary section of the BWV2H.

The controller $C_{VDCP,PSP}(s)$, has been designed following the same procedure described in the subsection IV-C2, i.e. by approximating the block $I_{P,ref} \rightarrow I_P$ with a first order low pass filter. The cutoff frequency of the control loop has been set to 10 Hz and the phase margin to 70°. The obtained Bode diagrams are shown in Fig. 30.

4) AL_V_{DCS}_B: CONTROL OF V_{DCS} VOLTAGE THROUGH P_B

The BC has the task to control the voltage across C_{DCS} to a value that allows the BC itself to operate correctly. This task is performed both during the charging and the discharging

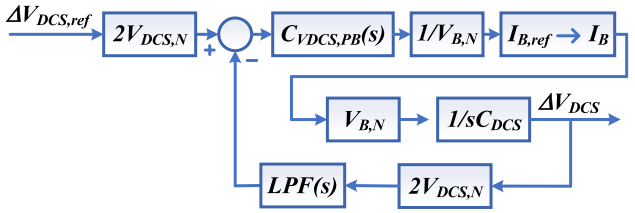

FIGURE 31. Linearized block diagram of the control loop of AL_V_{DCS}_B.

processes by manipulating the power P_B extracted from the capacitor and injected into the battery. According to Tab. 1, AL_V_{DCS}_B has an interaction of the first type with AL_V_{DCS}_C and AL_V_{DCS}_D, which are selectively enabled during charging and discharging of the battery. Moreover, AL_V_{DCS}_B has an interaction of the second type with AL_V_B_B, which controls the battery voltage. During the charging process AL_V_{DCS}_B tries to bring V_{DCS} to its lower reference $V_{DCS,ref,low}$ by discharging C_{DCS} and generates the reference for the power P_B from which $I_{B,ref}$ is derived. At the same time AL_V_{DCS}_C regulates the voltage V_{DCS} towards its higher reference $V_{DCS,ref,high}$ generating the reference for the transferred power P_{PS}, from which, in turn, $I_{S,ref}$ is derived. During the discharging process AL_V_{DCS}_B tries to bring V_{DCS} to its higher reference $V_{DCS,ref,high}$ by charging C_{DCS} with the power P_B that discharges the battery. At the same time AL_V_{DCS}_D controls V_{DCS} to its lower reference $V_{DCS,ref,low}$ generating $P_{SP,ref}$, from which $I_{P,ref}$ is derived.

Also in this case, the quantity actually controlled is V_{DCS}^2, and the control loop AL_V_{DCS}_B is described by the linearized block diagram of Fig. 31. The blocks $1/V_{B,N}$ and $V_{B,N}$ perform the conversions from the power reference $P_{B,ref}$ to the current reference $I_{B,ref}$ and then back from I_B to P_B. The block $I_{B,ref} \rightarrow I_B$ represents the control loop described in subsection IV-B4.

The Bode diagrams of the open-loop uncontrolled system is depicted in Fig. 32 with the dashed green line. Thanks to the integral action of C_{DCS}, the system inherently has a -20dB/dec slope at low frequencies. This characteristic assures that a proportional controller would be sufficient to achieve zero steady state error with respect to a constant reference. However, as demonstrated in subsection III-C, because of the interaction with AL_V_{DCS}_C and AL_V_{DCS}_D, it is necessary to use a PI controller in order to ensure that the battery charging or discharging power reaches the maximum value.

In designing the controller, a cut-off frequency of 10 Hz and a phase margin of 80 ° have been set for the open-loop controlled system. The obtained Bode diagrams of the open-loop and closed-loop controlled systems are drawn in Fig. 32 with the dashed red line and the solid blue line, respectively.

5) AL_V_{DCS}_C: CONTROL OF V_{DCS} VOLTAGE THROUGH P_{PS}

The procedure for the design of AL_V_{DCS}_C is quite similar and somewhat symmetric to that one adopted in subsection IV-C3 for AL_V_{DCP}_D. The linearized block diagram of the

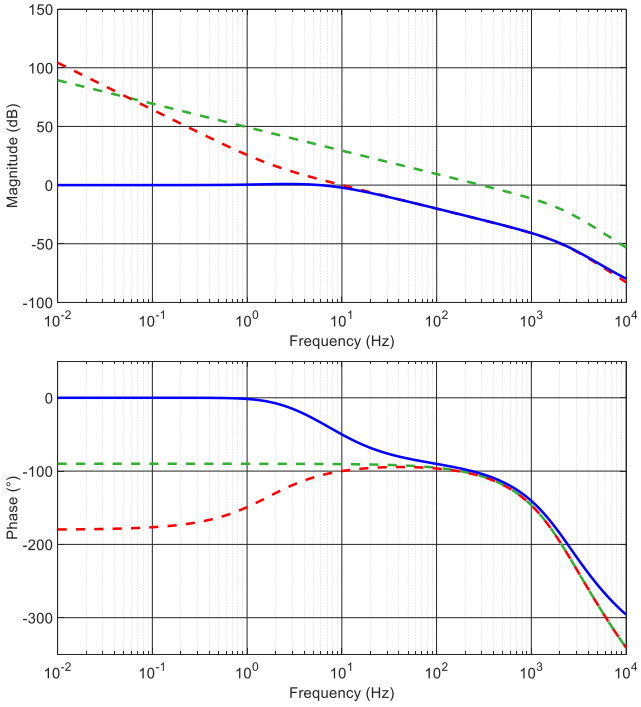

FIGURE 32. Bode diagrams relevant to AL_V_{DCS}_B. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue).

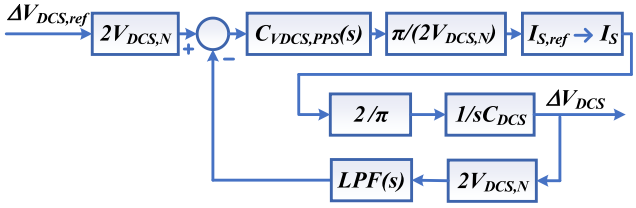

FIGURE 33. Linearized block diagram of control loop of AL_V_{DCS}_B.

system is reported in Fig. 33. It is equal to that of Fig. 29 apart for the absence of the notch filter. Indeed, now it is not needed because the oscillation frequency of V_{DCS} is much higher than that of V_{DCP} and falls outside the band of the control loop.

The system to be controlled has the open-loop Bode diagrams shown in Fig. 34 with the dashed green line.

Some preliminary tests carried out by simulation showed that to obtain satisfactory operations of the overall control system of the BWV2H it is necessary that the bandwidth of the control loop here considered is greater than that imposed in the previous subsection for AL_V_{DCS}_B. Then, the bandwidth has been set at 30 Hz, maintaining a phase margin of 80°. Due to the delay introduced by the block $I_{S,ref} \rightarrow I_S$, designed in subsection IV-B2, and whose implementation requires to transfer information between the two sections of the BWV2H, the zero of a conventional PI controller does not provide sufficient phase advance. To overcome this drawback, a leading network has been placed in cascade with

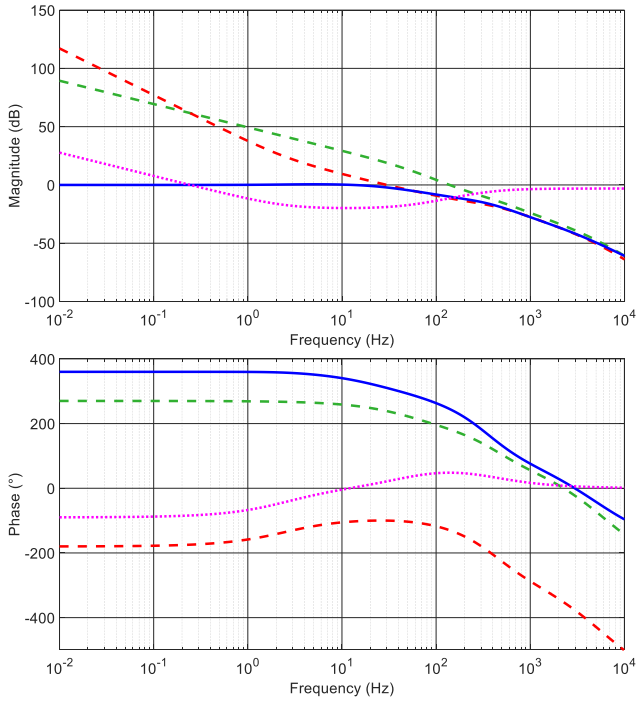

FIGURE 34. Bode diagrams relevant to AL_V_{DCS}_C. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue), controller (dotted magenta).

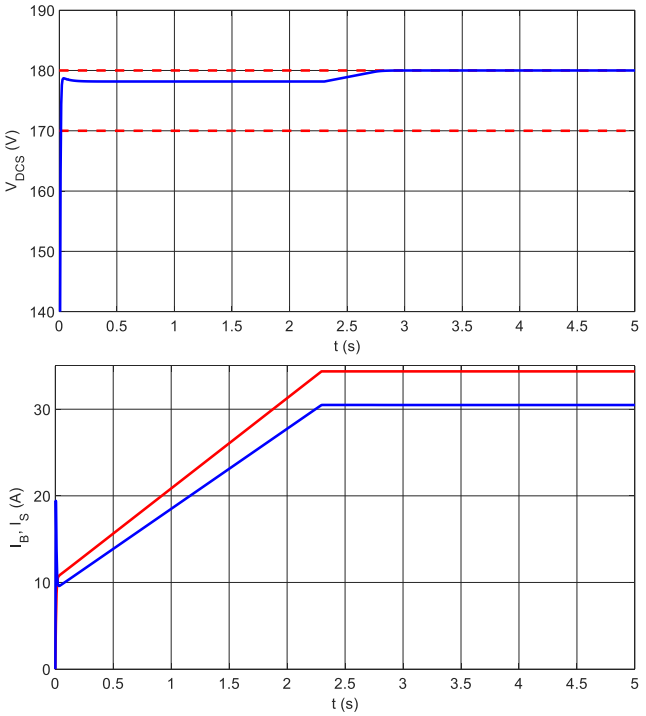

FIGURE 35. Top: Voltage V_{DCS} (blue), V_{DCS},ref,high (dashed red), and V_{DCS},ref,low (dashed red). Bottom: IS (blue) and IB (red).

the PI controller, so that the TF of the controller results in

$$C_{VDCS,PPS}(s) = \frac{1+s\tau_{PI}}{s\tau_{PI}} \frac{1+s\tau_z}{1+s\tau_P}. \tag{41}$$

The time constant τ_{PI} has been set at $1/(2\pi \cdot 50)$ s while τ_p and τ_z have been adjusted to get the desired performance. The Bode diagrams of $C_{VDCS,PPS}(s)$ are plotted with the dotted magenta line in Fig. 34. The open-loop and closed-loop Bode diagrams of the controlled system are plotted with the dashed red line and the solid blue line, respectively.

The interaction of the first type between AL_V_{DCS}_B and AL_V_{DCS}_C has been checked by simulation, obtaining the results reported in Fig. 35. The interactions of the second type with AL_V_B_B and AL_V_{DCP}_C have not been considered in the model because the first of them is not yet available. The test considered the charge of C_{DCS} from the nominal battery voltage up to its maximum voltage. In the initial phase of the simulation, the voltage increases rapidly and then, for about 2.3 s, remains at an intermediate value between $V_{DCS,ref,low}$ and $V_{DCS,ref,high}$. During this interval, the voltage errors with respect to the references are almost constant and consequently, due to the integral action of the controllers, the references for P_{PS} and P_B grow linearly. The corresponding current references behave in the same way. Given the fast response of the current control loops, at the time scale of the figure the actual currents, shown in the bottom half of Fig. 35, have the same behavior as their references. At about 2.3 s, the current I_B reaches its maximum and then maintains a constant value. Thanks to the controller $C_{VDCS,PPS}(s)$, I_S grows for a while so as to charge the capacitor up to the voltage $V_{DCS,ref,high}$, and then decreases down to the value that compensate the effect of I_B.

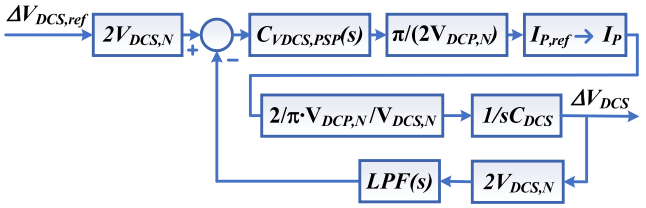

FIGURE 36. Linearized block diagram of control loop of AL_V_{DCS}_D.

6) AL_V_{DCS}_D: CONTROL OF V_{DCS} VOLTAGE THROUGH P_{SP}

The design of the controller $C_{VDCS,PSP}(s)$ used during battery discharge follows the same steps described in the previous subsection, with the difference that the internal control loop is related to I_P instead of I_S. Consequently, the block that represents the relation between the current i_P and the current that actually charges C_{DCS} considers the dc bus voltage ratio, as shown in the block diagram of Fig. 36. The controller must perform an integral action, and a cascaded lead network is needed to adjust the system phase margin. Some preliminary tests revealed that, in order to obtain from the algorithm AL_V_{DCS}_D a response comparable to that of AL_V_{DCS}_C, it is necessary to set the phase margin at 70° instead of 80° while maintaining the same bandwidth of 30 Hz.

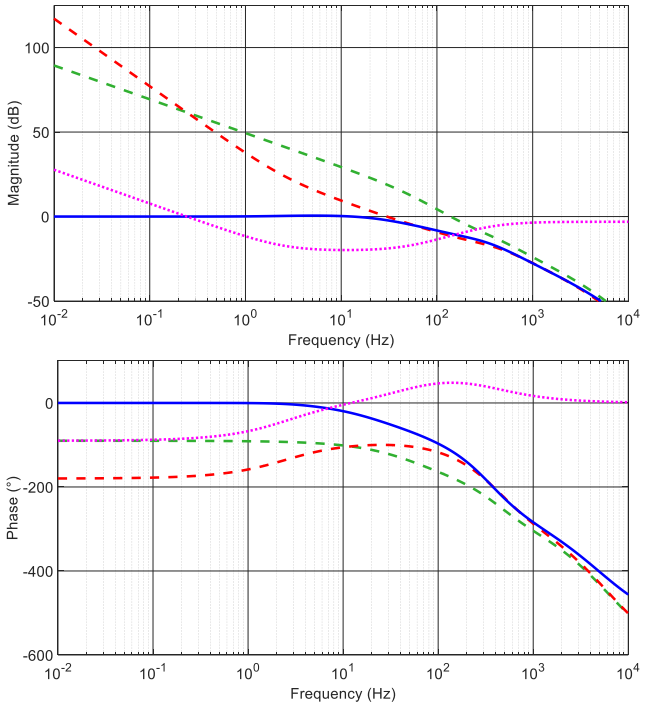

FIGURE 37. Bode diagrams relevant to AL_V_{DCS}_D. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue), controller (dotted magenta).

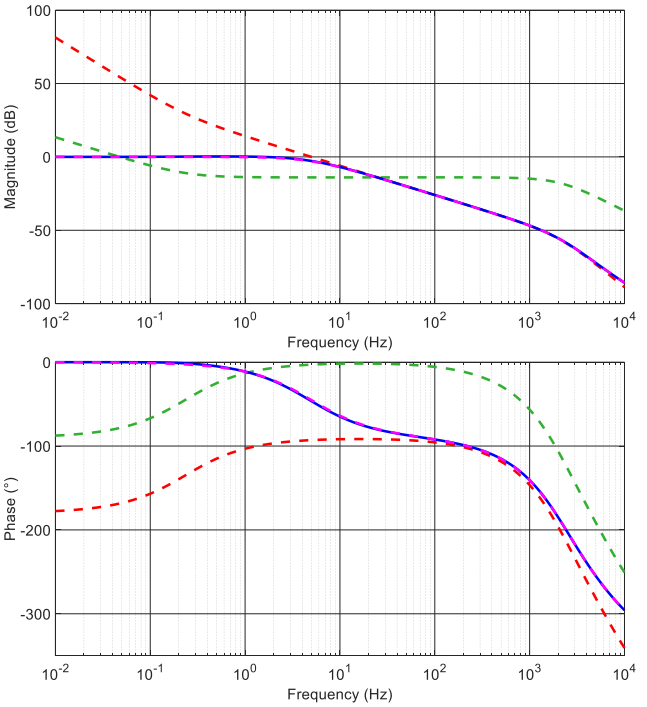

FIGURE 39. Bode diagrams relevant to AL_V_B_B. Open-loop uncontrolled system (dashed green), open-loop controlled system (dashed red), closed-loop controlled system (solid blue), closed-loop controlled system with battery (dashed magenta).

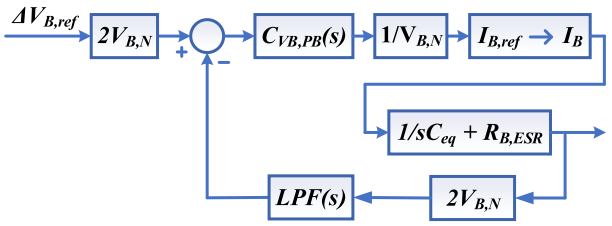

FIGURE 38. Linearized block diagram of control loop of AL_V_B_B.

The Bode diagrams in Fig. 37 refer to the open-loop uncontrolled and controlled system, to the closed-loop controlled system and to the controller.

7) AL_V_B_B: CONTROL OF V_B VOLTAGE THROUGH P_B

Like in the previous subsections, the controller $C_{VB,PB}(s)$ has been designed considering the square of the voltage as the controlled quantity. The block diagram of the control loop has been linearized around the nominal working point to obtaining the diagram shown in Fig. 38. The $1/V_{B,N}$ block accounts for the conversion between the power reference generated by the controller and the reference for the battery current. The latter one is provided to the internal level algorithm AL_I_B_B, represented by block $I_{B,ref} \rightarrow I_B$ and described in subsection IV-B4. For the controller design, the current control loop has been approximated with a low pass filter of the first order having a cutoff frequency of 1 kHz. The notch filter is not used because the transduced quantity V_B changes very slowly and without oscillations.

In order to speed up the simulations, the battery has been modelled as the large capacitor C_{eq} with a series resistance, following the same approach as in subsection IV-B4. Consequently, as shown in Fig. 39 by the dashed green plot, the amplitude Bode diagram of the open-loop uncontrolled system exhibits a slope of −20dB at low frequency, thus ensuring a null steady state error even if a purely proportional controller is used. However, when the battery is considered, the amplitude Bode diagram is horizontal at the low frequency, and a controller with an integral action must be used to provide the required slope in the amplitude diagram. The phase margin at the crossing frequency, set to 10 Hz, is close to 80° whether the battery or C_{eq} are considered, so a purely integral controller can be adopted.

The Bode diagrams of the closed-loop controlled system with the battery or with the equivalent capacitor are represented in Fig. 39 by the dashed magenta and the solid blue lines, respectively. The two diagrams are nearly perfectly superimposed, confirming that the controller $C_{VB,PB}(s)$ performs correctly in both cases.

The performances of the control algorithm have been checked by simulation imposing a square-wave reference for V_B. In order to speed up the simulation, the internal control loop of I_B has been substituted for by a current generator that

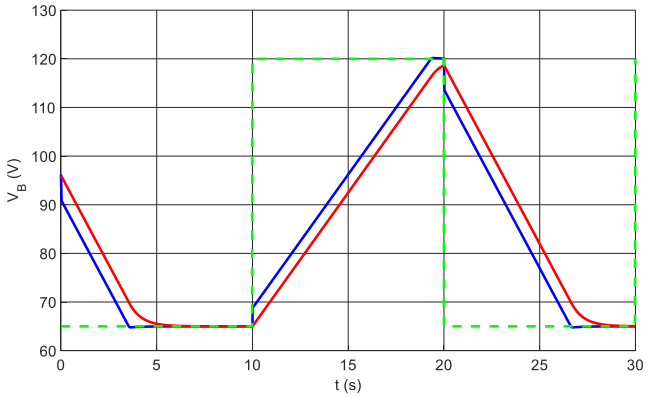

FIGURE 40. $V_{B,ref}$ voltage reference (dashed green), V_{Ceq} (solid red), V_B (solid blue).

supplies the current obtained processing $I_{B,ref}$ with a low pass filter having the same bandwidth as the current control loop.

The results of the simulation are reported in Fig. 40. The solid blue line shows the voltage V_B across the C_{eq}-$R_{B,ESR}$ series, the solid red line represents the voltage V_{Ceq} across C_{eq}, and the voltage reference is plotted with the dashed green line. The plots confirm that V_B faithfully follows the assigned reference even if, obviously, C_{eq} cannot be charged or discharged instantaneously because of the current limitations. Indeed, it actually takes about 10 seconds to charge C_{eq} from the minimum to the maximum voltage, as specified in determining its capacitance. The stepwise difference between V_B and V_{Ceq} is due to the voltage drop across $R_{B,ESR}$. It vanishes when the current I_B goes to zero at the end of the capacitor charge or discharge and V_{Ceq} actually reaches the reference value.

V. CHECK OF THE OVERALL CONTROL STRATEGY

With the aim of verifying the functioning of the overall control strategy, the control algorithms described separately in the previous Sections have been implemented in two simulation models, one related to the battery charge and the other related to its discharge. In order to speed up the simulations, the control loops of i_G and I_B have been represented using their TFs. On the contrary, the control loops of I_P and I_S and of V_{DCP}, V_{DCS}, and V_B have been simulated using the block diagram reported in the relevant subsections. Indeed, they have reciprocal interactions that could not be modeled considering only the resultant TFs. The HFPC and the HFSC have been represented by a delay equal to their switching periods, while the TFs between v_{HFS} and I_P and between v_{HFP} and I_S have been modeled using the gain $K_{VHFP,IS}$ given by (26). As in the previous Section, the battery has been modeled as a capacitor with a series resistor. The maximum integration step for these simulations has been set to 10 μs. The Appendix B reports the simplified flow charts relevant to the implementation of the control strategy in the two sections of the BWV2H during charging and discharging of the battery.

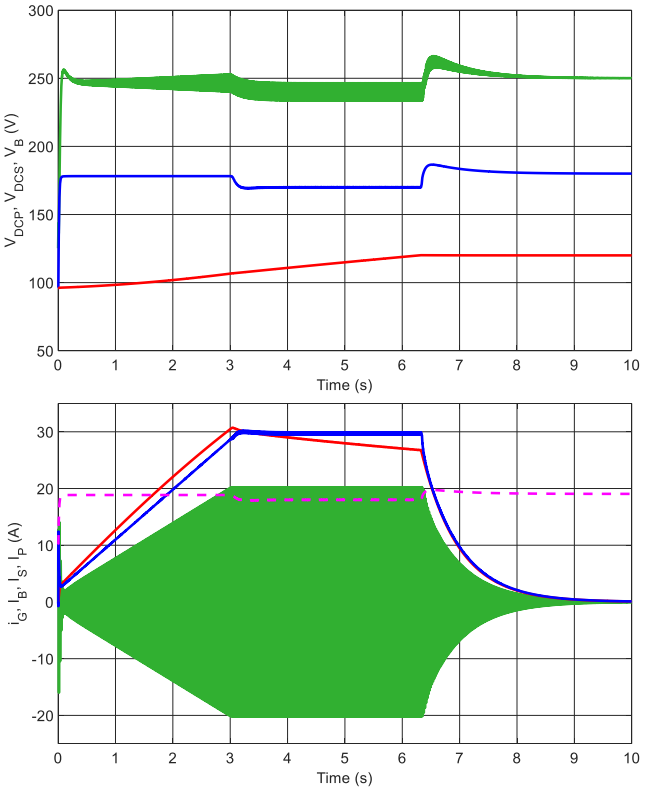

FIGURE 41. Top: V_{DCP} voltage (with an offset of −200V) (green), V_{DCS} (blue), V_B (red). Bottom: i_G (green), I_S (blue), I_B (red), I_P (dashed magenta).

A. BATTERY CHARGING

The behavior of the main quantities involved in the battery charging is shown in Fig. 41. In detail, it refers to the process that brings the voltage across the capacitor C_{eq} from $V_{B,N}$ to $V_{B,M}$. At the same time, the charging of the capacitors C_{DCP} and C_{DCS} is also performed, bringing them to their rated working voltage.

The top half of Fig. 41 shows the voltage across C_{DCP} in green. To facilitate the reading of the figure, an offset has been superimposed to V_{DCP} before plotting the graph, so 200 V must be added to the plotted quantity to obtain its real value. The blue line represents V_{DCS} while the red line corresponds to V_B. The bottom half of Fig. 41 shows the current i_G in green, the current amplitude I_S in blue, and the current I_B in red. The magenta dotted line represents the amplitude I_P, computed by

$$I_P = \frac{2P_{PS}}{V_{HFP}}, \tag{42}$$

where V_{HFP} is the amplitude of the first harmonic component of v_{HFP}.

By analyzing the figure, many of the behaviors reported in the previous Sections can be recognized. The initial charge of C_{DCP} and C_{DCS} is very fast compared to that of the battery, so their voltage can always be considered in steady state.

After charging C_{DCP} the amplitudes I_G and I_S continue to rise, as described in subsection IV-C2. The increase of I_S implies that an increasing power P_{PS} is transferred to the secondary section of the BWV2H thus increasing the voltage V_{DCS}. This phenomenon is counteracted by the increase of I_B, by which an ever-increasing power is injected in the battery.

After about 3 s, when the maximum grid power is reached, the output of $C_{VDCP,PG}(s)$ is limited and the amplitude of i_G becomes constant. This change in slope of I_G is not instantaneously matched by I_S, which continues to increase for few instants. This causes a decrease of V_{DCP} voltage because the transferred power P_{PS} exceeds the power P_G drawn from the grid. This decrease implies that AL_V_{DCP}_C, through $C_{VDCP,PPS}(s)$ reduces $P_{PS,ref}$, and, consequently, $I_{S,ref}$. The reduction of the transferred power is not immediately recognized on the secondary section of the BWV2H. Therefore, the balance between i_S, which charges C_{DCS}, and I_B, which discharges it by transferring power to the battery, is temporarily lost. This phenomenon causes a decrease of V_{DCS} to which AL_V_{DCS}_B reacts through $C_{VDCS,PB}(s)$ by reducing $P_{B,ref}$. A new equilibrium is thus reached in which V_{DCP} and V_{DCS} are constant and close to their lower references while the battery is charged with constant power equal to the maximum available from the grid. As V_B increases, I_B slowly decreases in order to keep P_B constant.

This operating mode carries on until 6.5 s after the system power up. At this instant, V_B reaches its end-of-charge value $V_{B,M}$ and AL_V_B_B through $C_{VB,PB}(s)$ decreases $P_{B,ref}$. When the P_B reference becomes lower than the power reference generated by AL_V_{DCS}_B through $C_{VDCS,PB}(s)$, the interaction of the second type between the two algorithms forces a reduction of the power injected into the battery. Again, there is a temporary unbalance between I_B and i_S so that V_{DCS} increases slightly. This phenomenon is opposed by AL_V_{DCS}_C that, through $C_{VDCS,PPS}(s)$, decreases the reference for P_{PS} to prevent V_{DCS} from exceeding the upper reference. The decrease of P_{PS} with respect to P_G causes an increase of the V_{DCP} voltage to which AL_V_{DCP}_B opposes through $C_{VDCP,PG}(s)$ by reducing $P_{G,ref}$, thus causing a decrease in the amplitude of i_G. A new condition is therefore established in which the amplitudes of all the currents decrease with an approximately hyperbolic profile while V_{DCP}, V_{DCS} and V_B maintain a constant value close to their upper references.

The analysis of the behavior of I_P and I_S deserves some particular considerations. The BWV2H considered in this paper adopts series-series compensation so that, neglecting the resistive voltage drops across the coils and the resonance capacitors, when the system actually transfers some power, the first harmonic component of v_{HFP} is equal to the voltage induced across the primary coil by i_S. Consequently, the first harmonic amplitude V_{HFP} of v_{HFP} is proportional to I_S. Since the HFSC is not controlled during battery charging, V_{HFS} is proportional to V_{DCS} and remains practically constant during the whole charging process.

In order to adjust P_{PS} it is necessary to manupulate I_S by acting on V_{HFP}. This condition explains why the waveform of I_S resembles that of I_B, which in turn is approximately proportional to P_{PS}. On the other hand, there is no direct relationship between V_{HFP} and I_P since, considering the symmetry of the operation of the coupled coils, the latter is proportional to V_{HFS} and therefore is almost constant. This behavior is not in contrast with the fact that at the end of the charging process the transferred power is almost zero. In this condition, I_B is almost zero and the equivalent load seen at the terminals of the series of the secondary coil and its resonant capacitor is practically an open circuit. Consequently, the primary coil operates as if there were no coupling between the two sections of the BWV2H. The impedance offered by the series of the primary coil and its resonance capacitor is ideally zero, and therefore a voltage v_{HFP} with a very small first harmonic amplitude is enough to maintain I_P at a value significantly greater than zero.

B. BATTERY DISCHARGING

The battery discharge process from voltage $V_{B,N}$ to $V_{B,m}$ is illustrated in Fig. 42. According to the conventions of Fig. 2, the current I_B is always negative since it discharges the battery. However, in Fig. 42 its sign has been changed to facilitate comparison with the other currents. The current i_G is represented by the green line, and the amplitude I_P by the dashed magenta line. In this case, symmetrically to what has been explained in the previous subsection about I_P, I_S is not a controlled quantity and has been computed from P_{SP} and V_{HFS} using an equation similar to (42). It is represented in Fig. 42 by the blue line.

From the comparison between Figs. 41 and 42 it is possible to recognize many similarities between the charging and discharging processes. In this case also, the initial charge of C_{DCP} and C_{DCS} is very fast compared to the discharge of the battery, so their voltages can be considered always in steady state. After loading C_{DCS}, AL_V_{DCS}_B and AL_V_{DCS}_D interact in order to ramp up the power P_B extracted from the battery and the power P_{SR} transmitted to the primary section of the BWV2H while at the same time maintaining V_{DCS} between its higher and lower reference. This behavior is highlighted in the figure by the ramp trend of the current I_B and of the amplitude I_P. In the primary section, the received power P_{SP} charges C_{DCP} increasing V_{DCP} but this effect is opposed by AL_V_{DCP}_B which reacts by acting on $I_{G,ref}$ to increase the power injected into the grid. At a first glance, no difference is visible between the waveforms of i_G shown in Figs. 41 and 42, but in the latter case i_G is in phase opposition to v_G while in the former case they are in-phase.

Approximately 3 s after switching on the system, the maximum power that can be injected into the grid is reached, so the output of $C_{VDCP,PG}(s)$ is limited and I_G remains constant.

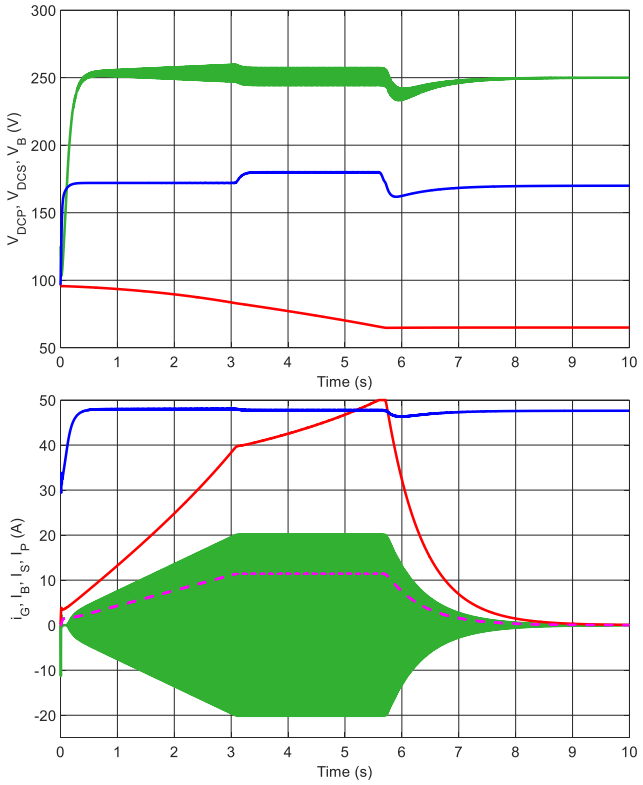

FIGURE 42. Top: VDCP voltage (with an offset of −200V) (green), V_{DCS} (blue), V_B (red). Bottom: i_G (green), I_S (blue), I_B (red), I_P (dashed magenta).

The change in slope of P_G is not instantaneously replicated on P_B which therefore charges C_{DCS} to a voltage close to $V_{DCS,ref,high}$. AL_V_{DCS}_B algorithm reacts reducing $P_{B,ref}$ to avoid a further increase of V_{DCS}. This action results in the presence of a cusp on the graph of I_B. From this instant, the battery is discharged at constant power and therefore, as V_B decreases, I_B increases in module. About 5.7 s from the start of the simulation, for few instants the absolute value of $I_{B,ref}$ is limited to its maximum value of 50 A, but immediately after V_B reaches the end-of-discharge value $V_{B,min}$ and the current discharging the battery is reduced. This involves a reduction of the current that charges C_{DCS} so that V_{DCS} decreases until AL_V_{DCS}_D reduces $P_{SP,ref}$, restoring the equilibrium condition and maintaining V_{DCS} constant. The reduction of the power coming from the secondary section causes a decrease in V_{DCP} that is compensated by AL_V_{DCP}_B, which reduces I_G. From now on, the battery discharge continues at a constant voltage so that the amplitude of I_B is reduced following an approximately hyperbolic curve. The same evolution is also followed by the power exchanged between the two sections of BWV2H and with the grid, as is recognizable from the profiles of I_G and I_P.

The amplitude I_S results about constant throughout the process. This behavior is explained in a symmetrical way to what was written about I_P in the previous subsection. During the battery discharge, the first harmonic component of v_{HFP} compensates for the voltage induced across the primary coil by the current i_S. Since the HFPC operates as a diode rectifier, V_{HFP} is proportional to V_{DCP} and follows its profile, so that I_S is also almost constant and shows only small variations corresponding to those of V_{DCP}.

VI. CONCLUSION

This paper faced the topic of developing a control strategy for a wireless battery charger system with V2H functionality. The proposed strategy is based on the control of the voltages of the dc buses and of the battery. It is carried out by manipulating the power exchanged between the grid and the battery through the static power converters and the coupled coils. This approach allows to satisfy the charging and discharging requirements of the battery without exceeding the voltage or current ratings of the converters. At the same time, the requirements about the grid power exchange are met.

The control strategy is arranged in two levels. The algorithms of the internal level process the current references and the feedback signals transduced from the BWV2H circuits to generate the gate commands for the static converters. The external level algorithms generate the references for the power to be exchanged between the various stages and between the two sections of the BWV2H.

The need to integrate the functioning of the different stages led to the development of interacting control algorithms. Their interaction allows to seamlessly switch from one operating condition to another, such as from constant current charging to constant voltage charging, without the need to exchange any information between them. The exchange of information between the two sections of the BWV2H is limited to one reference and one error quantity both during charging and discharging of the battery.

The functioning of the internal level algorithms has been verified in the Simulink environment using accurate circuital models of the power converters that constitute the BWV2H. In order to reduce the execution time, the operations of the external level algorithms have been simulated using the time-average models of the converters. The analysis of the simulation results confirms the correct functioning of all the algorithms. Finally, the whole control strategy has been implemented in a simulation model and checked both during charging and discharging of the battery. The obtained results, analyzed and discussed in detail in Section V, match perfectly with the expected ones.

APPENDIX A
ABBREVIATIONS

Table 3 collects the abbreviations and the definitions used in the text of the paper. In order to avoid unnecessary repetitions, the definitions given in Tab. 1 about the names of the control algorithms and of the controllers are not reported here.

TABLE 3. Abbreviations and definitions.

Abbreviation	Definition
BWV2H	Bidirectional wireless battery charger with V2H capability
BC	Bidirectional chopper
C_{DCP}	DC bus capacitor of the primary section
C_{DCS}	DC bus capacitor of the secondary section
C_{eq}	Capacitor used as equivalent of the battery
C_P	Compensating capacitors of the primary coil
C_S	Compensating capacitors of the secondary coil
D_x	Diode x of the power converters
EV	Electric vehicle
FEC	Front end converter
HFPC	High frequency primary converter
HFSC	High frequency secondary converter
I_B	Battery current
$I_{B,max}$	Maximum of I_B
$I_{B,min}$	Minimum of I_B
$I_{B,ref}$	Reference for I_B
I_{BC}	Average value of I_{DCS}
I_{DCP}	Rectified current at the input of the HFPC
I_{DCS}	Rectified current at the output of the HFSC
i_G	Input current absorbed from the domestic grid
$i_{G,err}$	Error on i_G
$i_{G,ref}$	Reference for i_G
I_G	Amplitude of i_G
i_P	Current in the primary coil
I_P	Amplitude of i_P
$I_{P,err}$	Error on I_P
$I_{P,ref}$	Reference for I_P
i_S	Current in the secondary coil
I_S	Amplitude of i_S
ISM	Industrial scientific and medical
$I_{S,err}$	Error on I_S
$I_{S,ref}$	Reference for I_S
L_G	Input filter inductance
LPF	Low pass filter
L_S	Inductance of the secondary coil
M_ϕ	Phase margin
NF	Notch filter
K_I	Integral gain of a PI controller
K_P	Proportional gain of a PI controller
P_B	Power injected in the battery
$P_{B,ref}$	Reference for P_B
P_G	Power absorbed from the grid
$P_{G,ref}$	Reference for PG
$P_{G,ref,max}$	Maximum positive value of $P_{G,ref}$
$P_{G,ref,min}$	Minimum negative value of $P_{G,ref}$
PI	Proportional integral controller
P_{PS}	Power transferred from the primary to the secondary section of the BWV2H
P_{SP}	Power transferred from the secondary to the primary section of the BWV2H
$R_{B,ESR}$	Battery equivalent series resistance
R_G	Parasitic resistance of L_G
T	Sampling period of the control system

TABLE 3. *(Continued.)* Abbreviations and definitions.

Abbreviation	Definition
T_x	Switch x of the power converters
τ_I	Time constant of a PI controller
TD	Transmission delay
TF	Transfer function
V2G	Vehicle to grid
V2H	Vehicle to home
V_B	Battery voltage
$V_{B,m}$	Minimum battery voltage
$V_{B,M}$	Maximum battery voltage
$V_{B,N}$	Nominal battery votage
V_{Ceq}	Voltage across C_{eq}
V_{DCP}	Voltage of the dc bus of the primary section
$V_{DCP,ref}$	Reference for V_{DCP}
$V_{DCP,ref,high}$	Higher value of $V_{DCP,ref}$
$V_{DCP,ref,low}$	Lower value of $V_{DCP,ref}$
V_{DCS}	Voltage of the dc bus of the primary section
$V_{DCS,ref}$	Reference for V_{DCP}
$V_{DCS,ref,high}$	Higher value of $V_{DCS,ref}$
$V_{DCS,ref,low}$	Lower value of $V_{DCS,ref}$
v_{FEC}	Voltage at the output of the FEC
$v_{FEC,ref}$	Reference for v_{FEC}
v_{HFP}	Voltage generated by the HFPC
V_{HFP}	First harmonic amplitude of v_{HFP}
$V_{HFP,ref}$	Reference for V_{HFP}
v_{HFS}	Voltage at the input of HFSC
V_{HFS}	First harmonic amplitude of v_{HFS}
$V_{HFS,ref}$	Reference for V_{HFS}
v_G	Domestic grid voltage
V_O	Voltage at the output of the BC
ω_{HF}	Supply angular frequency
ω_{PB}	Passband angular frequency
WPT	Wireless power transfer

APPENDIX B
CONTROL STRATEGY FLOWCHART

The following flow charts refer to the operations performed in the two sections of the BWV2H battery charger during battery charging and discharging. The symbol $C_{X,Y}(k)$ represents the discrete time version of the controller $C_{X,Y}(s)$. The operator $\min(\cdot,\cdot)$ gives the minimum of its arguments; the operator $\max(\cdot,\cdot)$ gives the maximum of its operators.

A. BATTERY CHARGING

1) PRIMARY SECTION

a. Initialize the system.
b. Acquire and process v_G, i_G, V_{DCP}.
c. Set $V_{DCP,ref} = V_{DCP,ref,high}$.
d. Implement $C_{VDCP,PG}(k)$ to work out $P_{G,ref,a}$.
e. Acquire $P_{G,ref,max}$ from an outer controller.
f. Set $P_{G,ref} = \min(P_{G,ref,a}, P_{G,ref,max})$.
g. Implement the PLL of Fig. 23.
h. Compute $i_{G,ref}$ using the scheme of Fig. 24.
i. Set $i_{G,err} = i_{G,ref} - i_G$.
j. Implement $C_{iG,VFEC}(k)$ to work out $v_{FEC,ref}$.

k. Set $V_{DCP,ref} = V_{DCP,ref,low}$.
l. Implement $C_{VDCP,PPS}(k)$ to work out $P_{PS,ref,a}$.
m. Send $P_{PS,ref,a}$ to the secondary section.
n. Receive $I_{S,err}$ from the secondary section.
o. Implement $C_{IS,VHFP}(k)$ to work out $V_{HFP,ref}$.
p. Use $v_{FEC,ref}$ to work out the control signals for the FEC.
q. Use $V_{HFP,ref}$ to work out the control signals for the HFPC.
r. Return to step b.

The pairs of steps "c", "d" and "k", "l" implement the interaction of the fist type between AL_V_{DCP}_B and AL_V_{DCP}_C. The steps "k", "l", and "m" implement the interaction of the second type between AL_V_{DCP}_C and AL_V_{DCS}_C. Step "f" avoids drawing from the grid a power higher than the available one.

2) SECONDARY SECTION

a. Initialize the system.
b. Turn off the switches of the HFSC.
c. Acquire and process I_B, V_B, I_S, V_{DCS}.
d. Set $V_{B,ref} = V_{B,ref,max}$.
e. Implement $C_{VB,PB}(k)$ to work out $P_{B,ref,a}$.
f. Set $V_{DCS,ref} = V_{DCS,ref,low}$.
g. Implement $C_{VDCS,PB}(k)$ to work out $P_{B,ref,b}$.
h. Set $P_{B,ref} = \min(P_{B,ref,a}, P_{B,ref,b})$.
i. Set $I_{B,ref,a} = P_{B,ref}/V_B$.
j. Set $I_{B,ref} = \min(I_{B,ref,a}, I_{B,max})$.
k. Implement $C_{IB,VO}(k)$ to work out $V_{O,ref}$.
l. Set $V_{DCS,ref} = V_{DCS,ref,high}$.
m. Implement $C_{VDCS,PPS}(k)$ to work out $P_{PS,ref,b}$.
n. Receive $P_{PS,ref,a}$ from the primary section.
o. Set $P_{PS,ref} = \min(P_{PS,ref,a}, P_{PS,ref,b})$.
p. Set $I_{S,ref} = \pi/2 \cdot P_{PS,ref}/V_{DCS,N}$.
q. Set $I_{S,err} = I_{S,ref} - I_S$.
r. Send $I_{S,err}$ to the primary section.
s. Use $V_{O,ref}$ to work out the control signals for the BC.
t. Return to step c.

The steps "d", "e", "f", "g", and "h" implement the interaction of the second type between AL_V_B_B and AL_V_{DCS}_B. The pairs of steps "f", "g" and "l", "m" implement the interaction of the fist type between AL_V_{DCS}_B and AL_V_{DCS}_C. The steps "l", "m", "n", and "o" implement the interaction of the second type between AL_V_{DCS}_C and AL_V_{DCP}_C. The step "h" avoids overcharging the battery or over-discharging C_{DCS}. The step "j" avoids injecting in the battery a too high current. The step "o" avoids overcharging C_{DCS} or over-discharging C_{DCP}.

B. BATTERY DISCHARGING

1) PRIMARY SECTION

a. Initialize the system.
b. Turn off the switches of the HFPC.
c. Acquire and process v_G, i_G, I_P, V_{DCP}.
d. Set $V_{DCP,ref} = V_{DCP,ref,low}$.
e. Implement $C_{VDCP,PG}(k)$ to work out $P_{G,ref,a}$.
f. Acquire $P_{G,ref,min}$ from an outer controller.
g. Set $P_{G,ref} = \max(P_{G,ref,a}, P_{G,ref,min})$.
h. Implement the PLL of Fig. 23.
i. Compute $i_{G,ref}$ using the scheme of Fig. 24.
j. Implement $C_{iG,VFEC}(k)$ to work out $v_{FEC,ref}$.
k. Set $V_{DCP,ref} = V_{DCP,ref,high}$.
l. Implement $C_{VDCP,PSP}(k)$ to work out $P_{SP,ref,a}$.
m. Receive $P_{SP,ref,b}$ from the secondary section.
n. Set $P_{SP,ref} = \min(P_{SP,ref,a}, P_{SP,ref,b})$.
o. Set $I_{P,ref} = \pi/2 \cdot P_{SP,ref}/V_{DCP,N}$.
p. Set $I_{P,err} = I_{P,ref} - I_P$.
q. Send $I_{P,err}$ to the secondary section.
r. Use $v_{FEC,ref}$ to work out the control signals for the FEC.
s. Return to step c.

The pairs of steps "d", "e" and "k", "l" implement the interaction of the first type between AL_V_{DCP}_B and AL_V_{DCP}_D. The steps "k", "l", "m", and "n" implement the interaction of the second type between AL_V_{DCP}_D and AL_V_{DCS}_D. The step "g" avoids injecting in the grid a power higher than the maximum allowable. According to the convention of Fig. 2, during the discharge of the battery, $P_{G,ref,a}$ and $P_{G,ref,min}$ are both negative. Hence, the $\max(\cdot, \cdot)$ operator is used to obtain the power reference with the smaller absolute value. The step "n" avoids overcharging C_{DCP} or over-discharging C_{DCS}. Following from Fig. 2, $P_{SP,ref,a}$ and $P_{SP,ref,b}$ are both positive and hence the $\min(\cdot, \cdot)$ operator can be used. It gives a positive result from which a positive reference for I_P is obtained.

2) SECONDARY SECTION

a. Initialize the system.
b. Acquire and process I_B, V_B, V_{DCS}.
c. Set $V_{B,ref} = V_{B,ref,min}$.
d. Implement $C_{VB,PB}(k)$ to work out $P_{B,ref,a}$.
e. Set $V_{DCS,ref} = V_{DCS,ref,high}$.
f. Implement $C_{VDCS,PB}(k)$ to work out $P_{B,ref,b}$.
g. Set $P_{B,ref} = \max(P_{B,ref,a}, P_{B,ref,b})$.
h. Set $I_{B,ref,a} = P_{B,ref}/V_B$.
i. Set $I_{B,ref} = \max(I_{B,ref,a}, I_{B,min})$.
j. Implement $C_{IB,VO}(k)$ to work out $V_{O,ref}$.
k. Set $V_{DCS,ref} = V_{DCS,ref,low}$.
l. Implement $C_{VDCS,PSP}(k)$ to work out $P_{SP,ref,b}$.
m. Send $P_{SP,ref,b}$ to the primary section.
n. Receive $I_{P,err}$ from the primary section.
o. Implement $C_{IP,VHFS}(k)$ to work out $V_{HFS,ref}$.
p. Use $V_{O,ref}$ to work out the control signals for the BC.
q. Use $V_{HFS,ref}$ to work out the control signals for the HFSC.
r. Go to step b.

The steps "c", "d", "e", "f", and "g" implement the interaction of the second type between AL_V_B_B and AL_V_{DCS}_B. The steps "k", "l", and "m" implement the interaction of the second type between AL_V_{DCS}_D and AL_V_{DCP}_D. The step "g" avoids overcharging C_{DCS} or over-discharging the battery. During discharging both $P_{B,ref,a}$ and $P_{B,ref,b}$ are negative and hence the $\max(\cdot, \cdot)$ operator is used to select the reference with the lower absolute value. The

step "i" avoids drawing from the battery a too high current. Also in this case the max operator is used because both $I_{B,ref,a}$ and $I_{B,min}$ are negative.

APPENDIX C
TFs OF THE CONTROL LOOPS

A. CONTROL ALGORITHMS OF THE INTERNAL LEVEL

The TF of the closed loop system relevant to AL_i_G_B is obtained from the block diagram of Fig. 7 in the form

$$TF_{iG,B}(s) = \frac{C_{iG,VFEC}(s)\,SD(s)\,\frac{1}{sL_G+R_G}}{1 + C_{iG,VFEC}(s)\,SD(s)\,\frac{1}{sL_G+R_G}LPF(s)}. \tag{a1}$$

The TF of the controller $C_{iG,VFEC}(s)$ has the structure given in (10) whilst the TFs of the sampling delay SD(s) and of the low pass filter LPF(s) are given by (16) and (22), respectively.

The TF relevant to AL_I_S_C is given in (a2). It comes from the block diagram of Fig. 12. The TF $C_{IS,VHFP}(s)$ of the controller encompasses an additional pole inserted to attenuate the high frequency gain of the closed-loop system. TD(s) represents the transmission delay due to the radio communication between the two sections of the BWV2H whilst PD(s) refers to the peak detector. These two TFs are equal to (16) and (22), respectively but, generally, with different values of the delay and of the time constant.

$$TF_{IS,C}(s) = \frac{C_{IS,VHFP}(s)\,TD(s)\,SD(s)\,K_{VHFP,IS}}{1+C_{IS,VHFP}(s)\,TD(s)\,SD(s)\,K_{VHFP,IS}PD(s)} \tag{a2}$$

The TF of the closed control loop relevant to AL_IP_D is nearly equal to (a2). As shown in (a3), the only formal differences are in the parameters of the controller $C_{IP,VHFS}(s)$ and in the gain between the voltage applied to secondary coil and the current flowing in the primary one.

$$TF_{IP,D}(s) = \frac{C_{IP,VHFS}(s)\,TD(s)\,SD(s)\,K_{VHFP,IP}}{1 + C_{IP,VHFS}(s)\,TD(s)\,SD(s)\,K_{VHFP,IP}PD(s)} \tag{a3}$$

The TF relevant to AL_I_B_B is given by (a4). It is obtained from Fig. 16 and results similar to (a1), provided that the PI parameters of $C_{IB,VO}(s)$ are used, and that L_B and $R_{B,ESR}$ are considered instead of L_G and R_G.

$$TF_{IB,B}(s) = \frac{C_{IB,VO}(s)\,SD(s)\,\frac{1}{sL_B+R_{B,ESR}}}{1+C_{IB,VO}(s)\,SD(s)\,\frac{1}{sL_B+R_{B,ESR}}LPF(s)} \tag{a4}$$

B. CONTROL ALGORITHMS OF THE EXTERNAL LEVEL

The TF of the closed loop system relevant to AL_V_{DCP}_B is derived from the block diagram of Fig. 21. After some simplifications is results as

$$TF_{VDCP,B}(s) = \frac{2C_{VDCP,PG}(s)\,TF_{iG,B}(s)\,\frac{1}{sC_{DCP}}}{1+2C_{VDCP,PG}(s)\,TF_{iG,B}(s)\,\frac{1}{sC_{DCP}}LPF(s)\,NF(s)}, \tag{a5}$$

where NF(s) is the TF of the notch filter given by (35) and $TF_{iG,B}(s)$ is given by (a1).

The TF of the closed loop system relevant to AL_V_{DCP}_C is derived from the block diagram of Fig. 26. It is similar to (a5), but encompasses the transmission delay. It is given by

$$TF_{VDCP,C}(s) = \frac{2C_{VDCP,PP}(s)\,TD(s)\,TF_{IS,C}(s)\,\frac{1}{sC_{DCP}}}{1+2C_{VDCP,PP}(s)\,TD(s)\,TF_{IS,C}(s)\,\frac{1}{sC_{DCP}}LPF(s)\,NF(s)}, \tag{a6}$$

where $TF_{IS,C}(s)$ is given by (a2).

The control algorithm AL_V_{DCP}_D has the control loop shown in Fig. 29. From it the following TF is derived

$$TF_{VDCP,D}(s) = \frac{2C_{VDCP,PSP}(s)\,TF_{IP,D}(s)\,\frac{1}{sC_{DCP}}}{1+2C_{VDCP,PSP}(s)\,TF_{IP,D}(s)\,\frac{1}{sC_{DCP}}LPF(s)\,NF(s)}, \tag{a7}$$

where $TF_{IP,D}(s)$ is given by (a3). TF (a7) is similar to (a6), apart for the transmission delay TD(s), which does not appear in the latter case.

The closed loop TF relevant to the algorithm AL_ V_{DCS}_B is obtained from the block diagram of Fig. 31 in the form

$$TF_{VDCS,B}(s) = \frac{2V_{DCS,N}C_{VDCS,PB}(s)\,TF_{IB,B}(s)\,\frac{1}{sC_{DCS}}}{1+2V_{DCS,N}C_{VDCS,PB}(s)\,TF_{IB,B}(s)\,\frac{1}{sC_{DCS}}LPF(s)}, \tag{a8}$$

where $TF_{IB,B}(s)$ is given by (a4).

The algorithm AL_V_{DCS}_C has the closed loop block diagram drawn in Fig. 33. Its corresponding TF is

$$TF_{VDCS,C}(s) = \frac{2C_{VDCS,PPS}(s)\,TF_{IS,C}(s)\,\frac{1}{sC_{DCS}}}{1+2C_{VDCS,PPS}(s)\,TF_{IS,C}(s)\,\frac{1}{sC_{DCS}}LPF(s)}. \tag{a9}$$

The TF of the algorithm AL_VDCS_D is derived from the block diagram of Fig. 36 obtaining

$$TF_{VDCS,D}(s) = \frac{2C_{VDCS,PSP}(s)\,TF_{IP,D}(s)\,\frac{1}{sC_{DCS}}}{1+2C_{VDCS,PSP}(s)\,TF_{IP,D}(s)\,\frac{1}{sC_{DCS}}LPF(s)}, \tag{a10}$$

that has the same structure of (a9).

Finally, according to the block diagram of Fig. 38, the closed loop TF relevant to the algorithm AL_V_B_B is

$$TF_{VB,B}(s) = \frac{2C_{VB,PB}(s)\,TF_{IB,B}(s)\left(\frac{1}{sC_{eq}}+R_{B,ESR}\right)}{1+2C_{VB,PB}(s)\,TF_{IB,B}(s)\left(\frac{1}{sC_{eq}}+R_{B,ESR}\right)LPF(s)}. \tag{a11}$$

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MANUELE BERTOLUZZO received the M.S. degree in electronic engineering and the Ph.D. degree in industrial electronics and computer science from the University of Padova, Padua, Italy, in 1993 and 1997, respectively.

In 2000, he joined the Scientific Disciplines' Group Electric Converters, Machines, and Drives, Department of Industrial Engineering, University of Padova, as a Researcher. Since 2015, he has been an Associate Professor and holds the lectureship of road electric vehicles and systems for automation for the master's degree in electric engineering. He is involved in analysis and design of power electronics systems, especially for wireless charging of electric vehicles battery.

ABHAY KUMAR received the B.Tech. degree in electrical engineering from DRIEMS, Cuttack, India, in 2012, and the M.E. degree in electrical engineering with specialization in power electronics from the BIT Mesra, Ranchi, India, in 2014. He is currently pursuing the Ph.D. degree with the University of Padova, Italy.

He was an Assistant Professor with NPSEI, Pithoragarh, India, from 2014 to 2019. His research interests include power electronics and control systems for power electronics converters, and wireless charging of electric vehicle.

AMRITANSH SAGAR (Senior Member, IEEE) was born in Saharsa, India. He received the B.Tech. degree in electrical and electronics engineering from the Birla Institute of Technology, Mesra, Jharkhand, India, in 2011, and the M.Tech. degree in power electronics and drives from the Sardar Vallabhbhai National Institute of Technology, Surat, India, in 2017. He is currently pursuing the Ph.D. degree with the Department of Industrial Engineering, University of Padova, Padua, Italy.

From August 2017 to December 2018, he was an Assistant Professor with Silver Oak University, Ahmedabad. From March 2019 to June 2020, he was a Junior Research Fellow with VIT, Vellore, India. His research interests include wireless power transfer, and modeling, design, and control of power.

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