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RESEARCH ARTICLE

Cryogenic In-Memory Bit-Serial Addition Using Quantum Anomalous Hall Effect-Based Majority Logic

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ABSTRACT Cryogenic compute in-memory (CiM) is a promising alternative to room temperature von-Neumann technologies since cryogenic electronics can provide high speed and energy efficiency while CiM can solve the von-Neumann and memory wall bottlenecks. Moreover, CiM can reduce the energy requirement which can solve the cooling issues associated with the cryogenic systems. Here, we demonstrate a cryogenic in-memory full adder using Majority logic implemented in quantum anomalous Hall effect (QAHE)-based memory system. The utilization of QAHE-based memory enables a number of unique advantages for Majority logic – (i) Majority outputs correspond to voltages with two opposite polarities irrespective of the number of inputs and hence, only a simple voltage comparator can be used, (ii) in-memory Majority logic (and hence, full adder) does not require any modification in the peripheral circuitry, and (iii) the topologically protected Hall resistance states provide robustness against external variations. This work makes the first attempt to harness the unique advantages of QAHE phenomenon in implementing complex operations beyond the primitive bitwise Boolean operations.

INDEX TERMS Cryogenic, full adder, in-memory computing, majority logic, quantum anomalous Hall effect, twisted bilayer graphene.

I. INTRODUCTION

Cryogenic electronics is one of the most promising alternatives to the complementary metal-oxide-semiconductor (CMOS) technology, thanks to its fast and energy efficient operations as well as the capability of solving the power dissipation issue resulting from the aggressive CMOS scaling [1], [2], [3], [4]. However, cryogenic electronics also suffer from *von-Neumann* and *memory wall* bottlenecks because of their *von-Neumann*- like architecture [5], [6]. *Von-Neumann* bottleneck affects the energy efficiency of the system as the data transfer between the processing and memory units consumes a huge amount of energy. On the other hand, *memory wall* bottleneck affects the throughput of the system because the processing unit is typically faster than memory and has to wait for the data transfer from the memory unit. Compute-in-memory (CiM) architectures can solve both of these bottlenecks by processing data inside the memory array. However, unlike the CMOS implementation, CiM accommodates usually the homogeneity of logic gates (only NAND or only NOR) [7]. In this regard, in-memory Majority logic proves to be more efficient compared to other logic primitives since Majority along with NOT gate is considered to be functionally complete.

Majority logic is a Boolean logic primitive which generates an output of logic '1' when there is a greater number of

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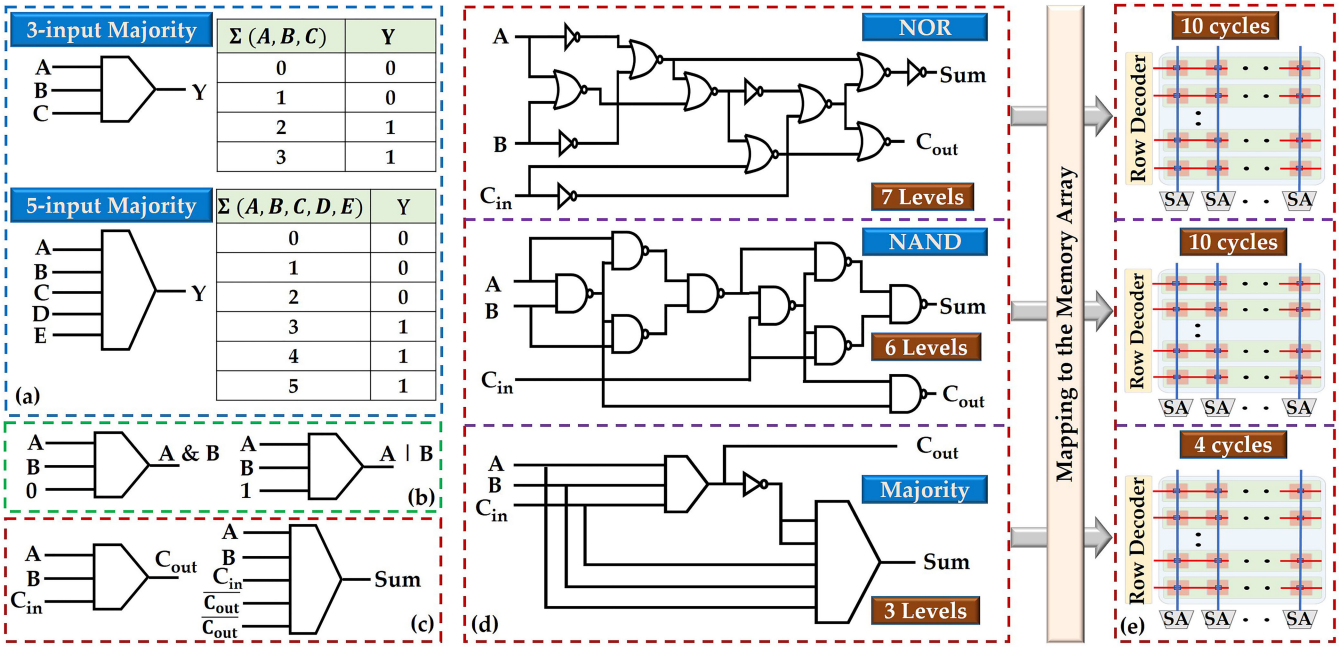

FIGURE 1. (a) Truth tables for 3-input and 5-input Majority logic. Implementation of (b) AND and OR gates, and (c) full adder using Majority logic. (d) Logic level and (e) in-memory implementation of full adder using NAND, NOR, and Majority. The use of Majority logic reduces the logical depth and number of cycles.

logic '1' among the inputs. Fig. 1(a) shows the symbols and truth tables for 3-input and 5-input Majority logics. The logic expression of a 3-input Majority gate is-

$$Maj\,(a, b, c) = (a\&b)\,|(b\&c)|\,(c\&a) \tag{1}$$

where a, b, and c are the inputs. The idea of Majority logic was first put forward in 1960 [8] and several beyond CMOS devices such as spin waves [9], single electron tunneling [10], quantum dot cellular automata [11], nanomagnetic logic [12], superconducting Josephson junction [13], etc. have been used to implement Majority logic. The advantages of Majority logic are- (i) other Boolean logic gates such as AND and OR can be implemented using Majority (Fig. 1(b)), (ii) in some technologies (for example, quantum dot cellular automata), the implementation of Majority logic is simpler and more efficient compared with other logic primitives such as NAND, NOR, and XOR, and (iii) Majority logic enables the efficient implementation of arithmetic-intensive systems with lower number of gates [7], [9], [10], [11]. The utilization of Majority logic in arithmetic-intensive circuits reduces the logical depth up to 33% compared to the AND implementation [14].

Usually in CiM architectures, one logic primitive (either NAND or NOR) is implemented and then, all the other logic functions are implemented based on that. Therefore, implementing an in-memory full adder requires the XOR gate to be implemented using either NAND or NOR which consequently increases the required logic levels. For example, the implementation of a XOR gate requires a sequence of four NAND operations. However, a 1-bit full adder can be implemented using one 3-input and one 5-input Majority gates (Fig. 1(c)) since the logic expression of a 1-bit full adder can be simplified to-

$$C_{out} = Maj(A, B, C_{in})$$

and,

$$Sum = Maj(A, B, C_{in}, \overline{C_{out}}, \overline{C_{out}}) \tag{2}$$

Fig. 1(d) shows the implementation of a 1-bit full adder using NAND, NOR, and Majority logic along with NOT gate which illustrates that the Majority gate-based implementation reduces the logic level by 50% (57.14%) compared to the NAND (NOR)-based implementation [7]. Now, when the full adders are mapped inside the memory system for in-memory implementation, the use of Majority logic reduces the number of required cycles by 60% compared to the NAND and NOR-based implementations (Fig. 1(e)) [7].

Here, we present a cryogenic in-memory Majority logic which is further used to design an in-memory full adder. Full adder is a critical component for the processing units in both room temperature and cryogenic electronics as it is required in the arithmetic logic unit, floating point unit, and address generation to access the memory unit [15]. Therefore, an efficient cryogenic full adder is required in the control processor of quantum computers, cryogenic electronics, and the processor used in the spacecrafts. In this work, we utilize a quantum anomalous Hall effect (QAHE)-based memory array [16] to implement the in-memory Majority function and full adder. QAHE-based memory array shows two unique characteristics that benefits the implementation of in-memory Majority logic- (i) during read operation, we get positive (negative)

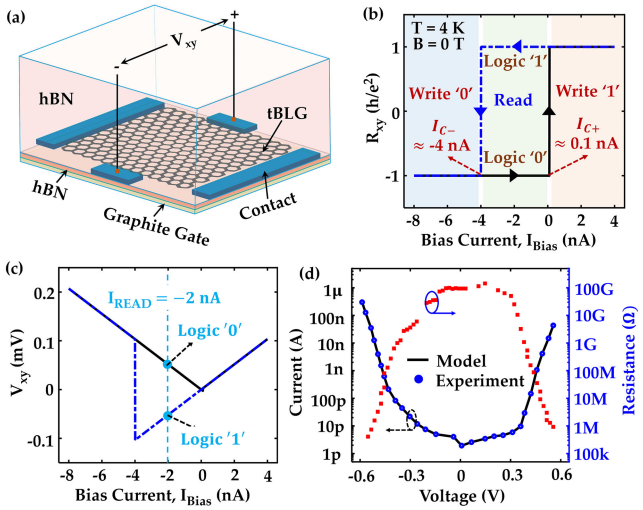

FIGURE 2. (a) Device schematic, (b) R_{xy} and (c) V_{xy} as a function of I_{Bias} of tBLG moiré heterostructure. (d) I-V characteristics of MIEC material-based selector.

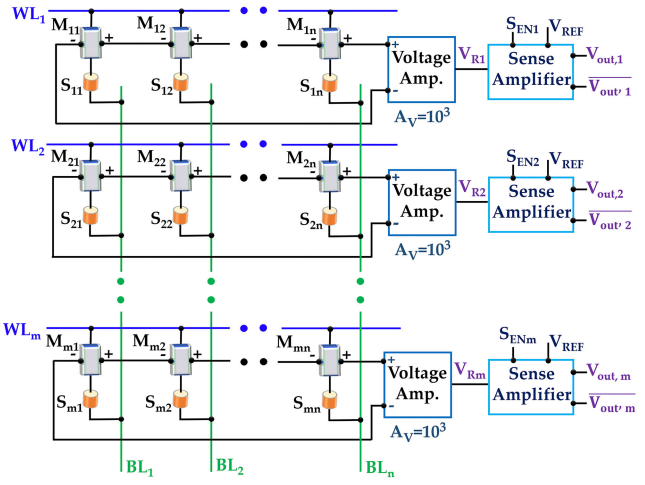

FIGURE 3. Schematic of the QAHE-based cryogenic memory system [16].

Hall voltage (V_{xy}) across a cell for logic '0' ('1') state and (ii) V_{xy} of all the cells in a row are algebraically summed. These two features lead to positive (negative) voltage corresponding to the Majority '0' ('1') output irrespective of the number of inputs which dramatically simplifies the design of peripheral circuitry.

The rest of the paper is organized as follows- section II describes the QAHE-based cryogenic memory system. In section III, we discuss how we utilize the QAHE phenomenon to perform in-memory Majority logic and full adder operation based on the Majority logic. Section IV presents the comparative analysis and highlights the advantage of using QAHE phenomenon to perform in-memory Majority logic and full adder operation. Lastly, section V concludes the paper by summarizing the findings.

II. QAHE-BASED CRYOGENIC MEMORY SYSTEM

We first discuss the QAHE phenomenon and QAHE-based cryogenic memory system that was proposed in [16]. Although different topological materials can exhibit the QAHE phenomenon, for the proof of concept, twisted bilayer graphene (tBLG) (twisted by an angle of 1.15°) on hexagonal boron nitride (hBN) moiré heterostructure was used (schematic shown in Fig. 2(a)) [17]. The tBLG moiré heterostructure offers several distinct advantages, making it a highly promising platform for a range of electronic and quantum devices. Firstly, it demonstrates remarkable Hall resistance quantization, achieving values within 0.1% of h/e^2 (where h is Planck's constant and e is the charge of an electron) even in the absence of a magnetic field, setting it apart from other magnetically doped systems. Secondly, the quantized Hall resistance (R_{xy}) states in tBLG exhibit impressive thermal stability, persisting at elevated temperatures of several Kelvin. Moreover, tBLG allows for precise and controlled switching of the R_{xy} states using nano-ampere level currents. This fine-grained control over the electronic states further underscores the versatility of this heterostructure. Finally, in tBLG, R_{xy} values remain largely unaffected up to temperatures of approximately 4 K. This resistance to temperature fluctuations highlights the robustness and reliability of tBLG for practical applications.

QAHE features two quantized Hall resistance (R_{xy}) states at zero magnetic field. As shown in Fig. 2(b), the application of suitable electrical current (I_{Bias}) can cause non-volatile switching of the R_{xy} states. The R_{xy} *vs* I_{Bias} characteristics shows two states of R_{xy} ($-h/e^2$ and $+h/e^2$) which define the memory states (logic '0' and '1', respectively). It is also evident from Fig. 2(b) that we can apply suitable I_{Bias} for write ($< I_{C-}$ for write '0' and $> I_{C+}$ for write '1') and read ($I_{C-} < I_{Bias} < I_{C+}$) operations. In order to implement the in-memory Majority logic, we necessarily perform the read operation (discussed later). Now, for sensing the memory state stored in the cell, the dependence of V_{xy} ($= I_{Bias} \times R_{xy}$) on I_{Bias} (shown in Fig. 2(c)) is utilized. Here, when a read current is applied, two V_{xy} with opposite polarities emerge for the two memory states. As shown in Fig. 2(c), a read current of $-2nA$ results in V_{xy} of around $+50\mu V$ and $-50\mu V$ for logic '0' and '1', respectively. More detailed discussion on the QAHE phenomenon is available in [17] and [18]. As we will discuss later, this distinction of V_{xy} in terms of polarity provides a significant advantage while implementing the in-memory Majority functionality.

Next, we discuss the QAHE-based crosspoint memory system. Fig. 3 shows the schematic of the complete memory array. QAHE-based cryogenic memory can operate with ultra-low-power and can provide high scalability (scalable to nanometer). Therefore, this memory system has the potential to solve the lack of a fast, low-power, and scalable memory for different promising cryogenic applications [4], [19], [20]. Also, this memory system features voltages of opposite polarity for two logic states during read, and high sense margin which allows the use of a simple voltage comparator as the sensing peripheral circuitry. In this memory system, a Cu-containing mixed-ionic-electronic-conduction (MIEC)

TABLE 1. Implementation of 3-input and 5-input in-memory Majority logic in QAHE-based memory.

	∑ Inputs	V_R (mV)	V_{out} (logic)	
3-input	0	150	0	$V_R > 0$, $V_R < 0$, $V_{out} = \{0, 1\}$
	1	50	0	
	2	-50	1	
	3	-150	1	
5-input	0	250	0	
	1	150	0	
	2	50	0	
	3	-50	1	
	4	-150	1	
	5	-250	1	

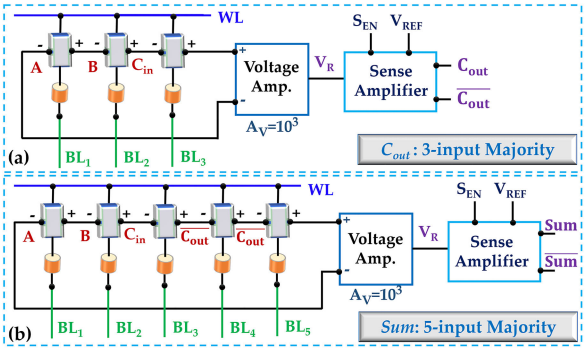

FIGURE 4. Calculation of (a) C_{out} and $\overline{C_{out}}$ and (b) *Sum* using 3-input and 5-input Majority logic, respectively.

material-based selector [21] is utilized to make sure that the applied current only flows through the specific cell during write and read operations. To implement MIEC-based selector, a look-up table (LUT)-based Verilog-A model is used [16]. The *I-V* characteristics of the MIEC-based selector along with the validation of the model is shown in Fig. 2(d). Details about the write and read operations of this QAHE-based memory can be found in [16].

III. IN-MEMORY MAJORITY LOGIC AND FULL ADDER

In this work, we utilize the same QAHE-based crosspoint memory array of Fig. 3 to implement in-memory Majority logic. In this array, a voltage amplifier [22] is used to convert the microvolt level V_{xy} to millivolt level. The output of the voltage amplifier is then connected to a voltage comparator, which can be implemented using either a Josephson junction FET-based [23] comparator or a CMOS-based [24] comparator, both suitable for cryogenic applications. CMOS voltage comparators excel at distinguishing voltage levels in the millivolt range, while the Josephson junction FET-based comparator can operate with microvolt-level voltages. Consequently, if the Josephson junction FET-based or a similar voltage comparator is utilized, the need for a separate voltage amplifier can be eliminated. This allows for a streamlined design, as the microvolt-level signals can be directly processed by the Josephson junction FET-based comparator without requiring

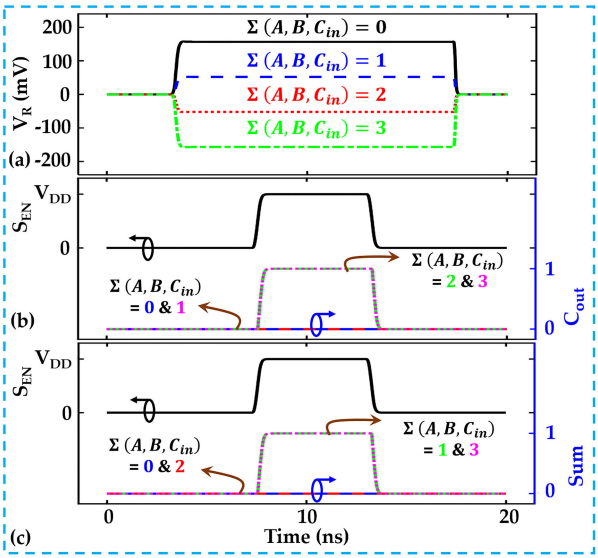

FIGURE 5. Simulation results for Majority-based in-memory 1-bit full adder.

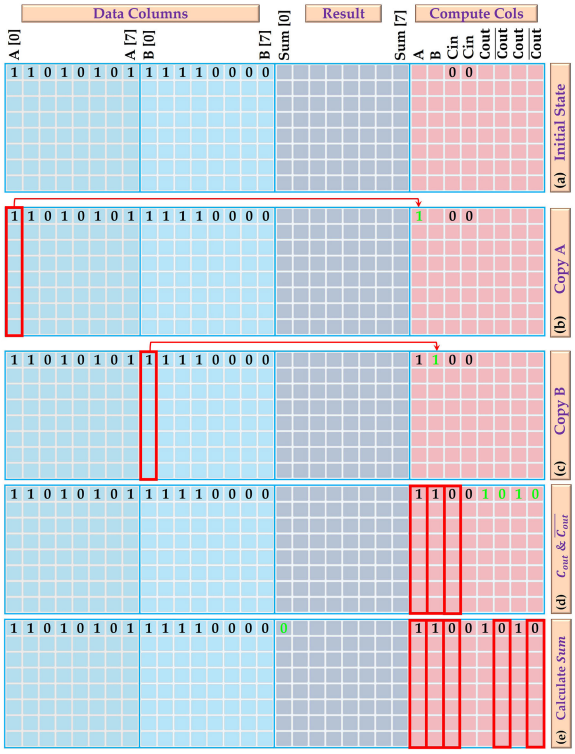

FIGURE 6. Steps of in-memory bit-serial addition in a QAHE-based cryogenic memory system.

an additional amplification stage. Now, to perform the Majority functionality, when odd number of cells are activated in a row, we get two distinguishable voltage levels (positive and negative) corresponding to the two logic outputs ('0' and '1', respectively). Table 1 shows the truth table along with the corresponding voltage levels for 3-input and 5-input Majority. As evident from this table, the Majority function

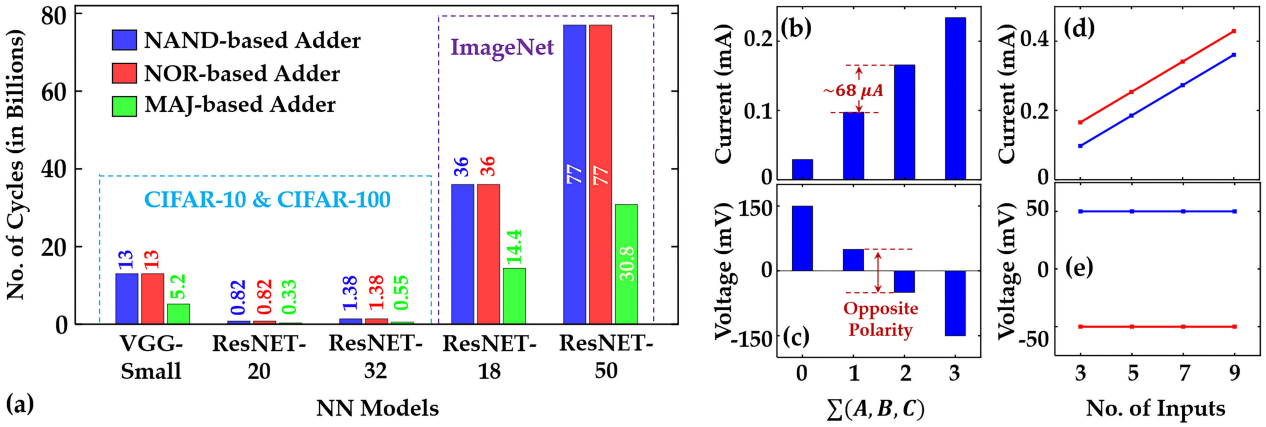

FIGURE 7. Comparison of our proposed QAHE-based in-memory majority logic with other approaches, highlighting the advantage of using QAHE.

can be implemented in the QAHE-based memory using only a simple voltage comparator which is used for the memory read operation. This advantage is unique to the QAHE-based memory system and there are two major reasons- (i) V_{xy} with two opposite polarities for two memory states and (ii) adding the V_{xy} of all the cells in a row. Another major advantage of QAHE-based in-memory Majority is that we will get this same distinguishability (positive and negative levels) in the voltage irrespective of the number of inputs (3, 5, 7, etc.). The cases of 3 and 5 inputs are shown in Table 1.

Next, we demonstrate the simulation results to implement 1-bit full adder using the in-memory Majority logic with the QAHE-based memory system. In our simulation, we utilize the Verilog-A-based and LUT-based models from [16] (both validated with experimental results) for the QAHE cells and the selector, respectively. We implement the 1-bit full adder by implementing one 3-input and one 5-input Majority logic. Fig. 4(a) shows the array structure to calculate C_{out} where three QAHE cells in a row storing the three inputs (A, B, and C_{in}) are activated. In this step, we calculate and store both C_{out} and $\overline{C_{out}}$ since C_{out} will be used in the next bit addition as C_{in} and $\overline{C_{out}}$ is required to calculate Sum according to (2). Therefore, the sense amplifier should be able to calculate both out and $\overline{out}$ at the output. Fig. 4(b) shows the activation of five QAHE cells to calculate Sum where three cells store the three inputs and two cells store $\overline{C_{out}}$. The simulation results for all the possible input combinations are shown in Fig. 5. Fig. 5(a) shows the different levels of voltage at the output of the voltage amplifier after applying suitable I_{Bias} to the cells storing the inputs. Then, when we apply the enable signal and reference voltage to the sense amplifier, we get C_{out} and $\overline{C_{out}}$ at the output performing 3-input Majority (Fig. 5(b)). Then, we store C_{out} and $\overline{C_{out}}$, and in the next cycle, we activate five cells together to perform 5-input Majority logic to calculate Sum (Fig. 5(c)).

Finally, we show an example of performing bit-serial addition in QAHE-based memory array using the in-memory Majority logic (Fig. 6). We consider that each of the inputs (A and B) consists of eight bits and we perform the Majority functionality by activating different columns in the same row. Here, we divide the memory array into data columns to store the inputs and outputs, and compute columns to calculate C_{out} and Sum. We again divide the data columns to store the inputs (A in the first eight columns and B in the next eight columns) and the addition result (Sum in the next eight columns). We use the compute columns to store the copied versions of A and B, C_{in}, C_{out}, and $\overline{C_{out}}$. In the compute columns, we store both C_{out}, and $\overline{C_{out}}$ twice because we will need C_{out} for the next bit addition and two $\overline{C_{out}}$ to calculate Sum. In Fig. 6, we only show the addition of the first bits of A and B. Fig. 6(a) shows the initial state where the inputs (A, B, and C_{in}) are stored. In the next two cycles (Fig. 6(b) and (c), respectively), we copy $A[0]$ and $B[0]$ to the corresponding compute columns (labelled A and B, respectively). Afterwards, we calculate and store C_{out} and $\overline{C_{out}}$ by activating three compute columns storing $A[0]$, $B[0]$, and C_{in}(Fig. 6(d)). In the final step, we calculate Sum by activating five compute columns (Fig. 6(e)) and store the result in the designated location. Similarly, the addition of the next bit will be performed where C_{out} will be used as C_{in}. As shown in Fig. 6, the proposed adder adds an overhead of eight additional columns to perform the computation. Note, even if we consider larger input size (1024 or 2048 bits instead of 8) of the inputs for different applications, the number of additional columns required will still be eight due to the use of bit-serial addition mechanism [15]. Another major advantage of this proposed in-memory adder is that due to the use of QAHE-based memory array, no modification in the memory array and the sense amplifier is required whereas all the existing in-memory implementations of adder require some degree of modification in the peripheral circuitry. Moreover, in terms of variation tolerance, the use of QAHE-based memory array entails a major advantage because the two R_{xy} states are topologically protected and remain constant at $-h/e^2$ or $+h/e^2$ for any temperature below 4 K [6], [17].

IV. COMPARATIVE ANALYSIS

In this section, we compare our proposed QAHE-based in-memory full adder with NAND and NOR- based implementations. AdderNet [25], a deep neural network (DNN), shows that the computationally complex multiplication operations can be replaced with addition. AdderNet not only achieves same accuracy as the binary and convolutional neural networks but also improves latency because the latency of multiplication is higher than addition. Here, we show the superiority of our proposed QAHE-based in-memory addition hardware for implementing AdderNet. Fig. 7(a) shows the number of cycles required to implement different DNN models for different datasets with NAND-, NOR-, and the proposed QAHE-based in-memory adders. Here, VGG-Small, ResNet-20, and ResNet-32 models are used for CIFAR-10 and CIFAR-100 datasets, while ResNET-18 and ResNet-50 models are used for ImageNet datasets [25]. In all the cases, we show that the QAHE-based in-memory adder requires a significantly smaller number of cycles than NAND and NOR implementations.

Next, we show the advantage of using QAHE to implement the Majority logic, comparing with the memristor-based implementation. Memristors have already been utilized to develop non-volatile memory [26], CiM architecture [27], neuromorphic system [28], associative memory [29], [30], etc. at room temperature. However, we show that our proposed QAHE-based Majority logic can offer unique advantage compared to the memristor-based implementations. Here, we use the one-transistor one resistor (1T1R) memristive array framework from [26] to simulate the Majority logic. Fig. 7(b) shows that for 3-input Majority logic, the memristive memory provides a separation of around $68\mu A$ (depends on the memristor and read voltage) for the sensing purpose. Note, all the conventional memory platforms (such as memristive, ferroelectric, spintronic, phase-change, etc.) will require differentiating between two current levels with same polarity (positive/negative) to detect the majority output. However, in our proposed QAHE-based majority logic, we get two voltage levels with opposite polarities (Fig. 7(c)). Moreover, for majority logic with higher inputs, it is seen that both the current levels (used to detect the majority output) increase (Fig. 7(d)) and require different reference levels to be set for the sensing operation. However, in the QAHE-based approach, we get voltage levels with opposite polarities and with same values (Fig. 7(e)) for any number of inputs. Therefore, the same sensing circuitry can be used to perform Majority logic with any number of inputs.

V. CONCLUSION

In-memory computing is envisioned to provide a unique advantage for cryogenic systems by improving the energy efficiency and consequently, reducing the cooling issue. Here, we proposed an in-memory adder based on Majority logic using the QAHE-based cryogenic memory. The QAHE-based memory allows us to implement in-memory Majority functionality without any modification in the peripheral circuitry. A simple voltage comparator can be used as the sense amplifier like the memory read operation. Finally, we utilize this in-memory Majority functionality to implement an in-memory adder which requires total $4n+1$ cycles for inputs with n bits. This proposed QAHE-based in-memory adder can be a promising candidate to perform addition tasks in different cryogenic applications.

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