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RESEARCH ARTICLE

Influence of Hole Current Crowding on Snapback Breakdown in Multi-Finger MOSFETs

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ABSTRACT The snapback breakdown behavior of multi-finger MOSFETs was investigated using a device simulation. It is shown that snapback breakdown voltage (SNBV) varies depending on the source/drain configuration, even with the same two-finger structure. This results from the hole current crowding below the shared source, which further increases forward biasing at the source-substrate junction and eventually leads to premature activation of the parasitic bipolar junction transistor (BJT). Double-pocket implantation successfully suppresses the hole current crowding and also achieves higher SNBV for two-finger MOSFET.

INDEX TERMS Snapback breakdown, impact ionization, parasitic bipolar junction transistor (BJT), pocket implantation, multi-finger MOSFET.

I. INTRODUCTION

The application of high-voltage MOSFETs has expanded considerably in recent years, and breakdown voltage has become a more important parameter. It determines the highest allowable voltage and restricts the power-handling capability of discrete MOSFET devices. Furthermore, the breakdown voltage determines the circuit reliability of nonvolatile memories where the peripheral circuit is exposed to high voltage stress [1]. Especially in the case of NAND flash memory, high voltage for the program and erase operation causes thermal damage to the peripheral circuit, leading to an entire defective bit line or word line. Therefore, an accurate understanding of the breakdown behavior is required for MOSFET device design and circuit reliability evaluation.

The underlying physics of breakdown in MOSFETs is now quite clear thanks to previous pioneering research [2], [3], [4], [5], [6]. The avalanche breakdown, mainly observed in long-channel MOSFETs, originates from the impact ionization occurring in the high-field region around the drain [2]. In avalanche breakdown, the multiplication factor and channel current are sufficiently large to ignore the substrate current feedback, so the abrupt increase in current is dominated by the secondary electrons being swept into the drain [3]. In contrast, snapback breakdown, induced by impact ionization and parasitic bipolar junction transistor (BJT), generally occurs in short-channel MOSFETs [4]. The secondary holes drift into the substrate, causing a voltage drop. Then, the source-substrate junction becomes forward-biased, and the parasitic BJT emerges, as depicted in Fig. 1a. The voltage drop (V_{sup}) can be expressed as the product of the hole current flowing through the substrate (I_{sub}) and the substrate resistance (R_{sub}). When V_{sub} reaches approximately 0.7 V, the parasitic BJT is completely turned on, and the electrons from the source are no longer confined to the channel but move through the substrate to the drain [5]. Thus, the drain current increases sharply, resulting in serious thermal failures such as melted packages or fused bonding wires. As the negative influence of parasitic BJTs on MOSFETs becomes stronger with decreasing channel length [6], snapback

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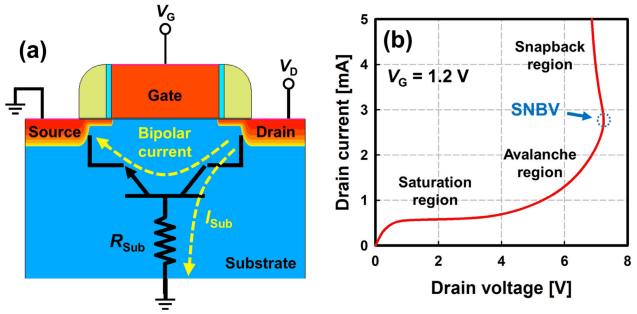

FIGURE 1. (a) Schematic diagram of an n-channel MOSFET. (b) Output curve of the simulated MOSFET with the snapback region.

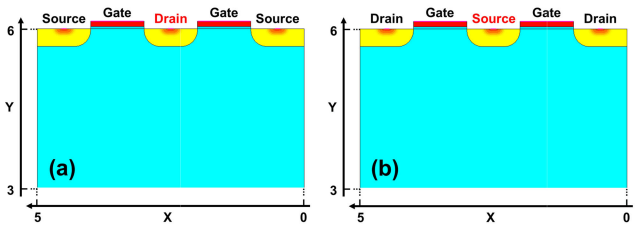

FIGURE 2. Simulated two-finger MOSFETs: (a) shared drain structure and (b) shared source structure.

TABLE 1. Summarized device parameters of the two-finger MOSFETs.

Parameter	Value
Gate length	1 μm
Gate oxide thickness	40 nm
Source/drain doping	1×10^{17} cm^{-3} (n-type)
Source/drain contact doping	1×10^{20} cm^{-3} (n-type)
Source/drain junction depth	330 nm
Substrate doping	1×10^{16} cm^{-3} (p-type)
Substrate thickness	6 μm

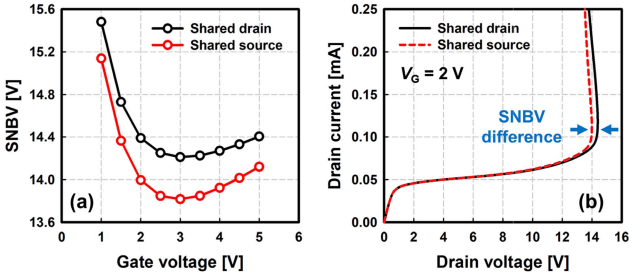

FIGURE 3. (a) Extracted SNBV as a function of V_G. (b) Output curves of the two-finger MOSFETs representing the SNBV difference.

breakdown is considered one of the major failure mechanisms of short-channel MOSFETs. Although snapback breakdown has been analytically and numerically studied [7], [8], [9], [10] at the single-device level, to the best of our knowledge, few studies have been performed on the snapback breakdown behavior of multi-finger MOSFETs.

In this study, the snapback breakdown behavior of multi-finger MOSFETs was investigated using a device simulation. Based on the simulation results, pocket implantation was introduced, and its effect on snapback breakdown was evaluated as a function of the pocket location.

II. SIMULATION ENVIRONMENT

A technology computer-aided design (TCAD) simulation was performed using a commercial device simulator [11]. Fig. 1b represents an exemplary simulated output curve of an n-channel 200 nm MOSFET. The drain current does not simply rise with the drain voltage (V_D), but folds at a certain point. A current source was forced at the drain to obtain this snapback region [12]. The snapback breakdown voltage (SNBV) value is extracted at the V_D where the output curve first folds. For device physics, Philips unified mobility, van Overstraeten impact ionization, Shockley-Read-Hall recombination and Fermi-Dirac distribution were used. Particularly, a thermodynamic model was applied to include the self-heating effect and secondary breakdown.

Fig. 2 shows two simulated two-finger MOSFETs. The first is called the shared drain structure, in which the drain is located between the two sources. The second is called the shared source structure, where the source is located between the two drains. Except for the source/drain configuration, all the other parameters were the same in both cases. The detailed device parameters are listed in Table 1. Although the substrate thickness is 6 μm, all figures in this study show only the upper 3 μm area of the substrate to focus on the hole current behavior near the channel. We fixed the source and substrate voltages at 0 V throughout this study.

III. SNBV DIFFERENCE IN MULTI-FINGER MOSFET

Fig. 3a shows the simulated SNBV of the two-finger MOSFETs under various gate voltage (V_G) conditions. Regardless of V_G, the shared source structure always has a lower SNBV than the shared drain structure. A detailed discussion is presented in Fig. 3b. When V_G was fixed at 2 V, there was no difference between the output curves of the shared drain and source structure up to the saturation region. However, in the avalanche region, the shared source structure shows a more abrupt increase in current compared to the shared drain structure. Thus, snapback breakdown occurs at V_D of 14.0 V in the shared source structure, whereas at V_D of 14.4 V in the shared drain structure. The SNBV difference between the two structures results from the hole current crowding effect, which is observed only in the shared source structure. Fig. 4 compares the hole current densities of the shared drain and source structure under the same bias conditions. As previously mentioned, the holes generated by impact ionization move toward the substrate. In this process, owing to the high potential at the drain, holes tend to move first toward the source with relatively low potential and then to the substrate. Accordingly, holes are dispersed on both sides of the substrate in the shared drain structure.

In contrast, in the shared source structure, holes are collected in the middle of the substrate, which is called "hole current crowding." The hole current crowding raises the

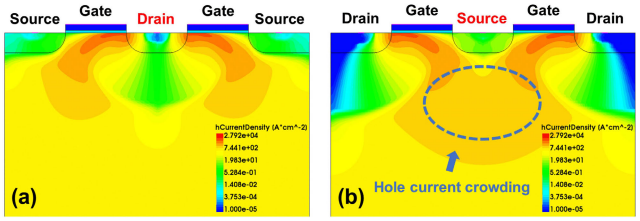

FIGURE 4. Hole current density in the (a) shared drain and (b) source structure at $V_G = 2$ V, $V_D = 13$ V.

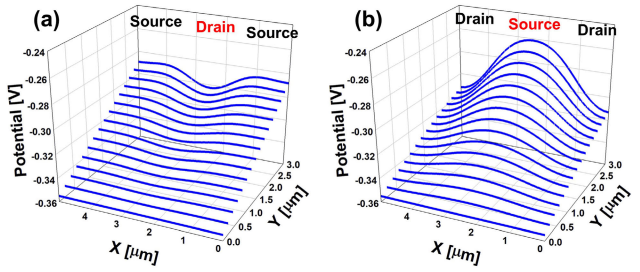

FIGURE 5. Electrostatic potential in the (a) shared drain and (b) source structure at $V_G = 2$ V, $V_D = 13$ V (X = 0 ~ 5 μm, Y = 0 ~ 3 μm).

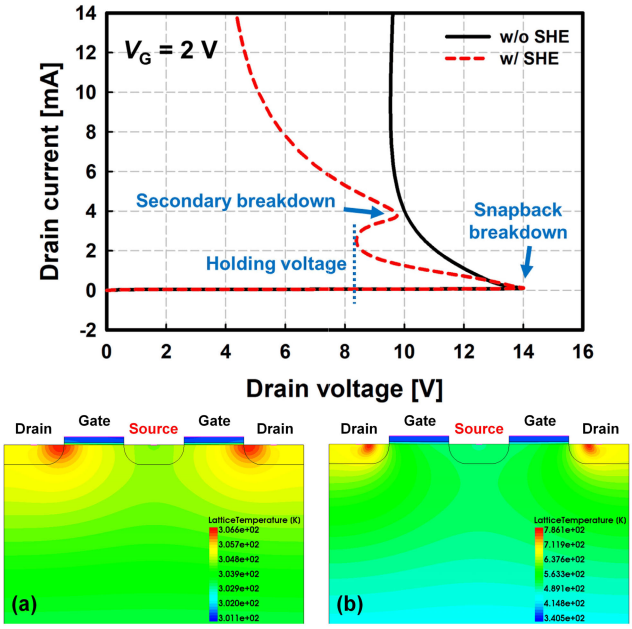

FIGURE 6. Output curves of the shared source structure. Also, the lattice temperature in the shared source structure is shown when the parasitic BJT is (a) turned off and (b) turned on.

voltage drop across the substrate and develops a high-potential region below the source. As shown in Fig. 5, the shared source structure exhibited a higher substrate potential than the shared drain structure, even with the same bias conditions. It means that the potential barrier of the source-substrate junction significantly decreases in the case of the shared source structure, and the parasitic BJT can be easily turned on. It should be noted that hole current crowding is a positive feedback process in which the reduced potential barrier of the source-substrate junction enhances the bipolar current and contributes to additional impact ionization.

Consequently, the SNBV difference between the two structures originates from the hole current crowding, which induces premature activation of the parasitic BJT. Therefore, when a voltage corresponding to the SNBV difference region (14.0 V $\leq V_D \leq$ 14.4 V) is applied to the drain, the shared drain structure operates normally, but a large current with high heat arises in the shared source structure. As shown in Fig. 6, the maximum temperature within the shared source structure at the holding voltage jumps from 306 K to 786 K when the parasitic BJT is turned on. This high heat causes thermal damage as well as secondary breakdown, leading to catastrophic failure. Thus, for the same operation of the two structures, the SNBV difference should be reduced as much as possible.

IV. POCKET IMPLANTATION METHOD

To alleviate the SNBV difference, the SNBV should be reduced in the shared drain structure or improved in the shared source structure. However, as the SNBV decreases, the safe operating area of multi-finger MOSFET decreases, so it is desirable to boost the SNBV in the shared source structure. Pocket implantation can be considered a simple and effective solution [13], [14]. If lightly-doped drain (LDD) masks are used in the process, pocket implantation can be performed without additional photolithography. For quantitative analysis, the substrate area was divided into two groups of mesh regions, as shown in Fig. 7. The square's dimensions are 0.2 μm × 0.2 μm. It is assumed that circular pockets with p-type doping concentration of 10^{20} cm^{-3} are inscribed in the squares. The pocket location is described by the X' – Y' coordinates. All simulation results for pocket implantation are obtained at $V_G = 2$ V, and $V_D = 13$ V.

Fig. 8a shows the simulated SNBV of the two-finger MOSFETs as a function of the pocket location. The empty symbol represents the shared drain structure, whereas the filled symbol represents the shared source structure. In both structures, SNBV exhibits non-monotonicity as the pocket implantation gradually approaches from source to drain. The SNBV increased by ~2.2 % when the pockets were located in the middle of the source and drain region (3 $\leq$ X' $\leq$ 4 and 1 $\leq$ Y' $\leq$ 2). This is because the highly doped pockets in the substrate current path effectively reduce the substrate resistance. As represented in Fig. 9a, the middle region corresponds exactly to the hole current path in the shared source structure. Thus, the voltage drop across the substrate decreases, and the parasitic BJT behavior is suppressed. As the shared drain and source structure are completely consistent with the X' coordinate, the same analysis can be applied to the shared drain structure.

When the pockets are located near the drain region (7 $\leq$ X' $\leq$ 9 and 1 $\leq$ Y' $\leq$ 3), the SNBV's of both structures increase again. This is because the pockets close to the drain can spread the generated holes throughout the substrate.

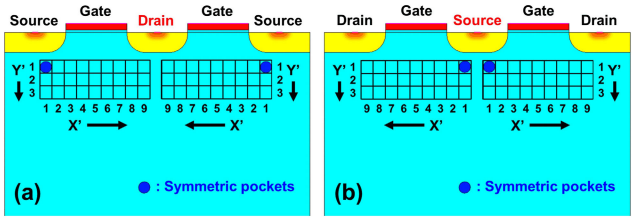

FIGURE 7. Pocket locations represented by X' – Y' coordinates in the (a) shared drain and (b) source structure.

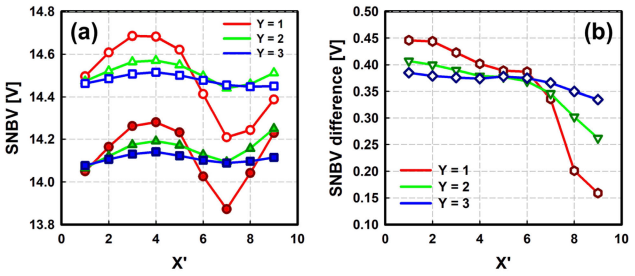

FIGURE 8. (a) Extracted SNBV of the shared drain (empty symbol) and source structure (filled symbol). (b) SNBV difference between the two structures as a function of the pocket location.

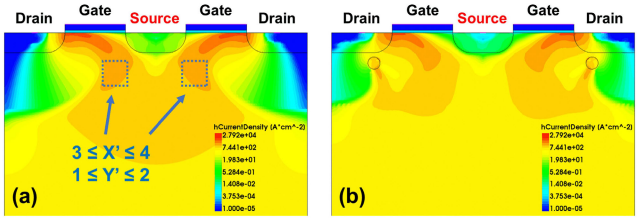

FIGURE 9. Hole current density in the shared source structure (a) without pocket implantation and (b) with pocket implantation.

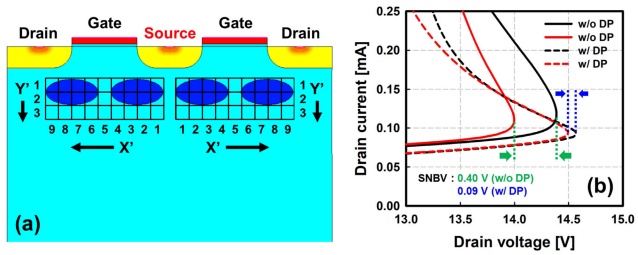

FIGURE 10. Double-pocket (DP) implantation for the two-finger MOSFET and the output curves representing DP implantation effect on SNBV.

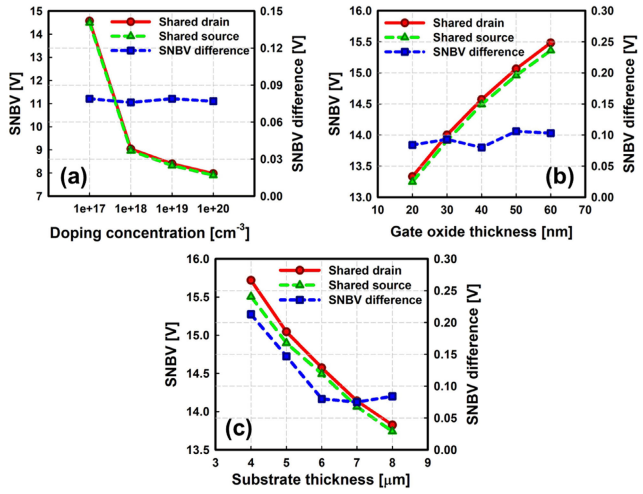

FIGURE 11. Double-pocket implantation effect on SNBV difference as a function of (a) doping concentration, (b) gate oxide thickness, and (c) substrate thickness.

The amount of hole current flowing into the substrate contact is maintained regardless of the pocket implantation. However, the maximum voltage drop decreases due to the distributed hole current. Moreover, the hole current crowding effect is suppressed as the holes are dispersed in the shared source structure. Fig. 9b shows the hole current density in the shared source structure when the pockets are located at X' = 9 and Y' = 1. Compared with Fig. 9a without the pockets, it is observed that the hole current crowding disappears. Fig. 8b shows the SNBV difference between the shared drain and source structure with varying pocket locations. The SNBV difference decreases as the pockets approached the drain. This means that the closer the pockets are to the drain, the more effectively the holes are dispersed. The SNBV difference becomes minimal when the pockets are located at $8 \leq X' \leq 9$, $1 \leq Y' \leq 2$, resulting in approximately 55 % lower SNBV difference. It should be noted that the pocket implantation effect on SNBV difference can be enhanced as the pockets are located closer to the drain, but if the pockets are too close to the drain, a large electric field can occur and the SNBV will decrease significantly.

To improve SNBV and SNBV difference characteristics simultaneously, double-pocket implantation was proposed. As shown in Fig. 10, the elliptical pockets were formed between the source and drain. This pocket shape not only covers both optimal regions mentioned above ($3 \leq X' \leq 4$, $1 \leq Y' \leq 2$ and $8 \leq X' \leq 9$, $1 \leq Y' \leq 2$), but also reduces manufacturing difficulty due to its symmetric location concerning the source and drain. Consequently, the SNBV increased by 3.6 % while the SNBV difference decreased by 78 % compared to the case without pocket implantation. This means that double-pocket implantation successfully suppresses hole current crowding and simultaneously reduces substrate resistance. It is also noteworthy that the effect of double-pocket implantation, as shown in Fig. 11, is insensitive to device parameters which directly control the current size such as source/drain doping concentration and gate oxide thickness. However, the SNBV difference decreases to 6 μm and then saturates in terms of substrate thickness. As the hole current is completely drained when it reaches the substrate contact, it can be inferred that the influence of the substrate contact on the hole current distribution within the substrate is minimized when substrate thickness is sufficient.

V. CONCLUSION

The SNBV difference in multi-finger MOSFETs according to the source/drain configuration was investigated for the first time. In the shared source structure, holes generated by impact ionization are collected below the source, causing hole current crowding and reducing the SNBV. Depending on the pocket location, SNBV difference can be reduced or SNBV can be enhanced. When double-pocket implantation was applied, the two-finger MOSFET exhibited 78 % lower SNBV difference with a 3.6 % higher SNBV than the case without pocket implantation.

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