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RESEARCH ARTICLE

A New High Voltage Gain Active Switched-Inductor Based High Step-Up DC–DC Converter With Coupled-Inductor

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ABSTRACT This paper propounds a new high step-up DC-DC topology based on the active switched-inductor (A-SL) technique, which utilizes a coupled inductor (CI) for performance enhancement. Among the features of the presented topology are the following: (a) Better voltage gain (VG) and efficiency, (b) Since there are low voltages across power switches, it is possible to reduce the amount of power that is lost as a result of using MOSFETs with a low voltage rating and reduced internal resistance, (c) By reducing the turn ratio of the CI, the VG is enhanced, (d) Through the series connection of a capacitor with the CI primary winding, zero DC bias is achieved, and the core saturation problem is solved, (e) Input current division between input inductors and switches, (f) There is no limitation on duty cycle ($0 < D < 1$), and (g) Simple switching patterns and simultaneously driven switches. The propounded converter's operation principle and steady-state analysis are explained in detail, and parasitic elements' effects on VG and efficiency are examined. In addition, the VG, the number of components, and the voltage tension on power switches, diodes, and capacitors are compared and analyzed. An experimental laboratory prototype with 30V input and 400V output voltage is used to verify the validity of the study and the performance of the propounded topology.

INDEX TERMS Active switched-inductor, coupled-inductor, DC-DC converter, high voltage gain.

I. INTRODUCTION

The use of step-up DC-DC converters with high voltage conversion ratios has grown significantly in the past few years. Hence, designing and introducing new topologies for these converters using various voltage-boosting techniques to obtain high voltage gain (VG) along with performance improvement has been a topic of numerous research in power electronics [1]. These converters are employed in industrial applications, including power supplies, microgrids, electric traction, automobiles, data centers, robotics, satellites, street lightings, and renewable energy sources (RES), such as fuel cells, solar panels, and wind turbines [1], [2], [3]. The use of step-up converters in such applications is common for converting the low-level input voltage (usually less than 50 volts) into the high output voltage (for example, 400 volts) [4], [5].

Theoretically, a high voltage conversion ratio is achievable at large duty cycles with conventional DC-DC converters, such as boost and quadratic boost, and flyback converters; However, practically, the high tension of the power switch, diode reverse recovery issue, conduction loss of the inductor limits the voltage gain (VG) or boost factor. In converters with a coupled inductor (CI) or transformer, such as flyback, VG is adjustable by turn ratio (n); however, some drawbacks, such as high volume, high switch voltage spikes because

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of the leakage inductance of the transformer, and core saturation, are added [5], [6]. As a remedy, configurations of classical step-up converters must be modified to enhance performance key indicators; for example, in [7], a regenerative snubber circuit is used. This circuit store energy during the transistor's on state, which is then released during the off state to reduce losses caused by the transistor's switching. This helps to increase the efficiency of the boost converter. In [8], the authors propounded a boost converter with soft-switching operation through an auxiliary circuit. Numerous voltage-boosting techniques are employed by conventional step-up structures to maintain adequate duty cycles and efficiency while maximizing voltage conversion ratios. These include voltage lift, switched capacitors (SC), voltage multipliers (VM), switched inductors (SL), interleaving, coupled-inductors (CI), and cascading [5], [6], [9], [10], [11]. The topologies presented in [12], [13], and [14] use interleaved and CI techniques. While the interleaving and CI techniques are well suited to high-power applications, these approaches increase the number of components. Topologies based on switched capacitors are presented in [15] and [16], which are works based on the charge/discharging of capacitors in each switching cycle. However, such situations typically result in poor voltage regulation, making this technique only appropriate when combined with other methods that can regulate the output voltage effectively.

By integrating capacitors with diodes or inductors with diodes, some switching cells (i.e., SC and SL cells) are formed and inserted in conventional converters to improve their VG [17]. An Active-Switched Inductor (A-SL) structure is utilized to develop three DC-DC converters [18]. This approach involves the simultaneous charging of two inductors with the same level of inductance in a parallel connection during the power switches' on-state and then their subsequent discharge in a series arrangement upon the switches' off-state. Despite improved VG, converters in [17] and [18] still suffer from some problems, like the high stress of the power switches. In [19] and [20], two CIs are used instead of two inductors of the A-SL unit; a passive clamped circuit is added to recycle the leakage inductor energy. In [21], the inductors in the A-SL unit are substituted with a passive switched inductor (P-SL) unit to create a new high-gain topology named hybrid switched inductor converter (H-SLC). In [22] and [23], using a capacitor instead of one of the diodes of the P-SL unit, a new cell is created and employed in the converter topology presented in [18]. Another high-gain DC-DC converter by a combination of A-SL and switched-capacitor network is presented in [24]. A passive switched capacitor (PSC) network is added to the A-SL topology to create an active switched-inductor step-up 2-cell (ASL-SU2C) converter [25]. In addition, a low-pass filter is used at the output. In [26], the replacement of inductors in the converter introduced in [25] by P-SL units has resulted in a new high-gain structure; however, the tradeoff is a lowered efficiency due to the increase in the number of components.

In [27], a new structure is presented, which is a combination of an active-passive inductor cell (APIC) and the topology represented in [18]. Expanding the topology by increasing the number of APICs is possible. Another extendable high-gain structure based on APICs is presented in [28]. However, in these converters, the component count rises for obtaining high VG, leading to increased loss and decreased efficiency. Adding an auxiliary switch and SC cell to the converter presented in [21] creates a new structure called an improved hybrid SL/SC converter, which is proposed in [29]. This converter provides a high gain, but the number of used components is too high. A single switch high step-up structure is introduced in [30], in which an $L^2C^3D^2$ network is utilized. In addition, two other single-switch single-ended primary-inductor converter (SEPIC) -based boost structures are proposed in [31] and [32]. In these converters, the current stress of the power switches is high leading to high conduction loss.

In [33], [34], and [35], three converters are introduced utilizing a CI. But unlike other CI-based converters, in these converters, VG is increased by lowering the CI's turn ratio (n), which theoretically provides a great advantage in reducing the overall size of the converter for higher voltage gain. Because of this inverse operating principle, the name "Trans-inverse (Tx^{-1})" is used in some papers [34]. However, the main problem with these converters is that the applicable range of the duty cycle to achieve voltage gain is narrowed down by lowering the CI's turn ratio. This results in having steep slopes near the D_{max} of the curves related to the VG of these converters. It means that, although these converters can theoretically reach high VGs, reaching such high VGs in practice is impossible for them. In addition, this very steep VG curve complicates the converter control because of greater output voltage sensitivity to the duty cycle. Therefore, to avoid the mentioned problems, CIs with $n = 3$ and $n = 4$ are used in [34]. In order to solve these problems and be able to take advantage of the Trans-inverse feature in practice, a new semi-SEPIC topology with a Tx^{-1} CI is presented in [36]. In this converter, the duty cycle is not limited, and the curve related to the VG has a mild slope. Although the mentioned problems have been solved, the VG, switch stress, and efficiency of [36] still need improvement.

In [37], an extendable n-stage single-switch impedance network (SSIN)-based converter is presented, which has some drawbacks, the inductors and diodes count has to increase to obtain high VG, and the switch voltage tension is half of the output voltage, which can be considered high.

In [38], a technique is proposed for switch current stress reduction of the converter proposed in [17]; however, the voltage stress of the switches is high ($V_S = V_O$). In [39], by adding two diodes and two capacitors to the converter that was introduced in [38], it is possible to ameliorate the performance, as well as reduce the voltage stress on the switches. Nevertheless, the tension on the switches continues to be remarkable (with $V_S = 0.5V_O$).

Another high-gain DC-DC converter based on switched capacitor-inductor network (SCLN) is introduced in [40]. Moreover, four other switched inductor-based converters are proposed in [41], [42], [43], and [44]. In [41], switched capacitors and a voltage multiplier cell are utilized to reach a high VG, but considering the components count, the VG is not high. An extendable switched-capacitor cell was incorporated on the output side of the converter in [42] to boost the VG; however, this yielded a disadvantage in the form of inrush currents that traversed through the switch, resulting in low efficiency and high conduction loss. The converter proposed in [43] has some drawbacks, like a limited range of duty cycles ($0 < D < 0.3$), low VG, and low efficiency. The authors in [44] presented a high-gain hybrid switched-inductor DC-DC converter with three power switches. The disadvantages of the converter are the high voltage stress of the switches necessitating the adoption of high voltage-rated MOSFETs with elevated on-resistance, high power loss of the switches, and low efficiency. In [45], an A-SL-based converter in which a three-winding CL is utilized instead of inductors of basic A-SL is presented. Furthermore, two additional switches are used in its structure. The main drawback is the high number of power switches. In [46], another A-SL-based converter where a quasi Z-Network is replaced instead of one of the inductors of basic A-SL is presented. Moreover, a voltage multiplier cell is added to the output. High component count and limited duty cycle range are its drawbacks.

An analysis of the literature and in-depth study of SL and A-SL-based high step-up DC-DC converters has revealed the need to improve their performance. This paper propounds a new topology in which a CI is utilized and added to the A-SL structure for performance enhancement. The main contributions are:

- ➢ High VG by considering components count.
- ➢ Low stress of the power switches.
- ➢ A high VG can be achieved by reducing the turn ratio of the CI; therefore, a high turn ratio is not needed to achieve a high VG.
- ➢ The total voltage stress to voltage gain is low (TVS/G). Therefore, the proposed converter provides high voltage gain with low total voltage stress on its components.

Furthermore, the following are the other features and benefits:

- The power switches' voltage stress is low, enabling the usage of low voltage rating transistors with low on-resistance.
- Due to the input current sharing between the power switches, the switches' current stress and conduction loss are reduced.
- Both switches are activated simultaneously, resulting in a very simple switching pattern.
- The duty cycle has no limitation ($0 < D < 1$).
- The energy stored in the leakage inductor recycles through the output diode, and the diode's current falls to zero, so the leakage inductance not only does not cause problems like voltage spikes on the power switches but also solves the reverse recovery issue of the output diode.
- Because of a series connection of a capacitor with the primary winding of the CI, zero DC bias of the CI is achieved, and the core saturation problem is remedied.
- Since the input current is divided between the input inductors, the sum of conduction losses in two input inductors of the propounded converter is half of the inductor losses of converters with one input inductor.
- The voltage tension of each capacitor is lower than the output.

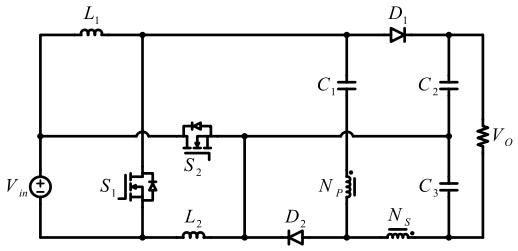

FIGURE 1. Configuration of the propounded converter.

Here is the organization of the remainder of the manuscript: Section II describes the propounded structure and its operation principle. In section III, steady-state analyses are done. Sections IV and V provide design guidelines and efficiency analysis, respectively. In Section VI, a comprehensive comparison study is done, and finally, experiments described in section VII are used to validate the analysis and performance of the converter, then the paper is concluded.

II. PROPOSED TOPOLOGY AND OPERATION PRINCIPLE

The configuration of the propounded converter is depicted in Figure 1. This circuit is formed by two inductors (L_1, L_2), two power MOSFETs (S_1, S_2), two diodes (D_1, D_2), three capacitors (C_1, C_2, C_3), and a coupled-inductor composed of a primary winding N_P and a secondary winding N_S, where $n = N_S/N_P$ indicates their turn ratio, which is modeled by a magnetizing inductor (L_m) and a leakage inductor (L_k).

The following are the assumptions that are taken into account when performing a steady-state analysis:

- ➢ All circuit components are non-dissipative and ideal.
- ➢ The capacitance of all capacitors is sufficiently large to make the voltage across them a constant value during switching.
- ➢ All inductors are large enough; hence, the current ripple associated with them can be ignored.
- ➢ The proffered converter operates in continuous conduction mode (CCM).

Figure 2 provides a graphical representation of the steady-state waveforms of the proffered converter for one switching cycle. This converter has four unique operating modes throughout each cycle.

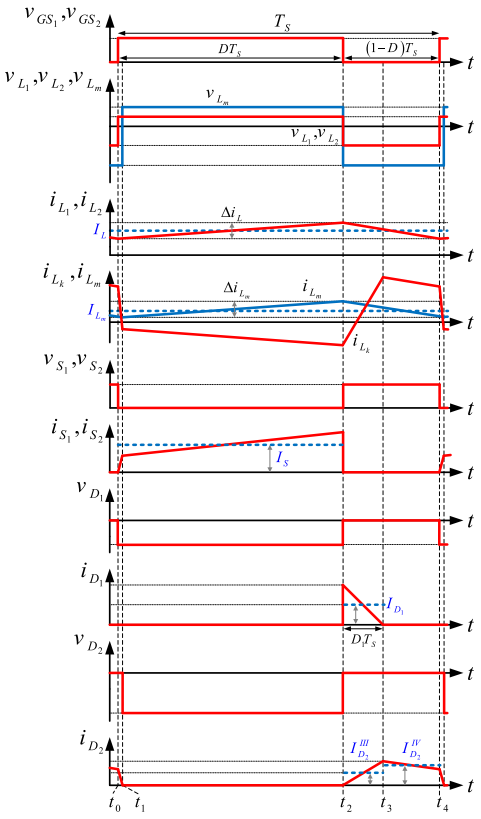

FIGURE 2. Steady-state waveforms of the propounded converter.

A. STATE 1

At $t = t_0$, switches S_1 and S_2 are enabled. Meanwhile, diodes D_1 and D_2 remain in their off-state and on-state, respectively. Subsequently, the input voltage source V_{in} energizes the two input inductors (L_1 and L_2), which, as a result, experience a progressive and linear increase in current. The magnetic inductor L_{m} is in a process of discharging, with its current diminishing in a linear way. Meanwhile, the leakage inductor L_{k} is also being discharged, with its current flowing through diode D_2. When the leakage current of the CI is depleted, diode D_2 will cease to be active, and this state will be terminated. This state's flow route is depicted in Figure 3(a). The following equations can be written:

$$i_{L_1}(t) = i_{L_2}(t) = \frac{1}{L}\int_{t_0}^{t} V_{in}dt + i_L(t_0) \tag{1}$$

$$i_{L_m}(t) = \frac{1}{L_m}\int_{t_0}^{t} (-\frac{V_{C_3}}{n})dt + i_{L_m}(t_0) \tag{2}$$

$$i_{L_k}(t) = \frac{1}{L_k}\int_{t_0}^{t} (-V_{C_1} - V_{in} + \frac{V_{C_3}}{n})dt + i_{L_k}(t_0) \tag{3}$$

Regarding (3), as the voltage of the leakage inductor in this state is a large negative value, and its inductance (L_{K}) is low, i_{Lk} reaches zero rapidly. Therefore, this interval is too short in duration.

B. STATE 2

This state is initiated when diode D_2 enters an off-state. The state of affairs remains unchanged with S_1 and S_2 still engaging, while D_1 continues to remain inactive. The current drawn from the input voltage source increases steadily as the inductors, which are connected in parallel, become charged. Moreover, the current of the magnetizing inductor rises in a linear manner due to a charge being applied. The current circulation path related to this mode is depicted in Figure 3(b). Capacitor C_3 is charged while capacitors C_1 and C_2 are discharged. The leakage inductor is discharged, and its current decreases linearly. Capacitor C_2 provides energy for the output load. Applying KVL in the equivalent circuit of this state leads to the derivation of the following equations.

$$V_{L_1} = V_{L_2} = V_L = V_{in} \tag{4}$$

$$V_{L_m} = (V_{C_3} - V_{C_1} - V_{in})/(1-n) \tag{5}$$

$$V_O = V_{C_2} + V_{C_3} \tag{6}$$

$$V_{D_1} = -V_{in} - V_{C_2} \tag{7}$$

$$V_{D_2} = -nV_{Lm} - V_{C_3} \tag{8}$$

Furthermore, utilizing KCL, one can formulate the following equations:

$$i_{C_1} = -i_{L_m}/(n-1) \tag{9}$$

$$i_{C_2} = -i_O \tag{10}$$

$$i_{C_3} = -i_O + i_{L_m}/(n-1) \tag{11}$$

$$i_{S_1} = i_{L_1} - i_{C_1} \tag{12}$$

$$i_{S_2} = i_{L_2} + i_{C_3} - i_{C_2} \tag{13}$$

Moreover, the current equations of the input inductors and magnetizing inductor in this mode are written below:

$$i_{L_1}(t) = i_{L_2}(t) = i_L(t) = \frac{1}{L}\int_{t_1}^{t} V_{in}dt + i_L(t_1) \tag{14}$$

$$i_{L_m}(t) = \frac{1}{L_m}\int_{t_1}^{t} \left((V_{C_3} - V_{C_1} - V_{in})/(1-n)\right) dt + i_{L_m}(t_1) \tag{15}$$

C. STATE 3

At $t = t_2$, S_1 and S_2 are switched off, and D_1 and D_2 are activated, thus commencing the third operation state. Figure 3(c) illustrates the equivalent circuit of this state. The series juncture of the input inductors and voltage source causes the transition of energy from these components to capacitor C_2 and the output load. As a result, the input inductors begin to empty out energy, and their current steadily declines. Moreover, capacitor C_2 is charged. The leakage inductor current was negative in the previous state; in this state, it decreases and reaches zero, changes its direction, and increases linearly. When the currents of the input inductors and L_{k} become equal, the current of diode D_1 reaches zero. Thus, diode D_1 is turned off naturally without a reverse recovery issue, and this operation mode ends. By applying the KVL law in the

equivalent circuit of this state, we can derive the subsequent equations:

$$V_{L_1} = V_{L_2} = V_L = (V_{in} - V_{C_2})/2 \tag{16}$$
$$V_L = \left(V_{in} - V_{C_1} + (V_{C_3}/n)\right)/2 \tag{17}$$
$$V_{L_m} = -V_{C_3}/n \tag{18}$$
$$V_{S_1} = V_{S_2} = V_S = V_{in} - V_L \tag{19}$$

Moreover, by applying the KCL law in this mode, the following equations can be obtained:

$$i_{C_1} = i_{L_m} + ni_{\text{sec}} \tag{20}$$
$$i_{C_2} = i_L - i_O - i_{C_1} \tag{21}$$
$$i_{C_3} = -i_O + (i_{L_m} - i_{C_1})/n \tag{22}$$
$$i_{D_1} = i_L - i_{C_1} \tag{23}$$
$$i_{D_2} = i_{C_1} + i_{C_3} + i_O \tag{24}$$

Furthermore, the current equations of the input inductors and magnetizing inductor in this mode can be written:

$$i_L(t) = \frac{1}{L}\int_{t_2}^{t} \left((V_{in} - V_{C_2})/2\right) dt + i_L(t_2) \tag{25}$$
$$i_{L_m}(t) = \frac{1}{L_m}\int_{t_2}^{t} (-\frac{V_{C_3}}{n})dt + i_{L_m}(t_2) \tag{26}$$

D. STATE 4

The transition to this mode begins at the exact moment when the current passing through diode D_1 falls to zero at time t_3. The switches are off-state, while diode D_2 is in the state of operation. In this state, all the inductors (L_1, L_2, L_k, and L_m) are discharged; thus, their currents decrease linearly. The remaining stored energy in the input inductors and the magnetizing inductor are transferred to capacitor C_1. The discharge of capacitors C_2 and C_3 enables capacitor C_2 to supply the energy of the output load. The flow of current in this state is illustrated in Figure 3(d). By applying the KVL and KCL, the ensuing equations can be written:

$$V_L = \left(V_{in} - V_{C_1} + (V_{C_3}/n)\right)/2 \tag{27}$$
$$V_{L_m} = -V_{C_3}/n \tag{28}$$
$$V_{S_1} = V_{S_2} = V_S = V_{in} - V_L \tag{29}$$
$$i_{C_1} = i_L \tag{30}$$
$$i_{C_2} = -i_O \tag{31}$$
$$i_{C_3} = -i_O + (i_{L_m} - i_L)/n \tag{32}$$
$$i_{D_2} = i_{C_1} + i_{C_3} + i_O \tag{33}$$

Finally, the current equations of inductors L_1, L_2, and L_m in the last mode are written below:

$$i_L(t) = \frac{1}{L}\int_{t_3}^{t} \left((V_{in} - V_{C_2})/2\right) dt + i_L(t_3) \tag{34}$$
$$i_{L_m}(t) = \frac{1}{L_m}\int_{t_3}^{t} (-\frac{V_{C_3}}{n})dt + i_{L_m}(t_3) \tag{35}$$

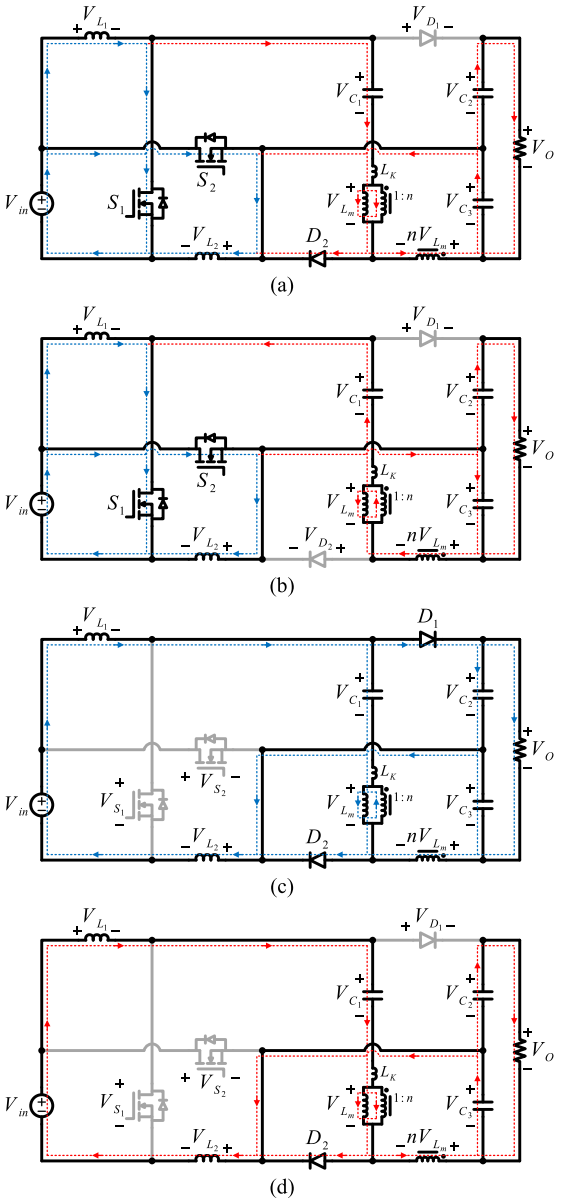

FIGURE 3. The propounded converter in various operational states. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

III. STEADY-STATE ANALYSIS

A. VOLTAGE GAIN CALCULATION

The propounded converter's VG can be calculated using the volt-second balance principle. Since the time interval of the first mode is extremely short compared to others, the first mode can be neglected in VG calculation. Based on (17) and (27), it is concluded that the voltage across the input inductors in operation modes III and IV have the same value. Similarly, using(18) and (28), it is clear that voltage across L_m remains the same value in states III and IV. Therefore, the time duration of modes III and IV is considered to be (1-D)T_S. This can be observed in Figure 2. By applying the volt-second law to the input inductors, using (4), (16), and (17), one can

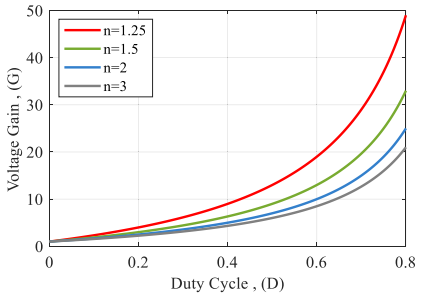

FIGURE 4. Voltage gain of the propounded converter.

derive the following equations:

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} \left((V_{in} - V_{C_2})/2\right) dt = 0 \tag{36}$$

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} \left(\left(V_{in} - V_{C_1} + (V_{C_3}/n)\right)/2\right) dt = 0 \tag{37}$$

The volt-second law for the magnetizing inductor is written as follows using (5) and (18):

$$\int_0^{DT_S} \left((V_{C_3} - V_{C_1} - V_{in})/(1-n)\right) dt + \int_{DT_S}^{T_S} (-\frac{V_{C_3}}{n})dt = 0 \tag{38}$$

From (36), the voltage equation of capacitor C_2 is obtained:

$$V_{C_2} = \frac{1+D}{1-D} V_{in} \tag{39}$$

From (37) and (38), the voltage equations of capacitors C_1 and C_3 are obtained:

$$V_{C_1} = \frac{n+D+nD-1}{(1-D)(n-1)} V_{in} \tag{40}$$

$$V_{C_3} = \frac{2nD}{(1-D)(n-1)} V_{in} \tag{41}$$

The VG equation of the propounded converter, using equations (6), (39), and (41), is written below:

$$G = \frac{V_O}{V_{in}} = \frac{3nD+n-D-1}{(1-D)(n-1)} \tag{42}$$

The curves for VG relative to the duty cycle with distinct turn ratios of the CI are depicted in Figure 4, clearly demonstrating that when n is reduced and selected near 1, the VG heightens. Based on the required VG, n is selected. For example, if an extremely high VG is required, n can be selected to be 1.25. Furthermore, the proposed circuit is operational across a full range of duty cycles, varying from zero to one.

B. VOLTAGE STRESS CALCULATION

It is a necessity to recognize voltage stress in order to effectively select applicable capacitors and semiconductor devices. The magnitude of the voltage that is applied to the capacitors can be established by using (39), (40), and (41). The voltage stress exerted on the electrical switches by (16), (19), and (39), is calculated and can be expressed using the equation provided below.

$$V_{S_1} = V_{S_2} = \frac{1}{1-D} V_{in} \tag{43}$$

Using (7) and (39), it is possible to ascertain the voltage stress experienced by diode D_1:

$$V_{D_1} = \frac{-2}{1-D} V_{in} \tag{44}$$

Similarly, using (5), (8), (40), and (41), we can formulate the following equation for diode D_2:

$$V_{D_2} = \frac{-2n}{(1-D)(n-1)} V_{in} \tag{45}$$

The voltage tension equations of the capacitors and semiconductor devices normalized to output voltage are obtained and listed in Table 1, and their corresponding plots when $n = 1.5$ and $n = 2$ versus D are shown in Figure 5. The utilization of switches having a low voltage rating and low on-resistance is enabled as the amount of tension imposed on the power transistors is insignificant. Moreover, the voltage of the output is dispensed among capacitors C_2 and C_3, which offers the advantage of being able to employ two capacitors with less voltage stress than the load voltage.

TABLE 1. Voltage stress of the capacitors and semiconductors.

C_1	C_2
$\frac{n+D+nD-1}{3nD+n-D-1} V_O$	$\frac{n-D+nD-1}{3nD+n-D-1} V_O$
C_3	S_1 and S_2
$\frac{2nD}{3nD+n-D-1} V_O$	$\frac{n-1}{3nD+n-D-1} V_O$
D_1	D_2
$\frac{-2(n-1)}{3nD+n-D-1} V_O$	$\frac{-2n}{3nD+n-D-1} V_O$

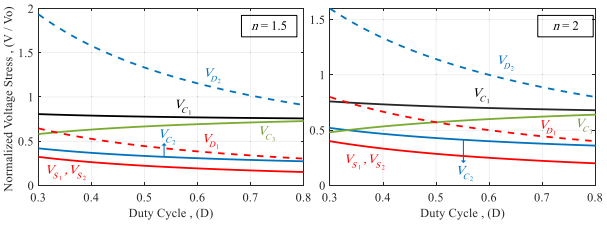

FIGURE 5. Voltage stress of the capacitors and semiconductor devices versus duty cycle for n = 1.5 and n = 2.

C. CURRENT ANALYSIS

The current flowing through the capacitors is calculated based on the ampere-second principle. By applying this principle

to capacitor C_2, using (10), (21), and (31), a formula can be expressed that is as follows:

$$\int_0^{DT_S}(-I_O)dt+\int_{DT_S}^{(D+D_1)T_S}(I_L-I_O-i_{C_1}^{III})dt+\int_{(D+D_1)T_S}^{T_S}(-I_O)dt=0 \quad (46)$$

From this equation, the current of capacitor C_1 in state III is calculated:

$$i_{C_1}^{III}=I_L-\frac{I_O}{D_1} \quad (47)$$

Using (22) and (47), the current of capacitor C_3 in state III is obtained:

$$i_{C_3}^{III}=-I_O+\frac{I_{Lm}}{n}-\frac{I_L}{n}+\frac{I_O}{nD_1} \quad (48)$$

By applying the ampere-second law to capacitor C_3, using (11), (32), and (48), the following relation can be written:

$$\int_0^{DT_S}(-I_O-\frac{I_{Lm}}{1-n})dt+\int_{DT_S}^{(D+D_1)T_S}(-I_O+\frac{I_{Lm}}{n}-\frac{I_L}{n}+\frac{I_O}{nD_1})dt+\int_{(D+D_1)T_S}^{T_S}(-I_O+(I_{L_m}-I_L)/n)dt=0 \quad (49)$$

Similarly, by applying it to capacitor C_1, using (9), (30), and (47), the following equation can be written:

$$\int_0^{DT_S}(\frac{I_{Lm}}{1-n})dt+\int_{DT_S}^{(D+D_1)T_S}(I_L-\frac{I_O}{D_1})dt+\int_{(D+D_1)T_S}^{T_S}(I_L)dt=0 \quad (50)$$

From (49) and (50), the average current of the magnetizing inductor is obtained:

$$I_{Lm}=nI_O \quad (51)$$

From (50) and (51), the average currents of the input inductors are obtained:

$$I_L=I_{L_1}=I_{L_2}=\frac{nD+n-1}{(n-1)(1-D)}I_O \quad (52)$$

Using (51), (52), and the capacitors' current relations, which were obtained by applying KCL in each operation mode in section II, the capacitors' current equations in terms of the output load current (I_O) are calculated and written in Table 2.

The current stress of the semiconductor devices can be determined using the following formulas:

$$I_{S_1}=I_{S_2}=\frac{2n-1}{(1-D)(n-1)}I_O \quad (53)$$

$$I_{D_1}=\frac{1}{D_1}I_O \quad (54)$$

$$I_{D_2}^{III}=I_O+\left(\frac{nD+n-1}{(n-1)(1-D)}-\frac{1}{D_1}\right)\left(1-\frac{1}{n}\right)I_O \quad (55)$$

$$I_{D_2}^{IV}=I_O+\left(\frac{nD+n-1}{(n-1)(1-D)}\right)\left(1-\frac{1}{n}\right)I_O \quad (56)$$

TABLE 2. Current equations of the capacitors.

	Mode II	Mode III	Mode IV
C_1	$\frac{-n}{n-1}I_O$	$\left(\frac{nD+n-1}{(n-1)(1-D)}-\frac{1}{D_1}\right)I_O$	$\frac{nD+n-1}{(n-1)(1-D)}I_O$
C_2	$-I_O$	$(\frac{1}{D_1}-1)I_O$	$-I_O$
C_3	$\frac{1}{n-1}I_O$	$\left(\frac{1}{D_1}-\frac{nD+n-1}{(n-1)(1-D)}\right)\frac{I_O}{n}$	$-\frac{nD+n-1}{n(n-1)(1-D)}I_O$

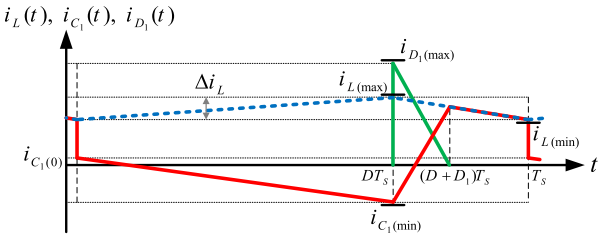

FIGURE 6. Current waveforms of the input inductors, leakage inductor ($i_{Lk}=i_{C1}$), and diode D_1.

According to (23) and Figure 6, the following relation can be written:

$$i_{D_1(\max)}=i_{L(\max)}-i_{C_1(\min)} \quad (57)$$

The maximum magnitude of the current across both input inductors and the minimum magnitude of the current through capacitor C_1 occurs at $t=DT_S$; therefore, allowing the following equations to be formulated.

$$i_{L(\max)}=I_L+\frac{DV_{in}}{2f_SL} \quad (58)$$

$$i_{C_1(\min)}=\frac{-DV_{in}}{f_SL_m(n-1)^2}-\frac{I_{Lm}}{(n-1)} \quad (59)$$

Using (57), (58), and (59), the maximum current value of diode D_1 is calculated:

$$i_{D_1(\max)}=I_L+\frac{DV_{in}}{2f_SL}+\frac{DV_{in}}{f_SL_m(n-1)^2}+\frac{I_{Lm}}{(n-1)} \quad (60)$$

Applying the principle of amperes-seconds, the average current through diode D_1 satisfies the following equation:

$$I_{D_1(ave)}=I_O\Rightarrow\frac{i_{D_1(\max)}D_1}{2}=I_O \quad (61)$$

Using (60) and (61), the duration of the operation mode III is calculated:

$$D_1=2/\left(\frac{2n-1}{(n-1)(1-D)}+\left(\frac{1}{2L}+\frac{1}{L_m(n-1)^2}\right)\frac{DR_{Load}}{f_SG}\right) \quad (62)$$

D. DISCONTINUOUS CONDUCTION MODE (DCM)

Theoretical waveforms of the inductors' and CI's voltage and current in DCM are depicted in Figure 7. As can be seen, the voltage across the inductors and CI becomes zero before the

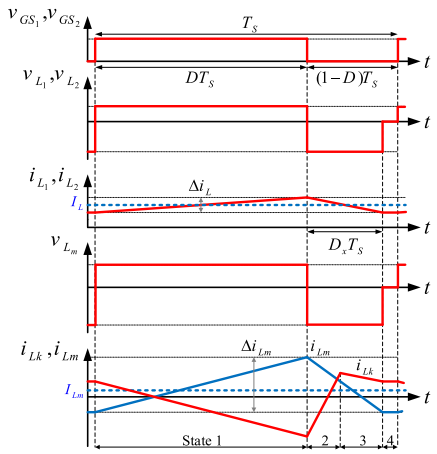

FIGURE 7. Waveforms of the inductors and CI in DCM.

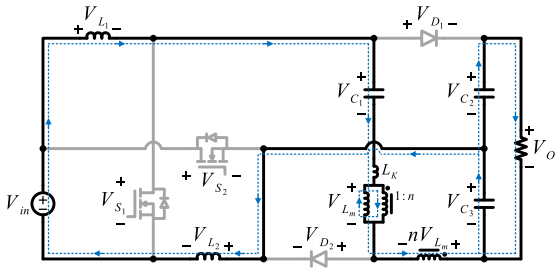

FIGURE 8. Operation state 4 of DCM.

end of the switching cycle; and their current becomes a constant value. Therefore, four states of operation are observed in DCM. The first three operation states of DCM are similar to states 2, 3, and 4 of CCM, respectively. The fourth operation state with its current flow path is shown in Figure 8. In this operation state, capacitor C_1 is charged, and capacitors C_2 and C_3 are discharged. By applying the KVL and KCL, the following equations can be written:

$$V_{L_1} = V_{L_2} = V_L = V_{L_m} = 0 \tag{63}$$

$$V_{C_1} - V_{C_3} = V_{in} \tag{64}$$

$$(n-1)i_L + i_{L_m} = 0 \tag{65}$$

$$i_{C_1} = -i_{C_3} = i_L \tag{66}$$

$$i_{C_2} = -i_O \tag{67}$$

By applying the volt-second balance principle to the input inductors and some derivations, the voltages across capacitors C_1, C_2, C_3, and output voltage are obtained as:

$$V_{C_1} = \left(\frac{2nD}{D_x(n-1)} + 1\right)V_{in} \tag{68}$$

$$V_{C_2} = \left(\frac{2D}{D_x} + 1\right)V_{in} \tag{69}$$

$$V_{C_3} = \left(\frac{2nD}{D_x(n-1)}\right)V_{in} \tag{70}$$

$$G_{DCM} = \frac{4nD + nD_x - 2D - D_x}{D_x(n-1)} \tag{71}$$

Furthermore, by applying the charge balance principle to the capacitors and some derivations, the inductors current can be obtained as:

$$I_L = \left(1 + \frac{(2n-1)D}{D_x(n-1)}\right)I_O \tag{72}$$

$$I_{L_m} = \left(\frac{(2n-1)(1-D)}{D_x} - n + 1\right)I_O \tag{73}$$

The following equation can be written for the inductors:

$$\begin{aligned} i_{L_{eq}}(t) &= i_L(t) + i_{L_m}(t)/(n-1) \\ \Rightarrow i_{L_{eq}}(t) &= 2\left(\frac{1}{2L} + \frac{1}{L_m(n-1)^2}\right)V_{in}t \\ \Rightarrow i_{L_{eq}}(DT_S) &= 2\left(\frac{1}{2L} + \frac{1}{L_m(n-1)^2}\right)\frac{D}{f_S}V_{in} \end{aligned} \tag{74}$$

L_{eq} is defined:

$$\frac{1}{L_{eq}} = \left(\frac{1}{2L} + \frac{1}{(n-1)^2 L_m}\right) \tag{75}$$

The average current of L_{eq} can be written as the following:

$$I_{L_{eq}} = I_L + I_{L_m}/(n-1) \tag{76}$$

If assumed $I_{Leq} = i_{Leq(peak)}/2$, then $i_{Leq(peak)}$ can be obtained as:

$$i_{L_{eq}(peak)} = \frac{2(2n-1)}{D_x(n-1)}\frac{V_O}{R_{Load}} \tag{77}$$

Using (74) and (77), D_x is obtained:

$$D_x = \frac{(2n-1)G_{DCM}f_S L_{eq}}{D(n-1)R_{Load}} = \frac{(2n-1)G_{DCM}\tau}{D(n-1)} \tag{78}$$

where τ is a dimensionless parameter, and it is defined below:

$$\tau = \frac{f_S L_{eq}}{R_{Load}} \tag{79}$$

Using (71) and (78), the DCM voltage gain of the PC is achieved:

$$G_{DCM} = \left(1 + \sqrt{1 + \frac{8D^2}{\tau}}\right)/2 \tag{80}$$

In order to get the boundary condition between the CCM and DCM operations, G_{CCM} equals G_{DCM}. Hence, the critical value of τ is obtained and plotted:

$$\tau_{critical} = 8D^2/\left(\left(\frac{7nD + n - 3D - 1}{(1-D)(n-1)}\right)^2 - 1\right) \tag{81}$$

IV. DESIGN CONSIDERATIONS

For the purpose of implementing a lab-based model of the presented structure and selecting appropriate components, some design considerations must be taken into account. Analysis of the performance of the converter will be carried out in varying output energies ranging from two hundred watts to three hundred watts. The input voltage is 30V. This necessitates that (42) be utilized to attain a 400V output voltage, implying that D and n should be adjusted to 0.68 and 2, respectively. The components must be designed for the most adverse conditions in the performance range.

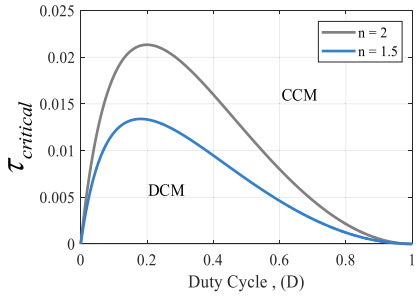

FIGURE 9. Boundary of CCM and DCM.

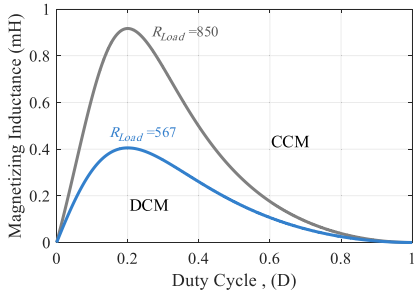

FIGURE 10. Minimum value of the magnetizing inductance for CCM operation when L_1=L_2=300μH.

A. DETERMINATION OF THE INDUCTANCES

Among the power ranges mentioned above, for inductors, two hundred watts (R_{Load} = 850Ω) is the adverse condition to determine the required inductance. The value of the inductors considering a current ripple of $\alpha = 40\%$ ($\Delta i_L = 0.4 \times I_L$) can be determined using the following formula:

$$L_1, L_2 \geq L_{\min} = \frac{D(n-1)(1-D)R_{Laod}}{(nD+n-1)Gf_S(\alpha)} = 285\mu H \quad (82)$$

According to (82), the inductance values of the input inductors are selected to be 300μH. It should be noted that both the input inductors can be assembled on one magnetic core to enhance power density and decrease size because they require the same inductance value and have the same operating conditions. Furthermore, it is necessary to determine the value of the magnetizing inductance and design it properly to guarantee that the proffered circuit is operating in CCM. Since the CI is located in the middle section of the circuit, it is not necessary to design it with a low current ripple; therefore, the magnetic core's volume, wire consumption, and conduction losses decrease. According to the assumption that the presented circuit operates in boundary conduction mode, using (75), (79), (81) and (82), the minimum required value of inductance L_m is determined and written below:

$$L_{m(\min)} = 1/\left(\frac{(2n-1)(n-1)}{(1-D)D}\frac{Gf_S}{R_{Load}} - \frac{(n-1)^2}{2L_{(\min)}}\right)$$
$$\Rightarrow L_m \geq L_{m(\min)} = 106\mu H \quad (83)$$

According to (83), the value of the magnetizing inductance is selected to be 380μH.

B. SELECTING MAGNETIC CORES AND WIRE

Choosing an appropriate magnetic core and wire for implementing the prototype is necessary. In this section, magnetic elements are designed using the geometrical constant (K_g) method. The maximum output power of the prototype (300W) must be taken into account for the design. For input inductors, the first step is a determination of core size by choosing a core that is large enough to satisfy the following inequality:

$$K_g = \frac{A_c^2 W_A}{(MLT)} \geq \frac{\rho L^2 I_{\max}^2}{B_{\max}^2 R K_u} 10^8 (cm^5) \quad (84)$$

where A_c (cm^2) is core cross-sectional area, W_A (cm^2) is core window area, MLT (cm) is mean length per turn, ρ (Ω-cm) is wire resistivity, $I_{\max}$ is peak winding current, $B_{\max}$ (T) is maximum operating flux density, R is winding resistance, K_u is winding fill factor. The numerical value of K_g for the input inductors is calculated as follows:

$$K_g = \frac{A_c^2 W_A}{(MLT)} \geq \frac{1.724 \times 10^{-6} \times (300 \times 10^{-6})^2 \times 6}{(0.25)^2 \times 35 \times 10^{-3} \times 0.5} 10^8$$
$$= 0.5107 \quad (85)$$

According to the datasheets of the ferrite cores, the closest core to the obtained value using (85) is PQ32/30, whose K_g is 0.5787. The second step is calculating the number of turns based on the selected core specifications.

$$n_L = \frac{LI_{\max}}{B_{\max} A_c} 10^4 = \frac{300 \times 10^{-6}}{0.25 \times 1.61} 10^4 = 45 \quad (86)$$

After determining the number of turns, the air gap length is calculated using the following equation, where μ_0 is the permeability of free space.

$$l_g = \frac{\mu_0 A_c n_L^2}{L} 10^{-1} = \frac{4\pi \times 10^{-7} \times 1.61 \times 45^2}{300 \times 10^{-6}} 10^{-1}$$
$$= 1.37mm \quad (87)$$

The third step is evaluating the wire size:

$$A_W \leq \frac{K_u W_A}{n_L} = \frac{0.5 \times 1.496}{45} = 0.0166cm^2 \quad (88)$$

According to the above value, AWG15 wire with a bare copper area of A_W=0.01651 is selected. In the end, the winding resistance can be computed:

$$r_L = \frac{\rho n_L (MLT)}{A_W} = \frac{1.724 \times 10^{-6} \times 45 \times 6.7}{0.01651} = 31.5m\Omega \quad (89)$$

Furthermore, for the CI, a large enough core can be selected by satisfying the following inequality:

$$K_g \geq \frac{\rho L_m^2 I_{tot}^2 I_{M,\max}^2}{B_{\max}^2 P_{cu} K_u} 10^8 (cm^5) \quad (90)$$

where I_{tot} is total rms winding currents, $I_{M,max}$ is peak magnetizing current, P_{cu} is allowed total copper loss. The numerical value of K_g for the CI is calculated as follows:

$$K_g \geq \frac{1.724 \times 10^{-6} \times (380 \times 10^{-6})^2 \times 6^2 \times (2.5)^2}{(0.25)^2 \times 0.5 \times 0.4} 10^8 = 0.4481 \quad (91)$$

A PQ35/35 core with K_g of 1.1299 is selected to satisfy (91) with ease. According to this core, the required air gap length is calculated:

$$l_g = \frac{\mu_0 L_m I_{M,\max}^2}{B_{\max}^2 A_c} 10^7 = \frac{4\pi \times 10^{-7} \times (380 \times 10^{-6}) \times (2.5)^2}{(0.25)^2 \times 1.96} 10^7 = 0.25mm \quad (92)$$

The primary and secondary windings' turn number is calculated using (93), where n is the turn ratio of the CI:

$$N_{pri} = \frac{L_m I_{M,\max}}{B_{\max} A_c} 10^4 = 20, N_{\sec} = n(N_{pri}) = 40 \quad (93)$$

Using (94) and (95), wire sizes are determined, where α is the fraction of the window area allocated to each winding.

$$A_{Wpri} \leq \frac{\alpha_{pri} K_u W_A}{N_{pri}} = \frac{0.4 \times 0.4 \times 2.206}{20} = 0.0176cm^2 \quad (94)$$

$$A_{W\,\sec} \leq \frac{\alpha_{\sec} K_u W_A}{N_{\sec}} = \frac{0.6 \times 0.4 \times 2.206}{40} = 0.0132cm^2 \quad (95)$$

According to the obtained values, a two-layer litz wire (AWG22) is selected for each winding. Finally, the resistance of each winding can be calculated as follows:

$$r_{pri} = \frac{\rho N_{pri}(MLT)}{2A_{Wpri}} = 40m\Omega, r_{\sec} = \frac{\rho N_{\sec}(MLT)}{2A_{W\,\sec}} = 80m\Omega \quad (96)$$

C. CAPACITORS DESIGN

In order to limit the fluctuation of voltage across the capacitors, it is imperative to set the capacity of the relevant capacitances. The worst condition for the capacitors is when the output power is 300W ($R_{Load} = 567\Omega$). Taking into account an allowable voltage ripple of $\alpha = 1\%$ ($\Delta V_C = 0.01 \times V_C$), the capacitances of the circuit can be determined using the following equations.

$$C_1 \geq \frac{nD(1-D)G}{(nD+n+D-1)f_S R_{Load}(\alpha)} = 6.94\mu F \quad (97)$$

$$C_2 \geq \frac{(1-D_1)(1-D)G}{(1+D)f_S R_{Load}(\alpha)} = 7.67\mu F \quad (98)$$

$$C_3 \geq \frac{D(1-D)G}{2nDf_S R_{Load}(\alpha)} = 3.88\mu F \quad (99)$$

According to the above calculations, the values of the capacitances are selected to be 10μF. Capacitors with a larger capacitance value can decrease voltage ripple; also, they have low power loss because of their low ESR.

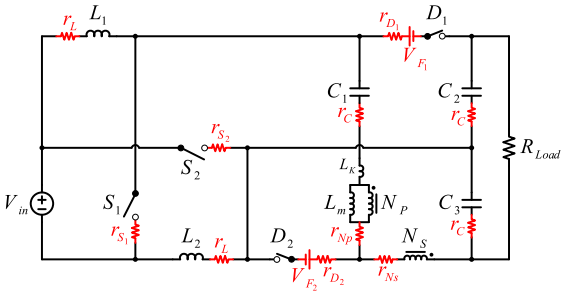

FIGURE 11. Equivalent circuit of the lossy propounded circuit.

V. EFFICIENCY AND NON-IDEAL VOLTAGE GAIN

To ascertain the efficiency and VG that is not ideal of the converter suggested, it is pertinent to compute the energy losses of each component - including the CI, input inductors, semiconductors, and capacitors - which can be discerned in the circuit that is displayed in Figure 11.

All of the power dissipated by the identified converter can be calculated using the accompanying expression.

$$P_{Total} = P_{CI} + P_L + P_S + P_D + P_C \quad (100)$$

Taking into consideration the inductor and CI currents (i_L, i_{Lm}) with no ripple, the copper losses will be calculated. The power dissipated by the CI (P_{CI}) is ascertained to be:

$$P_{CI} = r_{N_P} I_{P(rms)}^2 + r_{N_S} I_{S(rms)}^2 + P_{Core} \quad (101)$$

The input inductors' copper loss (P_L) is calculated by:

$$P_L = \sum_{i=1}^{2} r_{L_i} I_{L_i(rms)}^2 \quad (102)$$

The energy dissipated due to the operation of the power switches (P_S) is composed of both conduction and switching losses, which can be calculated using the accompanying formulae.

$$P_S = \sum_{i=1}^{2} \left((r_{S_i} I_{S_i(rms)}^2) + (t_{on_{Si}} + t_{off_{Si}})(V_{S_i} I_{S_i}) f_S / 2 \right) \quad (103)$$

The diodes conduction loss (P_D) is calculated by:

$$P_D = \sum_{i=1}^{2} \left(V_{F_i} I_{D_i(ave)} + r_{D_i} I_{D_i(rms)}^2 \right) \quad (104)$$

The capacitors loss (P_C) is calculated by:

$$P_C = \sum_{i=1}^{3} \left(r_C I_{C_i(rms)}^2 \right) \quad (105)$$

The conversion efficiency of the suggested converter can be represented utilizing the subsequent equation.

$$\eta = (100P_O)/(P_O + P_{Total}) \quad (106)$$

The non-ideal VG of the propounded circuit can be represented using the following equation.

$$G' = G/\left(1 + (P_{Total}/P_O)\right) \quad (107)$$

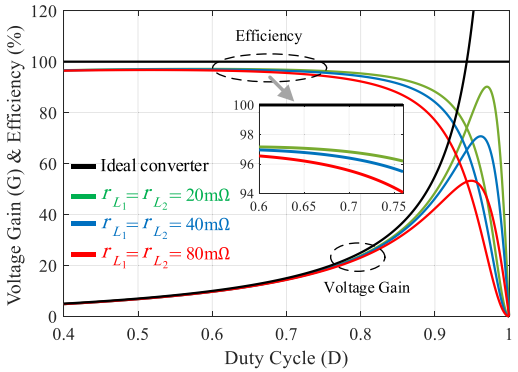

FIGURE 12. Efficiency and non-ideal VG of the propounded circuit.

The curves indicative of efficiency and VG considering the following condition, which are derived from analyzing the particulars listed in the datasheet of the elements constituting the manufactured example of the presented converter, are depicted in Figure 12.

$V_{in} = 30$; $n = 2$; $r_{Np} = 40\text{m}\Omega$; $r_{Ns} = 80\text{m}\Omega$; $R_{Load} = 567\Omega$; $r_C = 20\text{m}\Omega$; $r_{S1} = r_{S2} = 9.7\text{m}\Omega$; $t_{on} + t_{off} = 300\text{ns}$; $V_{F1} = V_{F2} = 1.5\text{V}$; $r_{D1} = r_{D2} = 10\text{m}\Omega$; $L = 300\mu\text{H}$; $L_m = 380\mu\text{H}$.

The aforementioned figure demonstrates that when in operation at high duty cycles, a rise in the inductor's resistance can lead to a substantial deterioration in the VG and efficiency of the converter being used. Therefore, It is important to design the inductors with a minimal degree of resistivity.

VI. COMPARISON STUDY

The main objective of the proposed topology is to improve the basic A-SL converter by adding a CI unit to its structure. Therefore, to evaluate the PC, it is necessary to compare it with other topologies that have tried to improve the basic A-SL structure [19], [20], [22], [25], [26], [27], [28] and [45]. Moreover, five other similar converters are provided for the comparison [30], [31], [32], [36], [37]. Several criteria are taken into account, including VG, the ratio of gain to component count, aggregate amount of voltage-induced tension on the power transistors, summation of voltages put on the power diodes, the total amount of voltage strain on the capacitors, the ratio of total voltage stress to VG, evaluating the input current ripple (ICR) characteristic, and a common ground connection availability. Comprehensive details of the converters can be found in Table 3. The turns ratio for this comparison is selected to be $n = 1.5$.

The magnitude of the voltage-boosting characteristics is portrayed in Figure 14(a). It is clear from the graph that among the converters investigated, the one proposed in this paper yields the greatest VG, while the lowest gain is credited to the method put forward in reference [31]. Moreover, the graphical representation of the proportion of VG to the number of constituent elements in Figure 14(b) for each converter shows that the suggested converter ranks most prominently. It can be observed from Figure 14(c) that both converters described in [32] and [36] and in the present work experience minimal total voltage tension on the transistors. Furthermore, Figure 14(d) illustrates the voltage tension comparison of each switch of the converters. It is clear that the voltage tension across each switch of the PC is the lowest; thus, the utilization of MOSFETs with a diminutive R_{on} to lessen the conduction loss and heighten the PC's efficiency is executable.

It can be inferred from the depiction in Figure 14(e) that six converters have diminished diodes voltage tension than the proffered converter. Considering the curves of the total amount of voltage strain on the capacitors, as depicted in Figure 14(f), there is no doubt that the presented topology is better than converters of [25], [26], [30], [31], [36], and [37]. Moreover, it shows that the lowest stress is related to converters of [27] and [28], and the highest stress is related to [31]. Finally, the ratio of total voltage stress to VG is plotted in Figure 14(g). This indicates that the presented structure exhibits the most reduced voltage stress in proportion to the given VG.

After discussing the benefits of the PC, it should be stated that the PC and structures presented in [19], [20], [22], [25], [26], [27], [28], [32], [37], and [45], there is not the same ground potential between their input and output. Common ground is preferred, but it should be noted that converters that do not have common ground can also be used in renewable energy applications [24], [37], [41], [43]. The ICR characteristics of non-isolated high step-up DC-DC converters are evaluated in [1] and are classified into seven groups with ratings of "A" (very low) to "G" (very high). Based on the results in [1], the pie chart depicted in Figure 13 shows each class's percentage. The ICR of the PC, like 11% of the converters, is placed in category E. Based on Figure 13, the PC has a lower ICR than 39% of the converters. Topologies in [30], [31], [32], and [36] are single-phase structures with a single input inductor; therefore, they are placed in category D. In some applications where the low ICR is required, for example, for tracking the maximum power point of PV panels, a simple low-pass input filter consisting of a capacitor and inductor can easily make the ICR as low as required. Moreover, it should be mentioned that in PV applications, the input filter is utilized by default, whether the ICR is high or low; therefore, converters with high ICR can also be utilized in solar PV systems or DC microgrids [37], [39], [40], [42].

To conclude, the proposed solution has significantly improved the performance of the basic A-SL converter compared with the other solutions that were applied to the basic A-SL converter. The highest VG, the highest ratio of the VG to total device count, the lowest voltage stress of each switch, and the lowest ratio of total voltage stress to VG belong to the PC. Therefore, the PC is a great candidate for high-gain applications.

VII. EXPERIMENTAL VERIFICATION

In order to corroborate the theoretical analysis and feasibility of the proffered circuit, a lab-based model is constructed

TABLE 3. Comparison of the proffered structure with other similar topologies.

Ref	VG	$\frac{\sum V_S}{V_O}$	$\frac{\sum V_D}{V_O}$	$\frac{\sum V_C}{V_O}$	Number of S / D	Number of C / L+CI	CG?	ICR class
[19]	$\frac{(2n+1)D+1}{(1-D)}$	$\frac{2}{(2n+1)D+1}$	$\frac{2n+2}{(2n+1)D+1}$	$\frac{(2n+1)D+2}{(2n+1)D+1}$	2 / 2	2 / $0+2^{2W}$	no	(E)
[20]	$\frac{(2n+1)D+1}{(1-D)}$	$\frac{2}{(2n+1)D+1}$	$\frac{2n+2}{(2n+1)D+1}$	$\frac{(2n+3)D+1}{(2n+1)D+1}$	2 / 3	3 / $0+2^{2W}$	no	(E)
[22]	$\frac{3+D}{1-D}$	$\frac{4}{3+D}$	$\frac{8}{3+D}$	$\frac{5-D}{3+D}$	2 / 5	3 / 4 + 0	no	(F)
[25]	$\frac{1+3D}{1-D}$	$\frac{2}{1+3D}$	$\frac{4}{1+3D}$	$\frac{3+5D}{1+3D}$	2 / 2	3 / 3 + 0	no	(E)
[26]	$\frac{1+5D+2D^2}{(1-D)}$	$\frac{2(1+D)}{1+5D+2D^2}$	$\frac{6+8D-2D^2}{1+5D+2D^2}$	$\frac{3+11D+2D^2}{1+5D+2D^2}$	2 / 8	3 / 5 + 0	no	(E)
[27]	$\frac{1+3D}{1-D}$	$\frac{4+3D}{1+3D}$	$\frac{4+D}{1+3D}$	1	4 / 5	1 / 4 + 0	no	(E)
[28]	$\frac{1+5D}{1-D}$	$\frac{3+5D}{1+5D}$	$\frac{6+8D}{1+5D}$	1	3 / 12	1 / 6 + 0	no	(E)
[30]	$\frac{1+2D}{1-D}$	$\frac{1}{1+2D}$	$\frac{3}{1+2D}$	$\frac{2+5D}{1+2D}$	1 / 3	5 / 3 + 0	yes	(D)
[31]	$\frac{3D}{1-D}$	$\frac{1}{3D}$	$\frac{1}{D}$	$\frac{1+8D}{3D}$	1 / 3	6 / 4 + 0	yes	(D)
[32]	$\frac{2+2D}{1-D}$	$\frac{1}{2+2D}$	$\frac{5}{2+2D}$	$\frac{3+4D}{2+2D}$	1 / 5	7 / 3 + 0	no	(D)
[36]	$\frac{nD+n-1}{(n-1)(1-D)}$	$\frac{n-1}{nD+n-1}$	$\frac{2n-1}{nD+n-1}$	$\frac{2nD+2n+D-2}{nD+n-1}$	1 / 2	3 / $1+1^{2W}$	yes	(D)
[37]	$\frac{2(1+2D)}{1-D}$	$\frac{1}{2}$	$\frac{5}{2}$	2	1 / 9	3 / 3 + 0	no	(E)
[45]	$\frac{1+n+D}{1-D}$	$\frac{4}{1+n+D}$	$\frac{2n}{1+n+D}$	$\frac{1+2n-nD+3D}{1+n+D}$	4 / 2	4 / $0+1^{3W}$	no	(E)
PC	$\frac{(3n-1)D+n-1}{(n-1)(1-D)}$	$\frac{2(n-1)}{(3n-1)D+n-1}$	$\frac{4n-2}{(3n-1)D+n-1}$	$\frac{2n+4nD-2}{(3n-1)D+n-1}$	2 / 2	3 / $2+1^{2W}$	no	(E)

PC: Proposed Converter; S: Switch; C: Capacitor; D: Diode; L: Inductor; CI: Coupled-Inductor; CG?: Common Ground?; ICR: Input Current Ripple.

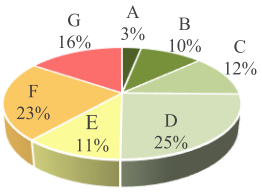

FIGURE 13. Classification of non-isolated high step-up DC-DC converters according to their ICR, based on Table 2 of reference [1].

and tested. This version is intended to accelerate a 30V input voltage into a 400V output load voltage in the power range of 200-300W. The details of the prototype and its respective components have been itemized in Table 4, with a visual representation of the model in its experimental environment as exhibited in Figure 15. An open-loop control mechanism is utilized, where the input voltage remains constant at 30V, and by using a microcontroller of the Arduino pro micro model, switching pulses having a frequency of fifty-kHz are produced at a duty cycle determined to be 0.68 to obtain the experimental results for the steady-state operation of the PC. The collected oscilloscope waveforms from the prototype under a load of two hundred watts are illustrated in Figures 16-18.

Examination of Figure 16(a) illustrates that the observable load voltage and the voltage measured on capacitor C_1 are both 400V and 270V, respectively, in correspondence with prior theoretical computations. It should be noted that the non-ideal VG is calculated to be 13.48 using (107), based on the components used in the laboratory prototype; therefore, the theoretical output voltage is 404V. Also, the voltage across capacitor C_1 is calculated to be 279V using Table 1.

The voltage across the capacitors C_2 and C_3 are provided in Figure 16(b); it is evident that the voltage across them is 161V and 239V, respectively, and their voltage ripple is very low. It is noted that the equations in Table 1 adequately predicted the voltages V_{C2} and V_{C3} across the capacitors.

The voltage waveform of the power transistors along with their current waveform, is observable in Figure 17(a). It is clear that during its off-state, the voltage on the switch is

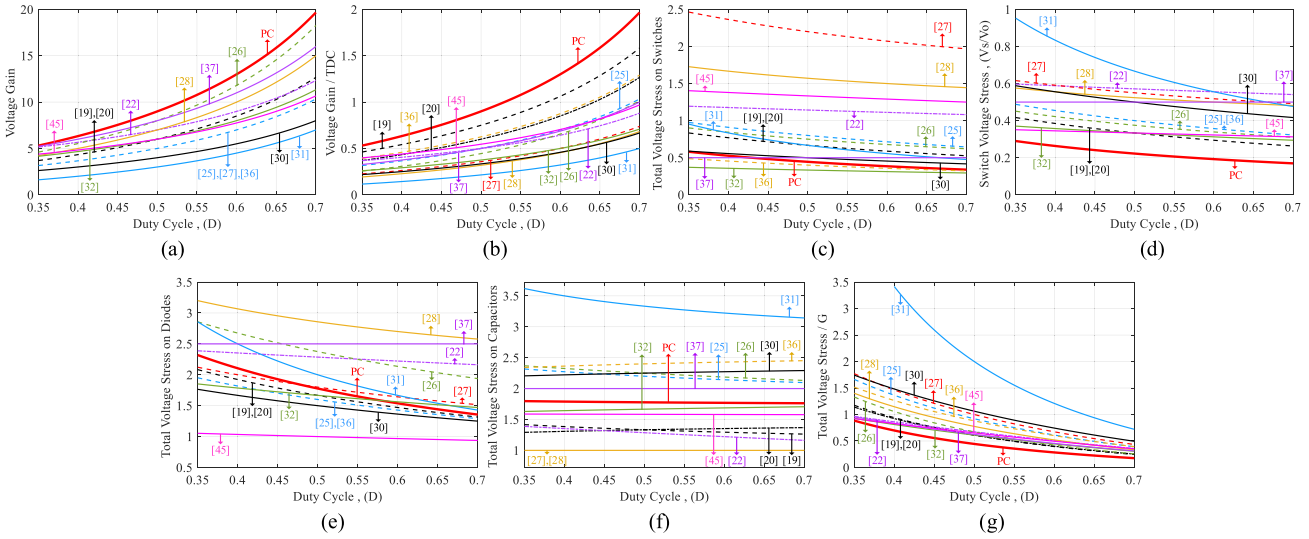

FIGURE 14. Comparison results (n=1.5); (a) Variation of VG with duty ratio; (b) Variation of ratio of VG to total device count with duty cycle; (c) Total voltage tension on the power switches; (d) Voltage tension on each switch; (e) Total voltage tension across the diodes; (f) Total voltage stress across the capacitors; (g) Variation of ratio of total voltage stress to VG with duty ratio.

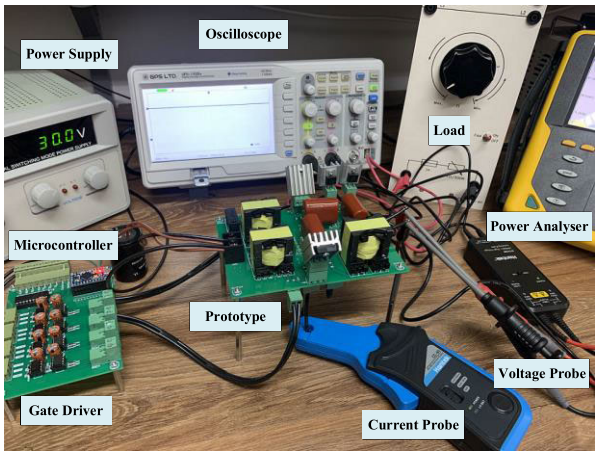

FIGURE 15. Experimental setup and prototype photograph.

TABLE 4. Parameters of the prototype.

Parameters	Value/Description
V_{in}	30V
V_{out}	400V
Power Range	200-300W
Switching Frequency	$f_S = 50$kHz
Input Inductors L_1 and L_2	300μH ($r_{L1} = r_{L2} = 35$mΩ)
Coupled-Inductor	Turns ratio = 2 Magnetizing inductance = 380μH Leakage inductance = 9μH ($r_{pri} = 40$mΩ , $r_{sec} = 90$mΩ)
Capacitors C_1, C_2, and C_3	10μF/400V (ESR = 20mΩ)
Power Switches (MOSFET)	IRFP4668PbF ($R_{DSon} = 9.7$mΩ)
Diodes D_1 and D_2	MUR2040 and MUR1060

constrained to a level of 99V, a quarter of the generated load voltage, and is congruent with the evaluation from (43). Therefore, it is feasible to apply lower-voltage rated switches with minimized on-resistance to augment the effectiveness of the converter.

The waveforms in Figure 17(b) representing the voltage and current of diode D_1 demonstrate an expected blocking voltage of 193V, which corresponds with the findings from the calculation of (44). Furthermore, the current of this diode can be seen to be abated to a null value, shutting off by its own accord under ZCS condition; this is because the energy stored in the L_k is recycled through diode D_1. Moreover, utilizing the current waveform of diode D_1, a measurement of operation mode III's duration has been made to be about 3μs, which is in accordance with the determined value from (62). The waveforms related to diode D_2 are shown in Figure 17(c). Observations indicate that the voltage tension across this diode is 356V, which is lesser than the load voltage, and verifies the calculation from (45).

The current waveform related to the input inductors is shown in Figure 18(a). It is clear that input inductors are charged when the MOSFETs are on-state and de-energized when they get off-state; therefore, as discussed in section III, reversed biased of diode D_1 in operation mode three has no impact on the voltage across the inductors and consequently on the converter's gain calculation. The measured average current through inductors L_1 and L_2 is equal to 3.65A, which is in accordance with the theoretical value calculated from (52). Furthermore, the measured current ripple of inductors is 1.3A which is very close to the calculated value (1.35A) using (82). It is determined that when the output power is 200W, the input inductor current ripple rate is approximately 37%, and the converter operates in CCM.

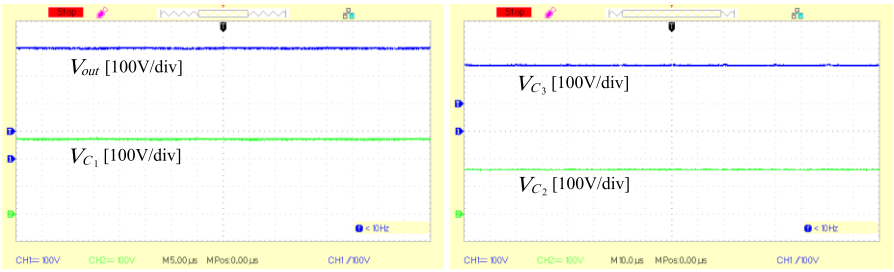

FIGURE 16. Experimental results; (a) Output voltage V_O and capacitor voltage V_{C1}; (b) Capacitors voltage V_{C2}, V_{C3}.

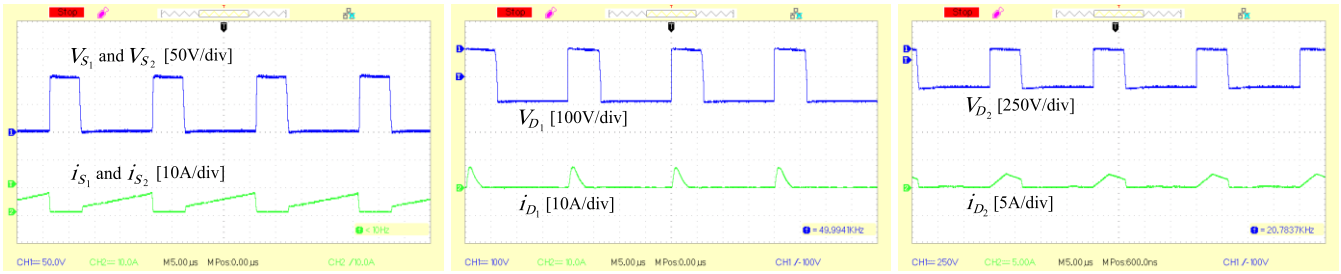

FIGURE 17. Experimental results; (a) Waveforms of the switches; (b) Waveforms of diode D_1; (c) Waveforms of diode D_2.

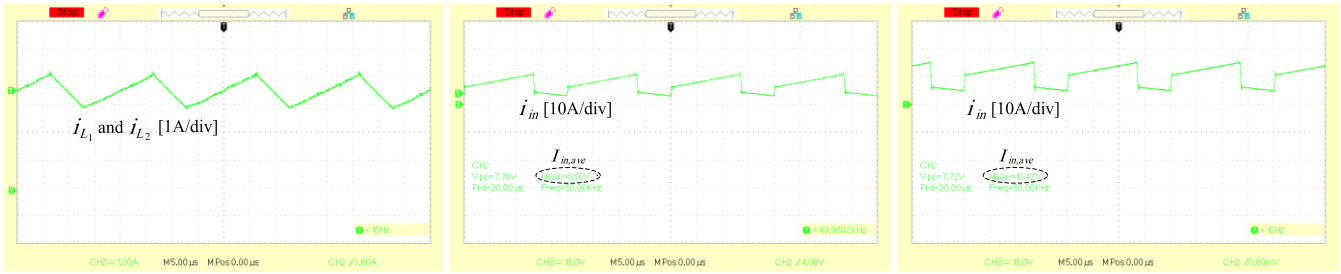

FIGURE 18. Experimental results; (a) Current waveform of inductors L_1 and L_2; (b) Input current waveform at P_{out}=200W; (c) Input current waveform at P_{out}=300W.

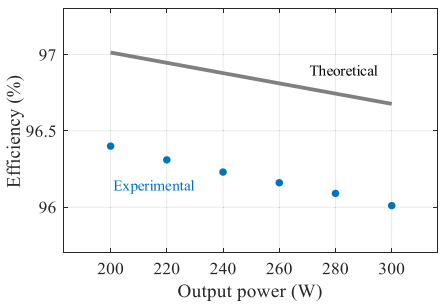

FIGURE 19. Experimental and theoretical efficiency versus output power.

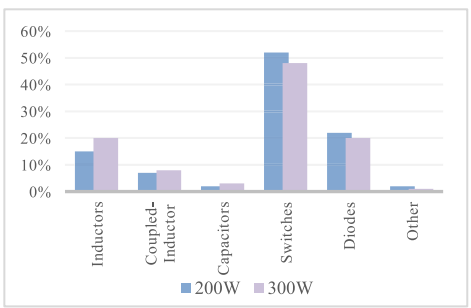

FIGURE 20. Power loss distribution of the propounded converter.

The efficiency of the prototype is measured by CHAUVIN ARNOUX 8336 Power & Quality Analyser to evaluate the quality of the presented converter. Figure 19 illustrates the theoretically plotted efficiency curve using (106) and experimentally measured efficiency at different output power levels from 200W to 300W. It shows that the efficiency of the prototype gradually declines by raising output power. In the operating power range, the conversion efficiency is greater than 96%, and at 200W, it reaches 96.4%.

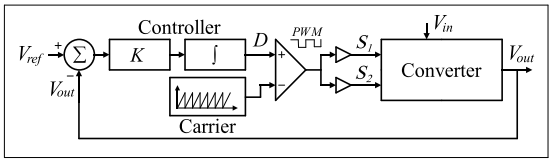

FIGURE 21. Schematic of the closed-loop control of the PC.

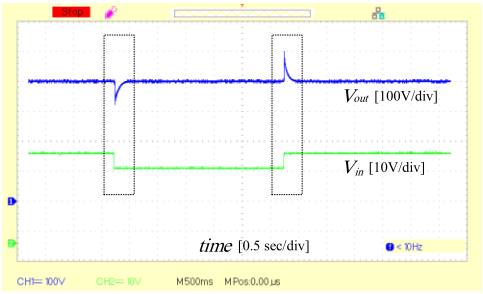

FIGURE 22. Dynamic response, step change of the input voltage.

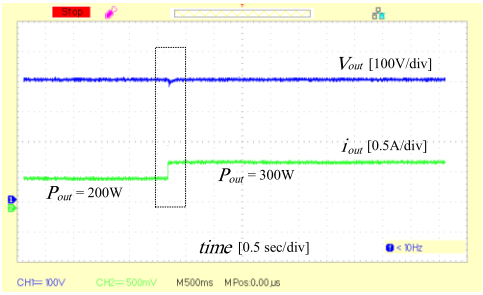

FIGURE 23. Dynamic response, step change of the load.

Furthermore, the input current waveforms with the measurements of $I_{in,ave}$ at the output power of 200W and 300W are provided in Figures 18(b) and 18(c), respectively, verifying the prototype's efficiency measurement. The theoretical and experimental results demonstrate that the PC can achieve high-level efficiency.

The power loss dispersion of the converter at two particular output powers is exhibited in Figure 20. It is evident that major losses in the presented circuit are related to the switches and, after them, related to the diodes. As the current flow increases with high output power, winding copper loss becomes dominant; for this reason, as is evident in Figure 20, at the 300W output power, the proportion of winding loss is increased compared with 200W. The major part of the diodes' losses is related to their forward voltage drop; therefore, better-graded diodes can be utilized to further improve efficiency.

For the dynamic analysis of the PC, the closed-loop control mechanism is used, and its schematic is depicted in Figure 21. The duty cycle of the switches is controlled to regulate the output voltage at the desired value (400V). The coefficient of the controller is set to be $K = 0.01$.

Figure 22 shows the dynamic response of the PC with the input voltage variations. It is seen that when the input voltage changes from 30V to 25V and vice versa, the output voltage is regulated at 400V successfully. Figure 23 represents the dynamic response of the PC with the output power change. As can be seen, when the output power changes between 200W to 300W values, the output voltage regulation is well achieved.

VIII. CONCLUSION

In this article, a new structure for high step-up DC-DC converters based on the combination of A-SL and CI techniques is propounded. The CI is used in this structure in a way that a greater VG is achieved by reducing the CI's turn ratio; hence, in this structure, a high turn ratio is not mandatory to achieve a high VG. The core saturation problem of CI is avoided by a series connection of the primary winding with a capacitor. Due to recycling leakage energy, the CI will not cause problems to the power switches, such as high voltage spikes. The input current is divided between the input inductors and power transistors, resulting in decreased conduction losses. Both the power switches are driven simultaneously, and a wide and unrestricted range of duty cycles is available. A description of the operating principle is presented, along with steady-state analyses to obtain equations for the voltage conversion ratio, voltage, and current tension within each component. The features of the presented structure are evaluated through a comparison study between other high-gain converters that use similar boosting techniques. After providing design guidelines, selecting the required components, and calculating the non-ideal VG and efficiency of the converter, a laboratory prototype is constructed to convert a constant input voltage of 30V to 400V. The prototype is tested in several output powers from 200W to 300W, and its conversion efficiency is measured and compared with theoretically obtained values. Results obtained from the tests support the analysis, assessment, and functioning of the introduced circuit. At the output power of 200W and VG of 13.33, the peak efficiency of 96.4% is measured; thus, this converter can adequately perform the task of high step-up conversions, making it ideal for a variety of applications.

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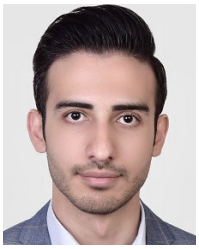

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