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RESEARCH ARTICLE

An Alternative Level Enhanced Switching Angle Modulation Schemes for Cascaded H Bridge Multilevel Inverters

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ABSTRACT This paper suggests an alternate level enhancing algorithm to operate the nine-level cascaded multilevel inverter (CHBMLI) for a 31-level output, which involves an inventive selection of optimal asymmetrical voltage values in separate DC sources (SDCs) and a quarter-wave symmetry pulse pattern pulse width modulation (QSP-PWM). The symmetrical CHBMLI structure involves the same DCs with an objectionable value of component count, especially at higher level outputs; consequently, there is a need to reduce the component count. It can be supported largely by the optimal set of asymmetrical voltage values (say 1:2:4:8), such an actualization is quite easy with photovoltaic (PV) applications. Additionally, many of the commonly used PWM methods of MLI are tedious especially when it comes to the generation of pulses. This paper also engraves a straightforward switching strategy apposite to the developed MLI topology. In addition, three new switching angle modulation schemes have been proposed to get the optimum performance, namely, incremental delay switching angle modulation scheme, random delay switching angle modulation scheme and sine referencing-based switching angle modulation scheme. The preliminary study on the tenet of suggested topology is done theoretically, then the performance is analyzed in MATLAB2019a software and finally, experimentally corroborated on a proof-of-concept (POC) prototype with the aid of ModelSim6.3f hardware description language simulation environment, Xilinx 14.5 project navigator tool and XC3S500E field-programmable-gate-array processor. The tested results for the inductive load demonstrate the output voltage synthesizing and the total harmonic distortion curtailment savvies of the proposed MLI and the switching strategies.

INDEX TERMS DC-AC power converters, harmonic analysis, modular multilevel converters, pulse width modulation inverters, total harmonic distortion.

I. INTRODUCTION

Modern industrial applications necessitate higher power conversion systems in the present era. The medium and megawatt drives become prevalent, wherein the industry started demanding improved efficiency. The performance of the inverter in the power conversion process is accounted for by the combined outcomes of the pulse width modulation (PWM) scheme and the power converter topology. For a medium voltage grid, it is hard to connect the power converter

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semiconductor switch directly. Since 1975, multilevel inverters (MLIs) have been used to overcome such issues. The first MLI circuit came out after an incessant contemplation on the two-level inverters. The proclamation of multilevel starts from the introduction of the three-level inverter. Afterward, several topologies of MLI have been mechanized. The basic concept of the MLI is to reach greater power through a series of power semiconductor switches with several lower DC voltage sources to accomplish the voltage ac in form of a staircase voltage waveform. An MLI has the following benefits over a traditional two-level inverter which incorporates high switching frequency PWM schemes.

1. dv/dt stresses: Admirable connection of commutable power switches along with multiple dc sources paves the way to get the high voltage at the output; however, the rated voltage of the power semiconductor switches is governed by only the rating of the DC voltage sources to which they are connected. So that the structure of the MLI reduces the dv/dt stresses; consequently electromagnetic compatible complications can be reduced.
2. Common Mode (CM) voltage: The CM voltage is influenced by the switching method. MLIs contribute to smaller CM voltage. The innovative modulation schemes are having the capability to remove the CM voltage.
3. Renewable Sources utilization: A MLI-based system for high-power applications can be straightforwardly integrated with renewable energy sources such as wind turbines or photovoltaic systems.
4. Distortion: MLI draws a low distortion input current.
5. Switching loss: MLI can be operated at both high/fundamental switching frequencies. It would be well-known that lower switching frequency incorporated inverters will produce lower switching losses.

Many MLI topologies have been suggested in the previous few decades. Based on the MLI structure, It can be divided into (i). H-Bridge (HB) MLIs, (ii) Diode clamped MLIs, and (iii) Flying capacitor MLIs. The HBMLI involves one H-bridge module for the synthesis of every step in the output. Amid the 4 switches, the concurrent turn on and turn off of the opposite switch pair will provide the voltage levels $+V_{dc}$ or $-V_{dc}$ across the load. The output will be zero if all the switches are turned off. Renewable energy source-based battery-backed applications and static VAR generations are using CHBMLIs. The electric system integrated with a multilevel cascaded static VAR generator has been established by Peng et al. for supplying or drawing reactive current from an electric system [1]. The ultra-capacitors can act as a separate DC source for cascaded inverters, which have been proposed to use as the main traction drives along with several batteries [2]. The neutral point converter suggested by Nabae, Takahashi, and Akagi in 1981 was fundamentally a three-level diode-clamped inverter [7]. The diode-clamped inverters serve as an interconnector between the high-voltage system and variable-speed drives [8], [9]. The outrageous drawback of this topology is the real power flow is difficult for a single inverter because of the fluctuating intermediate DC levels. The flying capacitor-based MLI prototype was developed by Meynard and Foch in 1992 [10]. The structure of this MLI is the same as the diode-clamped inverter, but the capacitor has been served instead of clamped diodes. One advantage of the flying capacitor-based inverter is that it has redundancies for inner voltage levels, that is, two or more valid switch combinations can be synthesized to get an estimated output voltage [11], [12]. For real power transmissions, the efficiency and switch utilisations are diminished in flying capacitor-type MLIs. Moreover, when compared with the clamped MLI, the flying capacitor MLI has large numbers of expensive capacitors, which are unavoidable elements. The packaging is also spectacularly challenging in those inverters while increasing the number of levels. Marquart has presented the first modular multilevel inverter (MMI) in 2001 [13]. The MMI configurations consist of the DC sources connected in series along with appropriate switches, and this module is connected to the upper and lower arms of the submodule (SM). The series of SMs are connected along with L and R between the DC terminals for each phase. The SM can be designed by a half-bridge [14], full-bridge [15], or clamp diode circuits [16]. MMCs can be interfaced with the HVDC voltage level since IGBT ratings are in the kV level and HVDC rating is normally in hundreds of kV, commonly several hundred SMs are used for one MMC [17]. A type of multiport converter (MPC), to effectively utilize the sources, has been coined in recent decades [18]. In this topology, the seven-level inverter with simple half-bridge switches is providing multiple levels. This scheme has the ability to exploit photovoltaic-based power supplies.

When it comes to using the DC sources for the MLIs, they can be divided into single DC Source based MLIs and multiple DC source-based MLIs. The Flying capacitor MLIs are powered by one DC source alone. In that, series and parallel connections between similar/dissimilar capacitors determine how many levels can obtain by the MLI. On the other hand, the MLI structure frequently adds and subtracts DC source voltages to get rid of capacitors. Using the DC sources as a basis, MLIs may be divided into (i). Unsymmetrical DC sources have different voltage values than symmetrical DC sources, which are all identical in voltage values. Joes et al. have demonstrated that cascaded symmetrical inverters can be connected in series with the electric system for static VAR compensation [3]. Manjrekar and Lipo have investigated a cascade topology that uses bizarre DC levels, which instead of being identical in value are multiples of each other [4], [5]. Trinary hybrid MLIs are the class of asymmetrical MLIs, wherein the DC voltage ratio is 1:3:. . . .3h-1, where, 'h' is the number of HBs [6].

To produce the desired output voltage, numerous modulation techniques are available. It can be classified into (a) Carrier-based MLI 2. Carrierless MLI. Pulse pattern (duration, position, and count) is synthesizing the output voltage shape and also provides the corresponding performances. The vertical shifted multi-carrier arrangements are commonly

applied modulation schemes in the industry [19], [20]. It can be easily implemented in low-voltage modules. The number of carriers will be decided based on the number of levels in the output. The carrier-based MLI can be subdivided into level-shifted PWM and phase-shifted PWM methods [19]. The level-shifted PWM is categorized into Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition [20]. In the APOD method, harmonics are cantered as sidebands around the carrier frequency. The carrierless PWM is the pulse generation method that does not have any carriers. Selective Harmonic Elimination (SHE) PWM is one among them, which is a widely used switching strategy to unambiguously remove the selected harmonics from the output waveform of the inverter [21], [22]. The specular characteristic of the SHE-PWM is the elimination of selected lower-order harmonics in the low switching frequency operation [23], [24]. The superiority of SHE-PWM techniques over other modulation methods is low switching frequency, direct control, and elimination of output waveform harmonics [25], [26]. The optimized switching angles are calculated by cracking the transcendental equation-based Newton-Raphson method for eliminating the harmonics. Nonetheless, the SHE PWM eliminates harmonics, it has several weaknesses listed below. (i) Leisurelier reaction during transient conditions, and (ii) difficulties in the real-time implementation of transcendental equations (high execution time, the requirement of more memories, and defining initial values). The best switching angles can be chosen by using anyone optimization algorithm [26]. But the implementation of such optimization algorithm-based PWM techniques is a challenging task. (iii) Moreover, those methods are carried out in offline mode. These best switching angles formulated PWM can be implemented in any digital controller for online mode, (iv) Apart from that, the ensuing switching angles should be preserved at less than $\pi/2$ [27], [28].

In [29], proposed the new SHE PWM-based MLI, which claims that the nonlinear equations are needed to be solved only once for the complete range of output voltage. The SPWM and SVM are instituted to eliminate all of these flaws [30]. The pristine SPWM compares a fundamental frequency sine reference with high-frequency triangular carriers through natural sampling. The PWM duty cycle (per carrier cycle) can be decided by the crossing points of the above two waves. Whereas, the pulse generation procedure in the case of SVM is purely based on the regular sampling involved with vector averaging time calculations. These calculations yield duration for two adjacent vectors to synthesize the output reference phasor, which in turn is converted into a duty cycle for every switch. The SVM is superior to the SPWM because of (i) better DC bus utilization. (ii) reduction in the common mode voltage, (iii) improvement in the output voltage with harmonic reductions [31]. The earlier attempts have revealed the fact that the inherent problem of unbalance in DC voltages of neutral point clamped MLI (NPC-MLI) could be solved through a virtual SVM, in which medium vectors are dodged. The detailed confabs on such type of MLI are presented in [32], [33], and [34]. A wide-ranging assessment was carried out on NPC-MLI using SVM techniques [35].

In recent years, researchers are gradually focussed on switched capacitor-based MLIs (SCMLI) due to the possibility of using a single voltage source to get the multiple levels. The concept of a switched capacitor has been introduced in 1977 [36], but the switched capacitor is an integrator for analog sampled data filtering applications. The rudimentary high-gain boost switched capacitors inverters have been coined in 2012 [37]. The SCMLI topologies are intended to get multiple levels by using the switched capacitor cells. Varieties of SCMLIs have been investigated [38], [39]. A new single source high step-up SCMLI has been discussed [40]. This topology has the ability to achieve multiple levels by using self-balancing capacitors in the asymmetrical mode. In this scheme, two half-bridge circuits are used on the left side and right side of the capacitor topology using the two half bridges to avoid the high-voltage full bridge circuit.

Most of the recent MLI topologies are being derived topologies from the previously topologies [41]. These inverters are called high-efficient reliable inverter concept (HERIC) topologies. A new-fangled DC decoupling five-level inverter has been proposed [42] and it is derived from the HERIC topology. The designed topology has the wherewithal to boost the input voltage by a factor of 2. A sequel of thereof three modulation schemes is used to achieve constant common mode voltage. The innovative 7-level SCMLI has been reported [43] with triple voltage boosting capability with a low input voltage by using the 12 switches and two capacitors. The multi-carrier-based PD-PWM schemes have been employed.

The gain improvement of the switched capacitor-related MLIs has been developed since 2016 [44]. In this design, 9 unidirectional switches have been used along with 2 capacitors and 2 diodes with a single voltage source. This resulted in more stress on the switches. The stresses of the switches are addressed in [45] and provided a solution. Nonetheless, this design is a version of the original design with some small alterations to the switch positions. The contemplated quadruple gain improved SCMLI has been coined in 2021 [46], which uses 8 switches, 2 diodes, and 2 capacitors along with a low voltage source. The main issue in those topologies is the drawing of the objectional value of capacitor charging.

The sextuple gain enrichment in SCMLI has been proposed [47], [48]. The wherewithal of these topologies is achieving 13 levels with 3 switched capacitors (ratio of 1:2:2) and using 14 and 15 switches individualistically. The intrinsic merit of these topologies is the maximum blocking voltage of less than half of the peak voltage. A parabola-based multicarrier SCMLI has been investigated and achieved nine levels with self-boosting capability [49].

However, the following criticisms are inescapable. (i) The switched capacitors' values are tedious to calculate with different ratios while attaining the multi-levels. (ii) The above

SCMLI schemes are claiming that they are avoiding the H-bridges, but they do use two half bridges along with the SCMLI topology, and (iii) SCMLI topologies are claiming that they involve reduced switches. However, the number of capacitors and diodes are increased when compared to regular H-bridge-based MLIs, and (iv) In the multi-carrier-based modulation schemes discussed in [47] and [48], some digital designs are obligatory to generate the PWM for the switches.

Any PWM technique involves changing the width of the pulses focusing to get an improved fundamental component, a conductive harmonic profile, and reduced Total Harmonic Distortion (THD). The amplitude of the dominating harmonics and their orders are also crucial factors while considering the acoustic noise in drives. The two-level SPWM exhibits the harmonics in and around the switching frequency. But, the switching frequency of the inverter switches is very less, and then the dominating order harmonics are accumulated at lower order harmonics, which are very dangerous for induction motor drives. Hence, the suppression of dominating harmonics is very much required which is achievable by a host of random PWM methods (Randomized switching frequency, randomized pulse position, or random switching) [24]. The generation of the above carriers and generating the pulses are very difficult to meet the requirement of the MLI [25]. Digital implementation of the above carriers-based PWMs is not the only challenging task for digital design engineers; fitting the architecture into the target digital processor too. Field Programmable Gate Array (FPGA) based digital controller offer benefits such as high speed, complex functionality, and low power consumption [26]. An additional advantage of FPGA based platform is their aptness to perform concurrent processes, allowing the parallel architectural design of digital controllers [27], [28], [29]. These are eye-catching features from the embedded systems perspective, especially for use with an MLI, which is required to control switches in parallel.

The Cruz of any PWM lies in the fashion of the varying gate pulse width of the switches. Carrier-less (optimal or regular sampled) PWM is a relatively new method to overcome such drawbacks.

The effectiveness of PWM is based on a unique modulation scheme to vary the pulse widths from one carrier cycle to the next. However, a tailor-made PWM strategy for a new MLI structure can increase the structure's acceptability. The carrier-less, digital PWM methods, are implementation friendly at a digital processor platform like FPGA. In this paper, the nine-level CBHMLI is operated to produce 31-level output in an asymmetrical mode with the formulaic switching sequence and timing of the designed level-enhancing algorithm (LEA). In addition to that, four inventive switching angle modulation schemes are examined. Those are namely (i). Quarter-wave Symmetry Pulse pattern Pulse Width Modulation (QSPPWM), (ii) Incremental Delay Switching Angle Modulation (ICDSAM), (iii) Random Delay Switching Angle Modulation (RDSAM), and (iv) Sine Referencing Switching Angle Modulation (SRSAM).

The organization of this paper is given as follows: In section II, modes of operation of the asymmetrical 31 levels MLI. In section III, proposed switching angle modulation schemes for H bridge switches is presented. In section IV, performance measures for various types of load. Section V describes the simulation results and discussion for the proposed modulation schemes and section VI describes the hardware implementation proposed schemes.

II. MODES OF OPERATION OF THE ASYMMETRICAL 31 LEVEL H BRIDGE INVERTER

The photovoltaic (PV) aided nine-level CHBMLI (four H-bridges) with the optimal SDCs values for making an asymmetrical 31-level operation is shown in Fig.1. 'i' is the total number of H bridges; 'm' is the number of output levels obtained from the CHBMLI during symmetrical operation; m' is a number of output levels obtained from the CHBMLI during asymmetrical operation with the LEA. The LEA can make, $m' = (2^2 - 1)$ levels from the m level CHBMLI. The suggested switching sequence (Table 1) and the optimal SDCs' values in the ratio 1:2:4:8 are mandatory. Table 1 has two descriptions: one is above the diagonal line, and the other is below the diagonal line, while a description represents the switch of a host of switches. A tick mark indicates the participation of switches described respectively by the above and below diagonal line descriptions for the positive and negative levels (indicated in the row description). In this configuration, each bridge's first leg power switches (PS_1, PS_5, PS_9, PS_{13}, PS_4, PS_8, PS_{12}, and PS_{16}) are operating under fundamental frequency, but the lower leg switches (PS_4, PS_8, PS_{12}, and PS_{16}) are 180° phase shifted. The first leg switches decide the type (positive/negative) of the half-cycle. At each positive half cycle, first leg upper switches are ON. On the contrary, at each negative half cycle, the first leg lower switches are ON. The successive states of the second leg switches (PS_2, PS_3, PS_6, PS_7, PS_{10}, PS_{11}, PS_{14}, and PS_{15}) are responsible for the multilevel output. In the H-bridge 1, second leg switches, PS_2 and PS_3, are responsible, respectively, for positive and negative half-cycles at any odd-numbered level. In the H-bridge 2, second leg switches, PS_6 and PS_7, are responsible for achieving the second and higher levels. Likewise, in the H-bridge 3, second leg switches, PS_{10}, and PS_{11}, are obvious for achieving levels from fourth. In H-bridge 4, second leg switches (PS_{14}, PS_{15}) are responsible for achieving the eight-level and above. In all the H-bridges, crossed switches (PS_1, PS_3, PS_5, PS_7, PS_9, PS_{11}, PS_{13}, PS_{15} or PS_4, PS_2, PS_8, PS_6, PS_{12}, PS_{10}, PS_{16}, PS_{14}) will be active whenever its PV array supply voltage needs for the load to achieve levels. Similarly, each H-bridge either the combination of upper leg switches (PS_1, PS_2, PS_5, PS_6, PS_9, PS_{10}, PS_{13}, PS_{14}) or the combination of lower switches (PS_3, PS_4, PS_7, PS_8, PS_{11}, PS_{12}, PS_{15}, PS_{16}) will be active whenever its PV array supply voltage does not need the corresponding voltage for the load to attain levels.

The 12V battery is used to provide a 12V DC supply for the first H-bridge, likewise, two 12V batteries for the second H-bridge, four 12V batteries for the third H-bridge, and eight 12V batteries for the fourth H-bridge to provide 24V, 48V, and 96V, respectively. The MPPT-based PV system is also possible to provide a 12V supply for the first H-bridge, likewise, multiple 1:2:4:8 PV system panels are required to establish the arrangements. But the PV panel is not able to provide a constant voltage due to the variable irradiance. Even though the 31 levels are possible by setting up PV panel arrangement in 1:2:4:8 order. For concentrating the switching angle modulation schemes, in this paper, batteries are used instead of PV panel systems in simulation, and a transformer and rectifiers are used in hardware implementation.

III. PROPOSED MODULATION METHODS

A. QUARTER WAVE SYMMETRY PULSE PATTERN PWM (EQUAL DURATION SWITCHING ANGLE MODULATION)

In the suggested QSPPWM, the switching angle (the instant of transition from one level to another) of n^{th} transition (where the maximum value of n is $(m'-1)/2$), α_n is determined based on the output frequency ($f_s = 50$ Hz), i and m. The duration between any two consecutive switching angles, say, α_n and $(\alpha_n + 1)$, are the same. If the required number of levels is 31, then the duration of each level could be

$$\frac{2}{(m+1)f_s} = \frac{2}{32 \times 50} = 0.0003125 Seconds \qquad (1)$$

Thus the resultant switching angles are $\alpha_1 = 0.0003125s = 5.625°$, $\alpha_2 = 0.000625s = 11.25°$, $\alpha_3 = 0.0009375s = 16.875° \ldots \alpha_{15} = 0.0046875s = 84.375°$. Fig.2 presents a simple combinational logic circuit to generate the gate pulse pattern for second leg switches of one H bridge based on the QSPPWM. A typical simultaneous gate pulse generation logic for all the second leg switches ($PS_2/PS_6/PS_{10}/PS_{14}$, $PS_3/PS_7/PS_{11}/PS_{15}$) requires four such modules. The figure consists of four AND gates, 5 NOT gates, and 2 OR gates. The gate pulses for the first leg switches are square pulses synchronized for the fundamental switching. The switching frequency selection in this QSPPWM scheme is based on the derived equations (2) for different H bridges.

$$f_{HBj} = \frac{f_s 2^{i+1}}{2^{j-1}} \qquad (2)$$

where, $j = 1, 2 \ldots i$; j denotes the H bridge for which the switching frequency is computed.

f_{HB1} –> Frequency of the first H-bridge, which is equal to 1600 Hz.

The f_{HB2}, f_{HB3}, and f_{HB4} are 800 Hz,400 Hz, and 200 Hz, respectively. f_k is a windowing signal, which has a frequency double that of the output (fundamental) frequency ($f_k = 2f_s = 100$ Hz). Equations (3) to (12) represent logical expressions for all the gate signals individually. The digital circuit (one module) and the derived power switch gate pulses

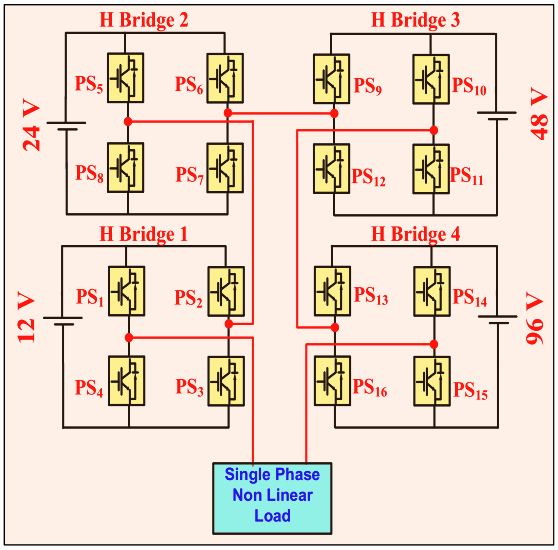


FIGURE 1. Asymmetrical 31-level H-bridge inverter.

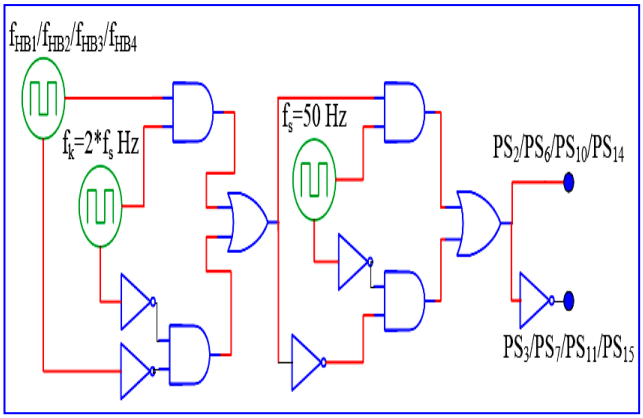


FIGURE 2. Quarter wave symmetry pulse pattern PWM.

are shown in Fig. 2 and Fig. 3 respectively.

$$PS_2 = \left(f_{HB1}f_k + \overline{f_k f_{HB1}}\right) f_s + \left(\overline{f_{HB1}f_k + \overline{f_k f_{HB1}}}\right) \overline{f_s} \qquad (3)$$

$$PS_6 = \left(f_{HB2}f_k + \overline{f_k f_{HB2}}\right) f_s + \left(\overline{f_{HB2}f_k + \overline{f_k f_{HB2}}}\right) \overline{f_s} \qquad (4)$$

$$PS_{10} = \left(f_{HB3}f_k + \overline{f_k f_{HB3}}\right) f_s + \left(\overline{f_{HB3}f_k + \overline{f_k f_{HB3}}}\right) \overline{f_s} \qquad (5)$$

$$PS_{14} = \left(f_{HB4}f_k + \overline{f_k f_{HB4}}\right) f_s + \left(\overline{f_{HB4}f_k + \overline{f_k f_{HB4}}}\right) \overline{f_s} \qquad (6)$$

$$PS_3 = \overline{\left(f_{HB1}f_k + \overline{f_k f_{HB1}}\right) f_s + \left(\overline{f_{HB1}f_k + \overline{f_k f_{HB1}}}\right) \overline{f_s}} \qquad (7)$$

$$PS_7 = \overline{\left(f_{HB2}f_k + \overline{f_k f_{HB2}}\right) f_s + \left(\overline{f_{HB2}f_k + \overline{f_k f_{HB2}}}\right) \overline{f_s}} \qquad (8)$$

$$PS_{11} = \overline{\left(f_{HB3}f_k + \overline{f_k f_{HB3}}\right) f_s + \left(\overline{f_{HB3}f_k + \overline{f_k f_{HB3}}}\right) \overline{f_s}} \qquad (9)$$

$$PS_{15} = \overline{\left(f_{HB4}f_k + \overline{f_k f_{HB4}}\right) f_s + \left(\overline{f_{HB4}f_k + \overline{f_k f_{HB4}}}\right) \overline{f_s}} \qquad (10)$$

$$PS_1 = PS_5 = PS_9 = PS_{13} = f_s \qquad (11)$$

$$PS_4 = PS_8 = PS_{12} = PS_{16} = \overline{f_s} \qquad (12)$$

TABLE 1. Switching states at different voltage levels.

Positive Half Cycle / Negative Half Cycle	$PS_1, PS_5, PS_9, PS_{13}$ / $PS_4, PS_8, PS_{12}, PS_{16}$	$PS_4, PS_8, PS_{12}, PS_{16}$ / $PS_1, PS_5, PS_9, PS_{13}$	PS_2 / PS_3	PS_3 / PS_2	PS_6 / PS_7	PS_7 / PS_6	PS_{10} / PS_{11}	PS_{11} / PS_{10}	PS_{14} / PS_{15}	PS_{15} / PS_{14}
0	√	×	√	×	√	×	√	×	√	×
±1 V_{dc}	√	×	×	√	√	×	√	×	√	×
±2 V_{dc}	√	×	√	×	×	√	√	×	√	×
±3 V_{dc}	√	×	×	√	×	√	√	×	√	×
±4 V_{dc}	√	×	√	×	√	×	×	√	√	×
±5 V_{dc}	√	×	×	√	√	×	×	√	√	×
±6 V_{dc}	√	×	√	×	×	√	×	√	√	×
±7 V_{dc}	√	×	×	√	×	√	×	√	√	×
±8 V_{dc}	√	×	√	×	√	×	√	×	×	√
±9 V_{dc}	√	×	×	√	√	×	√	×	×	√
±10 V_{dc}	√	×	√	×	×	√	√	×	×	√
±11 V_{dc}	√	×	×	√	×	√	√	×	×	√
±12 V_{dc}	√	×	√	×	√	×	×	√	×	√
±13 V_{dc}	√	×	×	√	√	×	×	√	×	√
±14 V_{dc}	√	×	√	×	×	√	×	√	×	√
±15 V_{dc}	√	×	×	√	×	√	×	√	×	√

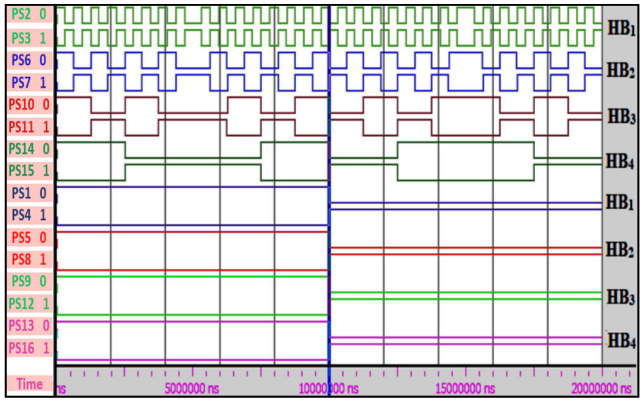


FIGURE 3. Quarter wave symmetry pulse pattern PWM.

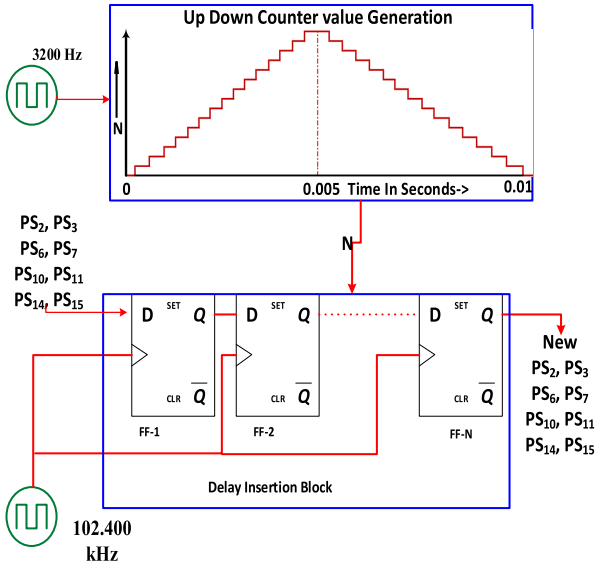


FIGURE 4. Incremental delay switching angle modulation scheme.

B. ICDSAM

This incremental counter delay switching pulse modulation is the extension of the QSPPWM shown in Fig 4. This logic has been implemented by using two modules. (i) The delay insertion block, which is getting the input of QSPPWM switching angle modulation. The delay has been chosen by the counter and shifts register-based module. The 4-bit up-down counter-based digital design has been synthesized and is being shifted left by using a single-bit left shift register. The resultant counter values are 0, 2, 4, 6 . . . . . .30.

The counter values decide the number of flip flops required to accomplish the delay of switching angles. Each Flip flop has been performing a delay of 0.000009765625 seconds or 0.17578125°. The delay varied 0.17578125° from varying 5.2734375°. The up-down counter is designed carefully to maintain the quarter-wave symmetry principle. Fig. 4. shows the up counter wrinkle in the half-cycle. Fig 5 shows the phase voltage and current at R=1 Ω with counter values.

C. RDSAM

This scheme is the extension of the incremental switching angle modulation scheme. Instead of the counter, random values are generated based on the 4-bit linear feedback shift register (LFSR). A random pulse width modulation scheme is a harmonic distributing scheme in the two-level inverter. All deterministic PWM approaches, like two-level VSI, result in a concentration of harmonic power around a band in MLI too, hence an attempt to include randomization notions in MLI is unavoidable. Fig. 5 shows the random switching angle modulation scheme.

D. SRSAM

This scheme is established based on the superimposing of the sine referencing waveform on the QSPPWM output

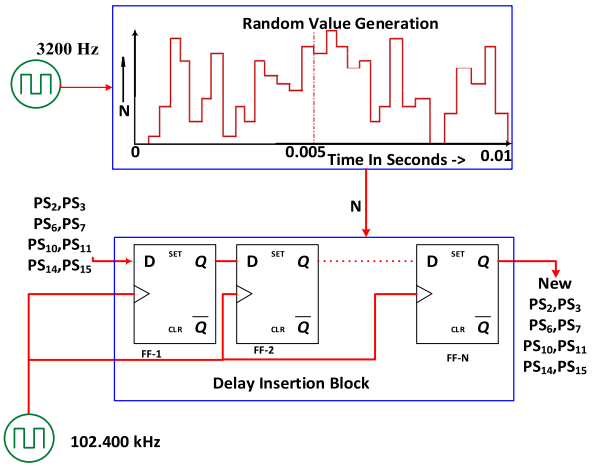


FIGURE 5. Random delay switching angle modulation scheme.

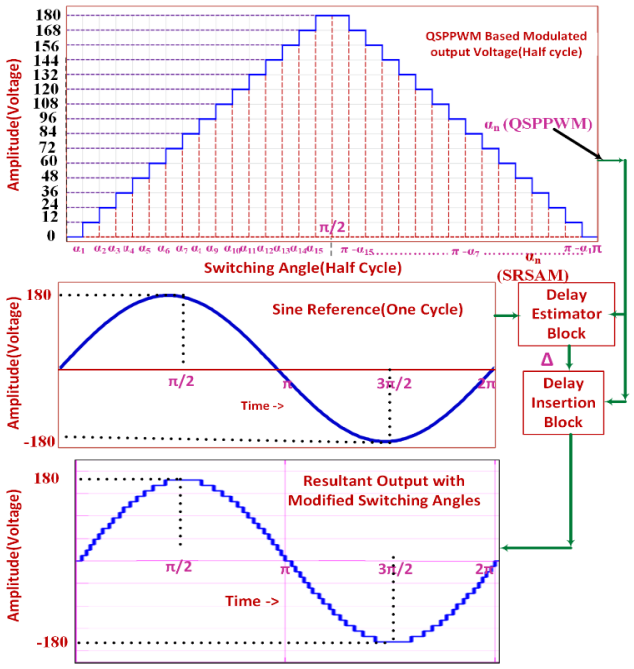


FIGURE 6. Sine referencing switching angle modulation.

waveform. The development of this scheme comprises of sine referencing waveform generation module, delay estimator, and delay insertion/advancing block along with a QSPPWM generation module. Fig 6. shows the pictorial representation of this modulation scheme. The delay advancing is considered based on the sine reference wave and the optimum new switching angle.

$$Delay\ \Delta = \alpha_{n(SRSAM)} - \alpha_{n(QSPPWM)} \tag{13}$$

E. SWITCHING ANGLE INTERPRETATIONS

Table 2. shows the resultant switching angles of all four schemes and the graphical representation is shown in Fig 7.

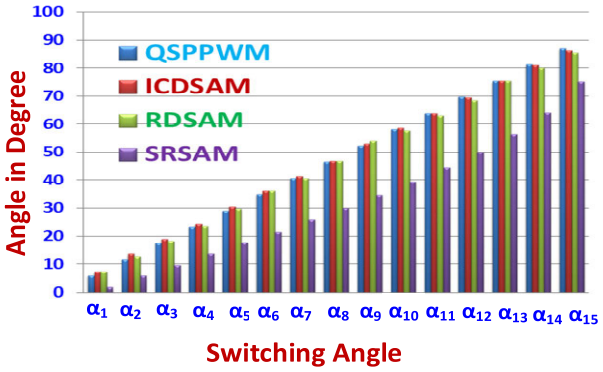


FIGURE 7. Exploring of switching angle in Quarter cycle.

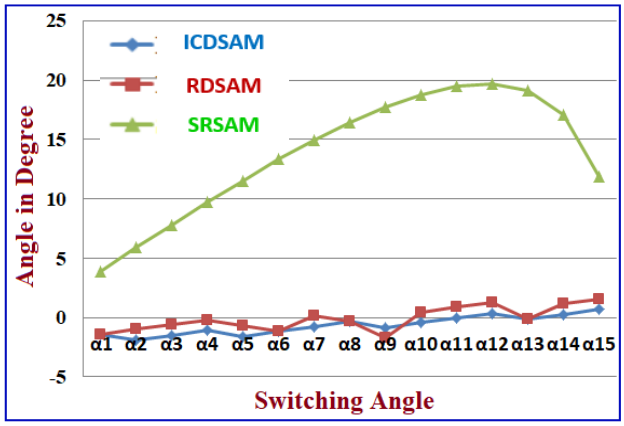


FIGURE 8. Exploring of difference between switching angle with QSPPWM in quarter cycle.

By comparing all the switching angles, the following interpretation is observed.

(i). The duration between the switching angles is constant in the QSPPWM. Whereas this duration differs in other schemes. Hence the QSPPWM scheme may also be named as the equal duration switching angle modulation scheme.

(ii). The incremental delay and random delay-based switching schemes are having the same exploration of the successive angles if the delay limit is less than 32 clock cycles (frequency of one clock cycle=102,400 Hz). While for more than 32 clock cycles, unacceptable switching angles will be formed, which are enveloping outside of the quarter cycle.

(iii). The best and most effective system is SRSAM, which satisfies quarter wave symmetry and produces an output that is surrounded by a sine wave.

(iv) Incremental and Random delay methods are developed by adding the delay at the edge of each switching angle. Whereas the sine referencing wave scheme is developed by advancing the switching angle from the QSPPWM switching angle.

(v). Fig. 8 shows the difference between the switching angle movements from the QSPPWM to the proposed schemes. Interestingly the switching angle of incremental and

TABLE 2. Switching angles of proposed modulation schemes.

Notch	Switching Angles			
	QSPPWM	ICDSAM	RDSAM	SRSAM
α_1	5.81	7.2	7.2	1.9
α_2	11.61	13.5	12.6	5.7
α_3	17.42	18.9	18	9.6
α_4	23.23	24.3	23.4	13.5
α_5	29.03	30.6	29.7	17.5
α_6	34.84	36	36	21.5
α_7	40.65	41.4	40.5	25.7
α_8	46.45	46.8	46.8	30.0
α_9	52.26	53.1	54	34.5
α_{10}	58.06	58.5	57.6	39.3
α_{11}	63.87	63.9	63	44.4
α_{12}	69.68	69.3	68.4	50.0
α_{13}	75.48	75.6	75.6	56.4
α_{14}	81.29	81	80.1	64.2
α_{15}	87.10	86.4	85.5	75.2

TABLE 3. Switching frequency attained by the proposed modulation schemes.

Switches	min/max	Switching Frequency(kHz) QSSPWM	ICD SAM	RD SAM	SR SAM
PS_2,PS_3	max	1.6	1.6	1.735	3.157
	min		1.4884	1.505	1.267
PS_6,PS_7	max	0.8	0.8	0.832	1.333
	min		0.769	0.769	0.9
PS_{10},PS_{11}	max	0.4	0.4079	0.407	1.333
	min		0.392	0.392	0.493
PS_{14},PS_{15}	max	0.2	0.2039	0.203	0.6
	min		0.1996	0.196	0.3
PS_1,PS_4, PS_5,PS_8, PS_9,PS_{12}, PS_{13},PS_{16}		.05			

random delay schemes swim around the QSPPWM switching angles, whereas the switching angles of the SRSAM modulation scheme are less than the switching angles of the QSPPWM scheme.

(v). The minimum and maximum switching frequency of the schemes attained is shown in Table 3. In QSSPWM scheme, the switching frequency is attained based on (2), whereas the other schemes switching frequency is based on the delay addition/advanced technique.

IV. PERFORMANCE MEASURES

The Performance evaluation of the proposed schemes is dignified through Weighted Total Harmonic Distortion (WTHD), IEC 1000-3-4 Regulation, THD, Harmonic Spread Factor (HSF) along with power density spectrum.

A. TOTAL HARMONIC DISTORTION (THD) AND WEIGHTED TOTAL HARMONIC DISTORTION (WTHD)

Significantly, WTHD and THD are the two primary indices to measure the worth of the PWM schemes incorporated in the conversion (DC-AC) process. However, WTHD is superior to THD especially for the non-sinusoidal converter output, because, it is calculated by using the weightage of individual harmonic orders.

The THD of the voltage is defined as

$$THD = \sqrt{\sum_{h=2,3,..} \left(\frac{V_{h,rms}}{V_{1,rms}}\right)^2} \tag{14}$$

and another expression of the THD in terms of peak values, i.e.

$$THD = \sqrt{\sum_{h=2,3,..} \left(\frac{V_h}{V_1}\right)^2} \tag{15}$$

The WTHD is defined as

$$WTHD = \frac{\sqrt{\sum_{h=2}^{\alpha} \left(\frac{V_h}{h}\right)^2}}{V_1} \tag{16}$$

B. HARMONIC SPREAD FACTOR (HSF) AND SPECTRUM ANALYSIS-POWER SPECTRUM DENSITY

The HSF is a precise assessment key of any waveform for analyzing its harmonic spreading effects. The HSF is defined as follows:

$$HSF = \sqrt{\frac{1}{N}\sum_{k=0}^{N}(H_k - H_0)^2} \tag{17}$$

$$H_0 = \frac{\sum_{j>1}^{N} H_j}{N-1} \tag{18}$$

where 'H_j' is the amplitude of j^{th} harmonics, 'H_0' is the average value of all 'N' harmonics.

The power spectral density of the signal describes the power present in the signal as a function of frequency. The common window functions are used to reveal the spectrum analysis. (i) Keiser window: this window will often reveal signals near the noise floor that other windows may unclear. This window is the default window in many spectrum analyzers. (ii) Hanning and Hamming: These are comparable; Hamming and Hanning window functions both have a sinusoidal profile. The dissimilarity between them is that the Hanning window touches zero at both ends, removing any incoherence. The Hamming window stops just afraid of zero, implication that the signal will still have a minor discontinuity. The Hanning window has been used in the power spectrum analysis tool for measuring the acoustic noise in induction motor drives controlled by a variety of PWM methods. The Hanning window has a shape analogous to that of half a cycle of a cosine wave. The subsequent equation defines the Hanning window.

$$w(n) = 0.5\left(1 - \cos\left(\frac{2\pi\, n}{N}\right)\right) \quad \text{for n} = 0, 1, 2, \ldots, \text{N} - 1 \tag{19}$$

where 'w' is the window value and 'N' is the length of the window.

TABLE 4. Performance comparison of proposed modulation schemes at modulation index=1.0.

Performance metrics	Modulation Schemes			
	QSPPWM	ICDSAM	RDSAM	SRSAM
H_1	147.9	147.9	147.7	**180.7**
%THD (Voltage)	14.5	14.52	14.55	**2.58**
%WTHD (Voltage)	1.54×10^{-4}	1.54×10^{-4}	2.5×10^{-4}	**5×10^{-4}**
HSF	1.4	1.57	1.57	**0.211**
%THD (Current)	4.60%	4.53%	4.53%	**1.27%**

TABLE 5. Fundamental voltage and % of THD of various modulation index.

Modulation index(m_a)	Fundamental Voltage(rms)	% of THD
1.0	127	2.5
0.95	121	2.84
0.88	113	5.52
0.84	107	6.78
0.74	95	10.81
0.41	52	24.21

TABLE 6. FPGA utilization summary.

Logic Utilization	Jsed	Jtilization
Number of Slices	214	4.5%
Number of Slice Flip Flops	192	2%
Number of 4 input LUTs	205	2.2%
Number of Bonded IOBs	18	7.7%
Number of MULT18X18SIOs	2	10%
Number of GCLKs	6	25%

TABLE 7. Simulation and experimental %THD comparison of existing and proposed schemes.

Results	Existing 31 Level scheme [57]		SRSAM based 31 level MLI (proposed work)	
	V_{THD}	I_{THD}	V_{THD}	I_{THD}
Simulation values	3.62	3.71	2.58	1.27
Experimental Values	3.71	3.71	1.00	1.00

TABLE 8. %THD (Voltage) comparison of existing and proposed scheme.

Scheme	Switching frequency	Number of levels attained	Type of the MLI	% THD (Voltage)
M. A. Sathik et al. 2022 [46]	5 kHz	9	single-stage nine-level (9L) switched-capacitor inverter, Multi carrier	13.1
Amani, M et al. 2022 [40]	1 kHz	9	self-balanced switched-capacitor multilevel inverter	4.49
V. Anand et al. 2022 [48]	5 kHz	13	Switched-Capacitor Multilevel Inverter With Single DC Source	9.741
C.Dhanamjayaku et al. 2019 [57]	1.6 kHz to 3 kHz	31	31-Level Asymmetrical Cascaded Multilevel Inverter	3.7
D. Prasad et al. 2021 [58]	2 kHz	31	31-Level Asymmetrical Inverter With Reduced Components	3.35
S. K. Gupta et al. 2018 [59]	2 kHz	31	31-Level Asymmetrical Multilevel Inverter Topology(Multicarrier)	3.95
SRSAM Scheme	maximum 3.167 kHz	31	Cascaded H Bridge (Asymmetrical Voltage Source, Four H Bridges,carrierless)	2.58

V. DISCUSSION ON SIMULATION RESULTS

In this section, measurement results with RL load under the above-proposed modulation schemes are presented. The performance measures are measured for R=1 Ω, L=100 mH. Fig. 9 shows the voltage harmonic profile of all modulation schemes up to the order of 500 with a modulation index of 1. Table 4 shows the performance comparison of proposed modulation schemes.

The following interpretation has been made when comparing all simulation results.

1. The fundamental voltage (H_1) is fabulously high in the Sine referencing schemes when compared with predecessor schemes. The difference between the SRSAM scheme with other schemes is almost 33 voltage.
2. The THD and WTHD of the voltage profile are also significant remarks and are better in the SRSAM scheme.
3. The WTHD is the parameter, which indicates the switching losses indirectly. Here, the WTHD is the same in all the first three schemes. But the SRSAM scheme is giving very little value.
4. When comparing the first three schemes, the Dominating Harmonics Orders (DHO) of all the methods are the same but the variations of amplitudes are less than 1% except for the 3^{rd}, 5^{th}, 7^{th}, and 11^{th} orders. The 3^{rd}-order harmonic amplitudes are in the range of 13% to 14% of its fundamental voltage. The 5^{th}-order harmonic amplitudes are in the range of 3.1% to 3.4% of its fundamental voltage. The 7^{th}-order harmonic amplitudes are in the range of 2.5% to 2.7% of its fundamental voltage. The 11^{th}-order

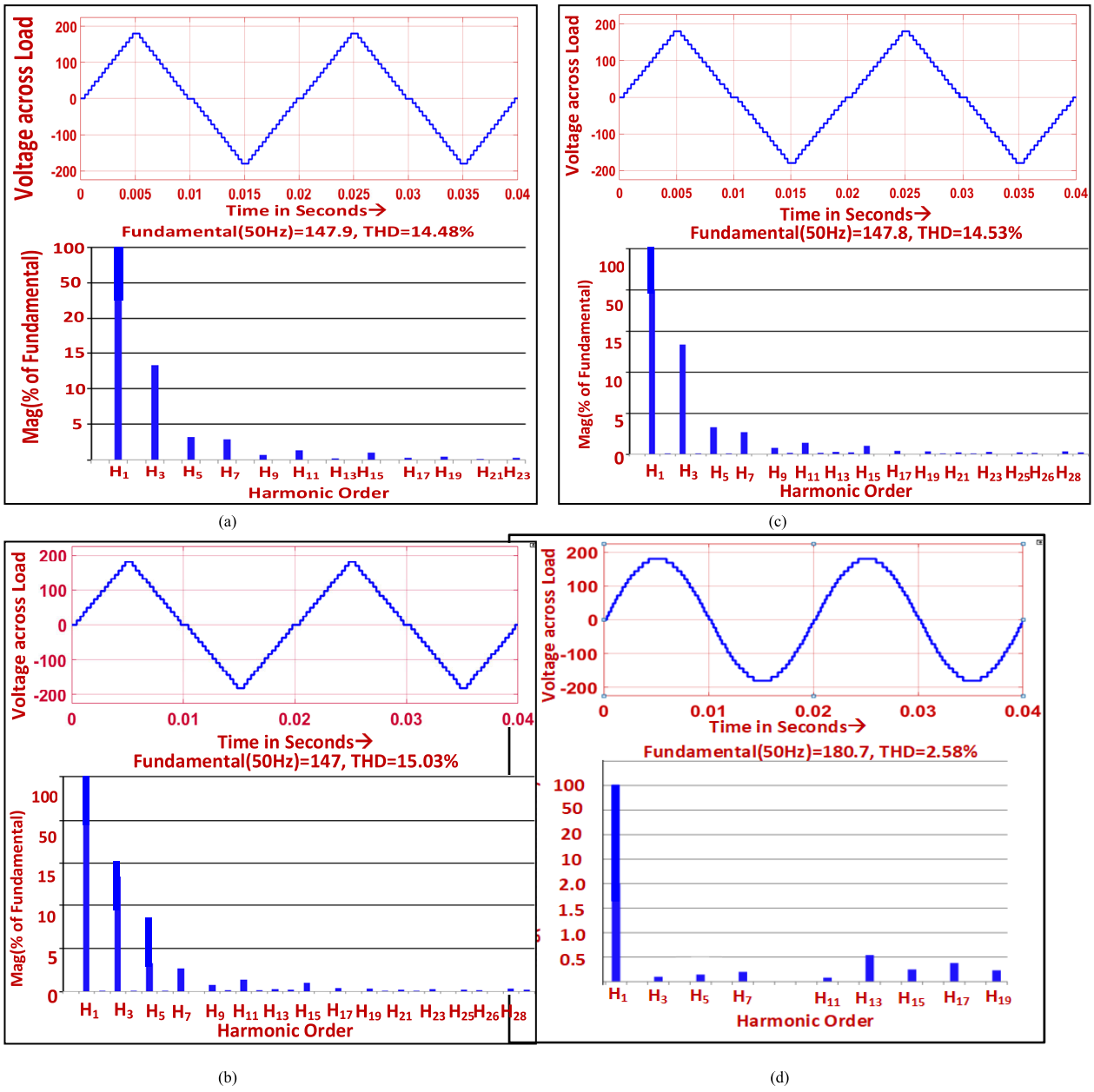
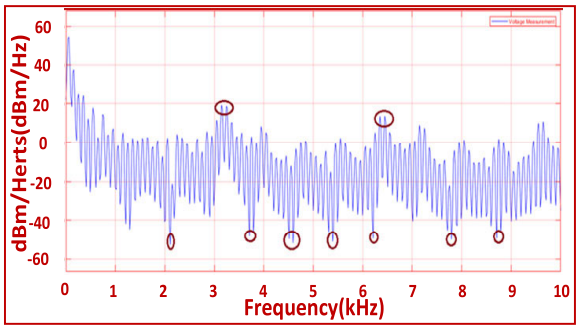


FIGURE 9. Voltage harmonic profile at $m_a = 1.0$ of (a). QSPPWM scheme (b). ICDSAM (c). RDSAM. (d) SRSAM.

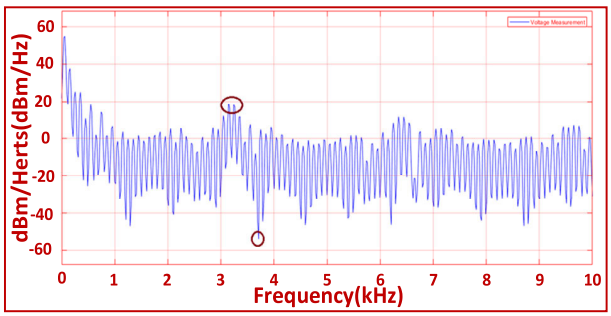
harmonic values are in the range of 1.4% to 1.6% of its fundamental. The remaining harmonics are less than 1 % of its fundamental values and the even-order harmonics are absent as expected.

5. When compared to other schemes, the SRSAM scheme is successful and dominates. All the harmonics are less than 1% of its fundamental. The harmonic order 13 provides 0.54% of the fundamental's value from the lower order harmonic band.
6. The THD of the current waveform is also less than 5% of the fundamental in all four schemes. But, the SRSAM scheme is giving an unbeatable performance in this aspect.
7. The HSF and PSD are performance-indicating indices of acoustic noise. The HSF of the SRSAM scheme is very low when compared with all predecessor schemes.

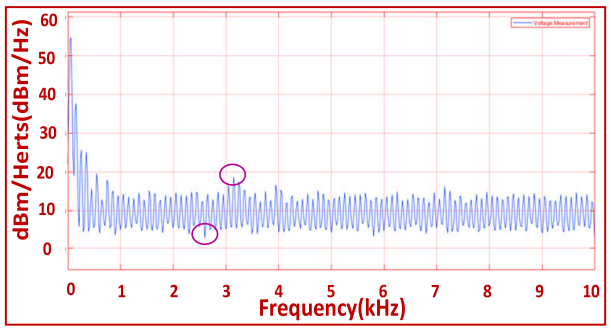
The PSD of the schemes is depicted in Fig. 10. The PSD of the QSPPWM switching, the angle scheme is drastically varying. It's swinging from 19 dBm/Hertz to −50 dBm/Hertz. Here, more frequency components touch their peak as well as lowest values, whereas the PSD of the ICDSAM scheme swings from the same 19 dBm/Hertz to −50 dBm/Herts. But only one frequency component reaches its peak and lowest values in the band of frequencies, which is marked with a circle. In the RDSAM scheme, the PSD swings from 18 dBm/Herts to −15 dBm/Hertz. From the



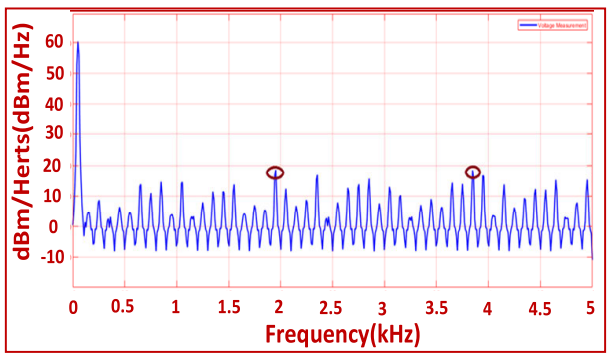
(a)



(b)



(c)



(d)

FIGURE 10. Power spectrum density of (a) QSPPWM switching angle scheme (b) ICDSAM (c) RDSAM and (d) SRSAM.

PSD point of view, the RDSAM scheme dominates the other two schemes. But when comparing all the above three

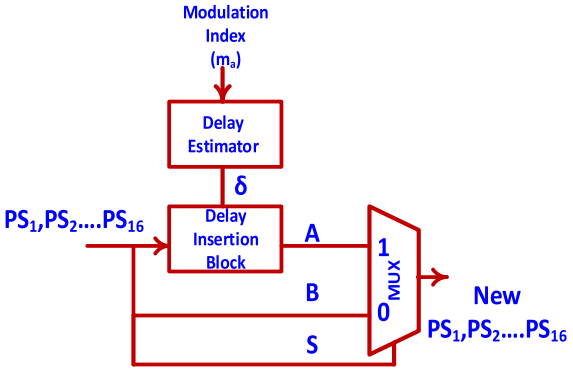


FIGURE 11. Duty cycle variation of the PWM in SRSAM scheme.

schemes with SRSAM switching scheme, it is triumph over the other three schemes. It's swinging from 18 dBm/Hertz to −8 dBm/Hertz.

At any PWM scheme, the duty cycle of the PWM can be varied to achieve the variable output voltage. Modulation index(m_a) is one of the control variables in the closed-loop control as well as open-loop control to vary the duty cycle. This research is focused on open-loop control with optimized switching angle techniques. Fig. 11 can adopt at the dynamic condition to get the variable output voltage at different m_a. The duty cycle of the PWM can be varied by using the delay insertion block and a MUX. The estimation of the delay derived from the m_a. The delay is inversely proportional to the modulation index.

$$A = \Delta PS_n(Delay\ inserted), \quad B = S = PS_n$$
$$New\ PS_n = A \times S + B \times \bar{S} \tag{20}$$

where n = 1, 2, 3 . . . 16, Δ −> delay.

Table 5 shows the RMS output voltage and THD for the various modulation indices for the SRSAM scheme. The research investigations are carried out when a sudden change in input voltages also. Each H-bridge input voltage is doubled for two cycles and bringing it back to the initial voltage for this analysis. Fig. 12.(a) shows the output voltage across the load when changing the input voltage. When the voltages are doubled, the achieved fundamental voltage (RMS) is 255.6V and the corresponding % of THD is 2.58%. When it comes down to the initial voltage, some glitches arise in each cycle which exhibits a fundamental voltage (RMS) is 166.7V and the corresponding % of THD is 25.36%. Which are unfavorable to any electrical systems. This problem has been solved by inserting the filter capacitor across the load (c=100 μF). Fig. 12 (b) shows the output voltage across the load after inserting the filter. This exhibits the fundamental voltage (RMS) is 130 volts and the corresponding % of THD is 1.56%.

VI. HARDWARE AND IMPLEMENTATION

The Experimental setup has been incorporated with a 10A auto-transformer along with a rectifiers section and FPGA

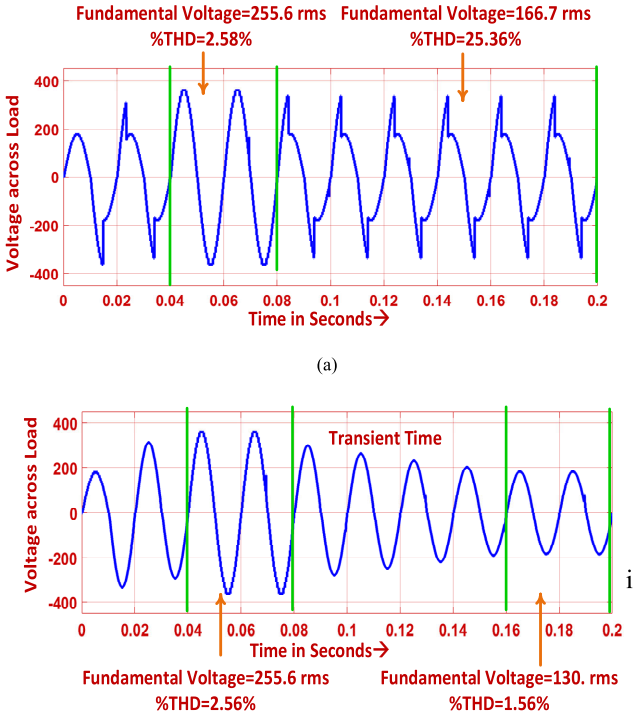


FIGURE 12. Voltage across load when a sudden change in input voltage (a). without Filter (b) with Filter (C=100μF).

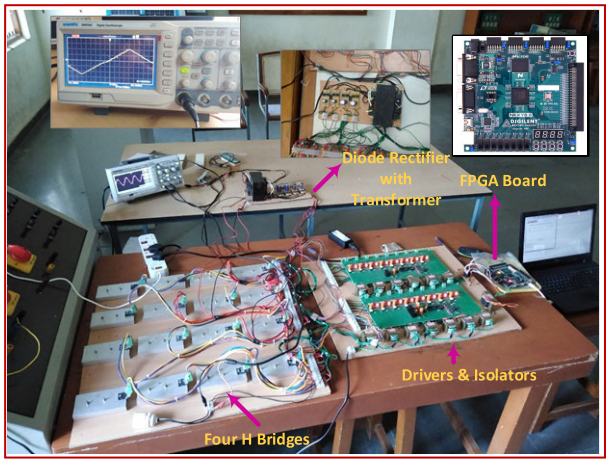


FIGURE 13. Experimental setup.

kit development board, a driver with an optocoupler circuit, and 4 H-bridges as shown in Fig. 13. Auto-transformer is used to step down 4 tap output voltage to the rectifiers. The ratio of the first tap is 5:1, the second tap is 10:1 and the third tap is 20:1 and the Final tap is 40: 1. These voltages are given to rectifiers and the output voltage of the rectifiers will be asymmetrical (12 V, 24 V, 48 V, and 96 V). These voltages are the input of the 31 levels of MLI H Bridges. Appendix. shows the rating of rectifier components. IGBT CT60AM-18F n-channel device is used as a switch in the experimental prototype of the MLI circuit. The maximum

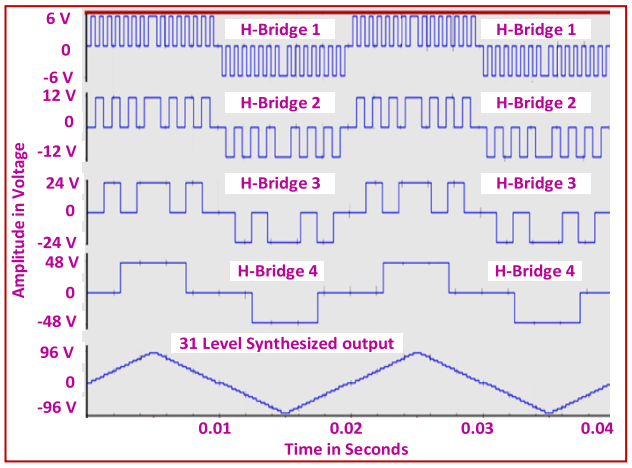


FIGURE 14. Synthesized voltages across each H-bridge and 31 level output.

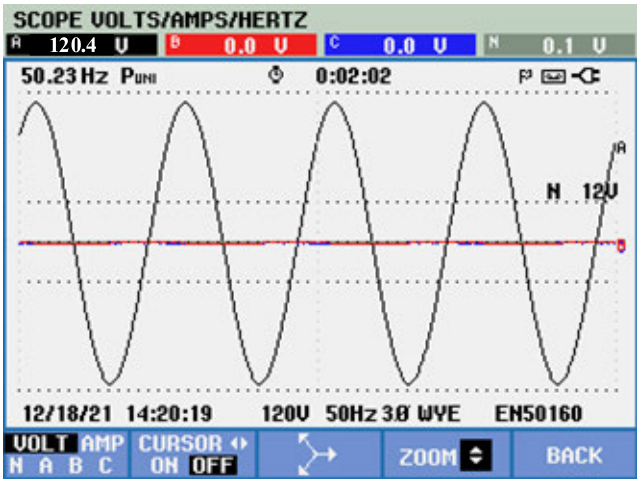


FIGURE 15. 31 level phase voltage profile of SRSAM scheme (m_a=1.0).

power dissipation (Pc) of IGBT is 180W. The maximum collector-emitter voltage is 900 V. MCT2E optocoupler is used to provide the isolation between the FPGA module and to MLI module. 16 heat sinks are provided to exhaust the heat generated from the IGBT devices. The pulses for 16 switches have been generated by using the FPGA device XC3S500E-320F device. The language VHDL is used to code for the PWM modulator. The development of the VHDL program incorporates the following modules.

(i). Clock divider module (ii). Deadtime insertion module (iii) delay insertion module and the (iv) top module.

The clock divider module is used to generate the derived clock of 50 Hz, 100 Hz, and 104.200 kHz clocks from the 50 MHz board clock oscillator. The 1.5 μ seconds have been inserted as a dead time to avoid shoot-through faults on the same leg switches. The delay insertion module has been used to insert the delay (successive delay or the advancing delay). The ICDSAM and RDSAM schemes are utilizing the successive delay and the SRSAM scheme uses by delay advancing concept. Fig. 3. shows the simulation results

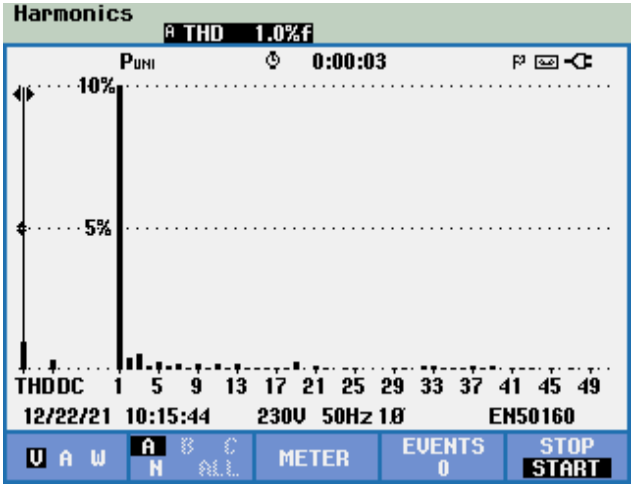


FIGURE 16. 31 level harmonic profile of SRSAM scheme at m_a=1.0.

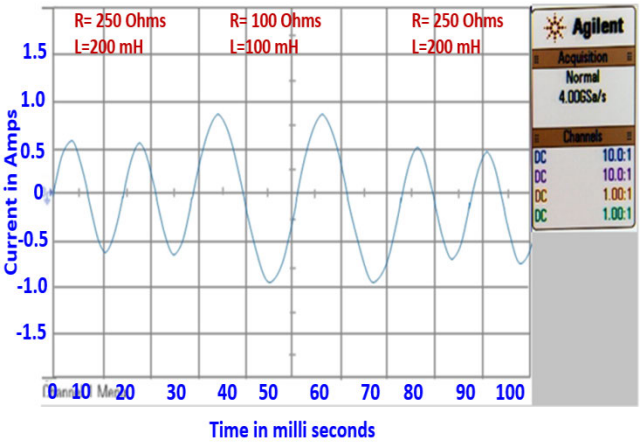


FIGURE 17. Current waveform when a sudden change in load (R=250 ohms, L=200 mH and R=100 ohms, L=100 mH).

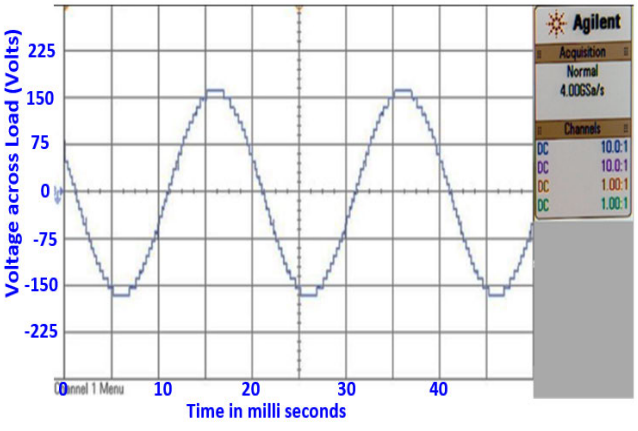


FIGURE 18. Phase voltage profile of SRSAM scheme at (m_a=0.9, R=100 ohms, L=100 mH)).

of PWM generation using Modelsim software for FPGA devices (QSPPWM). The delay insertion module is used for

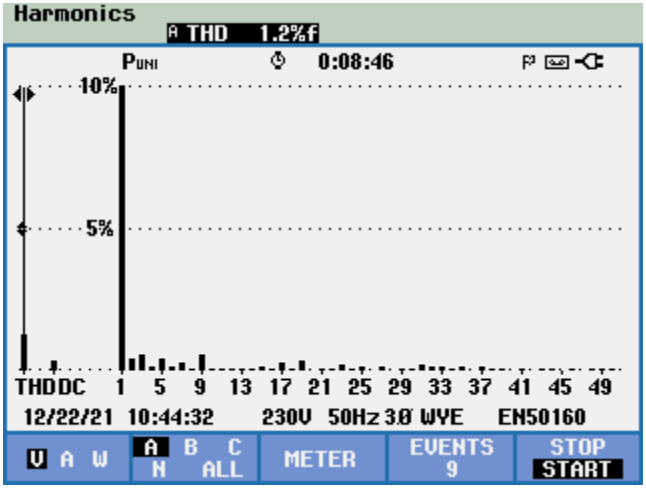


FIGURE 19. Harmonic profile of SRSAM scheme at (m_a=0.9 and R=100 ohms, L=100 mH).

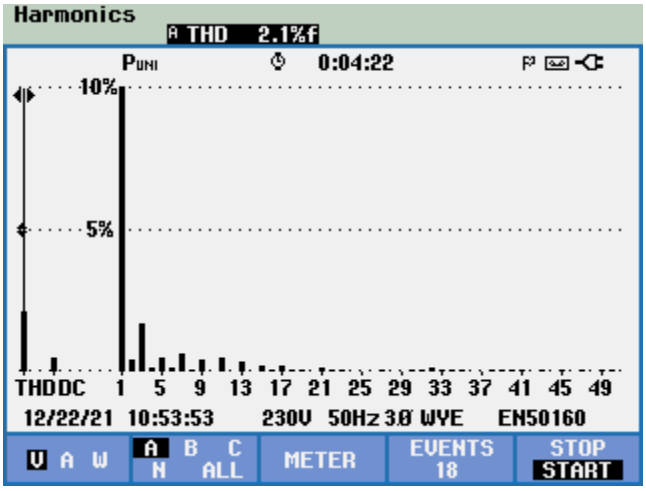


FIGURE 20. Harmonic profile of SRSAM scheme at (m_a=0.8 and R=100 ohms, L=100 mH).

ICDSAM, RDSAM, and SRPWM. The delay between α (QSPPWM) and α (ICDSAM, RDSAM, SRSAM) is calculated and added/advanced based on the scheme delay value.

The top module contains the simple code of equations (3) to (12) by using data flow modeling in VHDL. The entire program is synthesized by using Xilinx Project navigator tool 14.5 and downloaded by using adept downloading software provided by Agilent. Xilinx project navigator tool incorporated with the synthesis, static timing analysis place&root, and power estimator functions. The utilization summary of the FPGA device is shown in Table 6. The beautification of the LEA algorithm with the SRSAM is taking only 4.5% of available slices. The selected device contains only 500-kilo gates. This is one of the least gate availability devices when compared with the advanced FPGAs. The bonded input and output pins are 18, accounting for the 16 IGBT gate pins, one board clock, and a reset. The Timing Analyzer is used to verify the timing requirements of the critical path. There

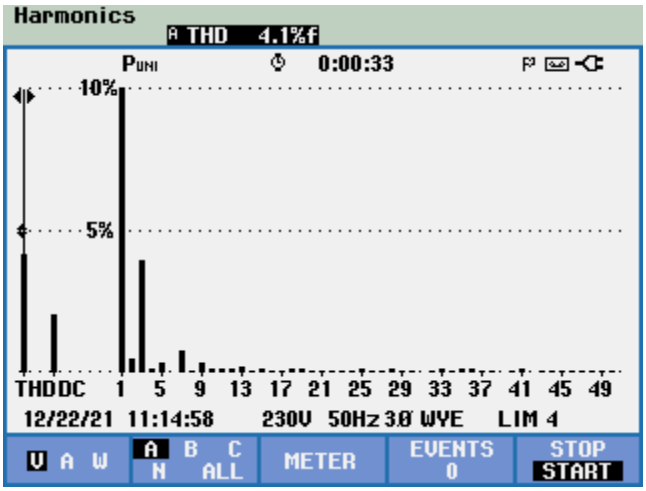


FIGURE 21. Harmonic profile of SRSAM scheme at (m_a=0.6 and R=100 ohms, L=100 mH).

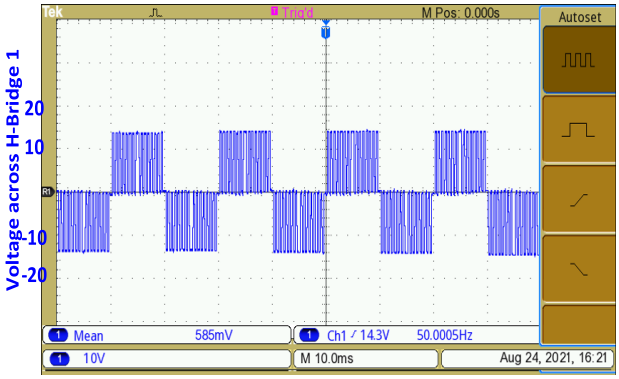


FIGURE 22. Voltage across H Bridge 1 of SRSAM scheme at (m_a=1.0 and R=100 ohms, L=100 mH).

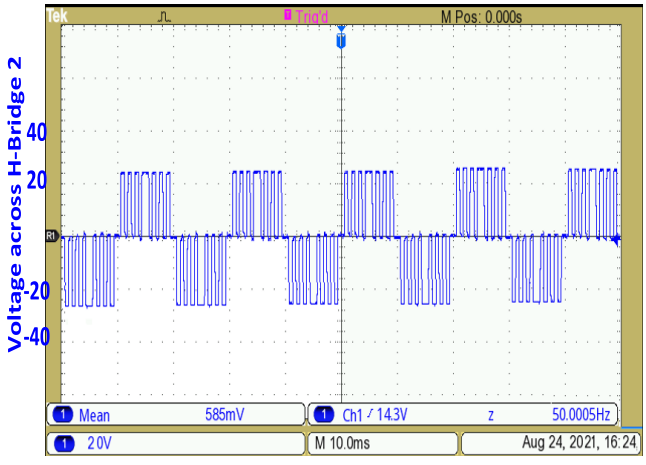


FIGURE 23. Voltage across H Bridge 2 of SRSAM scheme at (m_a=1.0 and R=100 ohms, L=100 mH).

are four timing paths are available. (i). input pin to output pin, (ii) input pin to Flip flop, (iii) Flip flop to Flip flop, and (iv) Flip flop to the output pin. This entire design requires

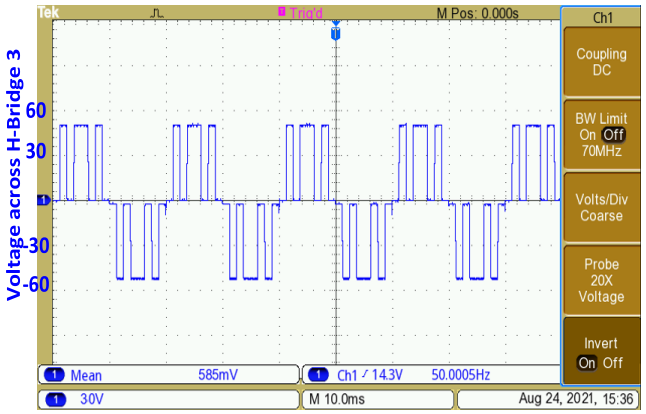


FIGURE 24. Voltage across H Bridge 3of SRSAM scheme at (m_a=1.0 and R=100 ohms, L=100 mH).

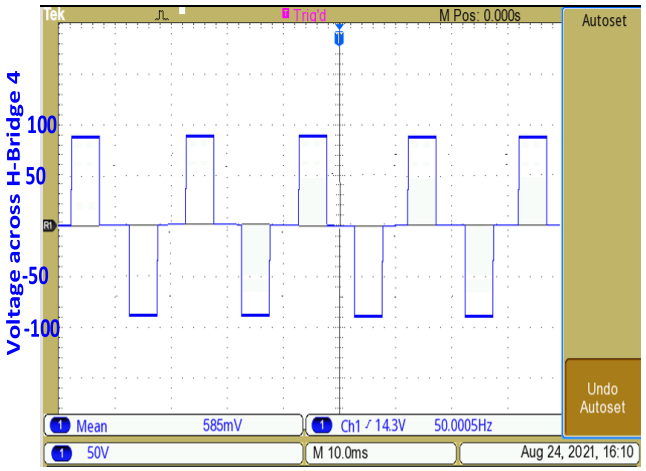


FIGURE 25. Voltage across H Bridge 4 of SRSAM scheme at (m_a=1.0 and R=100 ohms, L=100 mH).

a processing delay of a maximum of 10 ns. This means the entire design can run up to the speed of 100 MHz. The power utilization of the FPGA device is 112 mW, which includes static and dynamic power dissipation. The VHDL-based test bench is developed for verifying the VHDL MLI design. The synthesized output and the corresponding output voltage of each H-bridges are also shown in Fig. 14. Fig. 15. shows the voltage across the RL load in the MLI and Fig 16 shows the voltage harmonic profile across the load. Fig 17 shows the current harmonic profile when sudden change in non linear loading condition at m_a = 0.9. In Fig 18. shows the voltage waveform at m_a = 0.9. Fig 19, Fig 20 and Fig 21 shows the harmonic spectrum at m_a = 0.9, 0.8 and 0.6 respectively when R=100 ohms and L=100 mH. Fig 22, Fig 23, Fig 24 and Fig 25 shows voltage across each H Bridge respectively in the hardware for the m_a = 1.0. Fig 26 shows the harmonic spectrum of proposed SRSAM scheme with existing scheme [57] along with its comparison chart. From the view of the harmonic profile, the following observations are made

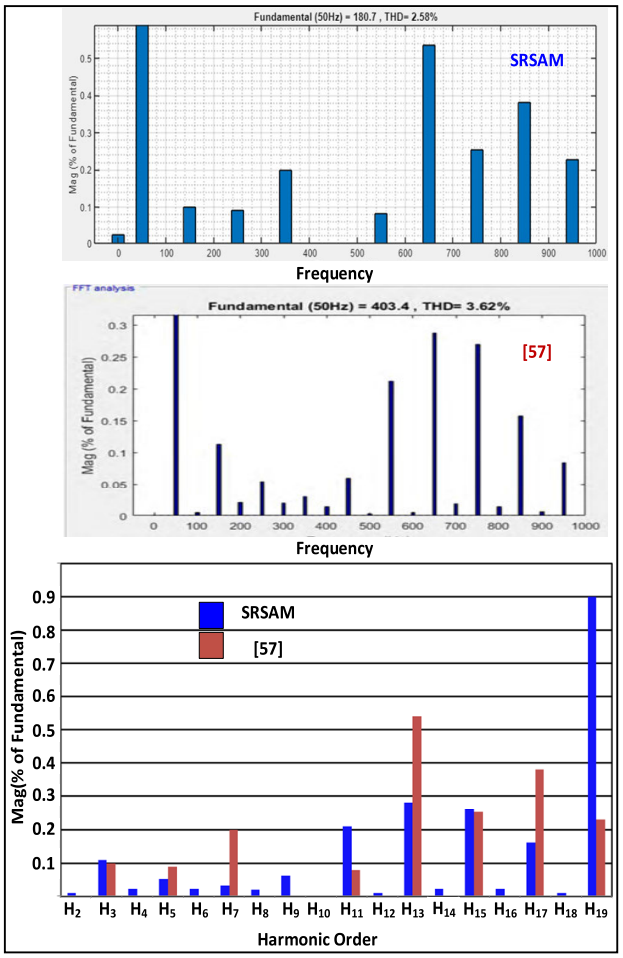


FIGURE 26. Voltage harmonic spectrum comparison of proposed scheme with existing scheme [57].

1. Existing scheme exhibits the tiny amount of even order harmonics, whereas these are disappeared in SRSAM scheme.
2. 3rd and 15th order harmonics are tiny more in proposed scheme when comparing existing scheme. As like these, the harmonic order 11th and 19th order harmonics also more in proposed scheme.
3. 5th,7th,9th 13th,17th order harmonics are generating more in existing scheme [57] when comparing with the proposed scheme.
4. Interestingly both the schemes generating problematic lower order harmonics are less than 1% only.
5. Fortunately, the even order harmonics are disappear in proposed scheme, where these are appear in existing scheme with insignificant magnitude.

VII. CONCLUSION

In this work authors successfully developed and verified an algorithm to establish a 31-level ac output voltage from four DC sources and four H bridges in a peculiar asymmetrical operation. A tailor-made PWM strategy and its simple implementation logic have also been suggested. The system has been tested both in simulation and also in the developed laboratory prototype. Further, the extended version of QSPPWM developed and brought out three novel modulation schemes for improving performance. As expected, the excellence of the output voltage profile was upgraded by adding the delay elements in the digital PWM (QSPPWM) technique and enveloping with a pure sine wave (SRSAM), then the current THD has reduced to less than 1% and voltage THD is reduced to 1.00% as shown in Table 7. Table 8 shows the %THD (Voltage) comparison of proposed and existing schemes. The SRSAM scheme can be adoptable to the switched capacitor MLIs also, in such a way that, the charging and discharging time of the capacitors will be decided by the base frequency (f_{HB1}, f_{HB2}, f_{HB3}, and f_{HB4}) and duty cycle of the QSSPWM.

This innovative PWM technique utilizes the least FPGA resources; increases the processing speed with the least power dissipation in the FPGA device. From this, it can be confirmed that the proposed scheme successfully achieved the objectives.

APPENDIX
RATING OF RECTIFIER COMPONENTS

Component	Number	Ratings
Diode	IN543M1X	100 V , 5 Amps
Capacitor	J4APET	63v,2200 µF,85 c
Capacitor	K1APET	25v,2200 µF,85 c

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