TOPICAL REVIEW

SiGe and CMOS Technology for State-of-the-Art Millimeter-Wave Transceivers

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ABSTRACT Innovation and evolution are paramount where the demand for wideband, data-intensive connectivity is ever-increasing, and the only constant is change. Standards that define the operation of next-generation mobile networks are moving away from the traditional radio frequency (RF) spectrum and into millimeter-wave (mm-wave) bands. The physical layer (PHY) for IEEE 802.11ad Wi-Fi and 802.11ay WLANs dictates operation in the unlicensed 60 GHz band. 5G New Radio (NR) applications utilize selected bands from 26 to 39 GHz. Additionally, newly developing Fourth Industrial Revolution (4IR) applications depend on 5G NR as an enabling technology. Satellite communications and wireless backhaul will occur in E-band between 70–86 GHz. Increasing demands from the market cause designers to push boundaries, and the development of standards guide technological advances. Perhaps the most substantial improvements are observed in integrated circuit technology. This article details the major Si processes, namely Complementary Metal Oxide Semiconductor (CMOS) and SiGe Bipolar CMOS (BiCMOS), and their foray into the wireless transceiver space traditionally dominated by GaAs. CMOS and BiCMOS have become popular in many communities because of their low fabrication cost and excellent digital integration capabilities. RF performance has matured to where Si is a serious competitor for tried-and-tested III-V technologies. Some extreme environments and sophisticated applications still favor GaAs and GaN, however. GaAs, for example, can yield unparalleled output power and excellent noise figure performance, albeit at a higher cost and increased design and manufacturing complexity due to the multi-chip nature of these circuits.

INDEX TERMS 5G new radio (NR), broadband communication, cellular vehicle-to-everything (C-V2X), CMOS, fourth industrial revolution (4IR), Internet of Things (IoT), millimeter-wave, SiGe BiCMOS.

I. INTRODUCTION

For the last few decades, the RF performance of semiconductor technologies has improved substantially, with CMOS and SiGe BiCMOS [1], [2] transistors able to reach increasingly higher frequencies. This means that transistors can be used to implement complex integrated circuits targeted at the higher microwave and millimeter-wave bands. Digital signal processing, data converters, clock generation, and other digital circuits implemented in silicon have improved

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in performance tremendously, and this serves as an excellent motivator for further funding and development. Performance characteristics that are of interest in the digital domain, such as power consumption and computational speed, also tend to improve as technology scales. Silicon system-on-chip (SoC) technology has been massively influenced by improvements in RF performance, which have subsequently led to numerous single-chip solutions for complex transceiver chains. A significant portion of the microwave monolithic integrated circuits (MMIC) market is occupied by automotive radar transceivers. Wideband silicon MMICs are more commonplace than they have ever been. Large and complex ICs can

be simplified since SoC integration relaxes the constraints on interconnect and reduces power consumption.

This paper is organized as follows. Section II highlights notable mm-wave spectrum allocations for the U.S. and other countries. Section III discusses important application-specific requirements imposed on semiconductor technology. Section IV notes some of the main points of comparison of CMOS and SiGe BiCMOS processes. Sections V through IX each summarize a handful of circuit implementations in the literature, ranging from passive components to integrated transceivers. Each of these sections identifies challenges with mm-wave implementation of circuit blocks and highlights design trends. Note that the figures displayed in this article are updated from the author's prior work [3], [4], [5].

II. SPECTRUM ALLOCATION AND REGULATORY CHALLENGES

Regulatory challenges with spectrum allocation, especially in the microwave and mm-wave bands above 6 GHz to about 100 GHz, have hindered the inevitable mainstream adoption of mm-wave operation, despite the numerous solutions it offers to the problems of current-generation systems [6]. The first desirable characteristic of mm-wave propagation is the increased attenuation that results from oxygen absorption, which one would assume is detrimental to its practicality. This roughly scales with frequency, but a few points of interest exist across the spectrum. Most notably, oxygen absorption peaks at 60 GHz and attenuation reaches about 20 dB/km at sea level [7]. A shorter propagation distance encourages frequency reuse in smaller sectors; this is utilized in pico- and femtocell architectures in the new generation of mobile networks [8], [9], [10]. The Federal Communications Commission (FCC) has published allocations for a number of mm-wave frequency bands. Starting in 2016, Upper Microwave Flexible Service (UMFUS) rules were adopted in preparation for 5G spectrum requirements. Some notable allocations are briefly summarized here [11]:

- The 28 GHz band contains numerous allocations between 24.45 and 31.8 GHz. Example applications include fixed and mobile satellite earth-to-space links, radio navigation, and space research.
- The 37 GHz band between 37 and 38.6 GHz contains a contiguous, unlicensed 1 GHz sector between 37.6 and 38.6 GHz. The FCC, fortunately, realized the importance of contiguous spectrum as bidders are often subject to high post-auction costs to assemble the required bandwidth.
- The 39 GHz band between 38.6 and 40 GHz is a good candidate for wireless backhaul, with a 1.4 GHz contiguous block. Currently, licenses are provided primarily for scattered 50 MHz blocks. The original intent for these blocks was 100 MHz bandwidth, so there is a possibility of a regulatory update in this regard. The rest of the band,

between 39.5 and 40 GHz, is licensed for mobile and fixed-satellite services.
- The V-band contains two 7 GHz areas of contiguous spectrum, 57-64 GHz and 64-71 GHz, and due to the propagation properties in this band, it is excellent for short-range unlicensed systems. Several lower V-band frequencies in the 40-50 GHz range are mostly allocated for radio astronomy and a number of satellite applications. The IEEE 802.11ad WiGig specification, the successor to 802.11ax Wi-Fi, stipulates usage of the V-band region.
- The E-band similarly contains two 5 GHz blocks, 71-76 GHz and 81-86 GHz. These bands are licensed informally, and they are suitable for backhaul infrastructure with smaller antennas reaching a couple of kilometers at most. Amid this, the 77 GHz automotive radar bands [12], [13]. Long-range radars operate between 76 and 77 GHz, while their shorter-range counterparts operate between 77 and 81 GHz.
- The W-band between 92 and 95 GHz region consists of 3 GHz bandwidth, suitable primarily for shorter-range applications such as mm-wave imagers and some radio astronomy systems [14]. Some automotive radars also operate in this band, typically around 94 GHz.

It is also informative to consider spectrum allocations throughout the rest of the world. China designated usage of the 59-64 GHz band for short-range wireless links in 2006 [15]. Furthermore, the 40.5-42.3 GHz and 48.4-50.2 GHz bands targeted point-to-point access systems. The IEEE 802.11aj standard describes mobile point-to-point networks operating in the 42.3-47 GHz and 47.2-48.4 GHz bands.

Three mobile operators in South Korea acquired portions of the 28 GHz band for mm-wave 5G via auctioning in 2018 [6]. 5G services were launched later that year, and local regulators are negotiating to extend the bandwidth to 3 GHz (up from 1 GHz), so that the coverage will be from 26.5 to 29.5 GHz. Japan was another early player in the 5G space and quickly allocated the 28 GHz band accordingly. Japan also assigned the 54.25-59 GHz band for licensed usage and the 59-66 GHz band for unlicensed operation.

The International Telecommunications Union (ITU) allocated numerous bands for fixed wireless access, 5G backhaul, and newer mobile communications systems. The 55.78-66 GHz, 71-86 GHz, 92-100 GHz bands are recommended globally for these types of applications. Moreover, the ITU also describes the 64-66 GHz band as suitable for mobile services.

The Canadian government permits unlicensed utilization of the 59-64 GHz band, primarily for low-power devices. Australia has also allocated the 59.4-62.9 GHz band for unlicensed devices and systems. Throughout Europe, multiple V-band spectrum assignments have occurred. The 59-66 GHz band is broadly allocated for mobile services, and the 58.2-59 GHz and 64-65 GHz bands are for radio

astronomy and remote sensing. Moreover, the 59-62 GHz bands are designated for radio local area networks (RLANs), and the 62-64 GHz bands for road transportation informatics (such as outlined by the CAR 2 CAR Communications Consortium). Some mobile network operations are also planned in the upper V-band spectrum.

The Telecommunications Regulatory Authority (TRA) in the United Arab Emirates (UAE) has a spectrum assigned for 5G NR in the 28 and 28 GHz bands. The Saudi Arabian Communications and Information Technology Commission (CITC) allocated the 24-28 GHz and 37-44 GHz bands for their 5G deployments.

III. TYPICAL MM-WAVE SEMICONDUCTOR REQUIREMENTS

The performance requirements imposed by the wireless system on the transceiver blocks – such as output power, linearity, and noise figure profoundly impact the performance requirements of semiconductor devices.

A. MOBILE BACKHAUL

The wide separation between the upper and lower E-band blocks facilitates and, in fact, encourages frequency division duplexing (FDD). Currently, most E-band transceivers leverage GaAs or GaN devices since ranges exceeding 2 km are currently unrealistic for CMOS and SiGe BiCMOS transistors due to their reduced output power and comparably worse linearity performance. On the other hand, V-band backhaul applications rely on significantly lower link distances since they deliberately use the 60 GHz band [16].

B. SMALL-CELL MOBILE BACKHAUL

Multi-hop and close-proximity street-to-street scenarios, are some examples of small-cell deployments, with links ranging from 100 to 500 m [17]. This reduction in link distance reduces the output power requirement generously, and E-band amplifiers would need to produce about 10 dBm, well within reach for just about any mm-wave PA MMIC. The system-level noise figure and phase noise specifications are generally similar to what one would expect in large-cell backhaul deployments. Reduced link distances once again encourage liberal frequency reuse, which suits V-band propagation characteristics. SiGe BiCMOS and CMOS are good options because of the large number of short-range links. Bill of Materials (BOM) cost is a priority in such systems, so direct integration with digital radios is highly beneficial.

C. FIXED BROADBAND

Wireless-to-the-home, a competitor for current fiber-to-the-home solutions, will utilize the 60 GHz band for its backhaul network. The operation of these systems is outlined in the IEEE 802.11ad standard and the subsequent 802.11ay standard [18], [19], [20]. Link distances in these types of systems rarely exceed 3 km, which is within the realm of SiGe BiCMOS and RF CMOS capability, again with the added benefit of reduced BOM cost. PA output power requirements

are relaxed, and the design effort can be directed towards improving linearity so that higher-order modulations required by the specification (which can exceed QAM-1024) can be supported. The demands on receiver sensitivity are also relaxed as a result.

IV. CMOS AND BiCMOS TECHNOLOGY BRIEF

The advancement of SiGe and RF CMOS devices has substantially improved the frequency capability of Si substrates. InP devices are often encountered above 100 GHz, but other technologies are certainly catching up. For example, LNAs with 10 dB gain in D-band (135-170 GHz) have been reported in 28 nm FDSOI CMOS [23]. However, InP devices (both HBTs and HEMTs) have been used in PA designs above 200 GHz, some with output power exceeding 20 dBm [24]. These devices have also featured in 300 GHz "beyond-5G" transceiver front ends [25].

The performance of GaN-based circuits has also steadily improved in recent years. PAs operating at 40 GHz have been reported with output power exceeding 40 dBm, all the way up to 205 GHz with $P_{out} = 18$ dBm [26]. Kim et al. reports a 5G integrated front-end operating at 39 GHz using Qorvo's $0.15 \mu m$ GaN process [27]. The transmit path yields 26 dBm average output power and -30 dBc adjacent channel power ratio (ACPR) with QAM-64 in OFDM. The receive path achieves 16 dB gain with noise figure of 4 dB.

GaN devices also offer excellent noise performance, making them an excellent choice for sensitive receivers. GaAs devices achieve comparable noise figure at higher frequencies. GaAs LNAs using metamorphic HEMT technology (mHEMT) have been reported with average noise figures less than 2 dB at 90 GHz and higher [21].

A. SUBSTRATE MATERIALS

The technology discussion begins with a brief overview of substrate materials. For the sake of completeness, III-V materials will also be included. Table 1 summarizes the characteristics of common semiconductor materials [22], [23].

B. RF PERFORMANCE AND RELIABILITY

Semiconductor foundries report the RF performance of their process technologies at the device level [24]. This is done via de-embedding parasitics, and procedures retain only the contact pads in their transistor models. This is especially true for MOS transistors, which are notoriously difficult to model to begin with [25]. Conversely, the performance of bipolar transistors is reasonably agnostic to the accuracy of the de-embedding process, which simplifies the generation and maintenance of process design kits (PDKs). Scaled CMOS processes, which generally have excellent input capacitance characteristics, can, unfortunately, experience notable degradation of f_T from interconnect parasitics [26]. Naturally, comparing the two technologies should take into account the performance impairments that result from the metal layer stack since it is heavily influenced by the process back-end-of-line (BEOL). In reality, the 45 nm and 28 nm CMOS

TABLE 1. Common semiconductor material characteristics.

Material	Bandgap (eV)	Electron mobility (cm²/V·s)	Dielectric constant (typical)	Typical frequency of operation (GHz)	Noise figure (dB)	Gain (dB)	Power handling
Si	1.12	1500	11.9	≤40	3-6	10-15	Low
SiGe	0.67-1.12	1900-5000	16-17	≤200	1-3		Low
SiC	2.3-3.3	800-2000	9.7-10.1	≤100	2-4		Moderate
GaAs	1.42	8000-9000	12.8-13.1	≤250	1-3	10-20	Moderate
GaN	3.4-3.5	900-1500	N/A[1]	≤300	0.5-2		High
InP	1.35	5000-12000	12.4	≤500	2-4		Low

nodes are where the RF performance peaks. Smaller devices are increasingly affected by parasitic gate capacitance and resistance, both of which degrade RF performance significantly, making further scaling pointless for RF performance. Instead, CMOS technology leverages process advances such as fully depleted silicon-on-insulator (FDSOI) and SoI fabrication to improve RF performance. The fabrication of FD-SoI is cheaper than e.g., FinFETs, and E-band PAs have been reported with good performance.

Bipolar transistors naturally offer higher transconductance and better $1/f$ noise. Bipolar devices also have higher breakdown voltages and better reliability than comparable MOS transistors [27]. Both of these characteristics are advantageous to PA design. Hot carrier injection is a detriment to MOS thermal reliability, in which the transconductance g_m and threshold voltage V_T gradually degrade at large levels of V_{DS} [28]. The lifetime and reliability can be improved by lengthening the gate pad (increased parasitics) or lowering the supply voltage (reduced dynamic range and output power). The consequence is that BiCMOS devices can generally provide higher output power and slightly better efficiency, seeing that these depend on reducing loss, increasing breakdown voltage, and increasing the voltage and current swing limits.

C. PASSIVES

Standard BiCMOS technologies offer optimized BEOL, which is not readily available in CMOS. As mentioned previously, the BEOL strongly affects passive device performance and Q-factor. In general, BiCMOS passives offer better RF performance. Passive devices are discussed in greater detail in Section V.

D. MANUFACTURING AND FABRICATION COST

The standard BiCMOS process flow is built on previous-generation CMOS nodes [29]. This means that older (and cheaper) PDKs can be used, lowering non-recurring engineering (NRE) costs. Wafer production is also cheaper since older and time-tested processes can be used and variations tend to be fewer. As such, BiCMOS technologies benefit

from reduced production volumes, although this is a function of the finalized die size. Newer CMOS processes achieve much better chip density so that more digital circuitry can be fit into the same chip area, which can be considered as a cost advantage on its own. However, it is still crucial to evaluate RF performance in determining whether the tradeoff is positive.

E. COMPARISON SUMMARY

Table 2 summarizes the comparisons of the previous few sections qualitatively. This table originates from prior work conducted by this authoring team [3], and it is based on several key performance specifications:

- Modulation up to QAM-256. The need to support higher-order QAM, sometimes up to QAM-1024, will become commonplace [30].
- Channel spacing of at least 50 MHz, so that applications such as 60 GHz small-cell scenarios can be readily implemented.
- Bit rates of at least 1 Gb/s, while 10 Gb/s is preferred. Future systems will likely require bit rates exceeding 10 Gb/s.
- Transceivers are implemented as single-chip designs, readily available in multiple processes from multiple vendors.

V. PASSIVE COMPONENTS AND CIRCUITS

Passive elements constitute a large part of mm-wave circuits. Their performance is also highly dependent on the process technology, substrate, and BEOL. Some challenges and solutions for Si processes are discussed in this section.

A. CHALLENGES WITH GROUND PLANES AND TRANSMISSION LINES IN SILICON

Realizing true ground references when using silicon substrates is a challenging procedure since through-wafer connections are not an option [31]. III-V technologies often make use of off-chip ground planes, and these can be used as reference planes for any on-chip component. This is a typical approach in multi-MMIC designs, where a single

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[1]GaN is typically only used in the epitaxial layers grown on top of a SiC substrate.

TABLE 2. Comparison of millimeter-wave technology options.

Technology	BOM Cost	Integration	RF Performance (qualitative)	RF Performance (quantitative)[2]	Target products
GaAs pHEMT / mHEMT	High RF modules requires multi-chip approach	Poor	Excellent, preferred for many RF applications	P_{sat} = 30-38 dBm NF = 0.5-3.5 dB G_P = 18-24 dB f_T / f_{max} = 200-500 / 380-1000 GHz V_{Br} = 2-4 V	PA, LNA, complete RF modules
GaN HEMT	Relatively new technology, unknown	Poor	Higher P_{sct} but worse linearity vs. GaAs	P_{sat} = 35-45 dBm NF = 0.5-3.5 dB G_P = 15-30 dB f_T / f_{max} = 330 / 550 GHz V_{Br} = 17-40 V	Future PA, LNA
InP pHEMT	Generally more than GaAs competitors	Poor, RF circuits are highly complex	Better f_T, f_{max} versus GaAs	P_{sat} = 25-30 dBm NF = 3-6 dB G_P = 15-30 dB f_T / f_{max} = 300-700 GHz V_{Br} = 4-6 V	Defense systems
SiGe	Lower, function of production volume, comparable cost for small-volume production	Good, but not suited for A/D and baseband integration within SoCs	High f_T, f_{max}, decent phase noise performance & low-loss BEOL[3] layer stackup	P_{sat} = 22-30 dBm NF = 4-6 dB G_P = 20-25 dB f_T / f_{max} = 300-500 GHz V_{Br} = 1.6-4 V	Medium to high-power mm-wave transceivers ICs
SiGe BiCMOS	Lower than competitors, but depending on production volume, SoCs result in good yield	Excellent integration with a wide range of logic, good power consumption for A/D and D/A converters	High f_T, f_{max}, decent phase noise performance & low-loss BEOL layer stackup		Medium to high-power mm-wave transceivers, can readily integrate with PLLs and A/D converters
RF CMOS	Mm-wave expansion of digital CMOS, therefore needing advanced lithography and costly NRE	Facilitates high-density digital circuitry integrated with RF, SoC integration a possibility with both digital baseband and memory blocks	Transistor f_T, f_{max} can easily reach mm-wave operation, requires miniaturized process nodes with very low breakdown voltages, and is therefore capable of lower power and efficiency compared to SiGe BiCMOS	P_{sat} = 20-25 dBm NF = 3-7 dB G_P = 15-20 dB f_T / f_{max} = 300-400 / 350-500 GHz V_{Br} = 2-3 V	Transceivers with A/D, PLL, and amplifier blocks with digital control possible, well suited for lower-performance applications
CMOS FDSOI	Lowest supply voltage and power consumption	Can integrate with high-density mixed-signal SoCs, relatively low power requirement for crossing chip boundaries	Substrate engineering can substantially improve RF performance, high f_T, f_{max} as well as good isolation and linearity		Very high-speed mixed-signal blocks (e.g., SerDes)

metallization layer connects all ground nodes in the system. On the contrary, silicon ground planes have to be predefined with on-chip metal layers and implemented deliberately. The main issue here is that metal layers are thin, and often only the top two layers are slightly thicker, so there is severe area constraints. Another issue is that bonding on-chip and off-chip grounds is also fairly complicated, adding to the production time and quickly driving up module costs.

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[2]Tabulated values are indicative of typical measured circuit-level performance from literature [3].

[3]Back End-Of-Line.

Additional parasitics arise from these bondwire connections, while the thin metal layers also introduce higher parasitics, making it difficult to isolate ground planes properly.

III-V technologies generally make use of semi-insulating substrates, which have much lower parasitic capacitance and, as a result, yield thicker 50Ω signal traces that can carry larger current signals. Additionally, low inductance substrate vias connect the chip ground to the package. This is a favorable grounding strategy. Silicon MMICs use thin dielectric layers internally to split signal and ground layers, significantly increasing parasitic capacitance. Furthermore, 50Ω signal traces are narrower, around 6μm for a 4μm thick separation, also impacting current carrying capability [31]. Typical transmission lines are much lossier than those found GaAs MMICs, constraining many blocks that rely on transmission line structures (such as matching networks, filters and power combiners). In fact, the area efficiency of silicon power combiners quickly hits diminishing returns as the number of branches is increased [32].

The achievable Q-factor is also inhibited as a result of the close spacing between signal and ground layers since capacitive coupling is larger.

B. RLC CIRCUITS

Mm-wave circuits rely extensively on passive components. In fact, the passive components in typical circuits often outnumber active ones by order of magnitude and a high premium is placed on their performance. Modern Si processes offer good polysilicon resistors with $\Omega/\blacksquare \approx 250$. These resistors can be placed below the semiconductor surface so that they do not affect other routing paths.

Inductors and capacitors are slightly more complex. High-Q inductors are large, difficult to design and place, and lossy. In many cases, simply using the transmission line equivalent is much more area efficient, but the Q-factor typical microstrip and lines are limited. Other alternatives, like active inductors, may also be considered [33]. These are slightly larger but provide very high Q-factors. Figure 1 shows a schematic drawing of a CMOS active inductor.

However, some notable limitations of active inductors are adverse effects on noise figure and linearity, and inclusion of an active device increases power consumption. Another viable approach for inductor synthesis is usage of slow-wave coplanar waveguide (S-CPW) transmission lines [34]. These are discussed in greater detail in Section V-D.

Fortunately, most silicon vendors provide inductor design kits as part of their PDK offerings or optional add-on purchases. This can alleviate some of the design complexity and produces a synthesized component for further simulation and validation.

Considering capacitors, SiGe technologies have a distinct advantage due to the presence of a dedicated MIM layer. Most processes offer good capacitance density on these layers, which eases the placement of bypass and coupling capacitors.
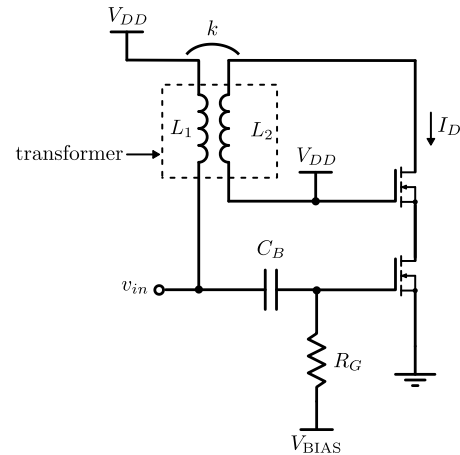

FIGURE 1. Active inductor circuit diagram.

C. THROUGH-SILICON VIAS

The through-silicon-via (TSV) approach to packaging offers several unique benefits for mm-wave ICs. Fanout wafer-level packaging (FOWLP) is a popular packaging technique that allows fanout of RF signals. However, the high setup costs implies that only higher volume production is cost-effective. One solution to this is to utilize TSV within a high-resistivity Si interposer and connect a BiCMOS chipset through Al-Al direct wafer bonding, as suggested by Wietstruck et al. [35], [36]. After de-embedding, transmission line loss of about 0.1 dB per transition was extracted. Additionally, this technique can be leveraged to combine different technologies (e.g. GaAs and CMOS) as well.

D. TRANSMISSION LINES

Substrate losses are one of the primary detrimental factors to Si transmission line performance. As such, any larger 2D transmission line structure is effectively limited in size – multi-stage matching works, large power splitters, spiral inductors, and so on. Implementing signal and ground on the same Si MMIC means that there is little dielectric separation between the two, in contrast to III-V substrates where the spacing is at least around 100μm. Si signal traces are therefore much thinner, only a few microns for typical dielectric spacing, which means that there is much larger Ohmic resistance involved.

Traditional CPW lines are widely used in RF design. They are wider and the dielectric thickness does not determine the signal-ground separation. The adjacent ground conductors, however, do not provide shielding from the substrate, and reduced Q-factor and higher losses result. A widely used alternative is to place floating shield strips on an adjacent metal layer [31], [34]. The shielding strips are incredibly effective and result in a significant performance improvement. Figure 2 shows the cross-section of this.

The floating shield strips slow down the propagation velocity, since electric fields are confined between the transmission
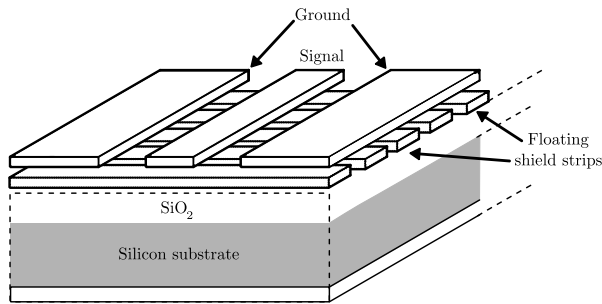
FIGURE 2. Shielded CPW transmission line.

line traces and shielding strips. The magnetic fields, on the other hand, pass through the shield.

Coupled lines are also extensively utilized in mm-wave RFICs, e.g. to implement miniaturized power dividers [37] and on-chip filters.

E. TRANSFORMERS

Transformers are highly versatile components in mm-wave circuits. They are used for DC isolation, impedance transformation, balanced-to-unbalanced (balun) conversion and biasing [38]. Their performance is unsurprisingly impacted by mm-wave technology constraints such as substrate losses, metal layer separation and surface wave excitation. However, careful modeling and parasitic extraction techniques can improve transformer performance, which allows designers to leverage their versatility.

VI. POWER AMPLIFIERS

Si devices can produce much less output power than III-V technologies. Fortunately, Si technologies provide substantially better integration and can provide sizeable cost advantages when mass-produced. Si devices can also operate at higher frequencies, aside from perhaps InP devices. However, InP devices cannot reach the reliability required by even modest wireless applications and come with a significantly higher price tag. CMOS PAs rely on aggressive gate length scaling. Typical bulk CMOS nodes have feature sizes around 180 nm, whereas advanced nodes are scaled down to 28 nm.

Some of the main PA figures of merit are output power, linearity and power-added efficiency (PAE). Often, these are competing requirements. For example, good linearity requires Class A or Class AB bias, but the PA efficiency is restricted to 78.5% [32]. Better efficiency can be achieved with Class E bias, where the device is switched at a particular duty cycle, but by virtue of driving the device into saturation, linearity is poor. PA designers contend with the technology to achieve the design requirements, which is where most academic efforts are concentrated nowadays.

Frequency is sometimes not the main driver for improving the process technology. This is quite evident in the widespread PA development targeting 5G NR applications in lower mm-wave bands [39], [40], [41] in 40 and 45 nm

bulk CMOS processes. Since 5G NR will operate on higher-order modulation, linearity is key and Doherty amplifiers are excellent options in this case. Their performance is limited mainly by the Class C auxiliary amplifier and the matching of the delay lines. Moreover, linearity requirements for the base station and the user equipment tend to differ, which means that the constraints on mobile devices are somewhat relaxed [42].

Achieving higher transit frequencies requires device scaling, which results in reduced breakdown thresholds, limiting the device's power handling capability. Even though numerous techniques to boost output power have been researched – such as spatial combining and transistor stacking – they introduce a number of other issues within the design [43].

Since most PAs drive the active devices to their limits, reliability becomes a key concern. Class E PAs, for example, rely on driving the HBT collector well past its B_{VCEO} point, up to B_{VCBO}, and maintaining safe operation in this regime is critical [44]. This means that higher supply voltages can be leveraged to increase the output power of SiGe HBT amplifiers. On the contrary, CMOS PAs (specifically FDSOI) can leverage transistor stacking for improving output power [45], [46].

BiCMOS processes offer heterojunction bipolar transistors (HBTs) and FETs on the same substrate, providing designers with excellent flexibility. HBTs can be used for high-performance analog circuits, while MOSFETs are used when digital blocks are required. This is one of the main attractions of silicon technology stacks.

A. POWER AMPLIFIERS IN THE 20-50 GHZ REGION

Figure 3 shows the saturated output power (P_{sat}) versus power-added efficiency (PAE) curve and trends for CMOS and SiGe PAs between 20 and 50 GHz (data from [47]).
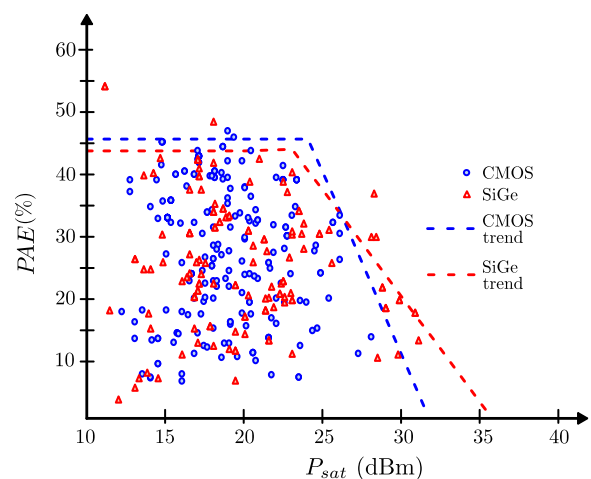

FIGURE 3. P_{sat} vs. peak PAE for PAs operating between 20 and 50 GHz.

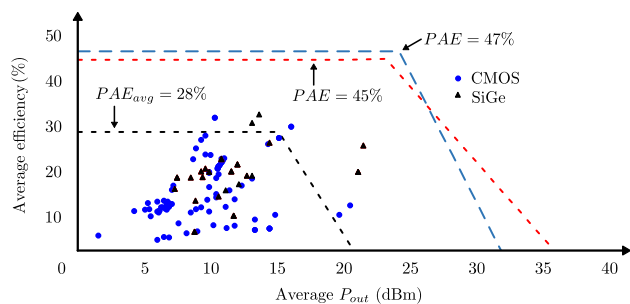The dotted lines indicate performance trends (blue for CMOS and red for SiGe) and the two technologies are

FIGURE 4. 20-50 GHz PA modulation performance comparison.

FIGURE 5. P$_{sat}$ vs. peak PAE for PAs operating above 50 GHz.

remarkably similar in performance. SiGe is barely ahead in terms of P$_{sat}$, and more so in the lower 20-40 GHz range, although this is small enough to be neglected. This similarity warrants further consideration of the best-performing amplifiers in either technology. The inherent advantages of high-performance analog bipolar devices are well documented. However, looking at the trend lines in Figure 3 and Figure 5, one can easily conclude that the difference may not be as significant as typically expected [4].

First, 20-50 GHz amplifiers are considered. Wang and Wang report a PA targeting 5G NR applications in the 24-30 GHz band [48]. It achieves at least 19 dBm output power and PAE higher than 19%. To boost linearity and backoff efficiency, the amplifier is implemented with a Doherty architecture. This is a key requirement for wireless modules using higher-order signaling schemes that involve amplitude modulation since efficiency drops significantly as the input power drops. The peak-to-average power (PAPR) ratio is commonly used to guage the potential effect of the modulation scheme on PA performance [32]. To this end, it should be noted that the PAE values plotted in Figure 3 are the maximum reported values. In most cases, average PAE is not reported, which could skew the results, primarily because higher PAPR signals (i.e., complex modulation schemes) do not really benefit from good peak PAE alone. In such cases, average PAE is a better indication of modulation and efficiency performance combined. Figure 4 compares modulation performance between 20 and 50 GHz (data from [47]).

CMOS PAs seem to achieve good PAE performance, with the bulk of amplifiers plotted in Figure 3 reaching between 40 and 50%. Garay et al. report PAE of 50% for a 45 nm CMOS-SOI PA, which also targets 5G NR systems [49]. Their architecture utilizes a dual-drive scheme, where the gate and source terminals are driven concurrently. Utilizing this driving technique alongside waveform engineering techniques improves drain efficiency as well as PAE.

SiGe PAs, however, perform slightly better in terms of average efficiency, which, as discussed earlier, is a better indication of modulation performance. Mm-wave systems rely on amplitude and phase-modulated waveforms to achieve higher data rates.
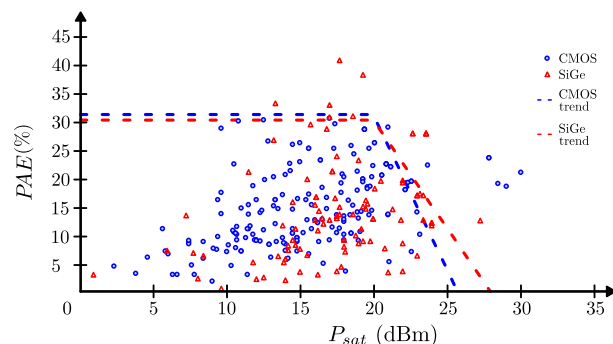
B. POWER AMPLIFIERS ABOVE 50 GHZ

Figure 5 shows the same comparison chart for PAs operating above 50 GHz (data from [47]).

The PA reported Song et al. is thus far unmatched with its 40.4% PAE. The amplifier achieved peak P$_{sat}$ = 17.7 dBm with 0.13 μm SiGe BiCMOS HBTs [50]. Additional emitter fingers are added and multiple HBTs are placed in parallel and in a cascode pair, which serves several purposes. First, the safe operating area (SOA) is extended since the current handling capability (and therefore also the output power potential) is improved. Second, the Class E capacitance is realized entirely by the parasitic output capacitance, and aptly sizing the device to match this requirement improves efficiency. Transmission line matching networks ensure wideband matching with acceptable loss. The quarterwave output network also ensures good harmonic termination, another reason for its high efficiency.

Considering Figure 5, SiGe amplifiers seem to have the advantage in terms of peak PAE. The closest CMOS PA with comparable power only manages to achieve PAE = 29.3 % and P$_{sat}$ = 17.4 dBm [51]. The PA is biased in Class AB and uses a transformer combiner to increase output power. This PA can switch between low and high-power operation. Its low-power mode achieves PAE = 19.6% and P$_{sat}$ = 12.6 dBm. On the contrary BiCMOS PNP transistors perform poorly at higher frequencies, limiting the potential for Class AB operation.

Another important observation from Figure 5 is that Watt-level output power (approaching 30 dBm) above 50 GHz surprisingly seems to be much more realistic for CMOS than SiGe, even though the situation is quite the opposite in the 20-50 GHz range. Datta et al. reported the first Watt-level PA implemented at 46 GHz with a BiCMOS technology [52]. This PA uses several combined Class E modulators with a tunable load network to mitigate some of the effects of PA load pulling at reduced input power levels.

The PA reported by Nguyen et al. is implemented in 45 nm CMOS-SOI, operates at 60 GHz, and uses a distributed active transformer (DAT) combiner [53]. The PA reaches 2 Gsym/sec symbol rate in QAM-64 and a peak PAE of 20.8%. The PA structure comprises 24 differential cells that

can deliver up to 30.1 dBm output power. This PA also provides good linearity performance and can support up to QAM-64 at about 10 dB backoff. The PA consumes a relatively large chip area (3×2.2 mm^2), which can be expected with large-scale power combining. The high PAE signifies the benefit of SOI substrates. Similar architectures relying on transformer combining and implemented in non-SoI technologies are not capable of PAE close to 20.8% due to the excessive substrate losses.

Spatial power combining seems to be flourishing in BiC-MOS. Roev et al. designed a K_a-band (23-33 GHz) PA in a 0.25 μm BiCMOS process from NXP [54]. The combiner consists of strongly coupled microstrip lines interfacing to a single substrate-integrated waveguide. The MMIC consists of four PA cells and mounts flipped onto a laminate. The measured saturated output power peaks at 30.8 dBm with 26.7% PAE. The technology used in this case provided many advantages, such as a combination of high and low-voltage HBTs, high-density MIM capacitors, deep trench isolation, and six metal layers.

Li et al. report a 142-182 GHz BiCMOS PA which utilizes slotlines for power combining [55]. The combiner consists of folded slots and CPW-to-slotline transitions, which provides impedance matching and combining simultaneously. A major advantage of this approach is its low loss (0.5 dB) and small footprint (126×240 μm^2). Additionally, the combiner covers a massive 80 GHz bandwidth from 140 to 220 GHz. The PA cells achieve 30.7 dB peak gain and a 40 GHz 3 dB badnwidth. The maximum output power is 18.1 dBm at 12.4 % PAE.

VII. LOW-NOISE AMPLIFIERS

Implementing mm-wave LNAs in SiGe or Si CMOS is challenging and it is evident that III-V technologies have a clear advantage in this domain [56]. Plainly put, processes with high gain, good linearity and low noise figure are favored for LNA design. Bulk CMOS processes are targeted at low-power commercial applications, and as such, they are not optimized for RF performance. This poses a number of challenges [57]:

- The digital origins of the process mean that the availability of good RF device models is limited, which means that in-house development of such models is often necessary. RF processes, on the other hand, generate and optimize their device models with extreme care, and these facilitate a much better correlation between simulation and real-world performance.
- Typical layer stackups are quite thin in comparison with RF CMOS processes, which inevitably increases the presence of parasitic resistances and capacitances. The dielectric separation between signal and ground layers is small, which restricts transmission line dimensions and further degrades performance. The achievable Q-factor is also notably lower, which inhibits the performance of
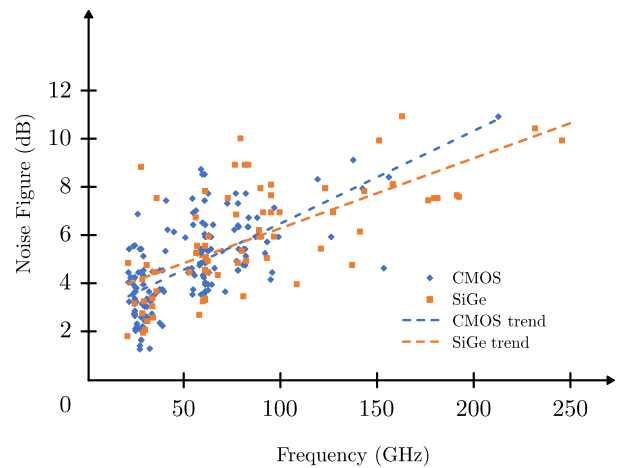

FIGURE 6. Reported CMOS and SiGe LNA performance, 20 GHz and higher.

planar inductors, transmission lines, filters, and many other passive circuits.
- Most bulk technologies have no dedicated MIM layers, so circuit designers have to use VNCaps implemented between layers or even resort to MOS capacitors. Neither of these options can realize high-Q capacitors with sufficiently high self-resonant frequencies. Issues such as supply ripple due to low-quality bypass capacitors and reduced bandwidth of matching networks result. RF-optimized technologies simply include dedicated MIM layers that solve these issues.
- Deep submicron scaling also results in significantly lower breakdown voltages, often in the range of 1 V. This limits the achievable power gain, and devices have much less headroom for voltage and current swing. Additionally, layout restrictions are generally more prohibitive, and significant process variations are commonplace.

Silicon technologies (particularly RF CMOS, CMOS-SoI and SiGe) are advantageous in this regard, even though both come with challenges and cost implications. Digital IP blocks available in high-performance CMOS technologies are typically not offered in comparable BiCMOS or RF CMOS nodes.

A. LNAs ABOVE 20 GHz

Figure 6 compares the noise figure of a number of SiGe and CMOS LNAs operating above 20 GHz (data from [58]).

Above 75 GHz, Figure 6 reveals that SiGe LNAs overtake CMOS in terms of noise figure performance. Below this point, the two technologies are very similar on average, even though CMOS LNAs have a slight advantage. Note that Figure 6 contains LNAs using CMOS FDSOI, RF-SoI, bulk, and SoI technologies. With that said, SiGe LNAs have higher power consumption in general, and it worsens as frequency increases. Additionally, CMOS LNAs have higher IIP3 values and therefore offer better linearity, in general.

Song et al. report a 95 GHz LNA [59]. This LNA achieves a best-case 3.5 dB noise figure at best and a peak gain of 34 dB. The gain is greater than 25 dB, and the noise figure is below 4.5 dB across the band. Moreover, the amplifier provides good matching with S_{11} below -10 dB. The LNA consumes only 15.6 mW DC power from a 1.2 V supply, and it is implemented with 90 nm SiGe HBTs. An LNA with similar performance is reported by Gao et al.; this one is implemented in 45 nm CMOS-SOI [60]. The amplifier achieves more than 10 dB gain between its 80 to 95 GHz operating band, and the best-case noise figure is 4.2 dB. The worst-case noise figure is less than 4.9 dB across the band.

The D-band LNA reported by Aksoyak et al. operates at 140 GHz with a 31 GHz bandwidth [61]. At 31 mW DC power, it achieves 20 dB gain with a -19.7 dBm 1 dB compression point. Its simulated noise figure is 5.9 dB, and its implemented with 0.13 μm BiCMOS devices. By using both noise-reduction and gain-peaking techniques, this design has the potential to yield the best FoM of any D-band LNA to date.

Artz et al. implemented their D-band LNA in 22 nm FD. The maximum gain was measured as 18 dB across the 3 dB bandwidth of 10.8 GHz. Passive gain control is implemented via back gate control, thanks to the FDSOI technology. Moreover, at maximum gain, the LNA consumes only 27.5 mW DC power, and this reduces to 17.5 mW at minimum gain.

The final LNA of note discussed here is reported by Vardarli et al. [62]. The design utilizes two-stage, broadband matching to achieve a flat 13.5 dB gain and 4.5 dB noise figure. It operates over E- and W-bands (62-110 GHz), uses a 0.7 V supply and consumes only 5.9 mW. This is the widest bandwidth, lowest power LNA reported to date.

VIII. DATA CONVERSION CIRCUITS

Any wireless communications system relies on converter circuits to move between the analog and digital domains [5]. The analog-to-digital (A/D) converter is the primary influencer in terms of the achievable overall data rate. Conversely, the digital-to-analog (D/A) converter largely determines the TX bandwidth and as such, also limits the maximum data rate. The primary goal in A/D converter design is to optimize the power-bandwidth product. This involves needs a careful balance between the sampling rate and bit resolution. Most mm-wave designs aim to maximize bandwidth – since multi-Gb/s data rates are a staple requirement – while keeping power consumption under control. A baseline requirement for 60 GHz transceivers is about five resolution bits and at least 1 GHz bandwidth [63]. With that said, applications such as wireless video conferencing and wireless personal area network (WPAN) enhancements described in the IEEE 802.15.3c standard could potentially require as many as 8 resolution bits and at least 2.5 Gs/s sample rates. Fairly high sampling rates are achievable in both SiGe and CMOS technologies, with the upper end of performance exceeding 30 Gs/s [64], [65], but this comes at immense power consumption. Another key issue is the clock jitter dependency

of the dynamic range. In this case, good integration between the analog and digital MMIC regions is hugely advantageous since it helps to keep the clock jitter under control.

Wideband D/A converters with good linearity are sought after in many mm-wave transmitter specifications [29], [66]. High-speed operation will typically favor BiCMOS devices, but CMOS alternatives offer their own unique advantages.

A. ADC PERFORMANCE CONSIDERATIONS

High-performance, next-generation wireless systems demand a higher effective number of bits (ENOB) and sample rates. A common approach to achieve higher sampling rate is to pipeline multiple stages. This relaxes the requirement on each individual stage, so a low-resolution quantizer is placed a lower-resolution multiplier D/A.

The new generation of fiber-optic systems will operate at extremely high bandwidths exceeding several hundred Gb/s, which requires data converters with a minimum bandwidth of about 30-32 GHz [29]. This kind of bandwidth is challenging to achieve in even the most advanced digital CMOS technologies. Scaled technologies can typically achieve very good SNDR performance. Their small footprint and low power consumption mean that highly scaled 7 nm and 14 nm FinFET process are excellent candidates for realizing SAR architectures [67]. These devices are constrained by large parasitic capacitances due to the small spacing between metal layers, which results in poor f_{max} and thereby also limiting converter bandwidth. In the process of scaling down from 65 nm bulk CMOS all the way down to 14 nm and smaller FinFETs, minimal progress to achieve better signal processing bandwidth has been made. SiGe HBTs have shown much better scaling potential.

ADCs are primarily characterized by two figures of merit (FoMs), namely the Walden and Schreirer FoMs (FoMW and FoMS, respectively) [68]. As a rule of thumb, wideband, high-resolution designs tend to achieve better FoMS, while FoMW is suitable for evaluating low-resolution converters.

B. BENCHMARK FLASH ADC CIRCUITS

Flash converters, with their capability for very fast conversion rates, are excellent candidates for mm-wave systems. As with most mm-wave implementations of a particular circuit block, flash converter designers need to overcome process and circuit limitations to achieve the desired performance. Consequently, numerous diverse architectures have been reported for mm-wave flash ADCs [65], [69]. The time-interleaved architecture of a flash converter necessitates parallel cores. This, in turn, implies that periodic and regular calibration for offset, skew and gain mismatch is a must. CMOS flash converters typically use some type of time-interleaved track-and-hold amplifiers (THAs). These amplifiers then drive several banks of sub-ADCs, all time-interleaved. SiGe amplifiers are preferred in this case since they are able to drive highly capacitive loads.
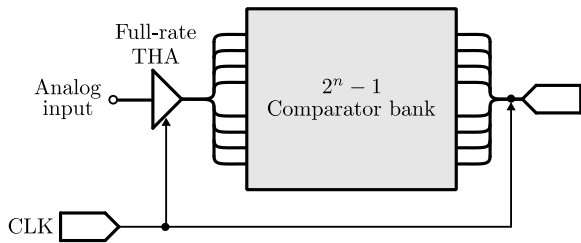
FIGURE 7. Flash ADC with direct comparator driving.

FIGURE 8. Mm-wave flash ADC architecture.

Driving the comparator bank as a lumped load can result in moderate improvements in conversion rates. Figure 7 shows one such architecture [70].

Cheng et al. managed to reach a 40 GHz sample rate with this architecture, using BiCMOS devices with $f_T / f_{max} = 210/310$ GHz [70].

Ali et al. implemented RF-sampling ADCs that reach 18 and 12 GS/s, respectively [71]. Both converters use wideband, integrated THAs and an expansive digital calibration block. With 16 nm FinFETs, the best-performing converter offers 12 resolution bits and consumes 1.3 W power. Moreover, with 8 GHz inputs, the SFDR is 54 dB.

Schvan et al. utilized a long transmission line, which absorbs the bulk of the input capacitance of the comparator bank [72]. The THA can therefore be removed, but the matching of the clock and data paths remains critical to avoid skew. Shahramian et al. [65] implemented a variation of this architecture. This design uses buffer trees to drive the capacitive load. A transimpedance amplifier (TIA) on the front-end is chosen as a low-noise gain block. This converter can handle very small voltages, in the range of 0.24 V_{pp} differential. The clock and data trees are routed symmetrically, providing significant skew reduction. The A/D is implemented in a 0.18 μm BiCMOS process and reaches 35 GS/s with four resolution bits, *SFDR* of 27.3 dBc at 11 GHz, at 4.5 W total power consumption. These are excellent results given the modest f_T / f_{max} of the technology, which is around 50 GHz and 160 GHz.

Du et al. [69] proposed an architecture like the one in Figure 8.

This ADC uses of a 4-bit flash core with an auxiliary Gray encoder that minimizes bubble errors. The encoder and performance of the flash core have the largest effect on the overall linearity. The core uses a traveling-wave topology, another solution to alleviate the requirement for a THA in the front end. The input signals travel synchronously between the comparators. The encoded outputs improve compatibility with the DSP interface. The combination of the 3 : 1 multiplexer, scrambler, and PRBS generator can be leveraged to implement sample storage on an FPGA. Moreover, this is one of the first reported ADCs with built-in digital encoding, solving the encoder bottleneck typically encountered in multi-Gb/s converters. The circuit is implemented in a 130 nm
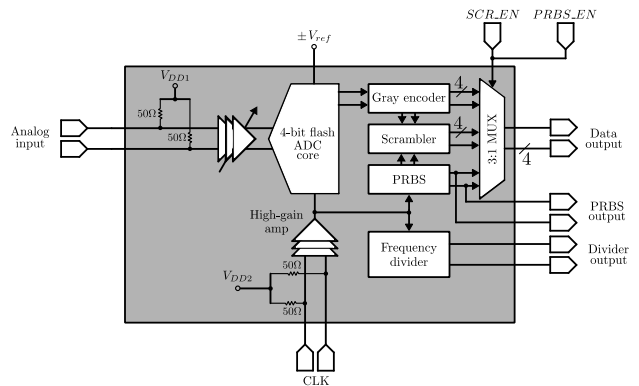
BiCMOS process, illustrating the benefit of high-performance analog and digital devices on one substrate. This converter achieves ENOB $\geq$3 and SFDR exceeding 4.8 dBc, with a maximum sample rate of 39 GS/s, and it can operate from DC to 20 GHz.

A viable alternative to flash converters is the folding ADC topology. This architecture uses two pipelined folding magnitude amplifiers, and the LSB and MSB streams are split at the input by a hard decision unit. As a result, the input capacitance of the converter is reduced and the converter core is simpler. High-bandwidth THAs sample the inputs at 24 GS/s, where the two-bit folding converters decode a four-level pulse amplitude modulated (PAM) signal into non-return-to-zero (NRZ) channels. The NRZ streams are then multiplexed to deliver the output data rate. The design reported by Fatemi et al., implemented in 130 nm BiCMOS, achieved 96 Gb/s data rate while consuming only 544 mW [73]. Peng et al. report a similar architecture, achieving 56 Gb/s PAM-4 in 40 nm CMOS [74].

Table 3 summarizes A/D converters of note from the literature.

C. MILLIMETER-WAVE DACs
Scaling of CMOS devices below 32 nm has been shown to provide several advantages for digital circuit designers. Transistors operating above 300 GHz are now everywhere, opening opportunities for a multitude of power-sensitive applications in the 60 to 100 GHz range [77], [78], [79]. Breakdown voltage reductions, as discussed earlier, have a large impact on performance. As such, pushing transceivers that can reach 10 Gb/s and higher data rates introduces significant challenges.

Considering a typical zero-IF transmitter, the DAC is followed by a mixer, PA and I/Q combiner. The mixer output is often split and fed into a beamforming network that drives a larger antenna array. The transmitters of the future will connect the mm-wave DAC directly to the antennas, but there are some challenges to overcome on the way there.

TABLE 3. Comparison of state-of-the-art Si mm-wave A/D converters.

Reference	[65]	[64]	[69]	[75]	[71]	[76]
Technology	180 nm SiGe BiCMOS (Jazz SBC18HX)	130 nm SiGe BiCMOS (IBM 8HP)	130 nm SiGe BiCMOS	22 nm FDSOI	16 nm FinFET	65 nm CMOS
Architecture	Flash	Time-interleaved	Flash	Cascaded SAR	Pipelined, THA	
Resolution (bits)	4	4	4	10	12	6
Sampling rate (GS/s)	35	40	40.32	128	18	0.1-40
SFDR (dBc)	28.5 below 1 GHz, 27.3 at 11 GHz	22	33 @ 1 GHz 30 @ 12 GHz 24 @ 20 GHz	N/A	56 @ 4 GHz 54 @ 8 GHz	40 @ 10 GHz 35 @ 18 GHz
SNDR (dB)	24.1 below 1 GHz, 19.8 at 11 GHz	N/A	N/A	N/A	52 @ 4 GHz 48 @ 8 GHz	34.6
ENOB (bits)	3.7	3.5 @ 10 GHz/channel	3.7 @ 1 GHz 3.0 @ 12 GHz 2.8 @ 20 GHz	N/A	N/A	4.5 @ 10 GHz 3.9 @ 18 GHz
Power consumption (mW)	4500	N/A	2500 (w/o DAC output drivers) 3500	300	1300	≤1500
FOM [4]	N/A	10 pJ/sample	8.3 @ 20 GHz (w/o DAC output drivers) 12.6 @ 20 GHz[5]	W: 162.9 S: 150.2	W: 222 S: 150.4	W: 828.6 S: 136.1

The data rate requirement for mm-wave DACs places extreme strain on digital I/O bandwidth. Consider that a modest DAC that is operating at 16 GS/s with 8 resolution bits. In this case, the DAC needs input data supplied at 128 Gb/s. Most D/A converters operating even at modest speeds overcome this issue with parallel input streams received from an FPGA and subsequently multiplexed [80]. The off-chip data transfer rate determines exactly how many streams can be combined in parallel.

Typical low-voltage differential signaling (LVDS) channels can provide around 500 Mbps. Meeting the targeted above data rate of 256 Gb/s requires 512 LVDS channels, placing significant strain on the FPGA I/O resources and also causing a large increase in chip area and power consumption. LVDS channels require synchronization to operate at full capacity. Implementing high-speed serializer-deserializer (SerDes) interfaces often used in modern digital systems (e.g., PCI Express transceivers and DisplayPort sources) are a potential solution. However, current-generation FPGAs are limited to a throughput of a few Gb/s at best. Even so, top-tier performing FPGAs have to be carefully integrated into the system and come at exorbitant price tags as well as their own size and power restrictions. This limits the practical applications to high-performance scenarios.

[4] W: Walden FOM (ENOB/$2^{power*fs}$, S: Schreier FOM (SNDR/(power*BW)
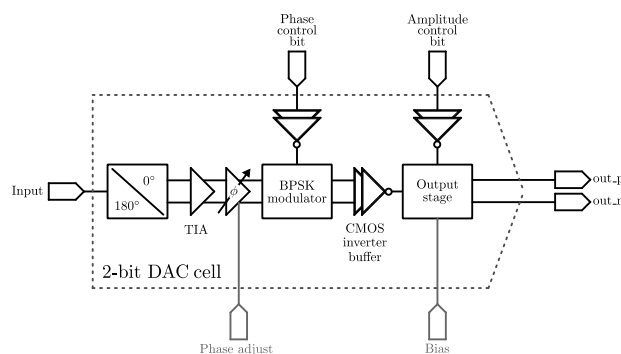
[5] $FOM = power/(2^{ENOB} * min(f_s, f_{in}))$

FIGURE 9. 2-bit power DAC cell.

D. BENCHMARK DAC CIRCUITS

Balteanu et al. propose using an array of 4 identical 2-bit DACs to essentially instantiate an 8-bit power DAC capable of I/Q signaling [66]. Figure 9 shows a single 2-bit DAC cell.

A 180° balun splits the input signal to provide a differential output. A broadband TIA then amplifies the input to improve its dynamic range before phase adjustment. The phase shifter provides I/Q phase imbalance calibration of up to 6.5 degrees [81], [82], [83]. Failing to do so can increase the bit error rate since phase imbalance degrades the modulation performance. A Class D pre-driver comprises a binary phase-shift keying (BPSK) modulator, and a CMOS inverter follows. It drives the output stage into saturation. I/Q

amplitude imbalance is eliminated by virtue of the rail-to-rail operation of the switching pre-driver stage.

BPSK up to 5 Gb/s on a 45 GHz carrier was demonstrated, with the added possibility of simultaneous 2 Gb/s ASK and 2 Gb/s BPSK. Additionally, the saturated output power peaks as high as 24.3 dBm, with PAE reaching 19.6% when run from a 4.4 V supply. The DAC is fabricated in 45 nm CMOS SoI.

Nguyen et al. implemented an interleaved switched-capacitor DAC in 22 nm FDSOI, the first of its kind [84]. This design uses a frequency tripler in the output stage, pushing the linear output power above 20 dBm. Additionally, the converter efficiency peaks at 36.7% and reaches 2.4 Gb/s with QAM-64 modulation. Yoo and Hong report an RF DAC with LO leakage cancellation [85]. It consists of an IQ source, two IQ amplitude Gilbert-cell modulators, and a linear PA. The DAC manages 3 Gb/s, also with QAM-64 signaling, and consumes only 12 mW from a 1.1 V supply in 28 nm bulk CMOS. Finally, it is targeted at 5G NR and operates at 28 GHz.

Table 4 compares a select few mm-wave DAC cells.

IX. MILLIMETER-WAVE SILICON TRANSCEIVERS
A. IEEE 802.11ad/AY WiGig
The IEEE 802.11ad standard describes small-scale wireless local-area networks requiring data rates up to about 6 Gb/s [18], [19], [20]. The standard was subsequently amended in 802.11ay so that the PHY and media access control (MAC) layers enable at least one mode that supports 20 Gb/s data rates. Four 2.16 GHz channels are allocated in the 60 GHz band for 802.11ad, but only one of the channels may be used. 802.11ay intends to leverage channel bonding, multiple channel allocation, and efficient beamforming to improve performance. Both standards aim to significantly improve the capabilities of current-generation systems. Single-carrier transceivers relying on QAM-16 can thus deliver up to 4.62 Gb/s while using OFDM and QAM-64 can boost data rates as high as 6.76 Gb/s for a single OFDM stream. Beamforming and multi-user MIMO (MU-MIMO), specifically in the downlink, are other pillars of next-generation Wi-Fi, but there are some technological issues to solve.

First of all, bonding four QAM-64 channels is practically quite difficult to achieve. Various requirements, such as wideband gain and low LO phase noise, affect the design significantly. 60 GHz CMOS transceivers will often use direct-conversion architectures to take advantage of their reduced power consumption and wider bandwidth [88], [89], [90]. Injection-locking techniques are often used to achieve decent phase noise [91], [92], [93]. However, adding wideband I/Q offset correction is a necessary precursor to channel bonding QAM-64 streams. This is challenging, since even small phase and gain mismatch can severely affect the modulation performance. Lower-frequency radios often use digital I/Q correction mechanisms to provide calibration capability,

but implementing these mechanisms on-chip is costly in terms of area, power and complexity.

An aggregated QAM-64 stream requires at least an 8-bit ADC with a 14.8 Gb/s sample rate, which implies opting for a sizeable time-interleaved architecture, inevitably driving up power consumption. In this example, the Nyquist rate is 7.04 GS/s, and filter and oversampling by a factor 2 results in the output sample rate of 14.08 GS/s. The immediate problem here is that an 8-bit ADC can likely only achieve an SNDR of 35-36 dB at most, leaving a window of about 10 dB to account for channel impairments. Table 5 is adopted from previous work published by this authoring team, and summarizes a select number of state-of-the-art WiGig transceivers [94].

B. 5G MOBILE COMMUNICATIONS
Component and subsystem specifications can be derived from system-level 5G performance requirements. The RF requirements for 5G mobile can be summarized as follows [6], [100], [101], [102]:

- **Wider bandwidth**: 4G and older 2G and 3G mobile communications systems operate below 6 GHz, with the majority of systems deployed globally operating below 3 GHz. Spectrum is massively congested in this range due to the scope of systems operating here, and this is one of the primary motivators for extending operation into mm-wave bands (28-300 GHz). Here, much wider carrier bandwidths are available, which directly translates into users experiencing higher bandwidth and throughput. Typical envisioned 5G deployments can also be separated into two layers. The first layer is serviced exclusively by more traditional microwave links. These handle some user traffic, but primarily control plane data. The other layer handles bandwidth-intensive user traffic and mm-wave links are employed in this case. Micro cells can be further separated as operating frequencies permit, which means that denser deployments will be required but user experienced bandwidth will improve.
- **Massive MIMO capable base stations**: Increasing carrier frequencies means that significantly larger array antennas can be leveraged. These antenna arrays provide high gain through spatial multiplexing, which counteracts the increased path loss. For mm-wave 5G bands, arrays with as many as 1024 antennas are practically feasible from both a performance and a manufacturing perspective. Moreover, each array can also consist of multiple sub-arrays and utilize polarization diversity. Massive MIMO also enables transmission to multiple users scattered across azimuth and elevation, largely because of precise beamforming. The limiting factor in user serviceability at the base station side is the number of spatial streams.
- **Increased network density**: Increasing network density enables efficient offloading of traffic to smaller cells, which not only reduces the single-cell traffic demand,

TABLE 4. Mm-wave DAC comparison summary.

Reference	[84]	[86]	[87]	[66]	[52]
Technology	22 nm CMOS SOI	40 nm CMOS	45 nm SOI CMOS	45 nm SOI CMOS	130 nm SiGe
Architecture	Class D, edge combining	Double-edge-triggered, digital IQ	6-stack power DAC, IQ	4-stack NMOS, IQ	8-way load-modulated digital PA / 1-bit Class E modulator
Supply voltage (V)	0.9 / 1.8	1.1 / 2.2	68	3.9 / 4.4 / 5.1	5
Resolution (bits)	6	2×8	4	8	3 / 1
Frequency (GHz)	28	73 / 83	85-90	45	46
Peak output power (dBm)	21.2	20.5	19	22.5 / 23.5 / 24.3	28.9 / 21.8
Efficiency @ peak power (%)	36.7	21.7 @ 77 GHz	8.9	19.4 / 19.6 / 14.6	18.4 / 18.5
Efficiency @ back-off (%)	19 (6 dB)	N/A	N/A	N/A	11 (6 dB) / N/A
Modulation	QAM-64	QAM-16 / QAM-64	ASK, OOK	BPSK	N/A / ASK
Data rate (Gb/s)	2.4	12 / 6	15	5 Gbps	N/A / 1.25
EVM (dB)	-29.6 (RMS)	-18.1 / -25.1	N/A	N/A	N/A
Area (mm²)	2.2	0.91 (core)	1.1×2.0 (including pads)	3.17×2.42 (packaged)	13.7 / 1.6

but also enables higher performance and throughput per cell. Dense environments in urban areas and indoor hotspots are good candidates that will benefit from reducing cell size. With that said, macrocell coverage via the aforementioned microwave links is still required for the control plane, and increasing cell density also increases the potential for interference at the cell edges. Naturally, cells can, therefore not be shrunk ad infinitum.

- **Waveform engineering**: Some 5G applications demand re-thinking and clever engineering of waveforms, multiple-access, and modulation schemes. OFDM, which was originally developed to improve spectral efficiency and improve performance of cellular systems, are not practical for applications such as M2M communications. In such systems, data packets are much smaller and the overall throughput is limited. The OFDM overhead will result in inefficient communications, especially considering that energy efficiency is high priority.

Table 6 compares beamforming transceivers for mm-wave 5G.

C. RADIO-ON-GLASS TRANSCEIVERS

Radio-on-glass (RoG) modules are a major advancement in packaging technology and are highly beneficial for mm-wave silicon circuits. Currently, the production of low-loss RF modules that require little to no tuning effort is a largely unmet need in the mm-wave packaging industry. Silicon substrates are notorious for their high losses at mm-wave. As an alternative, organic-based laminates are used, but these are moisture-absorbent and suffer from material inconsistencies, which makes them incompatible with mm-wave circuits.

Another option is low-temperature co-fired ceramic (LTCC) substrates [108], [109], [110]. However, these substrates are plagued by surface roughness issues, scalability, and inconsistent dimensional accuracy.

Glass is a good potential alternative that can be fabricated in a panel format, thereby saving costs. Glass is impervious to moisture, and its electrical properties are extremely consistent over a wide range of humidity and temperature. Moreover, glass can be manufactured in sheets of under $100 \mu m$, reducing the overall package height and enabling the use of smaller, higher-density vias. All of these characteristics are very attractive for mm-wave circuits operating in a wide variety of environmental conditions.

Some technology demonstrators have been reported that are of interest. Shahramian et al. report an E-band FDD module consisting of two transceivers and two PAs [111], [112]. The design utilizes a glass interposer on which all analog, RF, and power is routed. The interposer is also BGA compatible so that it can easily be integrated into a traditional PCB. Package pads allow access to I/Q IF components as well as decimated LO frequencies for both transceivers. Finally, a WR-12 port is provided as an antenna interface.

The low- and high-band ICs were fabricated in an IHP 0.13 μm SiGe BiCMOS technology with 300/500 GHz HBTs. Each IC measures 4.5×2.6 mm². The demonstrator achieves 24 dBm saturated power on average and 8 dB noise figure. The FDD modules also support up to QAM-1024 with less than 2% EVM at 15 dBm output power. Moreover, data rates up to 24 Gb/s were reached using QAM-64 signaling at 20 dBm output power.

Another similar reported design by Shahramian et al. operates in W-band and D-band ranges where the low band is between 115 and 155 GHz, and the high band is between

TABLE 5. 802.11ad/ay WiGig transceivers.

Reference	[95]	[96]	[97]	[98]	[99]
Technology	65 nm CMOS	28 nm CMOS	130 nm SiGe	65 nm CMOS	65 nm CMOS
Data rate and modulation used	21.12 Gb/s, QAM-64 with 2-channel bonding 28.16 Gb/s, QAM-16 with 4-channel bonding	27.8 Gb/s, QAM-16	5.9 / 4.6 Gb/s QAM-16	28.16 Gb/s, QAM-16 with 4-channel bonding 42.24 Gb/s, QAM-64 with 4-channel bonding	12.32 Gb/s, QAM-128, 1-channel 24.64 Gb/s, QAM-128, 2-channel bonding 42.24 Gb/s, QAM-64, 4-channel bonding 50.10 Gb/s, QAM-64, 10.44 GHz BW
TX power (dBm)	-4.2 dBm at -26.0 dB EVM	N/A	13.4-16.2 dBm at -20.5 dB EVM	8.5 dBm at -21 dB EVM / 7 dBm at -22 dB EVM	7.3 dBm at TX EVM = -22 dB
RX noise figure (dB)	5.4	7.0	3-5	5.7 / 5.7	
Core chip area (mm²)	0.96	1.1	4.97	7.92	Total: 2.92 TX: 1.07 RX: 1.09 PLL: 0.21 Calibration block: 0.19 Logic: 0.36
Circuit building blocks	TX, RX, LO	Digital polar TX, direct-conversion RX, TX, RX, LO, PLL	Digital I/O, monitoring, TX, RX, crystal + PLL	Direct-conversion, 1xRX, 1xTX, 1xLO / Direct-conversion, 2xRX, 2xTX, 2xLO, frequency-interleaved	Direct-conversion, TX, RX, PLL, calibration, logic
Power consumption (mW)	94 (TX mode) 105 (RX mode)	210 (TX mode) 110 (RX mode)	53 per m link distance	251 (TX mode) 220 (RX mode) / 544 (TX mode) 432 (RX mode)	169 (TX mode) 139 (RX mode)

135 and 170 GHz. This design uses the same 0.13 μm SiGe BiCMOS process. The saturated output power peaked at 13 dBm, with the receiver noise figure averaging around 8.5 dB. The module reaches 42 Gb/s using QAM-128, and a demonstration setup achieved 36 Gb/s with QAM-64 signaling on a 250 m wireless link.

Radio-on-glass technology looks certain to have a profound impact on the commercialization of mm-wave technology.

X. 6G AND THz SYSTEMS

THz band communication (100 GHz – 10 THz) is an important domain of research that impacts multiple disciplines in wireless communications. Multi-Gb/s and even Tbps links are desirable for numerous applications. The FCC recently published allocations for several bands above 95 GHz for research [113]. Network operators have gradually and cautiously lower mm-wave bands (particularly 28 and 39 GHz) for 5G, anticipating data rate demands

eventually exceeding 100 Gb/s. Practical testing of potential advanced 5G deployments has not been as promising, and speeds around 1 Gb/s have been documented thus far [114].

Many contributing factors play a role here, such as the complexity of accurately modeling a 5G wireless channel, circuit design issues, manufacturing imperfections, and process variations, and external interference. THz bands have been used for ultra-high-resolution imaging [115], [116], and spectroscopy [117], among many others.

Photonics and electromagnetic propagation in THz bands pave the way to some interesting opportunities.

A. USE CASES

THz spectrum can potentially be leveraged for a number of applications:

- **Dense local area networks**: Wireless links of less than 10 m can realistically operate in the 625-725 GHz and 780-910 GHz bands due to THz-optics bridges

TABLE 6. 5G Beamforming transceivers.

Reference	[103]	[104]	[105]	[106]	[107]
Technology	28 nm RF CMOS	180 nm SiGe BiCMOS (Jazz SBC18H3)	0.15 μm GaN HEMT (PA) / 0.25 μm GaAs (driver amps, LNA, mixers, PIN diode switches)	130 nm SiGe BiCMOS	65 nm CMOS
Architecture	Direct-conversion, injection-locked IQ LOs, RF beamforming	Differential, direct-conversion, RF beamforming	Direct IF (multi-chip), digital beamforming, FPGA bit streamer interface	Double-conversion sliding-IF, RF beamforming	Dual-band, Cartesian beamforming TX/RX, programmable gain amps
Frequency (GHz)	25.8-28.0	27.8-31.2	28	27-29	28 / 37
Beamforming elements	2×4 TX/RX	4 per TX/RX front-end, total of 2×4×4=32 per transceiver Beam steering: $\pm20°$ (E-plane), $\pm50°$ (H-plane)	Digital, 15 per transceiver, 480 in total (32 transceivers).	16 per transceiver, 64 (4 transceivers). $\pm30°$ beam steering in 1.4° steps	Two-layer hybrid MIMO 8-element, 4-stream
RX noise figure (dB)	6.7 at G_P=69 dB 13.6 at G_P=30 dB	7.5	Not reported	≥ 6.0 (with PA switched off)	7.9 / 8.8
TX EIRP (dBm)	31.5 @ P_{sat} = 9.5 dBm 24.0 @ 7.5 dB backoff (P_{out} = 2.0 dBm)	P_{1dB} = 41 dBm with 32 elements (Single PA: P_{1dB} =11.7 dBm)	68 with 480 array elements, P_{out} = 42 dBm at 7 dB backoff	28 (16 array elements)	P_{sat} = 15.5 dBm with TX gain = 43.5 dB / P_{sat} = 15.6 dBm with TX gain = 40 dB
EVM at medium power	RX: 2.15% @ P_{in} = -60 dBm TX: 2.20% @ P_{in} = 0 dBm (QAM-64, LTE w/ 20 MHz channels)	7.5% (QAM-64)	4.5% (QAM-64)	Not reported	TX: -27.7 dB RX: -27.9 dB / TX: -27.1 dB RX: -26.3 dB (both QAM-64)
DC power consumption (mW)	RX mode: 400 TX mode: 680	RX mode: 130 TX mode: 200	Not reported	RX mode: 3300 TX mode: 4600	RX mode: 98.75 TX mode: 168.75
Die size	2.8×2.6 mm^2	2.5×4.7 mm^2 per 4-element TX/RX front-end	Not reported	15.6×10.6 mm^2	1.05 mm^2
Line-of-Sight Coverage (m)	75 m (QAM-64 with TX EIRP = 20 dBm)	300 m (QAM-16 at 5 dB backoff)	1700	Not reported	Not reported

that provide a transition from wireless THz links to fiber-optic backhaul [29].

- **Wireless cognition**: This is a concept where a communications link between dislocated nodes facilitates real-time calculations on data collected from a machine or device. A fleet of drones, for example, does not have the size, weight and power (SWaP) budget to perform complex computational tasks on board. Given

a wideband communications link to a nearby device means that power-intensive tasks can be offloaded effectively. Other applications in robotics and autonomous vehicles are also possible [118].

- **Wireless personal area networks**: Data rates similar to and exceeding best-in-class fiber broadband can be achieved up to a few meters without needing any physical connections. At 140 GHz, a 14.5 cm piece of drywall

will attenuate the signal by about 15 dB [114]. Similarly, a 2.5 mm clear glass pane will attenuate a signal by about 87 dB at 300 GHz. With such restrictions in mind, the applications for THz systems could be significant in boardrooms, small offices, warehouses and factories.

- **THz Spectroscopy**: New methods to extract spectral information from THz radiation substantially expands the functionality of standard BiCMOS processes [119]. One technique measures the impressed current distribution that arises from THz radiation, and subsequently estimates the spectrum of the incident signal. Essentially, the excited current is spectrum-dependent.

- **Remote Sensing**: Sub-mm-wavelength propagation characteristics can be leveraged to gain detailed knowledge about the immediate environment by analyzing signal behavior. Small, high-gain antennas also enable pencil beam patterns for excellent spatial selectivity that improves as the operating frequency increases. Rapid beam scanning can also be utilized, further improving the resolution (and ultimately the utility) of the remote sensing system.

- **Wireless network-on-chip (WNoC)**: Transceiver requirements are headed towards tightly integrated designs (analog, digital and antenna front-end) and miniaturization. THz or optical links canreplace existing wired connections. Reliability, latency and energy efficiency will be key performance characteristics [120].

- **Imaging**: Light detection and ranging (LIDAR) imaging operates at infrared frequencies, and such sensors cannot operate in suboptimal weather conditions. In these environments, mm-wave and THz radars can provide much better performance. Applications such as assisted driving (or flying) and remote imaging via synthetic aperture radar (SAR) are very well suited for THz bands [115].

- **Nano- and pico-cell networks**: THz frequencies are suitable for nano-cell networks following the same line of reasoning as to why mm-wave is well-suited for pico-cell networks. Interconnected nano-devices and machines are a possibility because of excellent spatial frequency reuse [121].

- **Internet of NanoThings**: Nano-devices consuming significantly less energy than current IoT devices by using techniques such as energy harvesting are envisioned [122]. Moreover, such devices will rely either on encoded bits carried via molecules or plasmonic radiation.

- **Satellite communication**: Because wireless links between satellites do not have to contend with atmospheric attenuation, THz bands are worth considering for satellite-to-satellite links [123]. Beam alignment is not as strict as for optical links, in which case communication can continue and link stability improves as satellites tends to drift outside their orbit.

B. 6G TECHNOLOGY CHALLENGES

THz operation poses significant challenges to the design of transceiver hardware, most of which falls on the semiconductor technology. In most cases, the frequency operation will far exceed the maximum frequency at which even the latest and greatest transistors can provide power gain. The same issues arise as with mm-wave devices – device miniaturization is required to reach higher frequencies, at the cost of reducing breakdown voltages and power capability. Operating at 500 GHz with ten thousand individual antenna elements with $\lambda/2$ spacing of 0.3 mm means that the entire array will be about 3 cm $\times$ 3 cm [113]. To support this, the accompanying electronics should be more or less the same size so that the length of interconnects are minimized. Ultramassive MIMO arrays such as this one are likely to be utilized by 6G base stations in the future.

Indoor experiments with photonic signal generation have shown data rates around 50 Gb/s at 300 GHz with uni-traveling-carrier photodiodes [124]. Graphene-based devices have exceptional properties. Generalov et al. have demonstrated a 400 GHz graphene FET (GFET) detector with an optical responsivity of 74 V/W [125]. Zak et al. demonstrated a similar device that managed to detect and rectify a 600 GHz signal at room temperature [126]. Novel waveform shaping techniques based on harmonic extraction far exceeding the transistor's $f_{\max}$ have been demonstrated to yield down to 2.6 ps pulse widths at $f_0 = 107.5$ GHz and $f_1 = 215$ GHz. The fundamental EIRP in this case is 4.6 dBm, and that of the second harmonic is 5.0 dBm [127].

Some "beyond-5G" demonstrators have also shown promising performance. Using 130 nm BiCMOS technology, Karakuzulu et al. designed a D-band (110-170 GHz) four-channel phased array transceiver [128]. The design makes use of localized backside etching to implement a patch antenna array. At 15 cm, the transceiver achieves 180 Gb/s with QAM-16 and a 12.2% EVM, and 200 Gb/s with QAM-32 and an 8.3% EVM. Additionally, the radio-on-glass demonstrators discussed earlier are showing excellent potential in the move towards THz communications.

However, 500 GHz amplifiers and oscillators are not realizable with current-generation Si technologies. One option is to implement non-linear frequency multiplication, but this tends to negatively impact overall performance. At such high frequencies, the effects may be too severe for the device to really be useful. Combining the use of InP for the ultra-high frequency components and Si for baseband circuits could be an alternative solution. Moreover, with the demonstrators mentioned earlier and general technology capabilities, practical implementations of 6G links seem to be focused on D-band frequencies [118], [129], [130].

XI. CONCLUSION

This paper covered motivations for selecting Si-based process technology in the context of current and future-generation mm-wave applications. Several key aspects of Si CMOS

and BiCMOS technology platforms were evaluated, and each critical circuit block in a transceiver chain was analyzed with a couple of examples from the literature. RF CMOS nodes have improved significantly in recent years thanks to many substrate advancements such as FDSOI, but are still lagging behind the bipolar devices offered in SiGe BiCMOS processes. However, in the range of applications in the 28-86 GHz range, both CMOS and SiGe BiCMOS are attractive because they offer sufficient RF performance in many areas and are comparably cheaper than III-V competitors. As the next generation of wireless communications systems are already actively researched, technologies for D-band (110 to 170 GHz) operation are being identified. New substrate and processing technologies such as radio-on-glass have been demonstrated and offer good performance with BiCMOS devices. Moreover, the ubiquitous and ever-increasing complex nature of integrated digital processing and software-defined radio means that a very high premium is placed on analog and digital integration.

The circuit-level findings of this paper can be summarized as follows. Passive component performance is highly dependent on the specific process technology. Some questions need to be asked in this case, related to characteristics such as TSV and the details of the metal layer build in the process BEOL. Consequently, most modern IC manufacturers offer advanced features as part of their standard processes.

Power amplifiers perform remarkably similarly in both focus technologies, where the only area where SiGe devices have a slight advantage is modulation performance, as quantified by the average efficiency curve shown in Figure 4. Circuit designers often rely on unique techniques to improve output power and efficiency. For example, the low breakdown voltages of CMOS transistors (especially in FDSOI technology) are well suited for vertical stacking. On the other hand, BiCMOS transistors can be operated beyond their B_{VCBO} limits, and increased output power is achieved with higher supply voltages.

Si LNAs follow a similar trend, with little difference between reported SiGe and CMOS designs. Below 100 GHz, CMOS LNAs tend to offer better noise figures and lower power consumption. However, SiGe LNAs can achieve better gain, around 5-10 dB for a wide frequency range. However, low breakdown voltages and the resulting reduction in supply voltages provide an advantage to CMOS processes for A/D converters. Since advanced RF CMOS and aggressively scaled FDSOI devices can achieve excellent sampling rates, they can achieve better power consumption than SiGe, primarily because of reduced sampling rates.

Moreover, dynamic range and sampling rate performance is also excellent, especially in more advanced CMOS nodes. D/A converters and power DACs tend to perform similar to their PA counterparts, with the added factor of the bandwidth of the digital interface that must be accounted for. Both Si-based process families are advantageous in this regard, as high-performance digital blocks are significantly easier to integrate with the converter front-end.

Finally, transceiver performance and characterization is highly application dependent. This paper primarily focuses on 802.11ad/ay WiGig and 5G beamforming transceivers. These are an amalgamation of circuit building blocks and give a good perspective on the overall viability of a particular technology. Given that these two application areas operate at relatively lower frequencies (the 28, 39, and 60 GHz bands), less of a premium is placed on RF performance, compared to E-band and D-band systems. As such, other characteristics come into play, such as digital integration, antenna-on-package capabilities, and overall power consumption. Some good solutions have been reported in even moderately scaled Si processes, highlighting their migration into the mainstream as formidable competitors for III-V technologies.

Ultimately, the success of each design (component, circuit, or system level) will depend heavily on the ability to understand and leverage the intricacies of the process technology, which becomes increasingly difficult as processes become more complex. With their generally cost-effective offering of good RF performance and integration potential, substantial improvements in substrates, and device reliability, the future of Si technologies is bright.

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