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RESEARCH ARTICLE

A Component Level Digital Twin Model for Power Converter Health Monitoring

ANDREW J. WILEMAN[1], SOHAIB ASLAM[1], AND SURESH PERINPANAYAGAM[2]
[1]Integrated Vehicle Health Management (IVHM) Center, Cranfield University, MK43 0AL Cranfield, U.K.
[2]School of Physics, Engineering and Technology, University of York, YO10 5DD York, U.K.

Corresponding author: Suresh Perinpanayagam (suresh.perin@york.ac.uk)

ABSTRACT The proliferation of Power Electronic Converters (PECs) has had a pervasive affect in a variety of industries including the power generation, automotive and aerospace sectors, where their use brings reliability to the forefront, especially in applications where safety critical and harsh environments are experienced. Continuous improvements in the power density and efficiency through extensive research into new semiconductor technologies, passive components, circuit topologies and control methodologies has seen the performance of PECs improve indubitably. However, the manifestation of stresses occurring from significant heating due to high currents and switching frequencies; which over time can cause degradation in the performance of PEC components is still a real concern. This paper outlines a methodology for monitoring the degradation of PECs over the operational lifetime by utilizing a component level, physics based Digital Twin (DT). As well as providing a methodology for the real time comparison of parameters to realize the onset of faults subjected to operational stresses, the DT also provides a novel method of training a classifier by simulating the faults within the PEC, a process that in reality, would be difficult to achieve from a physical device. Feature extraction is via Wavelet Scattering and classification is provided using a Support Vector Machine (SVM) approach. The overall approach is one that is novel and expandable to a wide range of PEC topologies and will be beneficial to the optimization and maintenance of PECs in a variety of platforms.

INDEX TERMS Digital twin, power electronics, reliability, power system simulation, real-time systems, health monitoring, PHM, wavelet scattering, support vector machine.

I. INTRODUCTION

The proliferation of power electronic converters (PECs) has had a pervasive affect in a variety of industries and applications in recent years. Continuous improvements in the power density and efficiency through extensive research into new semiconductor technologies, passive components, circuit topologies and control methodologies has seen the performance of PECs improve appreciably. However, the replacement of traditional fossil fuel power generation technologies with renewables such as wind and solar, and their increased adoption by the automotive and aerospace sector brings reliability to the forefront, especially in safety critical and harsh environments [1].

Improvements in the understanding of why power components fail through analytical analysis has resulted in the development of improved design methodologies, such as design for reliability (DFR) [2], enabling the implementation of robustness and reliability in the PEC at the conception and design stages. Reliability in the field is confirmed through accelerated testing [3] and condition monitoring [4], [5], ensuring the PEC will perform to designed specifications throughout its lifetime. More recently, prognostics and health management (PHM) methodologies have permitted the evaluation of a system's reliability through monitoring the health of components, thereby enabling the prediction of its remaining useful life (RUL) by assessing the extent of deviation or degradation from its expected state of health in its operational usage conditions. Such prognostic information facilitates decisions related to safety and condition-based maintenance, ensuring adequate inventory and product life extension to be inferred [6].

A fundamental problem in any PHM methodology is the accurate modelling of failure behaviour. Traditionally, the

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models fall into two main categories, physics of failure (PoF) model based, and those derived from data [7]. Data driven approaches are comprised of often large, previously acquired data sets, and require limited domain knowledge. Data driven models tend to be tailored to the application, making transference between systems, with different operational parameters from its derivation, difficult.

PoF approaches are, in essence, derived from an understanding and ability to develop a mathematical model from the physical principles, conservation laws, and/or phenomenological behaviors of the failure mechanism [8]. PoF models offer transference between systems but can be complex and computationally expensive. In many cases, the details of failure mechanisms remain unclear. The derivation of robust models, often using the structure of a model, with reliance on data analysis aims to refine the models structure and determine values or related parameters to make robust predictions [9].

A more efficient concept increasingly adopted by researchers and industry, in a variety of applications, is the Digital Twin (DT). A DT can be defined as a virtual representation of a physical asset enabled through data and simulators for real-time prediction, optimization, monitoring, controlling, and improved decision-making [10]. The DT methodology provides a platform for performing testing, diagnostics and prognostics. It has seen wide adaptation in areas such as the manufacturing, aerospace, healthcare and automotive industries; [11] and [12] are a recent review of DT methods, challenges, and applications in these fields. Although DTs are successfully incorporated in production and design applications, the primary focus for DT usage is PHM.

Recently, proposals for application of digital twinning for power system and power electronic systems have started to gain ground in academia. Reference [13], proposes a new approach to the future of power distribution control centers based on dynamically mirroring the system state by digital twinning. Reference [14], provides a framework and potential applications of DTs to the management of equipment energy consumption within the manufacturing shop floor. Zhou et al. [15] proposed the use of DTs of power grids, using online analysis digital twins to reduce time for analysis of large power grids and operational decision making. Felsberger et al. [16] proposed the use of a DT based on a general model of system failure behaviour to maintenance optimization by combining existing methodologies into a general framework. Applying it to a real-world power converter use case, they were able to identify either reactive or preventive maintenance to be more cost-effective depending on the operating conditions; allowing for the prediction of optimal maintenance for existing and future systems.

Work on system level applications to power electronics is at present, small. Jain et al. [17] proposed an application- specific example of DTs for fault diagnostics of photovoltaic-based systems containing power converters. With [18] proposing a novel methodology to predict the remaining useful life of an offshore wind turbine power converter in digital twin framework, as a means of predictive maintenance strategy. The remaining useful life is estimated for both diagnostic and prognostic health monitoring, specific to the offshore operating environment.

Reference [19], proposed an approach for the online diagnostic analysis of power electronic converters utilizing real-time, probabilistic digital twinning. Under this approach, a DT of a power converter is defined as a real-time, probabilistic simulation model with stochastic variables, developed using a generalized polynomial chaos expansion. A non-invasive, health indicator estimation method based on the DT concept is proposed by [20] aiming for condition monitoring of power electronic converters. Application to a Buck DC-DC converter is demonstrated and a particle swarm optimization algorithm is applied to estimate the unknown circuit parameters from both the digital twin and the physical prototype. Observation of the degradation trends in key components, such as capacitors and MOSFETs is presented. Reference [21], again, uses a DC-DC converter to examine the degradation characteristic parameters. The capacitance, inductance, parasitic resistance and MOSFET on-state resistance being selected; identification is based on Bayesian optimization. A new approach for creating real-time models of power electronic converters using Dynamic Neural Networks (DDNs) is proposed in [22]. The models are time-domain, switch-averaged, large-signal, real-time, and embeddable, which may be used to create digital twins of the converter that can run on any platform, including locally on the converter's digital controller.

The primary focus of this paper is to develop a DT methodology for condition monitoring and classification of wear out and degradation in PECs over a long period of operational use. This is mainly due to the manifestation of stresses occurring from significant heating due to high currents and switching frequencies; which over time can cause degradation in the performance of PEC components. Detection methodologies for measuring the onset of these failure modes are well documented and also mentioned later in this paper. However, a fundamental problem exists in gathering sufficient failure data to successfully train a classifier to recognise these faults in the field.

Collection of field and lab based accelerated testing data goes some way to solving this problem, Fig 1. Repeated accelerated testing and collection of data over time, however, is both expensive and time consuming, with no guarantee of sufficient data being obtained to classify all faults or combinations of faults occurring in the PEC.

The solution proposed is to implement a DT of the PEC from accurate physics-based modelling of the active and passive components and associated thermal management strategies. An array of fault combinations can then be implemented within the components, and combined, with real time data, used to train the classifier via the anomalies in the PECs output.

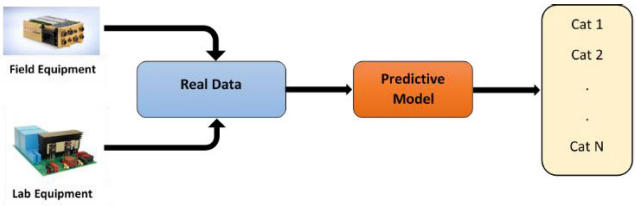


FIGURE 1. Classification of faults from field and accelerated test data.

Section II outlines the methodology in detail, and the proposed faults for demonstration are discussed in Section III. Section IV outlines the composition of the DT with Section V and VI describing fault simulation and the detection of faults, respectively. Feature extraction via Wavelet Scattering and classification using a Support Vector Machine (SVM) are discussed in Section VII and VIII. Finally, Section IX and X, respectively, report the results obtained and concludes with a discussion and proposed further work. To the authors' knowledge, as far as to the application, this approach is novel and will be beneficial to the optimization and maintenance of PECs.

II. METHODOLOGY

Numerous authors have explored fault classification in power electronics converters (PECs) [23], [24], [25]. The proposed methodology in this article for utilizing a digital twin (DT) for health monitoring and classification is outlined in figure 2, below.

Figure 2, utilizes the consolidated data comprising user-defined model/data specific to certain test cases; and/or environmental model/data, which describe the operational environment of the PEC. This is stored in the operational and test results databases, respectively. Additionally, historic simulation and highly representative reliability testing data, if available, are also combined with synthesized data from the DT. This synthesized data is used to supplement the real data in helping to develop an all-encompassing predictive model. From this model, the identification of key engineering features enables symptom vectors representing the health of the PEC to be identified and extracted.

The DT of the PEC feeds synthesized data providing two main benefits. First, a synthesized physical response from the DT helps to develop the classification model. Particularly when in the real PEC, certain fault conditions or degradation would be hard to observe, the DT is used to generate these fault conditions via simulation and inform the development of the classification model. Secondly, having a physical simulation provides an output that can be run in parallel with the real data. A 'snapshot' comparison of the two responses allows any divergence between them, indicating potential degradation to be realized. Hence, allowing trend monitoring, event detection and condition monitoring, as well as classification and prognostics to be supported via the diagnostic engine. Coupling with a decision support and reasoning system allows for case-based reasoning and asset maintenance planning to be carried out.

III. FAILURE MODES

This section outlines failure modes commonly experienced in PECs. The understanding of these faults enables them to be emulated in the DT. Extensive industry surveys of failures undertaken in assessing the reliability of power conditioning devices [1], [5], [26], report at the component level, semiconductor-switching devices e.g., Insulated Gate Bipolar Transistors (IGBTs) and capacitors as the crucial reliability-critical components. Temperature, vibration, and humidity are the three major environmental stressors that directly or indirectly induce failure in these power electronic components.

Switching between multiple states of operation, the high currents and switching frequencies experienced, lead to significant Joule heating and switching losses in the PEC. Failure to mitigate this heating by suitable cooling strategies, results in large temperature swings, which induce stresses due to the large mismatches between the CTE (coefficient of thermal expansion) of materials used within the device, and thus significantly reduce the operational lifetime. Bond wire detachment and solder delamination in the die are amongst the main causes of failure in power switches such as IGBTs [8], [26].

Passive components, such as capacitors and inductors are also prevalent in PECs. Capacitors are extensively used in applications such as DC links for balancing the instantaneous power difference between the input source and the output load, AC filtering, DC filtering, and along with inductors, for energy storage [27]. Capacitors especially suffer from reliability issues during their operational lifetime, such as electrolyte vaporization and dielectric film breakdown to name but a few [5].

Table 1 below, outlines the failure modes being monitored for in this paper, along with the respective health indicator. In general, a device is deemed to be undergoing critical failure when it deviates >20% from the nominal operational value [28]. Figure 3 outlines the position of the two IGBT based faults.

A. BOND WIRE FAILURE

The cause of mechanical bond-wire failures is twofold, namely heel cracking and lift-off, as illustrated in Figure 4 (a & b), respectively.

A typical power electronic module can contain hundreds of bond wires, which are instrumental in making the interconnection from the power substrate to the power devices, power substrate to the external connections and between the power devices within the module.

The bond wires are typically aluminium, but copper wires are becoming common in some applications [4]. Shear stresses set up between the bond wire and bond pad contribute to bond wire fatigue through repeated flexing of the bond wire, which eventually leads to detachment or cracking. Bond

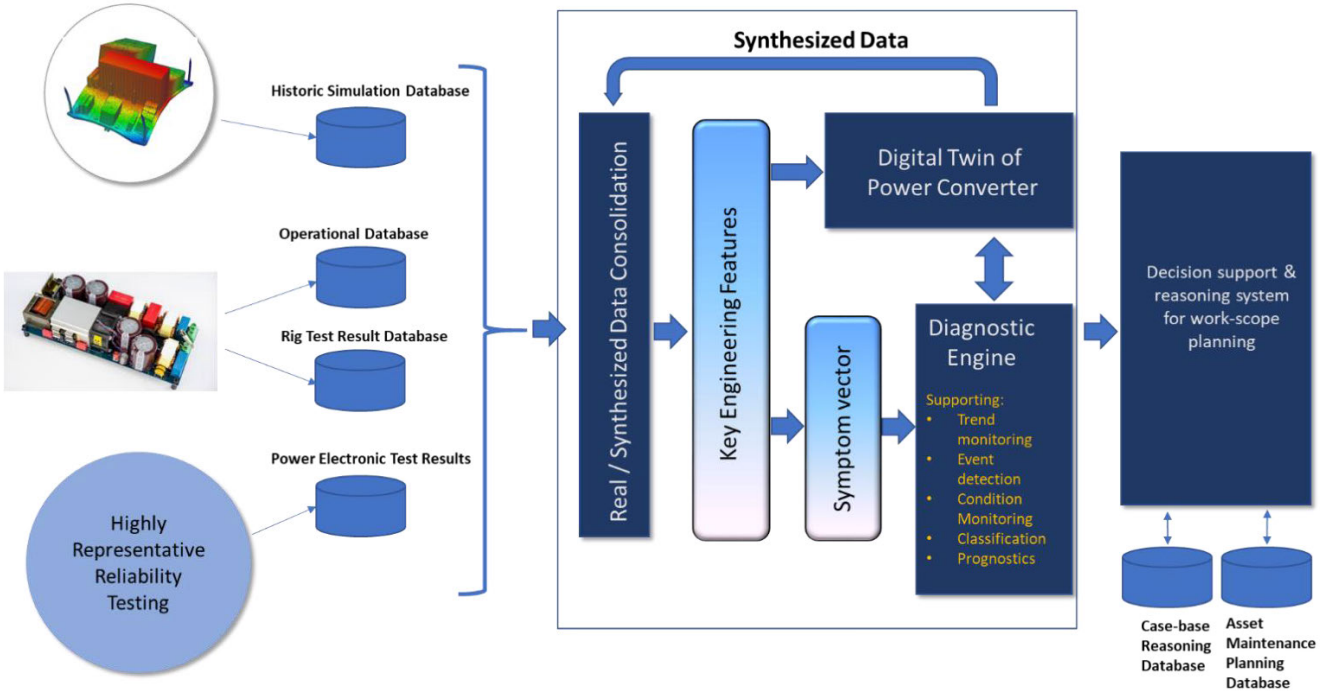


FIGURE 2. Outline of the proposed methodology.

TABLE 1. Failure modes for IGBTs and electrolytic capacitors.

Component	Fault Condition	Failure Mode	Health Indicator
IGBT	• Bond Wire Failure	• Flexing of the bond wire, which eventually leads to detachment or cracking	• Increase in V_{CE_sat} (may develop into open circuit) 20% increase [28,29]
	• Solder Delamination	• Solder fatigue and cracking between the module substrate and base plate or the device chip and the substrate	• V_{CE} has risen by 2 – 3% and R_{th} has risen by 20%. • Output harmonics [28, 30]
Capacitor (Electrolytic Aluminium)	• Open Circuit	• Dielectric breakdown • Terminal disconnection	• Increase in capacitor ripple voltage > 20% [29]
	• Short Circuit	• Dielectric breakdown of oxide layer	• ESR (20% reduction) [30, 31]
	• Wear out	• Electrolyte vaporization (e.g. degradation of oxide layer, anode foil capacitance drop	

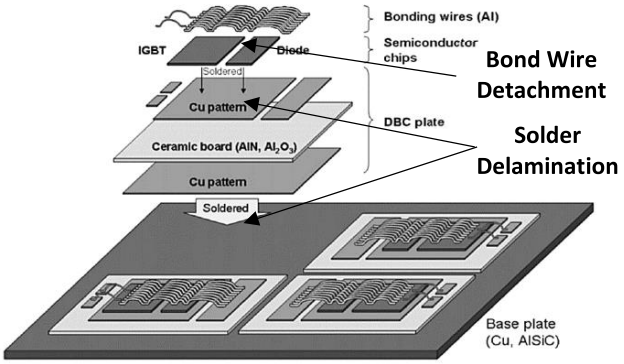


FIGURE 3. Location of bond wire and solder delamination faults in an IGBT.

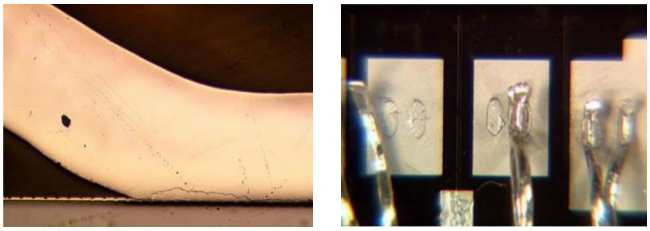


FIGURE 4. (a) Wire-bond cracking and (b) ultimate lift-off as a result of thermo-mechanical fatigue during power cycling [4].

wire lift-off, caused by the differences in the coefficient of thermal expansion (CTE) of the aluminium bond wire and silicon substrate, sets up a difference in strain, which in turn causes stress at the material interface. This resulting stress is temperature dependant. Over time, the resulting stress-strain hysteresis energy initiates crack propagation, which is a function of the temperature cycle during operation [4].

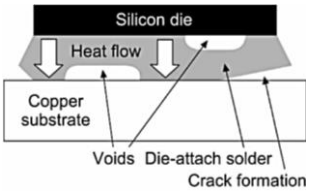


FIGURE 5. Cracking and void formation in die-attach solder [38].

Heel cracking of bond wires, again occurs due to thermo-mechanical effects.

Package or module encapsulation plays a role in bond wire heel cracking; however, the lift-off failure mechanism tends to dominate with heel cracking being rarely observed in modern advanced IGBT multichip power modules [32].

Bond wire lift-off is detectable by measuring $V_{CE,sat}$ under low I_C conditions. The criteria used to detect bond wire failure was a +5% increase in $V_{CE,sat}$ [33]. However, other failure mechanisms may also contribute to rise in $V_{CE,sat}$ [34].

B. SOLDER DELAMINATION

Solder fatigue occurs in soft solders, but not hard solders. Despite this, soft solder is employed for several different reasons [35]. The low reflow temperature avoids damage to sensitive components, having reasonable thermal and electrical resistivity, and displaying at least a modest level of chemical inertness. The high ductility prevents build-up of mechanical stresses in the package, relieved by plastic flow, hence reducing the changes of catastrophic package failure due to chip or other component fracture.

For an IGBT, as shown in Figure 3, the direct copper-bonded (DCB) substrate, comprised of ceramic and metallized copper films, is attached to the copper base plate by the solder layer. The IGBT chip is soldered onto the DCB substrate and the chip surface is connected to copper tracks via aluminium wire bonds, with the whole assembly housed in a plastic case and encapsulated with silicone gel [36].

For power modules, a major cause of failure is the solder fatigue and cracking between the module substrate and base plate or the device chip and the substrate [37], [38]. Again, differences in the CTE between the silicon die and copper substrate sets up shear stresses in the solder layer, which in turn, eventually cracks (voids), Figure 5. Due to the voids, reduction in effective area allowing heat to escape from the die by conduction causes an increase of temperature; the process leads to a thermal runaway. Ultimately, due to the localization of the heating, damage may result to the chip [36].

C. ELECTROLYTIC CAPACITOR FAILURE

The health of an electrolytic capacitor is strongly affected by its operating conditions. These include parameters, such as voltage, current, frequency, and ambient temperatures among others. In DC–DC power converters the degradation of capacitors increases the resistive component and decreases the capacitive component of the impedance in the AC path, which results in an increase in the ripple voltage magnitude superimposed on the desired DC voltage [39].

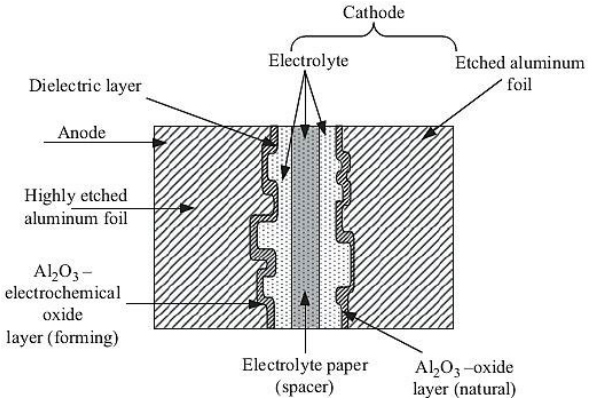


FIGURE 6. Cross-sectional details of internal capacitor structure [40].

A detailed view of the cross section of the electrolytic capacitor structure is presented in Figure 6. The etched anode and cathode plates are anodized by coating them with a thin aluminium oxide layer on the surface of the foil. This layer of aluminium oxide acts as the dielectric (insulator) and serves to block the flow of direct current between anode and cathode foil surface [40].

Electrolytic capacitor failures tend to be one of two types: Firstly, catastrophic failures, where there is complete loss of functionality, primarily short and open circuits, and secondly, degradation failures, where there is gradual deterioration of capacitor parameters due to accumulated internal damage. The primary reason for degradation in electrolytic capacitors is the deterioration of electrolyte quality, decrease in electrolyte volume due to evaporation, and weakening of the oxide layer, due to increased temperatures in the capacitor core [39], [41]. These degradation phenomena cause a drift in the two main electrical parameters of the capacitor: firstly, the equivalent series resistance (ESR) and secondly, the capacitance (C). The health of a capacitor is typically measured by the values of these two parameters. For the fault parameter in this paper, ESR, has been chosen, as the change relates directly to output voltage. ESR can be derived from the sum of two component resistances, Figure 7a, $ESR = R_C + R_E$. R_C remains relatively constant and R_E increases as the capacitor degrades, which can be attributed to the evaporation (i.e., decrease) of the electrolyte [42]. Where R_C is the combined series resistance of the mounting lugs, cathode and anode foils, respectively, which remains almost constant since it is a combination of the resistances attributed to mechanical aspects of the capacitor that do not change much over the life of the capacitor.

R_C and R_E are combined to define the overall degradation resistance, ESR, as summarized in Figure 7b. Hence, ESR manifests itself as an increase in the output voltage across the capacitor.

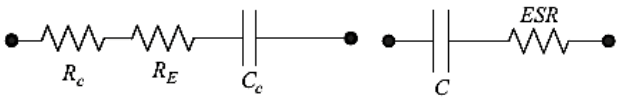


FIGURE 7. a & b. Simplified lumped parameter and lumped parameter ESR electrical models, respectively.

IV. COMPOSITION OF THE PEC DIGITAL TWIN

A digital twin constitutes three main requirements. Firstly, a model of the application it represents, in this case the PEC itself. Secondly, an evolving set of data relating to the application, based upon real time measurements at the output of the PEC, and lastly, a means of dynamically adjusting or updating the model in accordance with new data is required [43]. This opens up a discussion as to which is the best model to use to represent the PEC. The model should produce results, which are directly comparable to the measured parameters and will likely incorporate external measurements such as user defined data or environmental stressors (hence, the model updating process is data-driven). The main attribute of the DT concept is, by using evolving data, it provides an updated and accurate portrayal of how the modelled application changes with time. The model should not only be capable of providing a snapshot of the behaviour at an instance in time, but also be capable of making predictions over the operational life of the PEC taking into account operational degradation.

A DT may be comprised of any sort of model as long as it presents an acceptably accurate representation of the physical twin. The trade-off required is computational overhead versus instantaneous operation and accuracy. Ideally, the DT would use models derived directly from physics that take all phenomena likely to affect the quantities measured and updated into account, with no latency [43]. In the application presented in this paper, accuracy has been retained by using a physics-based simulation via Simscape® Electrical to model the DT, at the cost of operational time. This is justified, as the faults monitored are long-term degradation of components and hence the period for updating the DT is hours rather than seconds. This, in general, is the case for predictive maintenance applications where a DT is used to schedule maintenance; as the period for decisions will generally be hours/days and hence physics-based modelling is justified.

A digital twin without a physical twin is a model! In this case, the physical twin is the TRENCHSTOP™ 5 TO-247 4 pin Evaluation Board by Infineon [44] developed to be a simple but accurate test bench for evaluating IGBTs from the same manufacturer, however it could be any PEC circuitry. In many industrial applications, it is required to convert a fixed-voltage DC source into a variable-voltage DC source. From the basic topology, it is possible to configure the board as a step-down or step-up DC-DC converter. Figure 8, shows the experimental set-up used. The Step-Up or Boost converter provides an output voltage, which is greater than the input voltage – hence the name ''Boost'' [45]. For the Boost

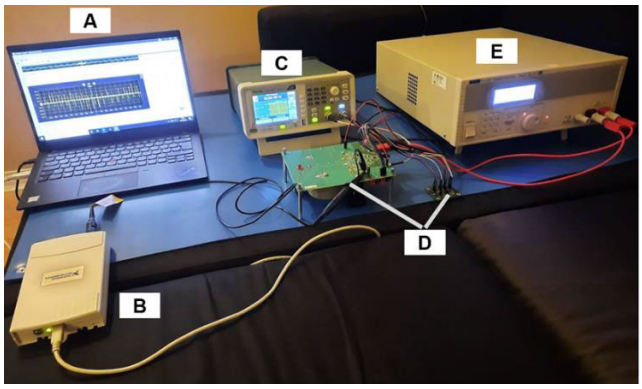


FIGURE 8. The physical twin set up – A. Computational Platform with Data Acquisition, B. 5133 NI Oscilloscope, C. Arbitrary Function Generator (PWM), D. Evaluation Board, E. Variable High Precision Power Supply.

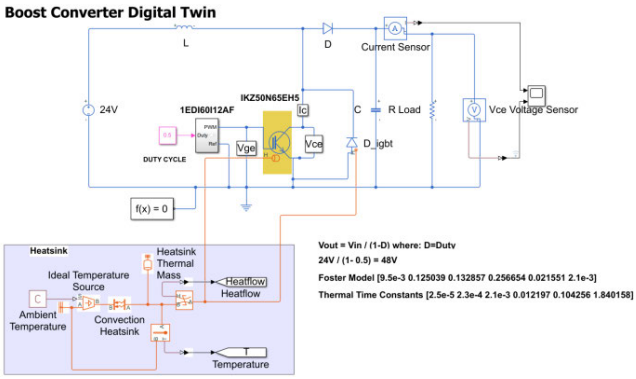


FIGURE 9. Digital Twin representation of the TRENCHSTOP™ 5 evaluation board.

converter digital twin, a 24V input voltage V_s and average output value, V_a of 48V, at a switching frequency f of 20 KHz, with a duty cycle of 0.5. The value of the inductance L is 250μH and the capacitance C is 220μF, being driven into a 20 Ω load.

The digital twin in Figure 9 represents the physical evaluation board in the step-up configuration complete with the heatsink. The output from the digital twin is shown in Figure 10 with zero mean white Gaussian noise $n \sim N\left(0, \sigma_n^2\right)$ superimposed on the output. The composition of the main components comprising the digital twin, namely the IGBT, diodes, capacitor, thermal parameters and heatsink are discussed in detail in sections A – F, respectively.

A. IGBT DEVICE MODEL

An IGBT combines the advantages of the Bipolar Junction Transistors (BJT) and Metal–Oxide–Semiconductor Field-Effect-Transistor (MOSFET). The N-Channel IGBT circuit symbol shown below in Figure 11(a) with Figure 11(b) being the equivalent circuit consisting of a PNP Bipolar Transistor driven by an N-Channel MOSFET.

The MOSFET model used in this work are threshold-based equations based on the Shichman-Hodges model, as shown in Figure 12a [46].

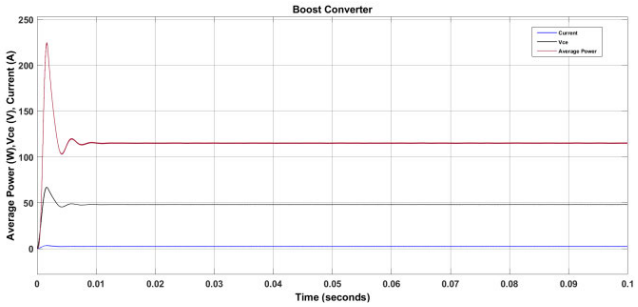


FIGURE 10. Output from digital twin with zero mean Gaussian noise.

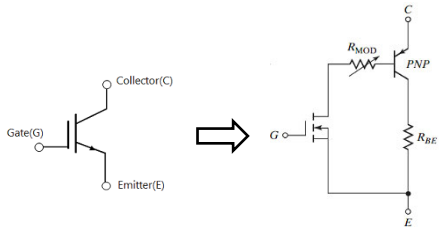


FIGURE 11. a) IGBT circuit symbol. b) equivalent circuit.

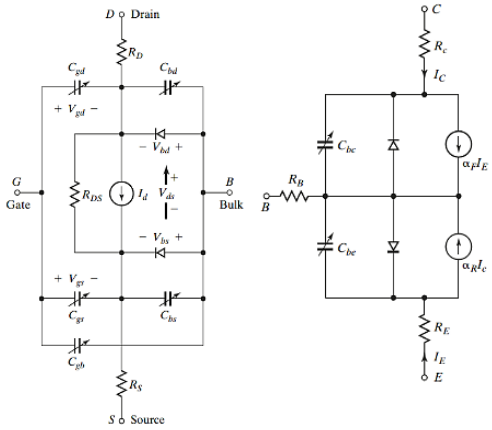


FIGURE 12. a) The Shichman-Hodges model representation and b) the Ebers-Moll that are used in the composition of the IGBT.

The drain-source current, I_{DS}, depends on the region of operation. In the off region ($V_{GS} < V_{th}$), the drain-source current is:

$$I_{DS} = 0 \tag{1}$$

In the linear region ($0 < V_{DS} < V_{GS} - V_{th}$), the drain-source current is:

$$I_{DS} = K\left(\left(V_{GS} - V_{th}\right)V_{DS} - V_{DS}^2/2\right)\left(1 + \lambda\left|V_{DS}\right|\right) \tag{2}$$

In the saturated region ($0 < V_{GS} - V_{th} < V_{DS}$), the drain-source current is:

$$I_{DS} = (K/2)\left(V_{GS} - V_{th}\right)^2\left(1 + \lambda\left|V_{DS}\right|\right) \tag{3}$$

where, K is the transistor gain, V_{DS} is the positive drain-source voltage, V_{GS} is the gate-source voltage and V_{th} is the

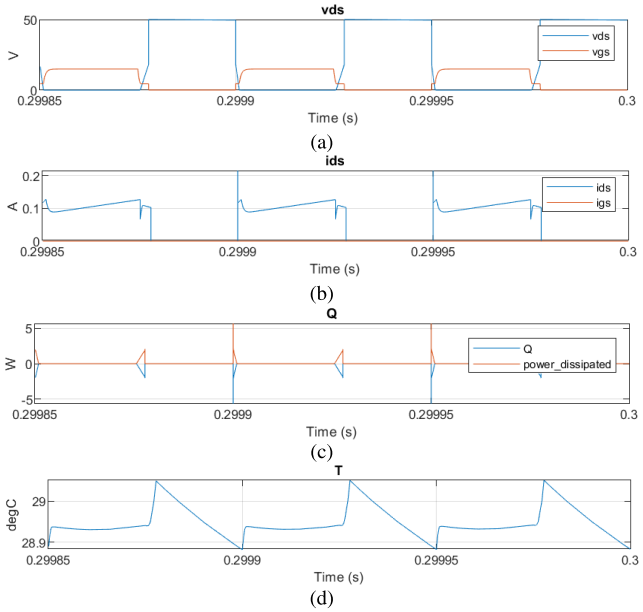


FIGURE 13. a. Voltage across the Drain and Source in the MOSFET. b. Drain Source and Gate Source currents in the MOSFET. c. Power and Heat Flow Q in the MOSFET. d. Junction temperature in the MOSFET.

threshold voltage, respectively. The simulated device parameters are shown in figure 13 a-d, respectively.

A variant of the Ebers-Moll equations is used to represent the PNP bipolar transistor. The equations are based on two exponential diodes coupled with two current-controlled current sources, as shown in Figure 12b. The model incorporates Early voltage affect, base, collector, and emitter resistances as well as optional fixed base-emitter and base-collector capacitances [47]. The collector and base currents are:

$$I_C = -IS\left[\left(e^{-qV_{BE}/kT_{m1}} - e^{-qV_{BC}/kT_{m1}}\right)\left(1 + \frac{V_{BC}}{V_A}\right) - \frac{1}{\beta_R}\left(e^{-qV_{BC}/kT_{m1}} - 1\right)\right] \tag{4}$$

$$I_B = -IS\left[\frac{1}{\beta_F}\left(e^{-qV_{BE}/kT_{m1}} - 1\right) + \frac{1}{\beta_R}\left(e^{-qV_{BC}/kT_{m1}} - 1\right)\right] \tag{5}$$

where, I_B and I_C are base and collector currents, defined as positive into the device. I_S is the saturation current, V_{BE} is the base-emitter voltage and V_{BC} is the base-collector voltage, respectively. β_F and β_R are the ideal maximum forward and reverse current gains, V_A is the forward Early voltage, q is the elementary charge on an electron ($1.602176e^{-19}$ Coulombs), k is the Boltzmann constant ($1.3806503e^{-23}$ J/K) and T_{m1} is the transistor temperature, as defined by the measurement temperature parameter value.

The internal n-channel circuit IGBT, can be implemented as a composite model connecting the existing PNP-BJT and n-channel MOSFET spice models. This has proven reliable with an acceptable computational overhead; however, neglects the accuracy of the IGBT behaviour. The static and dynamic device characteristics are dominated by parameters

such as internal carrier and charge effects that must be taken into account to simulate the device behaviour accurately. Equation based models [48], [49] implement physics-based equations derived from semiconductor physics theory. The increased complexity of the model however, means it can be computationally intensive.

Modelling of the drain-to-gate capacitance of the n-channel MOSFET, dynamic electrical properties have been found to be a major source of inaccuracy. During high-voltage switching, the drain-to-gate capacitance C_{dg} changes by two orders of magnitude due to any changes in drain-to-gate voltage V_{dg}. C_{dg}, is expressed by:

$$C_{dg} = \frac{\epsilon_{si} C_{oxd}}{\sqrt{\frac{2\epsilon_{si} V_{dg}}{qN_B}} C_{oxd} + A_{dg}\epsilon_{si}} \tag{6}$$

where, A_{dg} is the area of the gate over the base; ϵ_{si} is the dielectric constant of silicon; C_{oxd} is the gate–drain overlap oxide capacitance; q is the electron charge; N_B is the base doping density.

The MOSFET source is connected to the bipolar transistor collector, and the MOSFET drain is connected to the bipolar transistor base as depicted in Figure 11b. The MOSFET uses the threshold-based equations and the bipolar transistor uses the equations 4 & 5, but with the addition of an emission coefficient parameter N that scales kT/q.

The N-Channel IGBT uses the on and off characteristics specified to estimate the parameter values for the underlying N-Channel MOSFET and PNP bipolar transistor. As well as the off characteristics to calculate the base-emitter voltage, V_{be} and the saturation current, I_s. When the transistor is off, the gate-emitter voltage is zero and the IGBT base-collector voltage is large, so the PNP base and collector current equations simplify to:

$$I_b = 0 = -I_s \left[\frac{1}{\beta_F} \left(e^{-qV_{be}/(NkT)} - 1 \right) - \frac{1}{\beta_R} \right] \tag{7}$$

$$I_c = -I_s \left[e^{-qV_{be}/(NkT)} \left(1 + \frac{V_{bc}}{V_{AF}} \right) + \frac{1}{\beta_R} \right] \tag{8}$$

where, N is the Emission coefficient N parameter value, V_{AF} is the forward Early voltage, and I_c and I_b are defined as positive flowing into the collector and base, respectively.

Equation 7 can be solved for V_{be}. The base current is zero in the off-condition, and hence $I_c = -I_{ces}$, where I_{ces} is the Zero gate voltage collector current. The base-collector voltage V_{bc}, is given by $V_{bc} = V_{ces} + V_{ces}$, where V_{ces} is the voltage at which I_{ces} is measured. Hence, equation 8 can be re-written as follows:

$$I_{ces} = I_s \left[e^{-qV_{be}/(NkT)} \left(1 + \frac{V_{ces} + V_{be}}{V_{AF}} \right) + \frac{1}{\beta_R} \right] \tag{9}$$

β_R and β_F are set to typical values of 1 and 50, so these two equations can be used to solve for V_{be} and I_s:

$$V_{be} = \frac{-NkT}{q} log \left(1 + \frac{\beta_F}{\beta_R} \right) \tag{10}$$

$$I_s = \frac{I_c}{e^{-qV_{be}/(NkT)} + \frac{1}{\beta_R}} \tag{11}$$

The collector-emitter saturation voltage $V_{ce(sat)}$ and collector current at which $V_{ce(sat)}$ is defined are used to determine $V_{be(sat)}$ by solving the following equation:

$$I_{ces(sat)} = I_s \left[e^{-qV_{be(sat)}/(NkT)} \left(1 + \frac{V_{ces(sat)} + V_{be(sat)}}{V_{AF}} \right) + \frac{1}{\beta_R} \right] \tag{12}$$

The MOSFET gain K, is calculated using the following equation:

$$I_{ds} = I_b = K \left[\left(V_{GE(sat)} - V_{th} \right) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{13}$$

where, V_{th} is the Gate-emitter threshold voltage, $V_{ge(th)}$ parameter value and $V_{GE(sat)}$ is the Gate-emitter voltage at which $V_{CE(sat)}$ is the defined parameter value. V_{ds} is related to the transistor voltages as $V_{ds} = V_{ce} - V_{be}$. Substituting this relationship in (13), for V_{ds}, sets the base-emitter voltage and base current to their saturated values, and rearranges the MOSFET equation to give:

$$K = \frac{I_{b(sat)}}{\left[\left(V_{GE(sat)} - V_{th} \right) \left(V_{be(sat)} + V_{ce(sat)} \right) - \frac{\left(V_{be(sat)} + V_{ce(sat)} \right)^2}{2} \right]} \tag{14}$$

where $V_{ce(sat)}$ is the collector-emitter saturation voltage, $V_{ce(sat)}$ parameter value.

The primary IGBT parameters are shown in figures 14a-14d respectively.

The internal gate, collector and emitter of the IGBT consist of the physical attachment for the silicon device to the terminals used for mounting the device. Often in larger devices it is comprised of wire bonds and rugged metal terminals, which will have their own resistance. Later on, the bond wire resistance will be one of the parameters used in the failure classification, as simulating a rise in the collector resistance is akin to bond wire failure.

Within the device, this internal resistance is modelled and the parameters across the collector, emitter and gate resistance are shown in figures 15a-c, 16a-c, and 17a-c respectively.

In order to evaluate the IGBT model, the parameters from the data sheet, namely for the Infineon IGBT IKZ50N65EH5 [50] are used. The IGBT is set up in a test circuit configuration for the evaluation in conjunction with the equivalent model for the gate drive 1EDI60I12AF [51], again from Infineon. Connection to a load inductor via the collector as specified in the test instructions provided by the

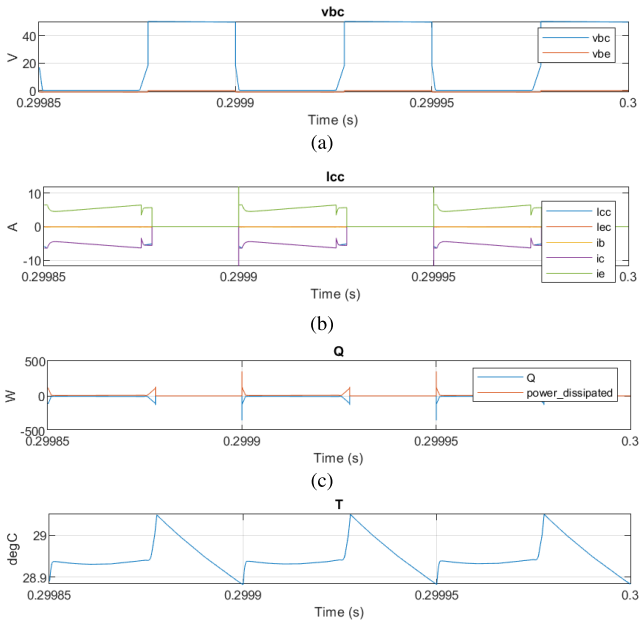


FIGURE 14. a. Voltages v_{bc} and v_{be}. b. Instantaneous currents in the Bi-polar transistor, i_b, i_c and i_e and bias currents I_{cc} and I_{ce}. c. Power and heat flow Q from the Bi-polar transistor. d. Bi-polar transistor internal junction temperature, T_j.

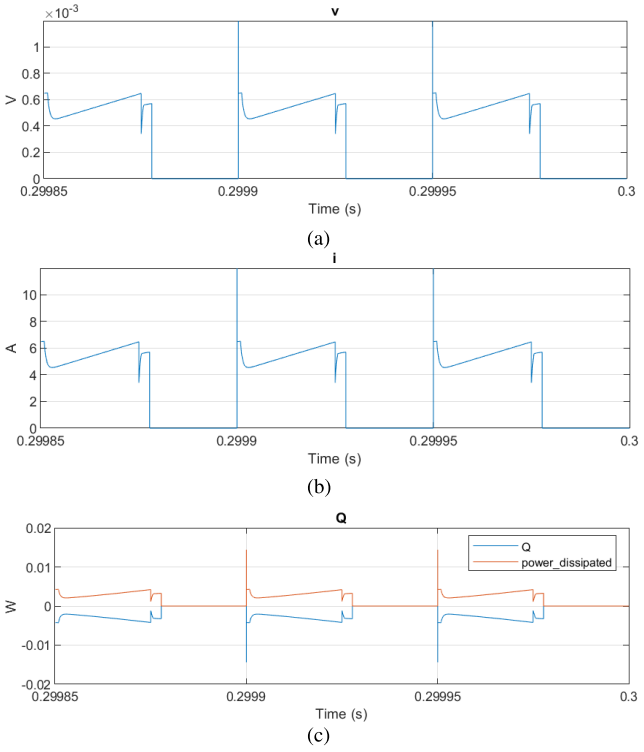


FIGURE 15. a. Voltage across the internal collector resistance. b. Current flow through the collector resistor. c. Heat flow and power dissipated by the collector resistor.

manufacturer is used. As a pre-requisite to matching dynamic characteristics to datasheet values or measured data, initial set-up of the parameters defining the static I-V curve is required.

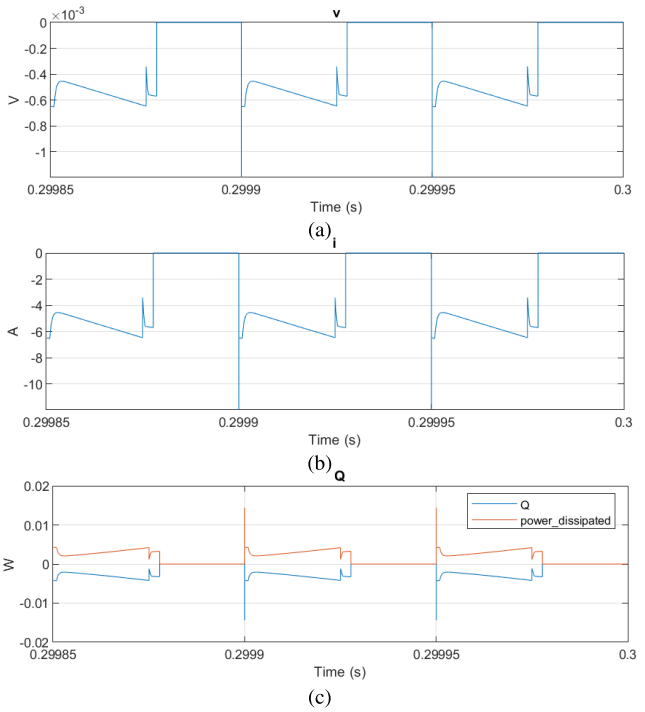


FIGURE 16. a. Voltage across the internal emitter resistance. b. Current flow through the emitter resistor. c. Heat flow and power dissipated by the emitter resistor.

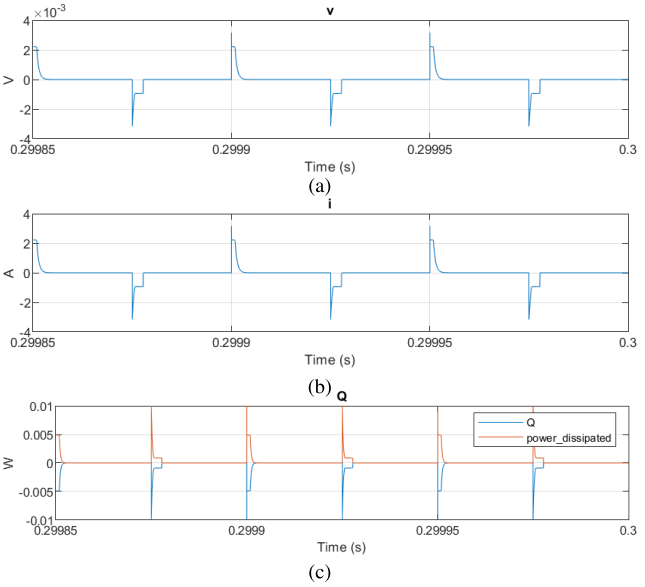


FIGURE 17. a. Voltage across the internal gate resistance. b. Current flow through the gate resistor. c. Heat flow and power dissipated by the gate resistor.

The generation of the I_C versus V_{CE} curves for the IKZ50N65EH5 IGBT [50] transistor defining the vectors of gate-emitter voltages and minimum and maximum collector-emitter voltages for the static parameters are plotted. The plot Figure 18, is compared against the manufacturer's datasheet, to confirm a correct implementation of the

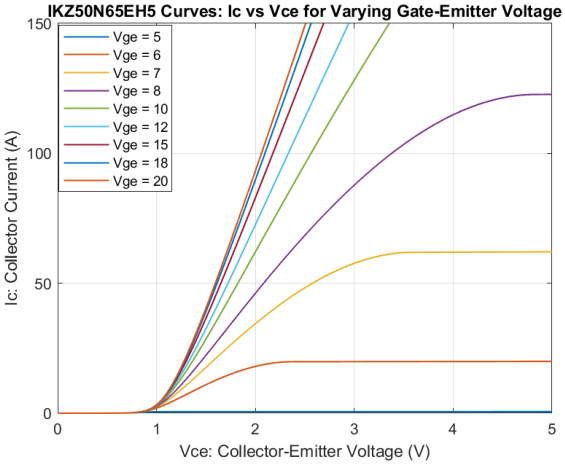


FIGURE 18. I_C and V_{CE} dynamic characteristics from the IKZ50N65EH5 [50].

transistor parameters. The relation of $V_{CE(ON)}$ to temperature is dependent on current and proves important to assessing the junction temperature of the IGBT [52].

B. IGBT DIODE

The IGBT diode is modelled externally in this work; however, in reality, it is integrated inside the IGBT package.

An exponential diode model is used to represent the relationship between the current I through the diode and the voltage V across the diode.

The equations are as follows [45]:

$$I = Is\left(e^{\frac{qV}{NkT_{m1}}} - 1\right) \quad \text{for } V > -BV \tag{15}$$

$$I = -Is\left(e^{\frac{-q(V+V_z)}{NkT_{m1}}} - e^{\frac{qV}{NkT_{m1}}}\right) \quad \text{for } V \leq -BV \tag{16}$$

where: q is the elementary charge on an electron ($1.602176\ e^{-19}$ coulombs), k is the Boltzmann constant ($1.3806503\ e^{-23} J/K$), BV is the Reverse breakdown voltage parameter value, N is the emission coefficient, Is is the saturation current, T_{m1} is the temperature at which the diode parameters are specified, as defined by the measurement temperature parameter value.

For commutation diodes, it can be important to model diode charge dynamics. When a forward-biased diode has a reverse voltage applied across it, it takes time for the charge to dissipate. The time taken for the diode to turn off is captured primarily by the transit time parameter. Once the diode is off, any remaining charge then dissipates, the rate at which this happens being determined by the carrier lifetime.

The diode model of Lauritzen and Ma [53] may be used to capture these effects. The defining equations are:

$$i = \frac{q_E - q_M}{T_M} \tag{17}$$

$$\frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{q_E - q_M}{T_M} = 0 \tag{18}$$

$$q_E = (\tau + T_M)\, i \tag{19}$$

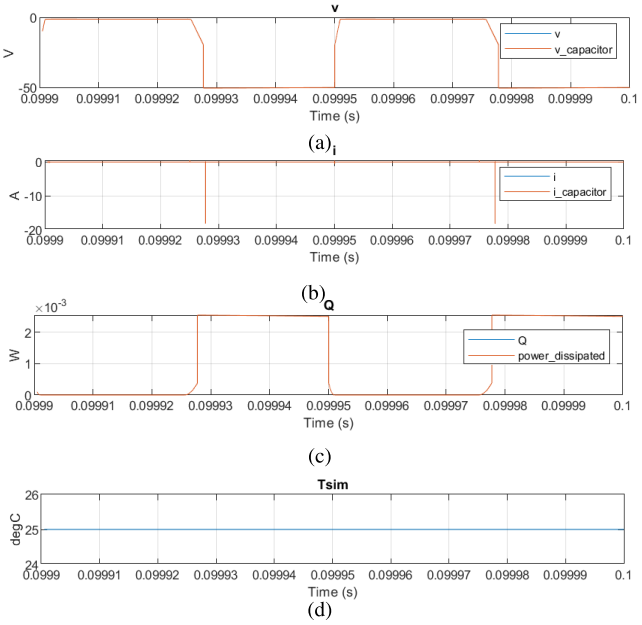


FIGURE 19. a. Voltage across the IGBT Diode. b. Current through the IGBT Diode. c. Power and heat loss from IGBT Diode. d. Temperature of IGBT Diode.

where: i is the diode current, q_E is the junction charge, q_M is the total stored charge, T_M is the transit time, τ is the carrier lifetime.

Data sheets for IGBTs typically quote values for peak reverse current for an initial forward current and a steady rate of change of current. The data usually provides values for reverse recovery time and total recovery charge. The voltage, current and power dissipated as well as the temperature for the IGBT diode is shown below in Figures 19a-d. In terms of the heat loss within the device, compared to the IGBT itself, the losses are very small.

C. THERMAL MODEL

The junction temperature of the device is one of the critical parameters considered in semiconductor selection. The measurement of the junction temperature within the IGBT is not physically possible due to the layout of the device. However, many of the manufacturers are recognizing the significance of being able to monitor junction temperature, and IGBT packages that provide Negative Temperature Coefficient (NTC) thermal sensors are becoming increasingly prolific in devices [54].

Online and offline approaches in literature have been devised that allow the operating conditions for particular power converters to be monitored, resulting in acceptable device temperatures and converter lifetimes. Offline approaches based on calculation and simulation include closed-form analytical calculations of device losses and device temperatures for particular steady-state levels of voltages and currents presented in [55] and [56], equivalent circuit model time-based simulations, or fast Fourier

analysis-based approach presented in [57] which uses thermal equivalent circuit models to greatly reduce simulation time compared with time-based simulation. Manufacturers usually provide thermal equivalent circuit models in their datasheets for the device; based upon experimentation and/or by Finite Element Analysis (FEA) [58], [59].

Strategies for online monitoring of device junction temperatures tend to be based on the measurement of secondary electrical parameters, which vary with temperature such as V_{CE}, or the ringing of the turn-on voltage spike to estimate the device temperature [60]. Although, state estimation by comparison with thermal models, has been also been explored [52].

The primary IGBT losses occur from conduction and energy dissipated from turn-on and turn-off losses, which in turn dominate the thermal operating characteristics of the device.

The common equations for losses are calculated using datasheet values for a given operating point and are provided in manufacturer's application notes and numerous papers including [61], [62].

The instantaneous conduction losses are a combination of the collector current and the collector-emitter voltage, v_{ce}, which is dependent on the collector current, i_c, its zero current collector-emitter voltage, v_{ce0}, and its collector-emitter on-state resistance, r_c as follows:

$$v_{ce}\left(i_c\right) = v_{ceo} + r_c \times i_c \tag{20}$$

From (27), the instantaneous conduction loss for an IGBT as a function of time is given as:

$$P_{cond,IGBT}\left(t\right) = v_{ce}\left(t\right) \times i_c\left(t\right) = v_{ceo} * i_c(t) + r_c \times i_c^2(t) \tag{21}$$

Most manufacturer's datasheets give the values for $v_{ceo}\,(i)$ and i_c along with the energy required for each turn-on and turn-off event at a base level which is used to calculate the switching losses for the device. For the total switching losses, all switching events in a cycle are summed, or may be approximated as an average by multiplying the turn-on and turn-off losses by the switching frequency as follows:

$$P_{sw} = f_{sw} \times \left(E_{on} + E_{off}\right) \tag{22}$$

Manufacturers usually present thermal models for semiconductor devices; parameters for two types are often given on datasheets, namely the Cauer and Foster Model [62]. The models represent the junction temperature, T_j, of the device with respect to the ambient temperature, T_a with a good degree of accuracy.

The Foster model is different in that it is an approximation based on measured values and curve fitting with a particular order system. Due to the ease in obtaining the Foster model based on simple lab measurement, manufacturers typically provide datasheet values for Foster thermal models. The intermediate values of the Foster model T_2, $T_3, \ldots T_N$ have no correlation to any actual physical temperature. The manufacturer, Infineon, provides the Foster coefficients on its data sheet which can be used to make analytical calculations [50].

The thermal impedance of a Foster model can be expressed as:

$$Z_{th}(t) = \sum\nolimits_{i=1}^{n} r_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{23}$$

where $\tau_i = r_i c_i$.

The corresponding coefficients are provided on the datasheet in tabular form as resistance (r) and time constant (τ) pairs. With specific switching and forward losses $P_L\,(t)$, and assuming a known case temperature $T_c\,(t)$, the junction temperature $T_j\,(t)$ can be determined as follows:

$$T_j\left(t\right) = P_L\left(t\right) \times \dot{Z}_{th(j-c)}\left(t\right) + T_c(t) \tag{24}$$

The simulated specific switching and forward losses $P_L\,(t)$, which is equated to heat flow Q over time from the IGBT is shown below in Figure 20a.

For each layer in the IGBT die between the junction and case, the simulated temperature through the layer can be derived, along with the temperature at the junction of the subsequent layer. With reference to Figures 27a-j, the attributes above in the two layers of interest, namely the solder between the IGBT and pattern and base are shown.

Altering the Foster coefficients of these layers, will form the basis of modelling solder delamination effects in the IGBT.

The heat sink model in Figure 9 is composed of two constituent components. Firstly, the thermal mass, which reflects the ability of a material or a combination of materials to store internal energy. This property is characterized by mass of the material and its specific heat.

The thermal mass is described with the following equation:

$$Q = c \times m \times \frac{dT}{dt} \tag{25}$$

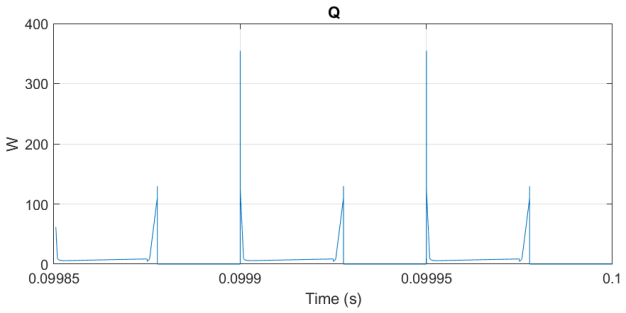
where Q is the Heat flow, c = Specific heat of mass (in this case Aluminium) material, m = Mass, T = Temperature, t = time.

The second component is the heat transfer by convection between two bodies by means of fluid motion. The transfer is governed by the Newton law of cooling and is described with the following equation:

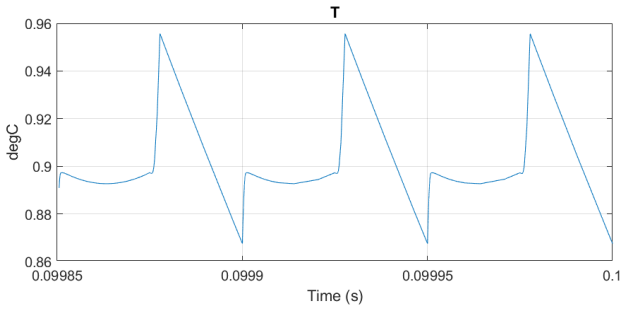
$$Q = k \times A \times \left(T_A - T_B\right) \tag{26}$$

where Q is the Heat flow from the base of the IGBT, k = Convection heat transfer coefficient, A = Surface area, T_A and T_B represent the Temperatures of the bodies.

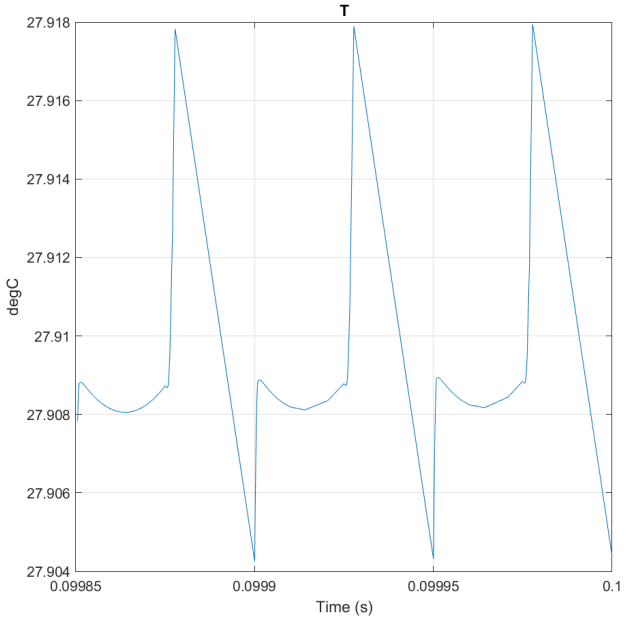
Determination of the value of the convective heat transfer coefficient for an actual thermal system can present challenges. Using tables [63] unforced cooling into air, k has been assumed to be 20 $\frac{W}{M^2}/K$ which is deemed a reasonable assumption. The reference temperature has been assumed to be 298.15K (25°C) throughout the model and T_B is set to be at this temperature.



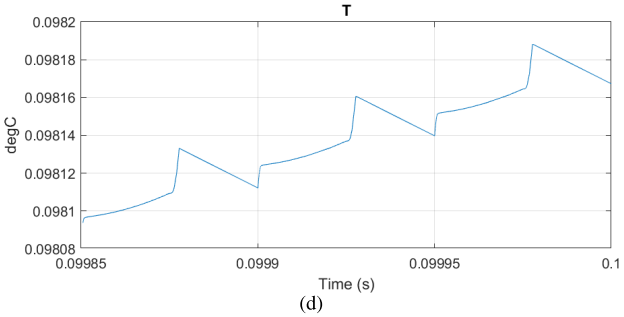
(a)



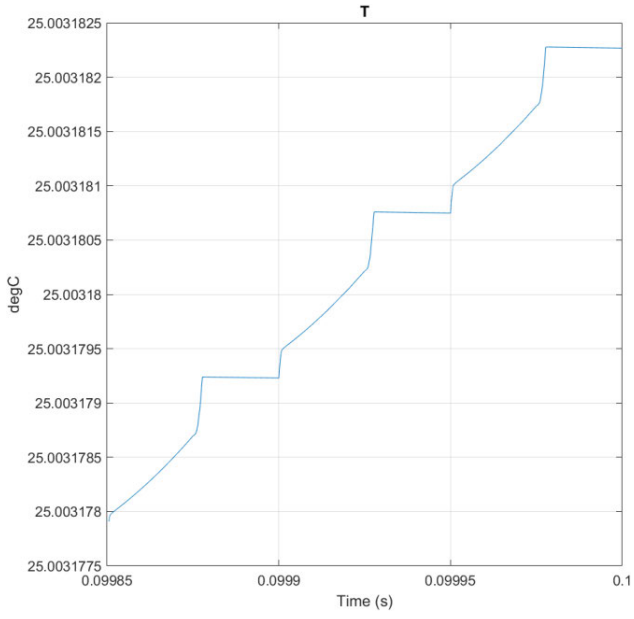
(b)



(c)



(d)



(e)

FIGURE 20. a. Heat flow from the IGBT due to switching losses. b. Temperature through the solder layer between the IGBT and copper pattern. c. Temperature across the solder layer between the IGBT and copper pattern. d. Temperature through the solder layer between the copper pattern and base plate. e. Temperature across the solder layer between copper pattern and base plate.

D. ELECTROLYTIC SMOOTHING CAPACITOR

A linear model of a capacitor is described with the following equation:

$$i = C\frac{dv}{dt} \tag{27}$$

where, i is the current, C is the capacitance, v is the voltage, and t is the time.

To model frequency-dependence in the capacitor with resistive and dielectric losses, the capacitance model parameter to dielectric relaxation (Debye) is used [64]. The Debye relaxation model considers a collection of non-interacting dipoles in the frequency domain. The result is in terms of a complex permittivity. The real (ε') and imaginary (ε'') parts of the complex permittivity are given by the equations:

$$\varepsilon' = \epsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + \omega^2\tau^2} \tag{28}$$

$$\varepsilon'' = \frac{(\varepsilon_s - \varepsilon_\infty)\,\omega\tau}{1 + \omega^2\tau^2} \tag{29}$$

where ω is the radial frequency, ϵ_∞ is the real permittivity at very high frequency, ε_s is the real permittivity at low frequency and τ is the relaxation time constant.

In the time-domain, the characteristic equation for a capacitor in the Debye model is:

$$\tau i = -q + C_s\,(\alpha\tau\dot{v} + v) \tag{30}$$

where C_s is the low-frequency capacitance, $\alpha = \varepsilon_\infty/\varepsilon_s$, q is the charge, i is the current and v is the voltage across the capacitor.

Equivalent series resistance (ESR) specified on manufacturer datasheets will be important later when simulating the failure mode within the capacitor. This resistance, defined for a linear capacitor via the dissipation factor (DF), which is also shown on many datasheets, is given by the relationship $DF = 2\pi fC \times ESR$, where f is signal frequency. For a Debye capacitor, the Dissipation factors (%) at f_1 and f_2 are corrected for this additional series resistance prior to computing α and τ.

The graphs, given in Figures 21a-c show the capacitors instantaneous v, power (W) output, and i from the model of the electrolytic smoothing capacitor used in the simulation.

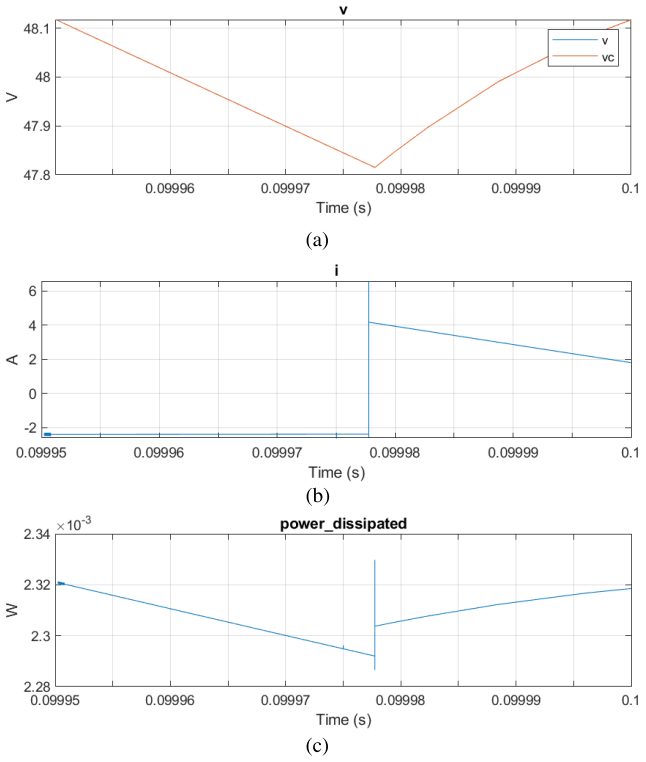


FIGURE 21. a. Voltage across the electrolytic smoothing capacitor. b. Current through the electrolytic smoothing capacitor. c. Power dissipated in the electrolytic smoothing capacitor.

V. PEC DIGITAL TWIN FAULT DETECTION

The digital twin provides numerous advantages; firstly, it provides a metric for health comparison of fault symptoms from designated monitoring features, and secondly, it provides simulated fault data from which a classifier is trained to recognize the fault. The methodology for using the DT for event detection and condition monitoring is outlined in this section.

It important to restate that the DT in this paper is intended for the monitoring of long-term degradation of component parameters, hence a comparison will be based upon a 'snapshot' at a set time interval δT, which may be hourly, daily or longer, depending upon the expected degradation/usage over the monitoring interval. A comparison $\boldsymbol{\gamma}\,(\delta T)$ of the designated measured symptom vectors $\boldsymbol{y}(\delta T)$ to the digital twin $\boldsymbol{z}\,(\delta T)$ is made by subtraction:

$$\boldsymbol{\gamma}\,(\delta T) = \boldsymbol{z}\,(\delta T) - \boldsymbol{y}\,(\delta T) = \begin{bmatrix} \gamma_1(\delta T) \\ \gamma_2(\delta T) \\ \vdots \\ \gamma_n(\delta T) \end{bmatrix} \tag{31}$$

Output voltage has been selected for the symptom vector in this work, as multiple component degradation parameters may be consolidated from the measurement. Comparison of Figure 22, to the real circuit output, shows there will be a difference between the digital twin and the measured feature. No mathematical model is perfect and unavoidable variation in parameters from device-to-device resulting from manufacturing, assembly, materials etc. as well as contributions from impedances and effects from stray capacitance and inductance combined with errors from measurement and noise etc., ensure no matter how carefully the DT has been composed, there will be an error Δ between measurements. This must be taken into account before any meaningful comparison takes place, and as long as this initial difference Δ is acknowledged, any further comparison with respect to this datum will be accurate.

In order to detect the onset of faults, a geometric moving average (GMA) is employed [65]. Given a 'snapshot' of

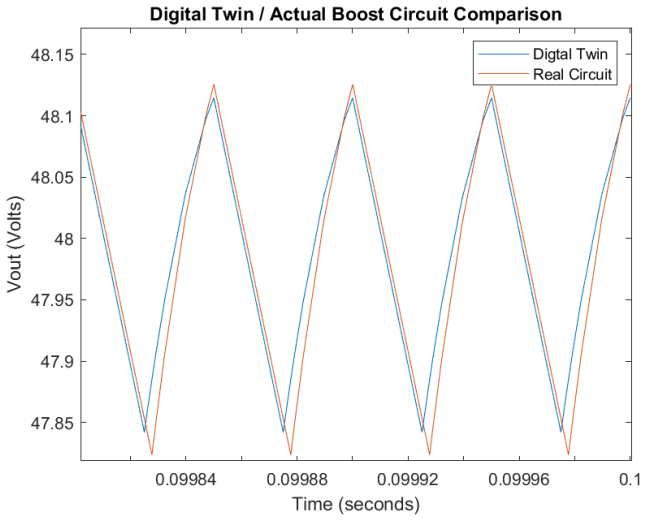


FIGURE 22. Difference between the real measurement $\boldsymbol{y}\ (\delta \boldsymbol{T})$ and the simulated measurement $\boldsymbol{z}\ (\delta \boldsymbol{T})$ from the DT, noting the slight difference Δ.

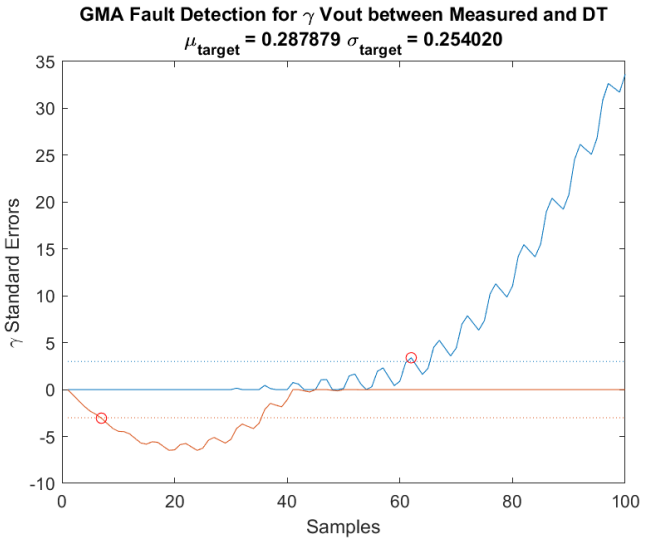


FIGURE 23. Geometric Average for fault detection in 'snapshot' comparison data $\boldsymbol{\gamma}\ (\delta \boldsymbol{T} + \Delta)$ with sample length n.

comparison data $\boldsymbol{\gamma}\ (\delta T + \Delta)$ with sample length n, successive sample averages are given by $\bar{\boldsymbol{\gamma}}_{\boldsymbol{1}}, \bar{\boldsymbol{\gamma}}_{\boldsymbol{2}} \ldots \bar{\boldsymbol{\gamma}}_{\boldsymbol{n}}$.

The healthy operational mean and variance are designated as μ_γ and σ_γ respectively. The GMA of the new sequence is given by:

$$S_0 = \mu_\gamma$$
$$S_m = r\bar{\boldsymbol{\gamma}}_m + (1-r)S_{m-1} \text{ where } \quad (m = 1, 2, \ldots) \tag{32}$$

where $0 < r \leq 1$ is a constant.

Expressing S_m directly in terms of the sample averages gives:

$$S_m = r\sum_{i=0}^{m-1}\left[(1-r)^i\,\bar{\boldsymbol{\gamma}}_{m-1}\right] + (1-r)^m\mu_\gamma \tag{33}$$

Using the summation formula for a geometric series the mean and variance of S_m are given as:

$$\mu_{S_m} = E\,(S_m) = \mu_\gamma \tag{34}$$
$$\sigma^2_{S_m} = Var(S_m) = \frac{r}{2-r}\left[1-(1-r)^{2m}\right]\frac{\sigma^2_\gamma}{n} \tag{35}$$

S_m tends to a constant value after a few samples:

$$\sigma^2_{S_m} \to \left(\frac{r}{2-r}\right)\frac{\sigma^2_\gamma}{n} \text{as } m \to \infty \tag{36}$$

Upper and lower fault bounds can be set at $\left(\mu_\gamma \pm a\sigma_{S_m}\right)$ where a is the standard error from the mean. r allows for the sensitivity to be altered, small values of r lead to high sensitivity and will enable the detection of small changes in the process mean. The crossing of the upper or lower fault bounds, in this case $\pm 3\sigma_{S_m}$ indicates deviation from healthy operation, figure 23 shows the development of degradation within the symptom vector.

VI. FAULT SIMULATION USING THE PEC DIGITAL TWIN

Having defined the DT in detail, the process of fault simulation is explained. Based on the discussion of the primary faults affecting the operational lifetime of the power electronic converter in section III, three faults, namely; bond wire fatigue, solder fatigue and capacitor degradation, respectively, were selected. For each fault, the prospective condition indicative of the fault is modelled. For the bond wire fatigue, this is replicated by an increase in the IGBT internal collector resistance, similarly solder fatigue is represented by an increase in the IGBT thermal resistance of the solder layer between the copper pattern and IGBT base in the Foster model. Finally, by increasing the internal equivalent series resistance (ESR) in the capacitor, the effects of capacitor degradation can be simulated.

The ability to alter these parameters within the model during simulation is a feature available within the Matlab® environment. Using the '**setVariable**' instruction, allows for the direct alteration of the Simscape® parameter within the operational model. Figure 24 shows the maximum failure mode effects with reference to the healthy operational model. All failures are referenced to one measurement, namely the output voltage, $V(\boldsymbol{F})_{out}$, where $\boldsymbol{F}$ is the fault vector.

It may be seen that the bond wire fault gives rise to small increase in the voltage output, where a similar trait is also observed for the thermal resistance fault. Whilst the ESR fault in the capacitor gives rise to an effect known as ESR jump.

A recent acquisition to the Mathworks® family is the Predictive Maintenance Toolbox [66], which amongst its features, has the ability to enable large ensembles of data to be generated from Simscape® models, whilst parameters within the model are altered. This paper has utilised this facility to generate an ensemble representing a set of fault combinations.

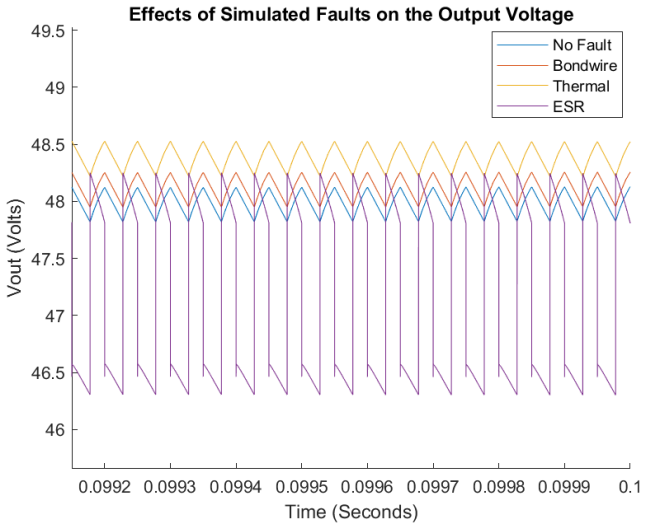


FIGURE 24. V_{out} as a function of the maximum simulated fault parameter with reference to no-fault operation.

The fault vector $\boldsymbol{F}$ containing the following elements is generated,

$$\boldsymbol{F} \in \{\boldsymbol{No\ fault}, \boldsymbol{Bondwire}, \boldsymbol{Thermal}, \boldsymbol{Capacitor(ESR)}, \boldsymbol{Bondwire\&Capacitor(ESR)}, \boldsymbol{Thermal\&Bondwire}, \boldsymbol{Thermal\&Capacitor(ESR)}, \boldsymbol{All\ faults}\} \tag{37}$$

Contrived from three fault vector groups, the number of elements in each fault group $= n$, where m is the number of faults. Initially, for the bond wire, thermal and capacitive elements an increasing fault parameter is generated, where element $a_1, b_1\&c_1$ denotes the no fault value and $a_m, b_m\&c_m$ the maximum fault value.

Bondwire Fault Vector

$$\boldsymbol{BFS} = [a_1 a_2 \ldots a_m] \ \ where\ a \in \mathbb{R}^{1\times m} \tag{38}$$

ESR Fault Vector

$$\boldsymbol{EFS} = [b_1 b_2 \ldots b_m] \ \ where\ b \in \mathbb{R}^{1\times m} \tag{39}$$

Thermal Fault Vector

$$\boldsymbol{TFS} = [c_1 c_2 \ldots c_m] \ \ where\ c \in \mathbb{R}^{1\times m} \tag{40}$$

No Fault Simulation Array

The no fault element is comprised of three vectors

$$Bondwire = \boldsymbol{B} = [a_1 \ldots \times n] \in \mathbb{R}^{1\times n} \tag{41}$$

$$ESR = \boldsymbol{E} = [b_1 \ldots \times n] \in \mathbb{R}^{1\times n} \tag{42}$$

$$Thermal = \boldsymbol{T} = [c_1 \ldots \times n] \in \mathbb{R}^{1\times n} \tag{43}$$

where $a_1 b_1 c_1$ are repeated n times.

Single Fault Simulation Array

idx is a random vector comprised of length m where $\boldsymbol{X} \sim U([0, 1])$ is rounded to an integer

$$\begin{aligned} \boldsymbol{idx} &= \lceil m \times \boldsymbol{X}(n) \rceil \ \ where\ \boldsymbol{X} \sim U([0,1]) \in \mathbb{R}^{1\times n} \\ \boldsymbol{B} &= \left[\boldsymbol{B}_{1\times n}\boldsymbol{BFS}(\boldsymbol{idx})^T\right] \in \mathbb{R}^{mn\times 1} \end{aligned} \tag{44}$$

where $B_{1\times n}$ is concatenated with transposes of ***BFS*** a function of ***idx***.

$$\boldsymbol{E} = [\boldsymbol{E}_{1\times n}\boldsymbol{E}_1 \cdots \times n] \in \mathbb{R}^{mn\times 1}$$

where $E_{1\times n}$ is concatenated with $\boldsymbol{E}_{1\times n}$ and E_1 repeated n times. This is repeated for $\boldsymbol{T}$ and $\boldsymbol{B}$ to give the single fault combinations

$$\begin{aligned} \boldsymbol{T} &= [\boldsymbol{T}_{1\times n}T_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{B} &= [\boldsymbol{B}_{1\times n}B_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{E} &= \left[\boldsymbol{E}_{1\times n}\boldsymbol{EFS}(\boldsymbol{idx})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{T} &= [\boldsymbol{T}_{1\times n}T_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{B} &= [\boldsymbol{B}_{1\times n}B_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{E} &= [\boldsymbol{E}_{1\times n}E_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{T} &= \left[\boldsymbol{T}_{1\times n}\boldsymbol{TFS}(\boldsymbol{idx})^T\right] \in \mathbb{R}^{mn\times 1} \end{aligned} \tag{45}$$

Double Fault Simulation Array

$$\begin{aligned} \boldsymbol{idxA} &= \lceil m \times \boldsymbol{X}(n) \rceil \in \mathbb{R}^{1\times n} \\ \boldsymbol{idxB} &= \lceil m \times \boldsymbol{X}(n) \rceil \in \mathbb{R}^{1\times n} \end{aligned} \tag{46}$$

Again, ***idxA*** and ***idxB*** are random vectors of length m where $\boldsymbol{X} \sim U([0, 1])$ is rounded to an integer

$$\begin{aligned} \boldsymbol{B} &= \left[\boldsymbol{B}_{1\times n}\boldsymbol{BFS}(\boldsymbol{idxA})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{E} &= \left[\boldsymbol{E}_{1\times n}\boldsymbol{EFS}(\boldsymbol{idxB})^T\right] \in \mathbb{R}^{mn\times 1} \end{aligned}$$

where $\boldsymbol{B}_{1\times n}$ and $\boldsymbol{E}_{1\times n}$ are concatenated with transposes of ***BFS*** and ***EFS*** are functions of ***idxA*** and ***idxB***

$$\begin{aligned} \boldsymbol{T} &= [\boldsymbol{T}_{1\times n}T_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{B} &= \left[\boldsymbol{B}_{1\times n}\boldsymbol{BFS}(\boldsymbol{idxA})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{E} &= [\boldsymbol{E}_{1\times n}E_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{T} &= \left[\boldsymbol{T}_{1\times n}\boldsymbol{TFS}(\boldsymbol{idxB})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{B} &= [\boldsymbol{B}_{1\times n}B_1 \cdots \times n] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{E} &= \left[\boldsymbol{E}_{1\times n}\boldsymbol{EFS}(\boldsymbol{idxA})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{T} &= \left[\boldsymbol{T}_{1\times n}\boldsymbol{TFS}(\boldsymbol{idxB})^T\right] \in \mathbb{R}^{mn\times 1} \end{aligned} \tag{47}$$

Triple Fault Simulation Array

$$\begin{aligned} \boldsymbol{idxA} &= \lceil m \times \boldsymbol{X}(n) \rceil \in \mathbb{R}^{1\times n} \\ \boldsymbol{idxB} &= \lceil m \times \boldsymbol{X}(n) \rceil \in \mathbb{R}^{1\times n} \\ \boldsymbol{idxC} &= \lceil m \times \boldsymbol{X}(n) \rceil \in \mathbb{R}^{1\times n} \end{aligned} \tag{48}$$

Again, ***idxA***, ***idxB*** and ***idxC*** are random vectors of length m where $\boldsymbol{X} \sim U([0, 1])$ is rounded to an integer

$$\begin{aligned} \boldsymbol{B} &= \left[\boldsymbol{B}_{1\times n}\boldsymbol{BFS}(\boldsymbol{idxA})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{E} &= \left[\boldsymbol{E}_{1\times n}\boldsymbol{EFS}(\boldsymbol{idxB})^T\right] \in \mathbb{R}^{mn\times 1} \\ \boldsymbol{T} &= \left[\boldsymbol{T}_{1\times n}\boldsymbol{TFS}(\boldsymbol{idxC})^T\right] \in \mathbb{R}^{mn\times 1} \end{aligned} \tag{49}$$

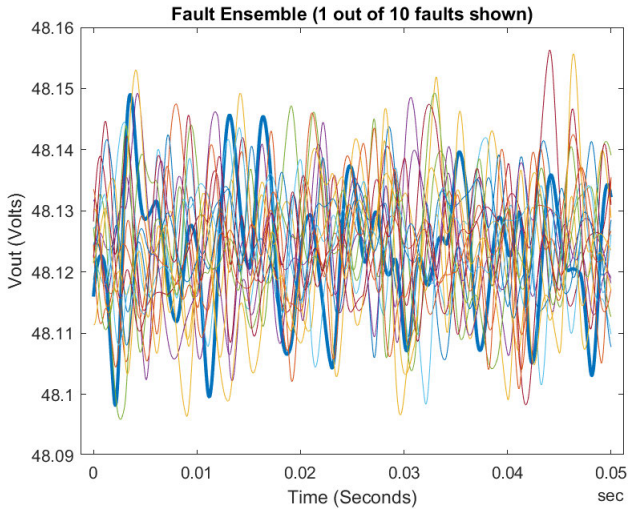


FIGURE 25. An ensemble (1 out of 10) of 160 generated faults.

where $\boldsymbol{B}_{1\times n}\boldsymbol{T}_{1\times n}$ and $\boldsymbol{E}_{1\times n}$ again, are concatenated with the transpose of ***BFS***, ***EFS*** and ***TFS***, which are functions of ***idxAidxB*** and ***idxC***.

The fault vector $\boldsymbol{F}$ comprising of the fault combinations produced by 46, 48 & 49, is used in conjunction with the DT to generate an ensemble of faults. At this stage, global environmental parameters such as temperature and vibration may also be introduced into the DT, to enhance the fault vector if desired. Figure 25 shows a typical fault ensemble of 160 combinations, with 1 of out 10 faults plotted to aid clarity.

VII. FEATURE EXTRACTION

In practise, sensor data in its raw form is unlikely to reveal the existence or enable the classification of faults, due to the presence of process and measurement noise. Hence, applying signal processing methodologies becomes necessary. Time domain feature analysis based on statistical parameters such as mean, standard deviation, root mean square (RMS), peak-to-peak, maximum, minimum, skewness, kurtosis, crest factor, wave factor, impulse factor, margin factor, have been extensively explored [67]. Time series models, such as fitted stochastic processes e.g., Hidden Markov and ARMA have also been used. Frequency domain methods include Fast Fourier Transforms (FFTs), envelope analysis and high-order spectral analysis.

An important aspect of failure signals is that the information of interest is often a combination of phenomenon that are transient and diffused. Such phenomenon is characterized by information that exist in the time/frequency domain or both. To analyse such signals, there is a need for methodologies such as short-time Fourier analysis, Hilbert–Huang transform [68], [69], and Wavelet transforms that are sufficiently versatile to capture events that are present in these extremes by localising information from a time-frequency point of view. Wavelets and the generalized wavelet-packet transforms [70] use in the detection of faults is well documented, particularly in the areas of transmission lines [71] and rotating machinery [72]. Wavelets divide the signal of interest into different frequency components, where each component is studied at a resolution matched to its scale.

A. WAVELET BACKGROUND

Wavelet analysis is essentially a pass band filtering operation, decomposing a signal into different frequencies at different energy resolutions [73].

Consisting of Father and Mother wavelets, the Father wavelet $\phi(t)$ being a dilated version of the Mother wavelet $\psi(t)$, is adept at resolving smooth and low frequency components of a signal as opposed to the Mother, which resolves detail and high frequency elements of the signal. The decomposition of the signal in the time domain is achieved by sliding the chosen wavelet function (of which there are numerous families [74] and suitability for the application requires investigation) across the signal where the similarities are computed at different instances of time by:

$$x(t) \approx \sum_{k} S_{J,k}\phi_{J,k}(t) + \sum_{j=J}^{1}\sum_{k} d_{j,k}\psi_{j,k}(t) \tag{50}$$

Techniques, such as minimum description length criterion allow not only the suitable wavelet filter to be selected, but also the optimum number of wavelet coefficients retained for the signal reconstruction [75].

In order to achieve the decomposition into the time-frequency components the wavelet transform, W_ψ has a scale-varying basis function.

$$W_\psi f(a,b) = \int_{-\infty}^{\infty} f(t)\frac{1}{\sqrt{a}}\psi\left(\frac{t-b}{a}\right)dt \tag{51}$$

where b is the translational parameter, and in order to achieve the high and low frequency resolution, the wavelet function $\psi\left(\frac{t-b}{a}\right)$ is scaled, where $a > 1$ is the low frequency and $0 \leq a \leq 1$ is the high frequency filtering operation.

The wavelet transform may be implemented either in a continuous or discrete manner. The Continuous Wavelet Transform (CWT) has a finer discretizing scale a than the Discrete Waveform Transform (DWT), achieved typically by fixing a base, which is a fractional power of two, for example, $2^{\left(\frac{1}{v}\right)}$ where v is an integer >1, often referred as the number of voices per octave. Different scales are achieved by raising the scale parameter a to a positive integer power $2^{\left(\frac{j}{v}\right)}$ where $j = 1, 2, 3\ldots$

$$W_\psi f(a,b) = \frac{1}{2^{\frac{j}{v}}}\psi\left(\frac{n-m}{2^{\frac{j}{v}}}\right) \tag{52}$$

and discretising the translational parameter b to an integer value m, gives the DWT representation, where voices per octave are normalised. The aforementioned technique allows components of interest to be extracted from the decomposed

signal, where features such as energy, mean, kurtosis, RMS may be used for classification.

The signal decomposition process takes the original time domain signal $x[n]$ and divides it into two components, a low pass filter (LPF) and a high pass filter (HPF). Due to the DWT employing a discrete set of scales which are a function of 2^j, $x\,[n]$ is down sampled by 2. The convolution of $x\,[n]$ with the HPF results in the detail coefficients and likewise the convolution with the LPF produces the approximation coefficients. This process of decomposition may be applied across multiple levels.

B. WAVELET SCATTERING CLASSIFICATION

Wavelet Scattering Networks (WSN) originally proposed by Mallat [76], are an extension of the above, utilizing a cascade of wavelets, modulus nonlinearities and low pass filters that allow, with minimum configuration, the extraction of low-variance features from time series and image data. The scattering transform yields representations that are translation or shift invariant and stable against time warping. They have provided state-of-the-art classification accuracies on simple to moderately complex datasets, such as textures in CUReT dataset [77], or musical genre and environmental sound classification [78], and images in MNIST dataset [79]. WSN have been used to extract features from ECG signals to classify four types of arrhythmias using neural networks trained on a reduced WSN feature space together with KNN classification [80].

The application of WSN to health monitoring has been explored in [81], using learnable wavelet scattering networks, for the fault diagnosis of circuits and rotating machinery, using a genetic algorithm-based optimization of second-generation wavelet transform operators. Reference [82] describes an algorithm for bearing fault detection using WSNs as a pre-processing step for feature space generation and [83] investigates the efficacy and applicability of the WSN feature domain relative to fault detection and diagnosis for the mechanical components of industrial robots. WSN are utilized, and incorporated with ML classifiers to design a framework for bearing fault classification in induction motors [84].

The basic theory for the scattering networks to extract either evident or invisible data features is based upon the wavelet transform, which is both a mode recognition and decomposition approach. There are deep mathematical connections between wavelets and Deep Convolutional Neural Networks (DCNNs) as shown by Mallat and co-workers, [77], [85]. Both methods utilize a succession of operations, Figure 26, involving convolution, dealing with non-linearity, and pooling/subsampling. These are outlined and the differences compared in Table 2.

Following Figure 25 above, the wavelet convolution process uses the selected mother wavelet (ψ_λ) and low pass filter ϕ_J to define local, translation invariant waveforms that behave as band pass filters at a predefined scale, T.

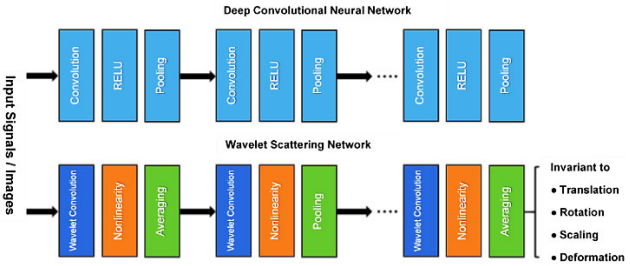


FIGURE 26. Comparing the successive operations of the DCNN and WSN.

TABLE 2. Outlining the diffences between DCNN and WSN.

DCNN	WSN
Convolution: The weights have to be learnt by successive approximation. Can be computationally expensive.	**Wavelet Convolution**: Predetermined set of families with known weights avoids the need for computationally expensive learning by iteration.
ReLU: DCNN typically employ a Rectifier or (ReLU) activation unit to help with interaction and non-linear effects.	**Non-linearity**: ReLU is replaced by the modulus. Integrating the modulus of the wavelet convolution results in the L_1 norm, which is invariant. As well as computing a lower frequency envelope of the signal.
Pooling: DCNN use pooling layers to reduce the dimensions of the feature maps, reducing the number of parameters to be learnt and the amount of computation.	**Averaging**: Imposes time-shift invariance and stability against time warping deformations.

Reference [77] found as long as the wavelet is complex, the outcome of the scattering transform is independent of the wavelet selection. The choice of mother wavelet in this study was the Gabor (analytic Morlet) wavelet due to its extensive documentation in condition monitoring [86].

$$\psi_\lambda = e^{-\alpha t^2} e^{j2\pi f_c t} \tag{53}$$

The filters, designated to cover the complete frequency spectrum found in the signal and when convolved with the input, $x(t)$, they decompose $x(t)$ into signals with specific bandwidths.

$S_0 x\,(t) = x * \phi_J(t)$ where $\phi_J(t)$ is the Father wavelet, being a dilated version of the Mother wavelet $\psi\,(t)$ defines a locally translation invariant feature of $x(t)$, but also results in the loss of high-frequency information. This may be recovered by the use of the wavelet modulus transform as follows:

$$|W_1|\,x = \{S_0 x\,(t)\,, |x * \psi_{\lambda 1}(t)|\} \quad \lambda_1 \in \Lambda_1 \tag{54}$$

where the multiscale high-pass filter banks are defined by dilated wavelets $\{\psi_{\lambda k}\}_{\lambda_k \in \Lambda_k}$, and Λ_k denote a family of wavelet indices having an octave frequency resolution, Q_k.

Integrating the modulus of the convolution of x and ψ_λ, results in the L_1 norm. Hence, if $x(t)$ translates in time, the modulus does not change, it is invariant.

$$\int |x * \psi_\lambda(t)|\, dt = \|x * \psi_\lambda\|_1 \tag{55}$$

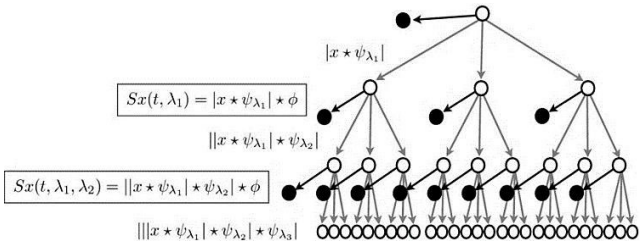


FIGURE 27. Process of feature extraction for 2nd order wavelet scattering [75].

The first-order scattering coefficients are obtained by averaging the wavelet modulus coefficients with ϕ_J. The averaging imposes, firstly a time-shift invariance and secondly, stability against time warping deformations, the overall operation is:

$$S_1 x\,(t, \lambda_1) = \left|x * \psi_{\lambda_1}\right| * \phi_J \tag{56}$$

yielding first order scattering coefficients, where λ_1 is the center frequency of the first order wavelets.

To recover the complementary high frequency information lost in the averaging process, where $S_1 x\,(t, \lambda_1)$ is deemed the low frequency component of $\left|x * \psi_{\lambda_1}\right|$,

$$|W_2|\left|x * \psi_{\lambda_1}\right| = \left\{S_1 x\,(t, \lambda_1), \left|\left|x * \psi_{\lambda_1}\right| * \psi_{\lambda_2}(t)\right|\right\} \tag{57}$$

where $\lambda_2 \in \Lambda_2$.

The second order coefficients are obtained by

$$S_2 x\,(t, \lambda_1, \lambda_2) = \left|\left|x * \psi_{\lambda_1}\right| * \psi_{\lambda_2}\right| * \phi_J \tag{58}$$

Again, continuing this process, results in equation 59. Generally, for most problems two filter banks are adequate.

$$S_m x\,(t, \lambda_1, \ldots, \lambda_m) = |||x * \psi_{\lambda 1}| * \ldots| * \psi_{\lambda m}| * \phi_J \tag{59}$$

Figure 27 below, illustrates the process, the scattering decomposition at each level provides discriminative information from which feature parameters can be extracted.

For three levels, the feature data will be comprised of sets $\{S_0 x, S_1 x, S_2 x\}$ or subset of this set or even a combination of elements from this set e.g. $S_0 S_2\,[\lambda_1]\,x$ or subset of $S_1 x = \{S_J\,[\lambda_1]\,x, S_J\,[\lambda_2]\,x, S_J\,[\lambda_3]\,x, S_J\,[\lambda_4]\,x\}$ where J is the scattering level.

VIII. CLASSIFICATION

Classification is the methodology of predicting the class to which an object belongs. The object known commonly as a pattern in classification will be the fault within this application. By assuming the pattern belongs to one and only one among a number of a priori known classes, each fault will then be uniquely represented by a set of values, known as features. Feature extraction via Wavelet Scattering allows l features representing the fault vector $\boldsymbol{F}$, $S_0 x, S_1 x, S_2 x \ldots S_l x$. These are used to form the components of the so-called feature vector $x \in \mathbb{R}^l$. The aim is to design a classifier, such as a function, $f(x)$, or equivalently a decision surface, $f\,(x) = 0$, in $\mathbb{R}^l$, so that given the values in a feature vector x, corresponding to a pattern, enables prediction of the class to which the pattern belongs.

The choice of support vector machine (SVM) [87], [88], [89] as a classifier is based on analysis of six of the most prevalent classification algorithms in literature: namely SVM, ensemble learning, k-nearest neighbors (KNN), naive Bayes (NB), decision tree (DT) and discriminant analysis (DA). From which SVM came out best for our data when evaluated against the metrics in section IX, equations 65 & 66, which were used to assess the performance. This coincides with results in literature for other papers on fault classification utilizing WSN derived feature vectors [81], [83], [84].

A. SUPPORT VECTOR MACHINE

Support Vector Machine (SVM) uses statistical learning theory based on Vapnik–Chervonenkis theory (VC-theory) that recently emerged as a general mathematical framework for estimating (learning) dependencies from finite samples [90]. SVM is the proposed method for fault classification in this paper due to its high accuracy and good generalization for a smaller number of samples. However, as more data becomes available, combined with increased computational resources, it is envisaged a deep learning classifier may be invoked. Given data input $\boldsymbol{x}_i (i = 1, 2, \ldots, M)$, where M is the number of samples. The samples are assumed to have two classes namely positive class and negative class. Each of classes associates with labels, $\boldsymbol{y_j} = 1$ for positive class and $\boldsymbol{y_j} = -1$ for negative class, respectively. In the case of linear data, it is possible to determine the hyperplane $f\,(x) = 0$ that separates the given data from:

$$f\,(\boldsymbol{x}) = w^T \boldsymbol{x}_j + b = \sum_{j=1}^{M} \boldsymbol{w}_j \boldsymbol{x}_j + b = 0 \tag{60}$$

for the classification labels $\boldsymbol{y}_j \in \{\pm 1\}$ where $\boldsymbol{w}$ is a M-dimensional vector and b is a scalar. Paramount to the SVM is determining w and b in a coherent way. Optimization is used to minimize the number of misclassified data points and at the same time create the largest possible margin. The loss function is defined as:

$$\begin{aligned} \ell\left(\boldsymbol{y}_j, \bar{\boldsymbol{y}}_j\right) &= \ell\left(\boldsymbol{y}_j, sgn\left(\boldsymbol{w^T x}_j + b\right)\right) \\ &= \left\{\begin{array}{l} 0\ \boldsymbol{if}\ y_j = sgn\left(\boldsymbol{w^T x}_j + b\right) \\ +1\ if\ \boldsymbol{y}_j \neq sgn\left(\boldsymbol{w^T x}_j + b\right) \end{array}\right\} \end{aligned} \tag{61}$$

A loss of unity is produced for each mislabeled point. The error due to training over M data points is the sum of the loss functions $\ell\left(\boldsymbol{y}_j, \bar{\boldsymbol{y}}_j\right)$.

The linear SVM optimization problem, therefore, becomes:

$$\begin{aligned} &\text{argmin}\,(\boldsymbol{w}, b) \sum_{j=1}^{M} \ell\left(\boldsymbol{y}_j, \bar{\boldsymbol{y}}_j\right) + \frac{1}{2}\|\boldsymbol{w}\|^2 \\ &\text{subject to } \min_j \left|\boldsymbol{x}_j.\boldsymbol{w}\right| = 1 \end{aligned} \tag{62}$$

Non-linear classification curves enable the feature space for SVM to be extended. For data embedded in a

high-dimensional space, nonlinear features are included by building hyperplanes in this new space. This is achieved by mapping the data into a nonlinear, higher-dimensional space

$$\boldsymbol{x} \longmapsto \boldsymbol{\Phi}(\boldsymbol{x}) \tag{63}$$

where, $(\boldsymbol{x})$ are new data observations and hyperplanes that optimally split the data into distinct clusters in a new space learnt by the SVM algorithm. The hyperplane function then becomes:

$$f(\boldsymbol{x}) = \boldsymbol{w}^T \boldsymbol{\Phi}(\boldsymbol{x}) + b \tag{64}$$

for the classification labels $\boldsymbol{y}_j \in \{\pm 1\}$ for each point $f\left(\boldsymbol{x}_j\right)$. (68) remains largely unchanged except $\boldsymbol{y}_j$ is replaced by $sgn\left(\boldsymbol{w}^T \boldsymbol{\Phi}(\boldsymbol{x}) + b\right)$

This ability to operate in higher-dimensional nonlinear spaces makes the SVM one of the most successful machine learning algorithms [87] and its use in condition monitoring and fault diagnosis is well founded [91].

IX. RESULTS

The results from the Digital Twin (DT) have been extensively shown in Section IV and V respectively. This section reviews the performance of the DT in terms of fault classification. In order to evaluate the performance of the classifier, a form of metric needs to be employed. An estimation of the error rate is obtained by subjecting the classification to a validation set, from which an estimated error rate is calculated from the misclassified samples with respect to the size of the validation set. The results can be visualized by representing the findings in a confusion matrix. The confusion plot shows for each combination of faults the number of times the fault combination was correctly predicted (the diagonal entries of the plot) and the number of times the fault combination was incorrectly predicted (the off-diagonal entries) [92].

By evaluating the performance of the trained classifier using the validation data and plotting the results on a confusion plot, two basic measures may be obtained. Firstly, the error rate and secondly, the accuracy. Error rate is calculated as the number of all incorrect predictions divided by the total number of the dataset. The best error rate is 0.0, whereas the worst is 1.0.

$$Error\ rate = (FP + FN)/(P + N) \tag{65}$$

The accuracy is calculated as the number of all correct predictions divided by the total number of the dataset. The best accuracy is 1.0, whereas the worst is 0.0. It can also be calculated by 1 – Error Rate. This is often expressed as a percentage.

$$Accuracy = (TP + TN)/(P + N) \tag{66}$$

In each of the Figures below (28-30), the size of the ensemble of generated faults is given, along with the error and accuracy as a percentage.

The results were carried out on a standard desktop PC, with relatively small ensembles of fault data, however, as the

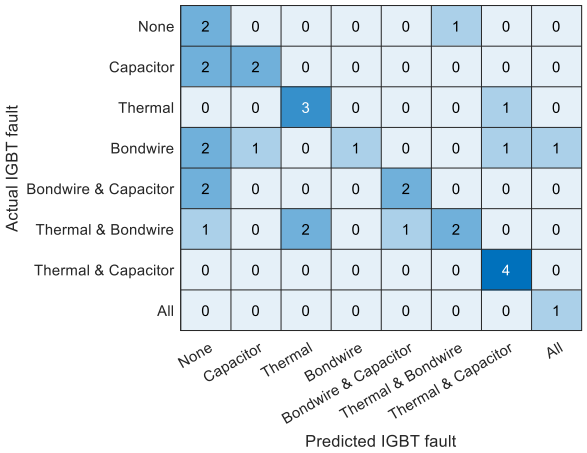


FIGURE 28. Fault ensemble size 80, prediction error rate 62.5%, fault validation accuracy 85.42%.

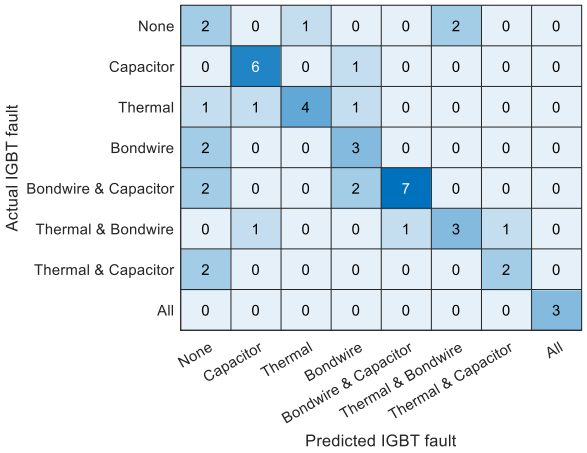


FIGURE 29. Fault ensemble size 160, prediction error rate 67.5%, fault validation accuracy 93.75%.

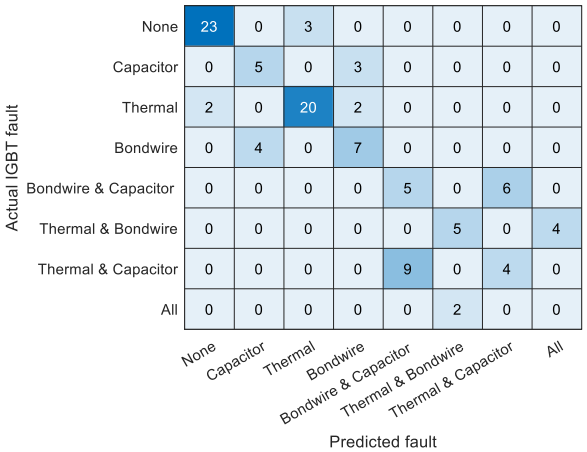


FIGURE 30. Fault ensemble size 240, prediction error rate 72.75%, fault validation accuracy 93.75%.

methodology in section I is implemented, the increased quantity of data available for classification will see a significant improvement in accuracy. From the confusion matrices, a key problem has been highlighted in distinguishing between multiple-faults as well as thermal and bond wire faults. From figure 24, there is considerable correlation in waveforms for these two faults which is a cause of abnormality in

classification. It may be argued that the classification of multiple faults is unnecessary as the probability of failure arising from two or more faults at similar times is unlikely.

X. CONCLUSION

This paper has presented a methodology to enable the detection and classification for the on-set of faults occurring within a Power Electronics Converter (PEC) assembly.

The development of a Digital Twin PEC has been presented in the form of a step-up converter (Boost converter) and along with a discussion of the operation, the theoretical results have been presented. The formation of the Digital Twin (DT) with the modelling of each component and associated faults, e.g., IGBT, capacitors, have been outlined in detail in terms of the development and the parameters obtainable from the DT. As well as the components, the effects of the thermal management of the PEC are also modelled within the D T.

The use of the DT to provide long term degradation condition monitoring of the PEC components via a 'snap shot' comparison of deviation from operation waveforms using a Geometric Moving Average (GMA) has been outlined, along with the use of the DT for producing synthetic operational data from the PEC. This includes the ability to introduce faults and ability to establish an accurate fault vector for classification. The classification process via a Support Vector Machine (SVM) has been examined, with the extraction of the features from the data using Wavelet Scattering to train the classifier being presented.

The results show that detection and classification of faults has been achieved in the order of 72.75% success with a validation accuracy of 93.75% from a relatively small data set. It is expected that this methodology may be expanded for implementation for other PEC topologies in the future.

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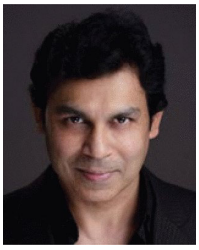
ANDREW J. WILEMAN received the B.Eng. degree (Hons.) in electronic engineering from the University of Nottingham, U.K., and the M.Sc. degree in digital communication systems from Loughborough University, U.K. In 2012, he joined the Integrated Vehicle Health Management (IVHM) Centre, Cranfield University, as a Ph.D. Researcher in prognostics for electronics/defense systems, sponsored by Thales, U.K., and Meggitt. He worked with the U.K. Ministry of Defence and other engineering companies within the U.K. He has lectured in electronics/communication engineering with further and higher education institutions for a number of years. After completing his Ph.D., he is currently working as a Research Fellow in power electronics reliability, AI systems and applications, digital twins, and data-centric engineering. His research interests include the development of IVHM solutions for power electronics systems in relation to more-electric aircraft (MEA), prognostic algorithms, and the application of digital twins for improving diagnostics and maintenance in aircraft and autonomous systems.



SOHAIB ASLAM received the B.Eng. degree in electrical engineering from the NED University of Engineering and Technology, Pakistan, in 1997, the M.Sc. degree in electronics and electrical engineering and management from the University of Glasgow, U.K., in 2014, and the Ph.D. degree in micro- and nano-electronics from Cranfield University, U.K., in 2020. From 1997 to 2013, he worked with the Navy, MoD (Pakistan), as a Systems Engineer (electronic warfare). He has wide-ranging experience in predictive and condition-based maintenance of naval electronic warfare systems. His research interests include AI systems and applications, semiconductor device reliability and security assessment, digital twins and data-centric engineering, and design for testability, prognostics, and security in field-programmable gate arrays (FPGAs) and systems-on-chip (SoCs).

SURESH PERINPANAYAGAM received the M.Eng. degree in aeronautical engineering from the Imperial College of Science, Technology and Medicine, London, and the Ph.D. degree from the Rolls-Royce University Technology Centre, Imperial College London, under the auspices of the European FP7 Program. During this tenure, he worked with major engine manufacturers in Europe (Rolls-Royce, U.K.; MTU, Germany; and SNECMA, France). He is a Professor of Engineering at the University of York. He was one of the pioneering researchers who was awarded $1 million project, funded by Boeing, EADS, and Singapore's Science and Engineering Research Council (SERC), under the auspices of the SERC Aerospace Research Program. The project looked at developing novel sensors and signal-processing techniques for the detection of defects on composites of the thickness of more than one inch, such as those on the Boeing 787 skin. He has published one book chapter on sensors, instrumentation and signal processing in the SAE International book on *Integrated Vehicle Health Management* and numerous research articles. He, as a Principal Investigator, has recently received more than half a million pounds in funding from Innovate U.K., and Airbus for exploring data-centric engineering and digital twin concepts for future landing gear platforms. His research interests include data-centric engineering and digital twins for intelligent systems, sensory systems, advanced reasoners, artificial intelligence, predictive capabilities, and decision-making for intelligent systems which demonstrate self-health awareness, operational resilience, failure recovery, system re-configurability, and end-of-life prediction. He is also a member of the Editorial Board of *Microelectronics Reliability*, Special Issue on Reliability of Power Electronics. He is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, Special Issue on Robust Design and Reliability in Power Electronics.