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RESEARCH ARTICLE

Effects of Interface States on Electrical Characteristics of Feedback Field-Effect Transistors

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ABSTRACT In this study, we examine the effect of interface trap states on the electrical characteristics of single-gated feedback field-effect transistors (FBFETs) using a commercially available computer-aided design simulation package. Interface trap states exist between the channels and the oxide layers, and these trap states act as acceptor-like trap states in regions of higher energy than the intrinsic Fermi energy (E_i) and as donor-like trap states in regions of lower energy than E_i in the energy band. The density distribution peaks at E_i + 0.28 eV for the acceptor-like trap states and at E_i – 0.28 eV for the donor-like trap states. The occupation mechanism of these trap states is analyzed by the density of the interface states and trapped charges, the energy band diagram, and the current-voltage curves. In n-channel (p-channel) FBFETs, the latch-up voltage varies by approximately 0.01 V as the acceptor-like (donor-like) trap states increase, whereas the effect of the donor-like (acceptor-like) trap states is negligible. Moreover, the FBFETs exhibit an operating speed of 4 ns and retention time of 900 s during a memory operation, despite the existence of the interface states.

INDEX TERMS Positive feedback mechanism, memory, interface state, trap, FBFET.

I. INTRODUCTION

Feedback field-effect transistors (FBFETs) have attracted considerable attention as promising memory devices owing to their near-zero subthreshold swings, high on/off-current ratios ($\sim 10^{10}$), bistable I–V characteristics [1], [2], [3], [4], nondestructive read capability, and long retention time [5]. Recently, various types of memory devices based on FBFETs, such as static random-access memory [6], quasi-nonvolatile memory [5], and one-transistor dynamic random-access memory [7], [8], have been proposed. FBFETs distinguish the memory states as the supply voltage above ∼0.5 V is applied, and the supply voltage is acceptable for their real applications as memory devices [22]. However, to ensure their acceptance as practical memory devices, the reliability of FBFETs has to be assured. Moreover, during the downscaling of the feature size, the device fabrication processes raise the interface states, that is, surface states or interface trap charges, and these states and charges eventually degrade the device performance [9], [10], [11]. In particular, the interface state density changes sensitively with variations in the fabrication processes, which causes device variability [12], [13], [14].

In this study, we analyzed the variation in the electrical characteristics of single-gated FBFETs owing to the interface states between the channels and gate oxide layers. Both acceptor-like (negatively charged when occupied) and donor-like (positively charged when occupied) trap states were explored in this simulation. In addition, transient simulations were performed by technology computer-aided design (TCAD) simulation to estimate the memory operation of FBFETs with these interface states.

II. DEVICE STRUCTURE AND SIMULATION METHOD

Figures 1(a) and (b) show the schematic of the n-channel FBFET (n-FBFET) and p-channel FBFET (p-FBFET). The dimensional parameters and doping concentrations were

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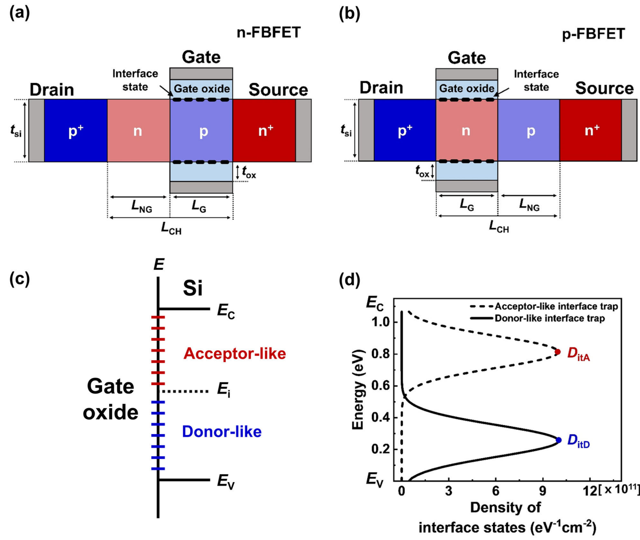

FIGURE 1. Schematic of single-gated (a) n- and (b) p-FBFETs with interface states between gated channels and gate oxide layers. (c) Acceptor- and donor-like trap states in the energy band. (d) The density of acceptor- and donor-like trap states distributions as a function of energy. D_{itA} (D_{itD}) represents the peak density of the acceptor-like (donor-like) trap states.

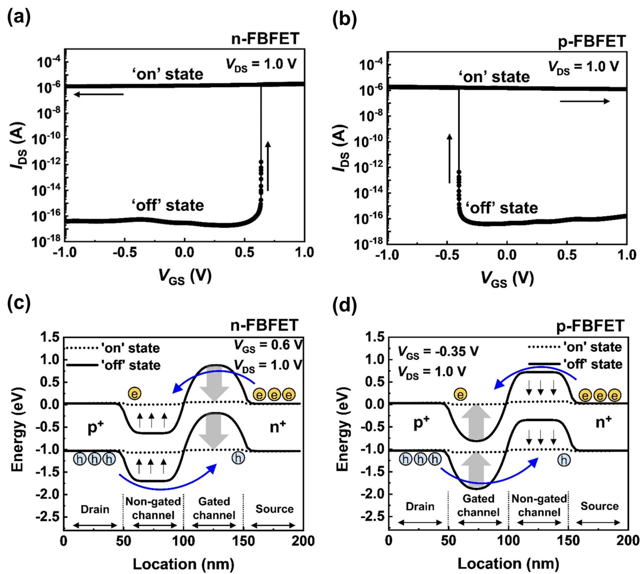

FIGURE 2. Transfer curves of (a) n- and (b) p-FBFETs. Energy band diagrams of (c) n-FBFET at a V_{GS} of 0.6 V and (d) p-FBFET at a V_{GS} of −0.35 V.

identical for both n- and p-FBFETs. The channel length (L_{CH}), silicon channel thickness (t_{Si}), and SiO_2 gate-oxide thickness (t_{ox}) were 100, 20, and 5 nm, respectively. The gated channel length (L_G) and non-gated length (L_{NG}) were 1/2 L_{CH}.

The doping concentration of the p-doped drain and n-doped source regions was 1×10^{19} cm^{-3}, and the channel regions were n- and p-doped with a doping concentration of 5×10^{18} cm^{-3}. The work functions of the gate metal for the n- and p-FBFETs were 4.5 and 4.0 eV, respectively.

Interface states were assumed to exist between the gated silicon channels and the gate silicon oxide layers. The interface states act as acceptor-like trap states in regions of higher energy than the intrinsic Fermi energy (E_i) and as donor-like trap states in regions of lower energy than E_i in the energy band (figure 1(c)). In figure 1(d), the density distributions of the acceptor- and donor-like trap state distributions are depicted as a function of energy using Gaussian-like profiles. The density distribution peaked at E_i + 0.28 eV for the acceptor-like trap states and at E_i − 0.28 eV for the donor-like trap states. The neutral traps are charged owing to the band bending, and the trapped charge density varies with the energy level of the interface trap states. The energy level of the interface trap states influences the trapped charge density. As the distribution of the interface trap states is shifted toward E_i, the trapped charge density increases. The increase in the trapped charge density influences the potential barriers in the gated and non-gated channel regions and thereby the device performance. In contrast, when the distribution of the interface trap states is shifted toward E_c or E_v, the interface states do not substantially influence the device performance. Thus, for the realistic simulation, the highest densities of the acceptor-like trap states (D_{itA}) and donor-like trap states (D_{itD}) were obtained from published experimental data [15].

The simulation was performed with a two-dimensional structure using a commercial device simulator, Synopsys Sentaurus (O_2018.06) [16]. The Lombardi, Philips unified mobility and high-field saturation models were used to consider the doping and field dependences of the carrier mobility. Fermi statistics was applied to perform an accurate simulation. Bandgap narrowing (Slotboom model), Shockley–Read–Hall (SRH) recombination with concentration-dependent lifetimes, and surface SRH recombination were considered for the interface, Auger recombination, and nonlocal path band-to-band tunneling. Furthermore, an area factor of 20 nm was specified in the simulation to determine device width.

III. RESULTS AND DISCUSSION

A. OPERATING PRINCIPLE OF FBFETs

Figure 2 shows the transfer curves with the open memory windows and energy band diagrams of the n- and p-FBFETs at a drain-to-source voltage (V_{DS}) of 1.0 V. For the n-FBFET in the off-state, two potential barriers in the channel region blocked the charge carrier injection (figures 2(a) and (c)). As the gate-to-source voltage (V_{GS}) was swept from −1.0 to 1.0 V, electrons were injected from the source region into the non-gated channel region owing to the lowering of the height of the potential barrier in the gated channel region. Subsequently, the accumulation of electrons in the potential well lowered the height of the potential barrier in the non-gated channel region, thereby allowing the injection of holes from the drain region to the gated channel region. The repeated accumulation of charge carriers activated a positive feedback loop, thereby eliminating the potential barriers.

Consequently, the device was switched to the 'on' state with a sudden rising of the drain-to-source current (I_{DS}) corresponding to the latch-up phenomenon. Because of the accumulation of charge carriers, the device remained in the 'on' state even in the V_{GS} sweeping from 1.0 to −1.0 V. Thus, the device exhibited bistable characteristics. For the p-FBFETs, as V_{GS} was swept from 1.0 to −1.0 V, the injection of holes from the drain region to the channel region stimulated the positive feedback loop, and subsequently, the device was switched to the 'on' state with a latch-up phenomenon (figures 2(b) and (d)). After V_{GS} was swept back to 1.0 V, the device remained in the 'on' state owing to the accumulation of charge carriers in the channel region. In this study, the effect of the interface trap on the n- and p-FBFETs in the 'on' state is analysed in the open memory window.

B. INTERFACE STATES DISTRIBUTIONS AND OCCUPATION MECHANISM

The acceptor- and donor-like trap states located at the interfaces affected the operation of the n- and p-FBFETs. For the n-FBFET, the trap occupation mechanism depended on the location of the trap states at the interface between the gated channel and gate oxide (figure 3(a)). In the 'off' state (V_{GS} = 0.6 V and V_{DS} = 1.0 V), electrons flowing from the non-gated channel and source regions were captured on the trap states at the interface, and subsequently, electrons trapped at the central interface part were emitted to the gated channel. For the acceptor-like trap states, the trapped charge density was highest at the interface edge near the source region (150 nm in figure 3(b)); electrons were supplied primarily from the source region. In contrast, for the donor-like trap states, as captured electrons were emitted to the gated channel, the trapped charge density was highest at the central interface part (125 nm in figure 3(b)). The highest trapped charge density of the acceptor-like (donor-like) trap states was approximately 10^{11} (10^{10}) cm^{-2} at D_{itA} (D_{itD}) = 10^{12} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. However, the trapped charge density was approximately 10^{8} cm^{-2} at the interface edge near the non-gated channel region (100 nm in figure 3(b)) at D_{itA} (D_{itD}) = 10^{12} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. Distributions of charges trapped at the interface edge nearby the source region are plotted in solid lines as a function of energy in figures 3(c) and (d) for the acceptor- and donor-like trap states, respectively; for comparison, distributions of interface trap states (plotted in dotted lines) are shown in these figures. For D_{itA} (D_{itD}) = 10^{12} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$, the trapped charge density peaked at 0.78 eV (0.35 eV) and its value was 8.6 × 10^{11} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ (4.7 × 10^{11} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$).

For the p-FBFET, the trap occupation mechanism was opposite to that of the n-FBFET (figure 3(e)). Electrons were supplied from the gated channel at V_{GS} = −0.35 V and V_{DS} = 1.0 V and then captured at the interface. Subsequently, electrons captured at the interface edge near the drain region were emitted to the drain region. Therefore, the trapped charge density of the acceptor-like trap states was the highest at the central interface part (75 nm in figure 3(f)),

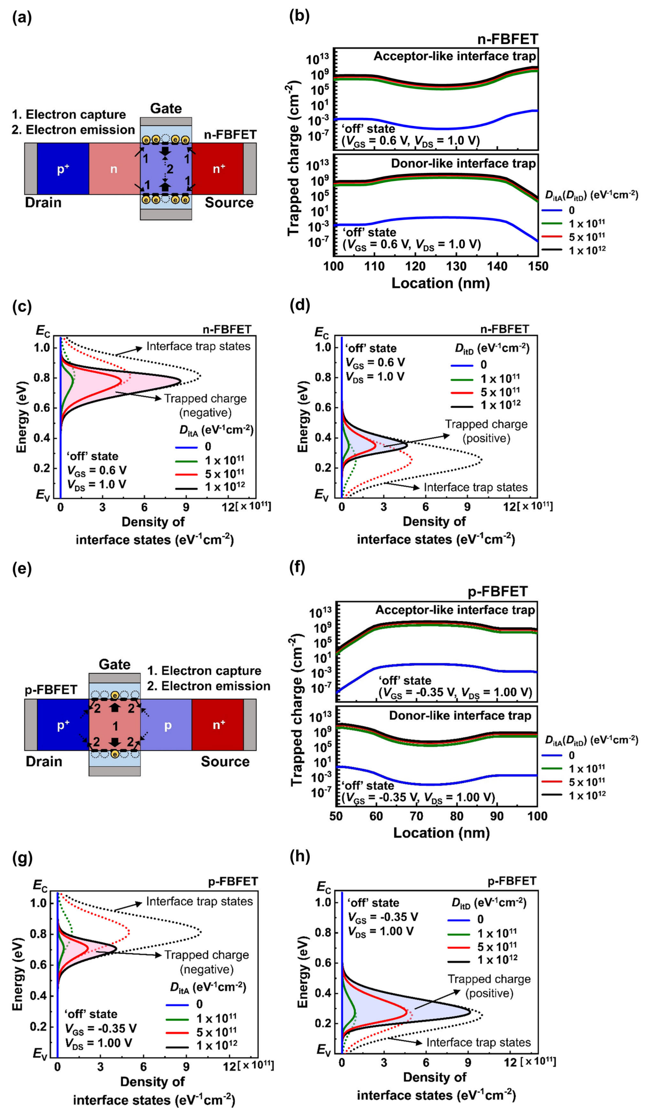

FIGURE 3. For n-FBFET, (a) schematic of trap occupation mechanism, (b) trapped charge densities along gated channel, and trapped charge density distributions of (c) acceptor- and (d) donor-like trap states. For p-FBFET, (e) schematic of trap occupation mechanism, (f) trapped charge densities along gated channel, and trapped charge density distributions of (g) acceptor- and (h) donor-like trap states.

whereas that of the donor-like trap states was the highest at the interface edge near the drain region (50 nm in figure 3(f)). For D_{itD} (D_{itA}) = 10^{12} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$, the highest trapped charge density was approximately 10^{11} (10^{10}) cm^{-2} for donor-like (acceptor-like) trap states. However, the trapped charge density was approximately 10^{8} cm^{-2} at the interface edge near the non-gated channel region (100 nm in figure 3(f)) when D_{itD} (D_{itA}) = 10^{12} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. The distributions of charges trapped at the interface edge near the drain region are plotted as solid lines as a function of energy in figures 3(g) and (h) for the acceptor- and donor-like trap states, respectively. For D_{itA} (D_{itD}) = 10^{12} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$, the trapped charge density peaked at 0.70 eV (0.27 eV) and its value was 4.1 × 10^{11} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ (9.1 × 10^{11} $\mathrm{eV}^{-1}\mathrm{cm}^{-2}$).

Note that the acceptor-like trap states are negatively charged, whereas the donor-like trap states are positively charged. These charged trap states at the interface between the gated channel and the oxide layer affect the potential barrier in the channel owing to Coulomb interaction. Moreover, they vary with the bias voltage, which causes variance in the electrical characteristics. The detailed variations are described in Section III-C.

C. ELECTRICAL CHARACTERISTICS VARIATION BY THE INTERFACE STATES

Figures 4(a) and (b) show enlarged transfer curves of the n-FBFET. As D_{itA} increased from 0 to 10^{12}eV^{-1}cm^{-2}, the latch-up voltage ($V_{latch-up}$) shifted from 0.637 to 0.649 V (figure 4(a)), whereas as D_{itD} increased to 10^{12} eV^{-1}cm^{-2}, $V_{latch-up}$ was marginally shifted by 0.001 V toward the lower voltage region (figure 4(b)). Consequently, the $V_{latch-up}$ variation depended on acceptor-like trap states rather than donor-like trap states. To investigate the $V_{latch-up}$ variation, we analysed the energy band diagrams under the 'off' state ($V_{GS} = 0.6$ V and $V_{DS} = 1.0$ V) before the latch-up. As shown in figure 4(c), as D_{itA} increased to 10^{12}eV^{-1}cm^{-2}, the conduction band in the non-gated channel and the valence band in the gated channel shifted by 0.006 and 0.008 eV toward the lower and higher energy regions, respectively. Thus, the height of the potential barrier in the channel region increased. The raised potential barrier height weakened the carrier injection, thereby causing a variation in the $V_{latch-up}$ of approximately 0.01 V when the acceptor-like trap states existed at the interface. However, as D_{itD} increased to 10^{12} eV^{-1}cm^{-2}, the energy shift in the valence band in the gated channel was negligible, whereas the conduction band of the non-gated channel shifted by 0.004 eV toward the lower energy region (figure 4(d)). Because the V_{GS} sweep controls the switching operation (figure 4(b)), the band modulation in the gated channel triggered a positive feedback loop. Thus, $V_{latch-up}$ varied negligibly when donor-like trap states existed at the interface, despite the lowered height of the potential barrier in the non-gated channel.

Figures 4 (e) and (f) show enlarged transfer curves of the p-FBFET. As D_{itA} increased to 10^{12} eV^{-1}cm^{-2}, the $V_{latch-up}$ shifted by 0.002 V toward the higher voltage region (figure 4(e)), whereas as D_{itD} increased from 0 to 10^{12}eV^{-1}cm^{-2}, the $V_{latch-up}$ shifted from −0.401 to −0.411 V. As shown in figure 4(g), as D_{itA} increased to 10^{12} eV^{-1}cm^{-2}, the increase in the height of the potential barrier in the gated channel was negligible before the latch-up. However, as D_{itD} increased to 10^{12} eV^{-1}cm^{-2}, the height of the potential barrier in the gated channel increased by 0.006 eV.

Accordingly, for the p- FBFET, the variation in the $V_{latch-up}$ was found to be more dependent on the donor-like trap states than on the acceptor-like trap states (for details, see supplementary information).

The height of the potential barrier in the non-gated channel was affected by both acceptor- and donor-like trap states for the n- and p-FBFETs; however, the height of the potential barrier in the gated channel was not. At the interface edge near the non-gated channel, the density of charge carriers trapped in the acceptor-like trap states was nearly the same as that of the donor-like trap states (figures 3(b) and (f)). For the n-FBFET, the negative (positive) charges trapped at the acceptor-like (donor-like) trap states induced Coulomb repulsion (attraction) to the n-doped non-gated channel, thus resulting in an increase (decrease) in the height of the potential barrier in the non-gated channel. The mechanism of the p-FBFET is opposite to that of the n-FBFET. The height of the potential barrier in the non-gated channel was lowered with the acceptor-like trap states, whereas it increased with the donor-like trap states. Although the non-gated channel did not significantly affect the $V_{latch-up}$ variance, it is important to the memory operation because the potential barrier variation of the channel induced current level variation [17].

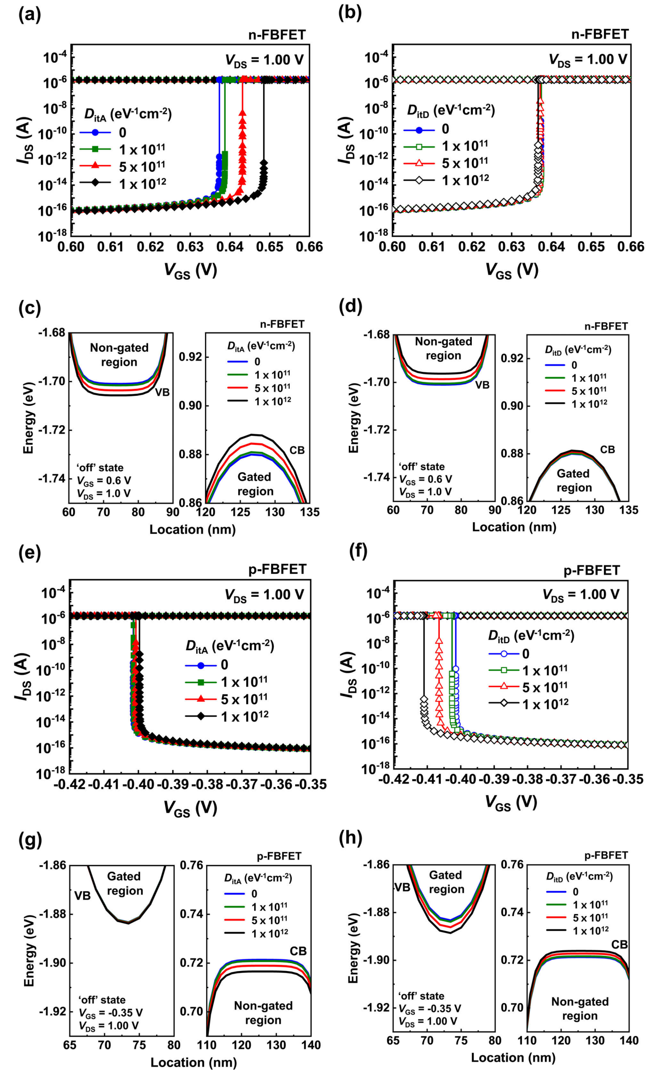

FIGURE 4. For n-FBFET, transfer curves depending on (a) acceptor- and (b) donor-like trap states. Enlarged energy band diagrams depending on (c) acceptor- and (d) donor-like trap states. For p-FBFET, transfer curves depending on (e) acceptor- and (f) donor-like trap states. Enlarged energy band diagrams depending on (g) acceptor- and (h) donor-like trap states.

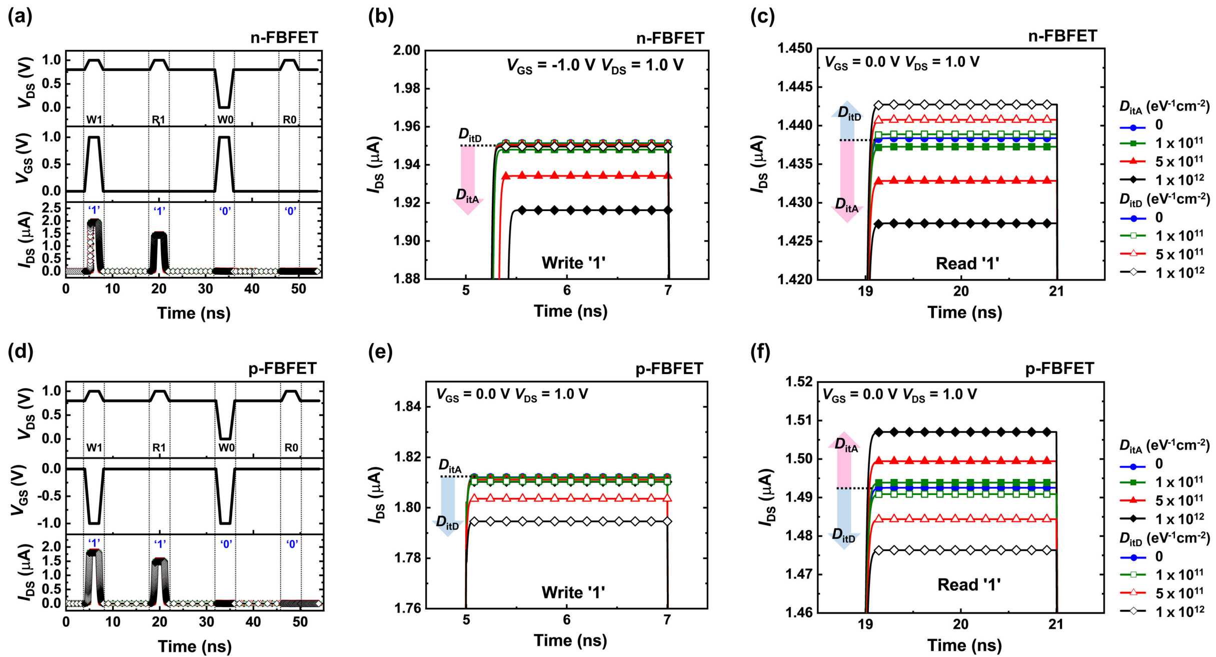

FIGURE 5. Timing diagrams for the memory operations of (a) n- and (d) p-FBFETs with the interface states. Enlarged drain currents of (b) n- and (e) p-FBFETs with the interface states during write '1' operation. Enlarged drain currents of (c) n- and (f) p-FBFETs with the interface states during read '1' operation.

TABLE 1. Memory operating conditions of the n- and p-FBFETs.

Device	Voltage	Write '1'	Write '0'	Read	Hold
n-FBFET	V_{DS} (V)	1.0	0.0	1.0	0.8
	V_{GS} (V)	1.0	1.0	0.0	0.0
p-FBFET	V_{DS} (V)	1.0	0.0	1.0	0.8
	V_{GS} (V)	−1.0	−1.0	0.0	0.0

Figures 5(a) and (d) show the timing diagrams for the memory operation of the FBFETs. The memory operation conditions are listed in Table 1. The write '1' ('0') operations accumulated (evacuated) excess charge carriers in the potential well in the channel. In the read '1' operation (with $V_{DS} = 1.0$ V and $V_{GS} = 0.0$ V), I_{DS} reached approximately 1.438 and 1.493 μA for the n-FBFET and p-FBFET, respectively. In the read '0' operations, I_{DS} was negligible because of the high potential barriers in the channel region. To investigate the variations in the memory characteristics, we analyzed the write and read operations of the n- and p-FBFETs. For the n-FBFET, in the write '1' operation, I_{DS} decreased as D_{itA} increased to 10^{12} $eV^{-1}cm^{-2}$. However, I_{DS} was not dependent on the donor-like trap state density (figure 5(b)). For the p-FBFETs, I_{DS} did not vary with D_{itA}, whereas I_{DS} was lower as D_{itD} increased (figure 5(e)). This observation is consistent with the variation in $V_{latch-up}$ (figure 4). However, the read '1' operations were affected by both acceptor- and donor-like trap states, differing from the write '1' operations, for both the n- and p- FBFETs. In the n-FBFET, I_{DS} decreased with increasing D_{itA}, whereas I_{DS} increased with increasing D_{itD} (figure 5(c)). In contrast, for the p-FBFET, I_{DS} increased whereas I_{DS} decreased with increasing D_{itD} (figure 5(f)). This is because the charges trapped at the interface affected the carrier mobility owing to Coulomb scattering [18], [19], [20]. The negative charges of the acceptor-like traps or the positive charges of the donor-like traps were present at the interface between the gated channel and the oxide layer, and these charges had Coulomb interaction with charge carriers flowing in the channel. The Coulomb interaction caused the surface scattering of charge carriers at the interface, indicating the Coulomb scattering. This Coulomb scattering degraded the mobility of charge carriers. Thus, the read current level was consistent with the variation in the potential barrier in both the gated and non-gated channels (figure 4).

The results show that the n- and p-FBFETs store the data '1' and '0' up to 900 s and that the acceptor- and donor-like trap states do not degrade the storage of the data (figure 6). Pulses with a time width of 4 ns were applied to the devices for the write and read operations. The hold bias of V_{DS} = 0.8 V maintained the presence (absence) of excess charge carriers, which determined the generation (elimination) of the positive feedback loop under the read condition. After holding operations for 900 s, the FBFETs exhibited recursive read operations despite the existence of acceptor- and donor-like trap states in the interfaces.

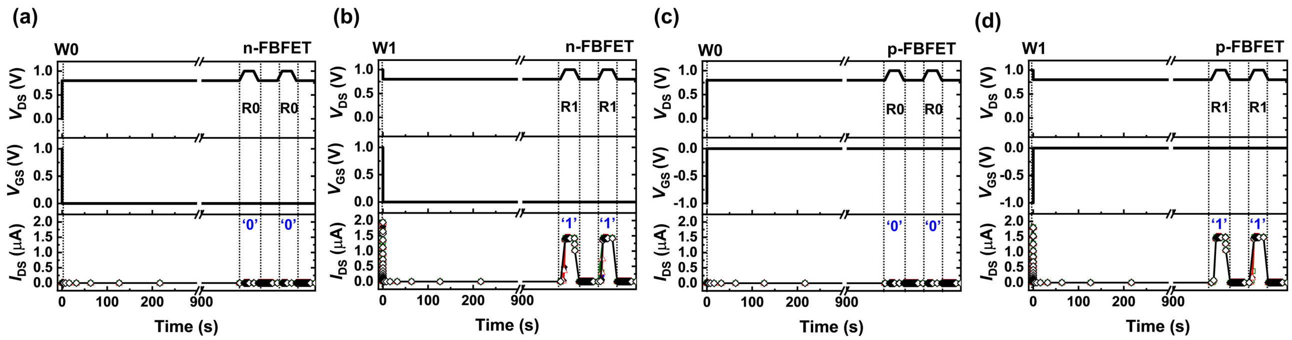

FIGURE 6. Retention characteristics of '1' for (a) n- and (c) p-FBFETs with the interface states under recursive read operations. Retention characteristic of '0' for (b) n- and (d) p-FBFETs with the interface states under recursive read operations. The data symbols and their color in this figure are the same as those in figure 5.

This study demonstrated variations in the $V_{latch-up}$ with trapped charges (both positive and negative) at the Si/SiO_2 interface. These resulted from the variation in the potential barrier height of the gated and non-gated channels of the FBFETs. Furthermore, the change in the t_{ox} affected the $V_{latch-up}$. As the t_{ox} changed, the oxide capacitance varied, leading to the change in the electric field in the gated channel and thereby the change in the gated channel potential. The change in the electric field caused the variation of the negative charge density for the acceptor-like trap states or the variation of the positive charge density for the donor-like trap states at the interface between the gated channel and the oxide layer. The variation of the trapped charge density changed the gated channel potential. The change in the gated channel potential affected the $V_{latch-up}$. (for details, see supplementary information). Nevertheless, the FBFETs exhibited a negligible $V_{latch-up}$ variation since the latch-up phenomenon occurs by the positive feedback mechanism rather than by interface traps. Because the FBFETs operate with the reciprocal interaction between potential barriers and charge carriers, the $V_{latch-up}$ varies negligibly even though the potential barrier varies with the interface trap states.

In general, performance variability has been observed in capacitorless memory devices because the interface states are related to surface recombination [14]. Retention degradation owing to the interface states has been reported experimentally, in particular, for other strained-silicon-on-insulator capacitorless single-transistor dynamic random-access memory cells [21]. Nevertheless, memory operations for FBFETs exhibit immunity against the interface states. Once the positive feedback loop is triggered, the feedback loop is maintained as long as the accumulated excess carriers exist in the channel, and the hold bias of 0.8 V compensates for the recombination of the carriers in the potential well. Thus, the rapid generation of a positive feedback loop enables stable and fast memory operations despite the interface states. Besides the FBFET-based memory, the immunity against the interface trap states ensures the realization of the FBFETs-based logic gates in the CMOS logic scheme [23], [24].

IV. CONCLUSION

We investigated the effects of the interface states on the electrical characteristics of n- and p-FBFETs. They exhibited the $V_{latch-up}$ variations when acceptor-like (donor-like) trap states were present at the Si/SiO_2 interface, whereas the effect of the donor-like (acceptor-like) trap states was negligible. These $V_{latch-up}$ variations were caused by the potential barrier modulation owing to the interaction with the trapped charge. Therefore, when the n- and p-FBFETs operated as memory, the I_{DS} values of the data '1' varied for the different trap densities. Nevertheless, the FBFETs exhibited an operating speed of 4 ns and retention time of 900 s, regardless of the presence of the interface states. The results verify the performance of the FBFETs in a practical environment.

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