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RESEARCH ARTICLE

A Compact Integrate-and-Fire Neuron Circuit Embedding Operational Transconductance Amplifier for Fidelity Enhancement

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ABSTRACT In this study, a compact CMOS integrate-and-fire (I&F) neuron circuit embedding an operational transconductance amplifier (OTA) has been designed for enhancing the fidelity in output generation. The OTA block in the neuron circuit allows for maintaining stability in I&F functions even under high-frequency operation conditions. The designed neuron circuit consists of OTA circuit, membrane capacitor, inverter, and reset MOSFET, from which the area occupancy is approximated to be $22 \times 43\ \mu m^2$. Featuring the simple and compact structure, the proposed neuron circuit shows the capability to control the firing frequency by adjusting the amplitude and temporal width of the synaptic pulse, resulting in high fidelity in I&F function. Series of circuit simulations have been performed to validate the systematic operations of the neuron circuit by HSPICE presuming the 0.35-μm Si CMOS technology. Moreover, temperature dependence was also investigated so that the robustness and stability of the neuron circuit at elevated operation temperatures were verified. The results provide a practical way of designing a compact and reliable neuron circuit working with the synaptic devices having deviations in operation characteristics in the hardware-oriented spiking neural network (SNN).

INDEX TERMS Integrate-and-fire neuron circuit, operational transconductance amplifier (OTA), fidelity, circuit simulation, stability, hardware-oriented spiking neural network (SNN).

I. INTRODUCTION

Advanced computing architecture is on explosive demand for dealing with the massive data processing, with an increased processing parallelism, for making good decisions under various circumstances. For this goal, brain-inspired neuromorphic computing has attracted a great deal of attention as a scalable, mobile, and energy-efficient solution that outperforms the conventional computers in Von Neumann computer architecture in data-intensive tasks such as recognition, classification, and perception [1], [2], [3], [4]. In particular, the neuromorphic computing architecture which mimics the human nervous system more actively, by introducing area and energy-efficient synaptic devices and neuron circuit, allows us to expect a dramatic reduction in power consumption in processing complex data and information [5], [6], [7]. While a synaptic device can be realized by a single memory component [8], [9], the neuron still needs to be implemented by circuitry for higher completeness in functionality and stronger stability in handling numerous fan-ins. There is much room to reduce the power consumption in neuron circuits for approaching the extremely high energy efficiency of the human brain [10], [11], [12]. From the viewpoint of digital electronics, the integrate-and-fire (I&F) function

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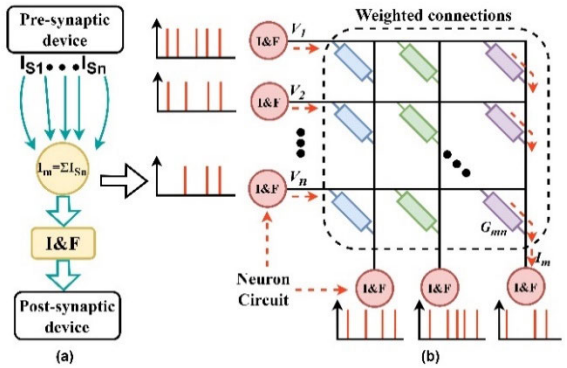

FIGURE 1. Schematic of the interneuron operation. (a) Signal flows showing the functions of synapse and neuron. (b) Symbolic representation of the pre- and post-synaptic neurons and synapse array.

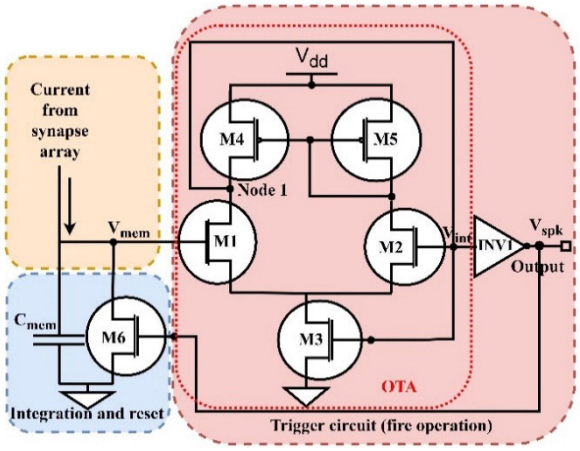

FIGURE 2. Circuit diagram of the designed I&F neuron circuit embedding an OTA block in this work.

might have analogy to analog-to-digital conversion (ADC) since the neuron accepts analog inputs and fires an identical output at every period of event [13]. On the other hand, in the biological neuron, the peculiarity lies in its autonomy in generating the output. The I&F neuron circuit realizes the autonomous pulse generation in the hardware manner in a way that it can fire an output signal modulating the interneuron connectivity only when the threshold is reached as the accumulation of charges is progressed [14], [15], [16]. In this sense, stability and robustness of a neuron circuit against the variation in electrical signals from the synapse array are essential for better predictability and reliability of the system.

In this work, a compact I&F neuron circuit embedding an operational transconductance amplifier (OTA) with full Si processing compatibility is designed, characterized, and evaluated by a series of circuit simulations. The compactness was achieved by reducing the number of components for higher area efficiency in comparison with the typical CMOS neuron circuits recently reported [17]. The OTA block was embedded for enhancing the output fidelity of the neuron circuit, and the responses to the inputs with variations in frequency were closely investigated in the design. In addition, the dependence of the firing behavior of the designed neuron circuit is further examined to ensure that system stability can also be expected at elevated temperatures under the proposed design scheme.

II. STRATEGIES IN DESIGNING THE NEURON CIRCUIT

The most striking similarity of the advanced computing architecture to the human brain calls for area efficiency, low power consumption, and a low training cost for realizing the extreme parallelism in massive data processing [18], [19]. For this goal, a more hardware-oriented spiking neural network (SNN) supported by I&F neuron circuits and synapse arrays are considered a plausible solution that enables event-driven computing [20], [21], [22], [23]. The mathematical and symbolic representations of the functions of neuron circuits and synaptic devices are schematically shown in Figs. 1(a) and (b). Memory devices with high scalability have been sought for the synaptic devices in hardware-oriented SNN to achieve high densities of synapse arrays and low power consumption while maintaining the tunability of multiple weights. Although memristors are commonly found in recent electronic synapse studies due to their high cell scalability and ease of process integration, there is still much room for improving the scalability, reliability, and reproducibility of Si processing for mass production at the chip level [24], [25], [26]. The operation of neuron circuits can be affected by variations in synapse arrangement and parameter distributions. Therefore, the non-uniformity must be considered in the neuron circuit design to improve the fidelity and robustness of operations to the environment. For the purpose, as OTA is applicable for ADC owing to its genuinely large output gain [27], [28], it can be introduced in designing a neuron circuit.

A. CIRCUIT DESCRIPTION

An I&F neuron circuit with an OTA block was designed as schematically shown in Fig. 2 and simulated using HSPICE. The design task was presumably based on 0.35-μm Si CMOS technology. The width and length of the n and p-type MOSFETs were $W = 0.35$ μm and $L = 0.7$ μm, respectively, and the drive voltage (V_{DD}) = 1.0 V. The membrane capacitance (C_{mem}) was 100 pF. The input current per event was assumed to be 1 μA. The neuron circuit consists of two parts: integration/reset part and trigger/fire one. In this work, the latter part is constructed by an OTA scheme. C_{mem} is responsible for integrating the current signals repeatedly delivered from the synapse array and can control the firing frequency depending on how fast it is charged. Also, C_{mem} determines dimensions of the NMOSFET, M6, that resets the neuron circuit. The membrane potential (V_{mem}) is increased until it reaches the threshold voltage (V_{th}) of the NMOSFET, M1, as the charges are accumulated in the membrane capacitor. As V_{mem} exceeds the V_{th} of M1, M1 is turned on, which causes the node 1 potential to become low (if it was originally high). Then, the potential of the inverter 1 (INV1) output

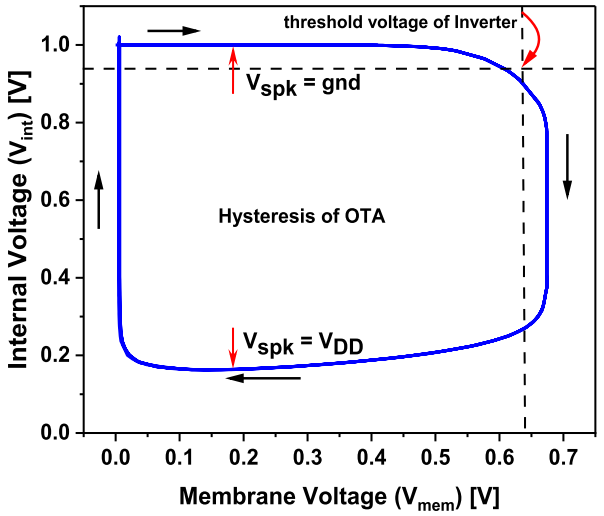

FIGURE 3. Hysteresis characteristic by the OTA block in the designed neuron circuit (V_{spk}: spiking node of the neuron circuit).

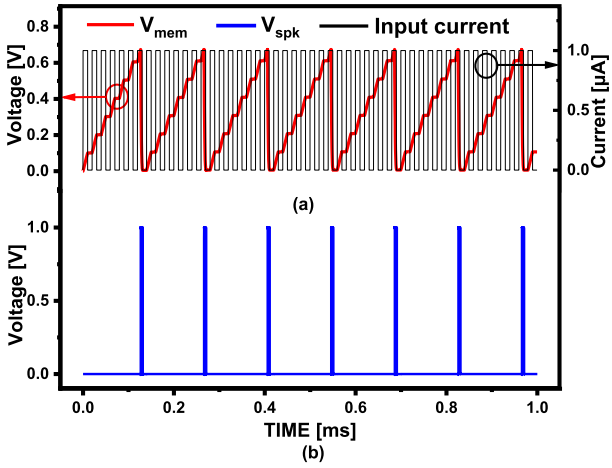

FIGURE 4. Transient analysis results of the designed I&F neuron circuit. (a) Input current and V_{mem} vs. time. (b) Spike firing at the neuron output as a function time.

node is switched from low to high state, turning on M6 and allowing the membrane capacitor in parallel with M6 to be discharged. The triggering part is embedding an OTA block, as shown in Fig. 2, which is basically a comparator consisting of a current mirror with two PMOSFETs, M4 and M5, and a differential pair circuit with two NMOSFETs, M1 and M2. In order to obtain a high-gain output from the OTA block, all the MOSFETs should be operated in saturation mode. As shown in Fig. 3, the OTA block demonstrates a positive feedback loop through the input node of INV1, resulting in the hysteresis between V_{mem} and the potential of the INV1 input node. As V_{mem} approaches V_{DD}, V_{int} tends to be gradually lowered and shows a sudden drop above the inverter threshold. The potential of the INV1 output node (or spiking node), V_{spk}, transits to high potential by the inverter operation, which in turn drags V_{mem} down to low potential by turning on M6. Over the hysteresis operations, shunting is continued until V_{mem} reaches 0 V, the ground potential. The ground potential is achieved with a certain amount of time delay. During this time, the output voltage V_{spk} remains at V_{DD}, while the output is connected to ground out of this time period. As a consequence, the OTA-embedded circuit explicitly demonstrates the I&F behavior, which makes it effectively work as a neuron circuit. The beneficial feature of the designed neuron circuit with the OTA function block comes with the capability of performing the I&F at higher speed with the frequency tunability.

B. VERIFICATION OF THE I&F BEHAVIORS

The integration and fire operations of the designed neuron circuit were verified by HSPICE and shown in Fig. 4(a) and (b),

$$I_{in} \cdot T_{pulse} = \Delta V_{mem} \cdot C_{mem} \tag{1}$$

$$\Delta V_{mem} = \frac{I_{in} \cdot T_{pulse}}{C_{mem}} \tag{2}$$

respectively. The integration was carried out by input currents of I_{in} (amplitude) = 1 μA and T_{pulse} (period) = 10 μs. C_{mem} was set to 100 pF so that the change in V_{mem} could be 0.1 V, as an arbitrary value, by the results calculated by Eq. (1) and (2) with the given I_{in} and T_{pulse}. The increment in V_{mem} of 0.1 V over the current integration can be confirmed by Fig. 4(b) and the integration is continued until V_{mem} reaches the V_{th} of M1. Once V_{mem} exceeds the V_{th} of M1, an output spike is fired at the output terminal of INV1 as shown in Fig. 4(b). At this moment, M6 is switched on, and the membrane capacitor is shortly discharged so that the initial state of the neuron circuit is established (reset). V_{spk} denotes the output signal of the designed neuron circuit and plays the role of the input signal modulating the weight of a synaptic device connected to a post-synaptic neuron in the end. It is observed that the amplitudes of the output spikes fired from the neuron circuit are maintained, and thus, the presented neuron circuit shows the output stability throughout the observation window.

III. CHARACTERIZATION AND EVALUATION OF NEURON CIRCUIT

A. DEPENDENCY OF SPIKE FIRING ON SYNAPTIC CURRENT

The synapse array in the SNN architecture usually has a high density of memory cells. Thus, the operation parameters of the synaptic device have deviations that make up a statistical distribution rather than a uniquely located sharp distribution. As a result, the frequency of firing events at the neuron circuit always reflects the imperfections in the synaptic operations in the synapse array. As a simple scenario, the number of firing spikes in the required time from the designed I&F neuron circuit depends on the amplitude and the temporal width of the current pulse from the synapses. The dependencies of the firing spikes are shown in Fig. 5(a) and (b). The larger the amplitude or temporal width of the current from synaptic device, I_{synaptic}, the shorter the time for V_{mem} to reach the firing threshold voltage gets. As a result, the number of firing spikes in each time increases. The number of firing spikes

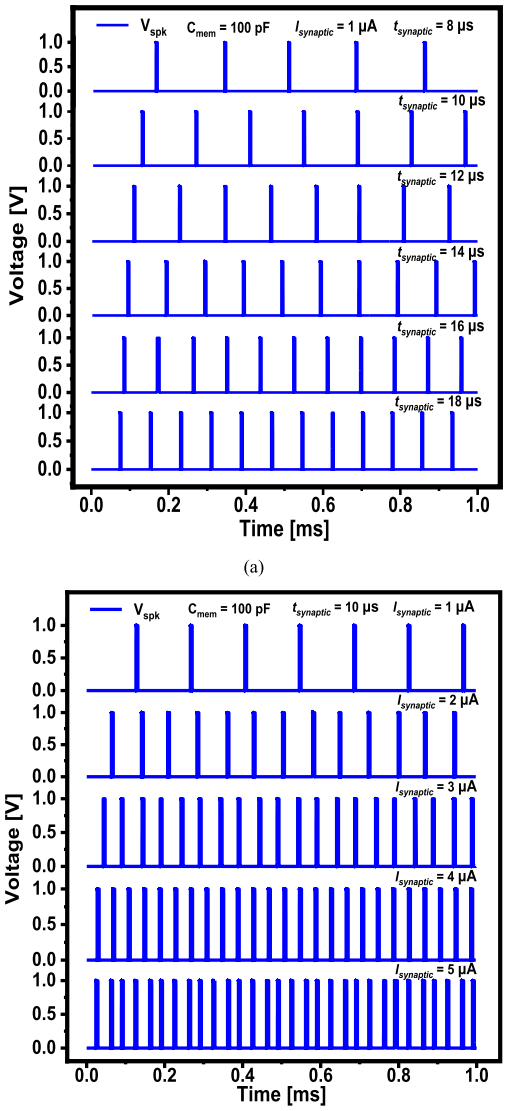

FIGURE 5. Number of firing spikes as a function of time (a) at different temporal width ($t_{synaptic}$) of the synaptic input currents ($I_{synaptic}$ = 1 μA), from 8 μs to 18 μs by an increment of 2 μs and (b) at different $I_{synaptic}$ amplitudes from 1 μA to 5 μA by an increment of 1 μA ($t_{synaptic}$ = 10 μs).

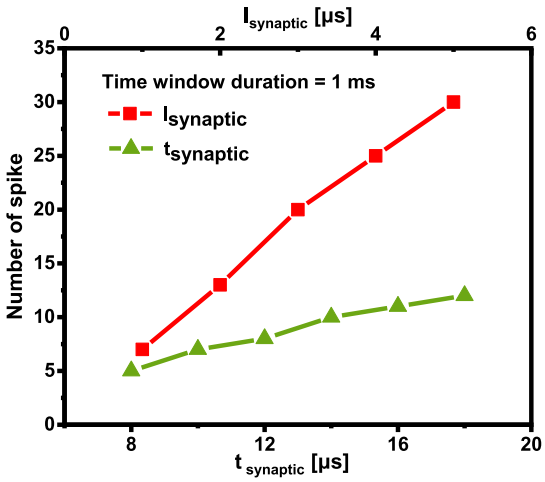

FIGURE 6. Number of firing spike as a function of the time width and amplitude of the $I_{synaptic}$ pulses.

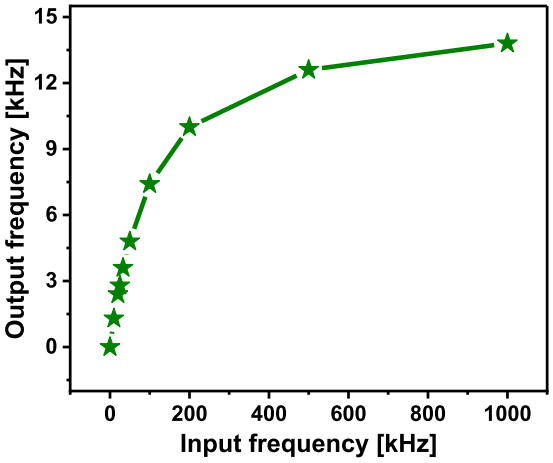

FIGURE 7. Input vs. output frequency in the designed I&F neuron circuit for the duration of 1 ms.

increased from 5 to 12 within a 1-ms window as the time width of I_{synaptic} pulses with an amplitude of 1 μA was widened from 8 μs to 18 μs (increased with an interval of 2 μs), as depicted in Fig. 5(a). Also, the number of firing spikes increased from 7 to 30 in the given time window of 1 ms as I_{synaptic} was increased from 1 μA to 5 μA with a temporal width of the I_{synaptic}, t_{synaptic}, was set to 10 μs as shown in Fig. 5(b). $C_{\text{mem}} = 100$ pF was maintained.

Fig. 6 shows how sensitively the firing rate can be affected by the variation in temporal width and amplitude of the synaptic current. As the temporal width gets about two times larger (8 μs $\rightarrow$ 18 μs), the number of firing events shows a two-fold increase (5 $\rightarrow$ 12) (green curve). This can be understood by Eq. (1) in which the temporal width and the change in membrane potential are in the linear relation so that wider temporal width shortens the firing period and increases the number of spikes in each time in the linear manner. Also, the firing rate shows a proportional increase with the amplitude of input current and the underlying reason can also be grasped by Eq. (2). Since the amplitude of input current is in the proportional relation with the change in membrane potential, the ratio of increase in I_{synaptic} (1 μs $\rightarrow$ 5 μs) and that of increase in number of firing spikes (7 $\rightarrow$ 30) are comparable.

B. DEPENDENCY OF SPIKE FIRING ON SYNAPTIC CURRENT

A series of circuit simulations have been carried out with variations in the frequency of the input current to evaluate the output frequency and fidelity of the designed neuron circuit. Featuring the OTA block in the neuron circuit, it became possible to preserve the I&F function even under a high-frequency operation of 1 MHz, as depicted in Fig. 7. It is notable that the increase in output frequency is ranged only up to 15 kHz when the input frequency goes higher, up to 1 MHz. Thus, the overall firing events take place insensitively to the change in input frequency. Further, in the relative high input

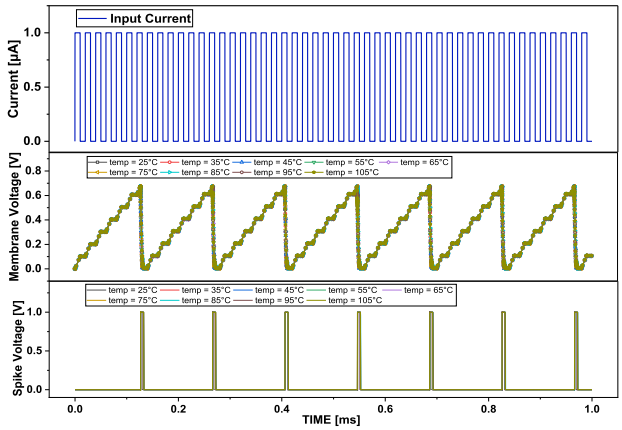

FIGURE 8. Temperature dependence of the I&F operations in the designed neuron circuit.

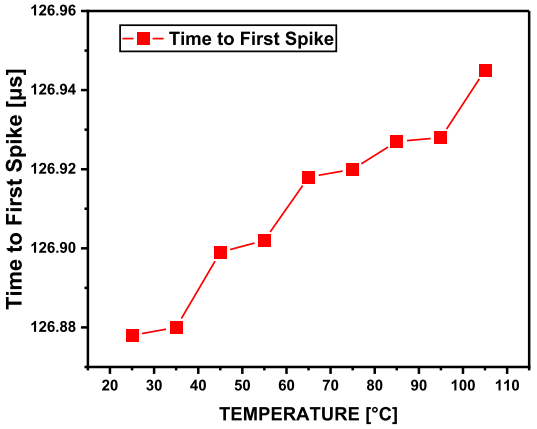

FIGURE 9. Time-to-first spike (TTFS) as a function of temperature.

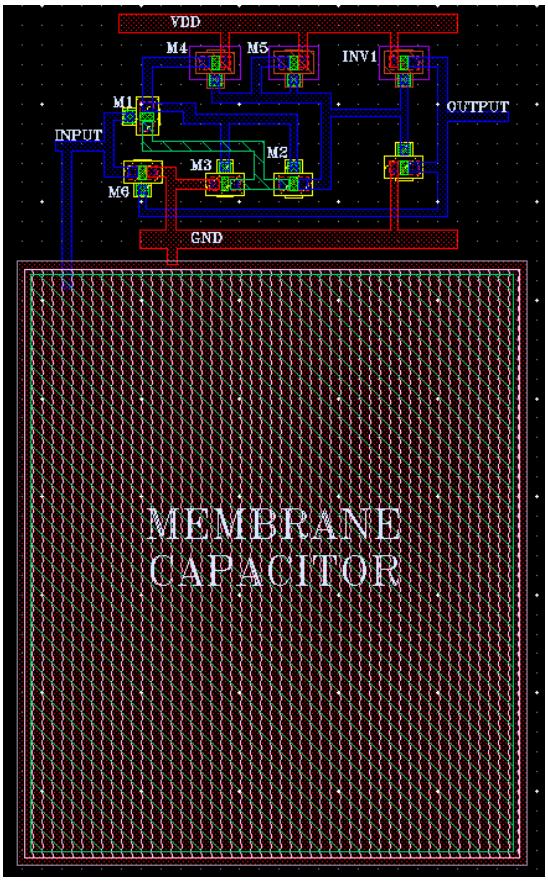

FIGURE 10. Presumably designed layout of the I&F neuron circuit.

frequency region between 500 kHz and 1 MHz, the output frequency shows saturation and a small corresponding change within 3 kHz is merely observed as shown in Fig. 7. Thus, it can be addressed that the designed neuron circuit equips the capability of dealing with higher input frequency in realizing the I&F operations, with higher output stability.

Further, dependence of the I&F neuron circuit operations on change in temperature is thoroughly investigated in Fig. 8. It is revealed that the characteristics of the presented neuron circuit are maintained up to 105 °C without a significant change in time for the appearance of the first spike by the help of genuine operational merit of the differential pair in the OTA block. As the differential-pair voltages of the OTA block go in different directions due to their opposite polarity configurations, the temperature effect follows in the same way. Thus, it cancels out the effect of temperature variation in the neuron circuit. As a result, the proposed neuron circuit accompanies a strong robustness in the operations at high temperatures as well. Fig. 9 depicts time-to-first-spike (TTFS) as a function of temperature. In order for a more quantitative analysis, gradient of TTFS can be further defined:

$$R_{TTFS} = \frac{t_{temp,\max} - t_{temp,\min}}{(T_{\max} - T_{\min}) \cdot t_{temp,room}} \tag{3}$$

More specifically, R_{TTFS} is the gradient of TTFS normalized by the TTFS at room temperature in terms of temperature as defined in Eq. (3) and is expressed in the unit of $^{\circ}\mathrm{C}^{-1}$. Here, $T_{\max}$ and $T_{\min}$ are the boundaries of temperature of interest, which correspond to 105 °C and 25 °C, respectively. $t_{\mathrm{temp,max}}$ and $t_{\mathrm{temp,min}}$ are the TTFS values at the boundary temperatures. $t_{\mathrm{temp,room}}$ is the TTFS at room temperature, 27 °C. From the values obtained in Fig. 9, R_{TTFS} is calculated to be $6.6 \times 10^{-6}/^{\circ}\mathrm{C}$ between 25 °C and 105 °C, over a wide operational temperature window of 80 °C. It is confirmed that the neuron circuit has a strong robustness against the change in operation temperature. Fig. 10 shows a presumable layout design of the proposed neuron circuit based on 0.35-μm CMOS technology. Although the overall circuit can be schemed to be simple with a small number of component, most of the area is dedicated to the membrane capacitor. The truncation of the secondary (shunt) capacitor usually found in the triggering part in the conventional neuron circuit has been made possible by introducing the OTA block for capacitorless triggering part and a great deal of area reduction has been achieved. The total area of the layout in Fig. 10 is calculated to be 22×43 $\mu\mathrm{m}^2$. This presumable layout work made without any violation of design rule would provide a tangible prediction in fabricating the hardware spiking neural network chip.

IV. CONCLUSION

In this work, a fully Si processing-compatible compact I&F neuron circuit featuring an OTA subcircuit has been designed and evaluated through HSPICE simulations, based on 0.35-μm CMOS technology. The benefit of the OTA function in the neuron circuit has been primarily found as its higher output fidelity. The behaviors of the designed neuron circuit have been closely investigated through varying the amplitude and temporal width of the synaptic input current. The firing frequency shows linear relations with the variables associated with the input current profile as expected by the mathematical foundation, which proves that the OTA block works adequately in comparison with the conventional neuron circuit. Also, it has been revealed that the output frequency of the OTA-embedded neuron circuit is rather insensitive to the change in input frequency. Last but not the least, the temperature tolerance of the designed neuron circuit has been evaluated. The results demonstrate that only a small retardment within 70 ns in time-to-first spike occurs over the controlled temperature range from 25 °C up to 105 °C, which ensures the strong temperature robustness of the proposed neuron circuit. The OTA cell can be a plausible function block for making up an area-efficient CMOS neuron circuit working with imperfections of the synaptic devices in the hardware-sense SNN architecture.

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