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RESEARCH ARTICLE

Reduction of Phase and Gain Control Dependencies Within a 20 GHz Beamforming Receiver IC

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ABSTRACT This paper studies the phase and gain control dependencies of a variable gain amplifier (VGA) and a vector interpolator phase shifter (VIPS) within a 20 GHz beamforming receiver. First, the mechanisms of gain control and phase variation in a classic current-steering VGA are analyzed and design techniques are proposed such that the gain-dependent phase variations (GDPV) introduced by the amplifiers are well balanced. Second, similar analysis is performed to evaluate GDPV within a vector interpolator, where we show how the same techniques only partially apply due to the cross-coupling structure of the interpolator's VGAs. We evaluate our techniques within a 20 GHz beamforming receiver IC realized in GlobalFoundries 45 nm RFSOI. Very low GDPV is observed within the VGA, with less than 0.3-deg. root-mean squared phase variation for a 9 dB gain control, whereas the VIPS achieves worst-case GDPV of 14 deg. The full beamformer channel achieves 29 dB gain, 2.2-2.4 dB noise figure, -26 dBm input 1 dB compression and consumes 111 mW. Based on these results, improvements to the interpolator are proposed and validated through simulation. The result is a near-ideal Cartesian interpolator that has less than 2-deg. GDPV and very low crosstalk between the VGAs.

INDEX TERMS Variable gain amplifier (VGA), vector interpolator, phase shifter, gain dependent phase variation, IQ crosstalk, CMOS, SOI, beamformer, phased arrays.

I. INTRODUCTION

Phased arrays are widely used in satellite-terrestrial communications [1] and 5G cellular communications [2]. These arrays must provide accurate gain and phase control together with suitable RF performance. Depending on the architecture used within the beamforming IC (BFIC), the circuits can exhibit unwanted gain and phase dependencies, where controlling the amplitude introduces unwanted phase shift and controlling the phase introduces unwanted amplitude shift. These effects are illustrated in Fig. 1 for a typical receiver (RX) array. Ideal orthogonal gain and phase control is shown in Fig. 1(b) whereas more common gain and phase interdependency is shown in Fig. 1(c).

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Techniques to reduce gain-dependent phase variation (GDPV) in variable-gain amplifiers (VGAs) and vector interpolating phase shifters (VIPS) have been studied in prior literature, though detailed analysis is often omitted. For digital-controlled VGAs, resonant [3] or switched-transistor techniques [4] have been used to manage the parasitic capacitance that would otherwise cause GDPV. Likewise, in analog-controlled current-steered VGAs, a variety of techniques have been used to reduce GDPV such as cross-coupled neutralization [5], capacitor compensation [6], RC compensation [7], inductor compensation [8], [9], and second-stage amplifier compensation [5], [10]. However, all these works require additional circuitry that can increase the design complexity, calibration complexity, footprint and/or power consumption. Similar non-ideal gain and phase control also are common in VIPS circuits [11], [12], [13] which may increase calibration complexity. For example, in a

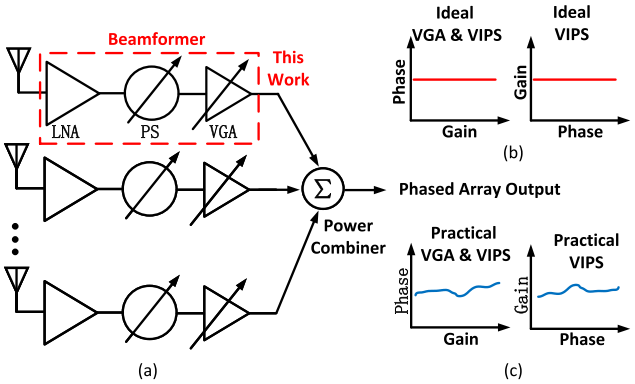

FIGURE 1. (a) Block diagram of a typical phased-array receiver system. (b) Ideal phase/gain controls. (c) Practical phase/gain controls.

recent calibration technique [14], the behaviors of the phase shifter have to be accurately modeled otherwise errors are introduced in the calibrated results. More ideal VIPS behavior can simplify or eliminate calibration and simplify overall beamformer design.

The contributions of this paper are summarized as follows:

1. The current-steering VGA GDPV principles are analyzed in depth for the first time. In contrast with other works where additional phase compensation circuits are required, we propose a new design methodology such that no extra circuitry is needed to achieve near zero GDPV. A 20 GHz VGA with 9 dB gain tuning range is designed and measured. It achieves $< 1^\circ$ root-mean squared (RMS) GDPV across 15.6% fractional bandwidth.

2. The VIPS GDPV mechanisms are then investigated using the same analysis above. Methods are presented for achieving more ideal vector interpolation, and these are demonstrated in measurement using the same 20 GHz beamforming receiver element. In addition, new techniques are introduced to achieve nearly zero GDPV and zero I/Q cross-talk and these are demonstrated through simulation.

The paper is organized as follows. Section II presents an overview of the beamformer architecture; Section III presents new design approaches for VGA with low GDPV; Section IV applies these same analysis to the VIPS; Section V presents measurement results for a 20 GHz beamforming element; and Section VI concludes. In the Appendix, additional approaches for achieving near ideal vector interpolation are presented and validated using simulation.

II. RECEIVER ELEMENT ARCHITECTURE

The 20 GHz RX element employs a traditional architecture, using a low-noise amplifier (LNA), a VIPS, and a VGA [15], [16], [17]. Each element is designed for integration into four-element BFICs that can then be tiled at board level to construct larger arrays [18]. The design goals for the BFIC are to achieve 28 dB electronic gain, 2.2 dB front-end noise figure (NF), -26 dBm input-referred 1-dB compression point (iP_{1dB}), 6-bit phase shifter resolution across a 360° range, 0.75 dB VGA resolution across a 9 dB range, $<$ 0.2 dB RMS gain error, and $<$ 2° RMS phase error across a 19.2-21.2 GHz (1 dB bandwidth) frequency range.

A schematic of the beamforming receiver element is shown in Fig. 2. This design is implemented in GlobalFoundries 45nm RFSOI technology with transformers, inductors, and parasitic optimization designed using EMX [19]. All individual component values are indicated on the schematic in the associated tables, where all transistors are designed using 40 nm channel length. Additionally, on-chip transmission lines typically have 50 Ω impedance.

The first stage of the element is a two-stage LNA, designed for minimum NF and moderate gain at 20 GHz. In simulation, it achieves 18.7 dB gain with 1.7 dB NF, −14.6 dBm iP_{1dB}, while consuming 20 mW power from a 1 V supply. Following the LNA is the VIPS, consisting of a lumped-element realization of a Lange coupler, two baluns, and then in-phase (I) and quadrature-phase (Q) VGAs, whose outputs are combined within an output transformer. The VIPS is designed to achieve 0 dB gain, 12 dB NF, −2 dBm iP_{1dB}, while consuming 54 mW power from a 1.8 V supply. Finally, the element includes a differential VGA that is designed to achieve 9 dB maximum gain, 0 dB minimum gain, 3.5 dB NF, $< 2^\circ$ GDPV, and above −5.5 dBm iP_{1dB}, while consuming 27 mW power from a 1.8 V supply. The differential output of the VGA is converted to single-ended with a balun. The variable amplifiers within the beamforming element are designed to achieve low GDPV using the techniques that follow.

III. VGA ANALYSIS

In this section, we analyze the GDPV of the current-steering VGA and present a transconductance (G_m) and load optimization design technique such that the phase variations are well balanced and canceled. In this way, we achieve low phase variation by leveraging the circuit's own properties without adding any other elements.

A. VGA MECHANISMS

The classic fully-differential, current-steered VGA is the final block in Fig. 2. T_{V0} is the differential G_m cell for the RF input. The cascode devices, T_{V1} and T_{V2}, are the current commutator for gain tuning, controlled by differential control voltage ΔV, where T_{V2} directs current to the load and T_{V1} directs current to the supply. I_{V1} and I_{V2} are the DC currents of T_{V1} and T_{V2}, respectively, with $I_{V1}+I_{V2}=I_{V0}$. Since I_{V0} is constant regardless of the gain tuning, the input impedance and the small-signal parameters related to T_{V0} are largely independent of gain tuning.

To understand the VGA's working principle, we perform a small-signal analysis on an equivalent half-circuit shown in Fig. 3. The overall gain of the circuit can be written as

$$Gain\,(\omega)=\frac{v_{out}\,(\omega)}{v_{in}\,(\omega)}=g_{m0}\cdot Z_{Eq}\,(\omega)\,, \tag{1}$$

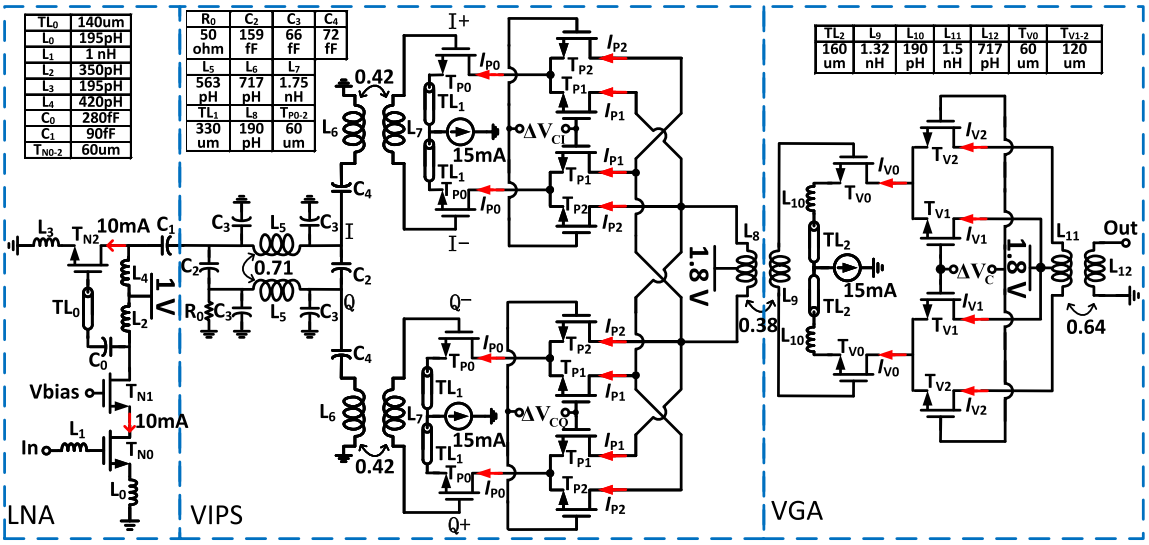

FIGURE 2. Schematic of the beamformer receiver channel which is composed of an LNA, a VIPS and a VGA.

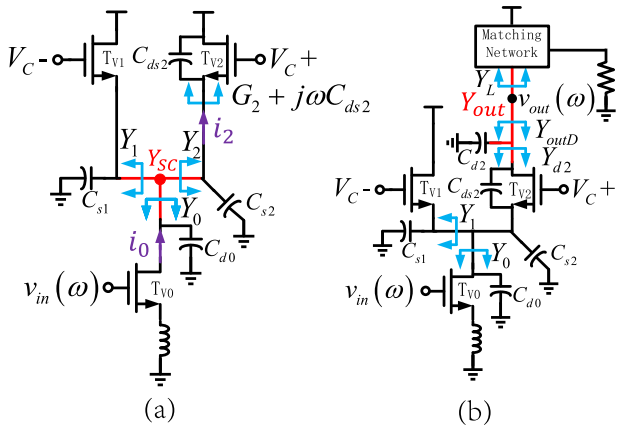

FIGURE 3. (a) Small signal current analysis of the current steering VGA. (b) Admittance analysis of the current steering VGA.

where an equivalent transimpedance is defined to capture all gain dependencies, as follows:

$$Z_{Eq}(\omega) = \frac{v_{out}(\omega)}{i_0(\omega)} = \frac{G_2 + j\omega C_{ds2}}{Y_{SC}(\omega)} Z_{out}(\omega). \quad (2)$$

This includes a current division ratio in admittance form times the output impedance, both of which will vary as a function of gain setting. G_2 is a gain-dependent transconductance through T_{V2} (equal to $g_{m2} + g_{ds2}$) and Y_{SC} is the intermediate node admittance with the output load shorted, as shown in Fig. 3(a)).

G_2 is the predominant term in the gain tuning and we can coarsely predict the VGA gain behavior by evaluating G_2 as ΔV_C changes. When $\Delta V_C = 0$, DC current I_{V0} is equally split between T_{V1} and T_{V2}; thus, G_2, Z_{Eq}, and *Gain* are all at their minimum values. When ΔV is maximum, T_{V1} is off and DC current I_{V0} is fully steered to T_{V2}; thus, G_2, Z_{Eq} and *Gain* are at their maximum values

The total gain tuning range $\Delta Gain(\omega)$ is defined as

$$\Delta Gain(\omega) = g_{m0} \left| Z_{EqLow}(\omega) - Z_{EqHigh}(\omega) \right|. \quad (3)$$

Likewise, the GDPV can be calculated as follows:

$$\begin{aligned} &\Delta\angle Gain(\omega) \\ &\quad = \Delta\angle Z_{Eq}(\omega) \\ &\quad = \Delta\angle (G_2 + j\omega C_{ds2}) - \Delta\angle Y_{SC}(\omega) + \Delta\angle Z_{out}(\omega), \end{aligned} \quad (4)$$

where the Δ operator is evaluated between the minimum and maximum gain settings. As shown, GDPV is composed of three terms: the phase variation of T_{V2}'s transadmittance, the phase variation of the intermediate node impedance with output load shorted, and the phase variation of the output node impedance. In the following subsections, we analyze each term and discuss a method to cancel the variation.

B. GDPV ANALYSIS OF CURRENT SPLITTING

We begin with the GDPV associated with the current splitting, i.e., the $G_2 + j\omega C_{ds2}$ and Y_{SC} terms. Both have phase variation due to g_{m1} and g_{m2} varying. In both cases, we recast the admittance as $Y(\omega) = G \cdot (1 + jQ(\omega))$, where a quality factor and the associated time constant are

$$Q(\omega) = \omega\tau = \frac{\omega C}{G}. \quad (5)$$

The phase of Y is arctan (Q) and phase variation is therefore arctan (Q_{Low}) − arctan $(Q_{High}) \approx \Delta Q$. This approximation is valid for small Q values. The overall phase variation can then be approximated as

$$\Delta\angle Y \approx \Delta Q(\omega) = \omega \cdot \Delta\tau = \omega \left(\frac{C_{Low}}{G_{Low}} - \frac{C_{High}}{G_{High}} \right) \quad (6)$$

For GDPV from $G_2 + j\omega C_{ds2}$, we know that $G_{2High} > G_{2Low}$ and $C_{ds2High} \approx C_{ds2Low}$. Thus, we approximate

$$\Delta\angle (G_2 + j\omega C_{ds2}) \approx \omega \cdot \Delta\tau_{G2} > 0, \quad (7)$$

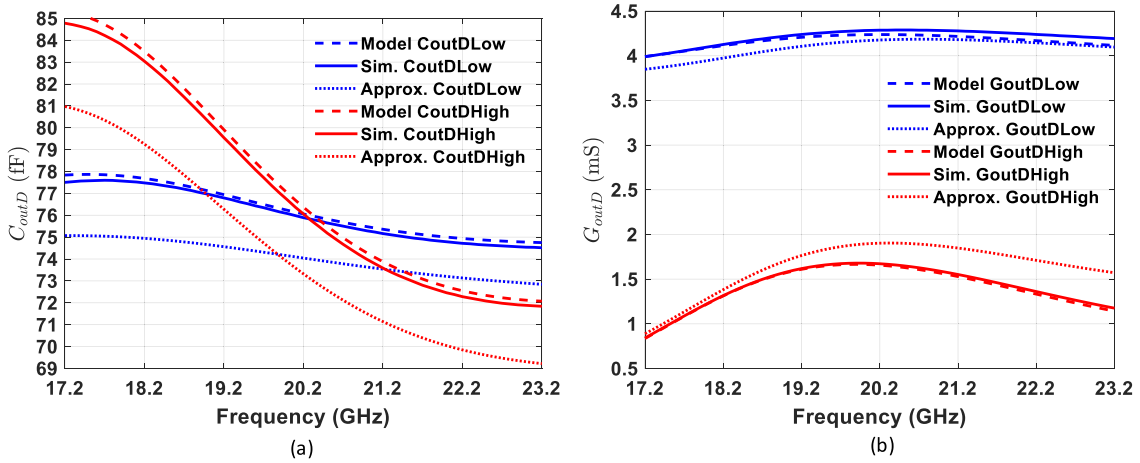

FIGURE 4. (a) Capacitance (model and approximation according to (11) and (13), respectively) and (b) conductance (model and approximation according to (11) and (12), respectively) looking down from T_{V2} drain terminal in the lowest and the highest gain settings.

indicating that the phase of the low-gain mode leads that of the high-gain mode.

For GDPV from Y_{SC}, from Fig. 3(b), we define the intermediate node admittance as follows:

$$Y_{SC}(\omega) = G_{012}(\omega) + j\omega\left(C_{012}(\omega) + C_{ds2}\right), \tag{8}$$

where $G_{012}(\omega) = G_{d0}(\omega) + G_1 + G_2$ is the total conductance at this node and $C_{012}(\omega) = C_{d0}(\omega) + C_{s1} + C_{s2}$ is the total capacitance to ground. Given that $C_{012High} \approx C_{012Low}$ and $G_{012High} < G_{012Low}$ (since g_{m1}+g_{m2} in low-gain mode with current equally split is larger than g_{m2} in high-gain mode with all current steered to T_{V2}), the *negative* of phase variation of Y_{SC} is calculated as:

$$-\Delta\angle Y_{SC}(\omega) \approx \omega \cdot |\Delta\tau_{SC}(\omega)| > 0. \tag{9}$$

Overall, the GDPV of the current splitting function is seen to be positive, equal to $\omega(\Delta\tau_{G2}(\omega) + |\Delta\tau_{SC}(\omega))|$.

C. GDPV ANALYSIS OF THE OUTPUT IMPEDANCE

As shown in Fig. 3(b), the output admittance $Y_{out}(\omega)$ is

$$Y_{out}(\omega) = Y_L(\omega) + Y_{outD}(\omega), \tag{10}$$

where $Y_L(\omega)$ is the output load admittance and $Y_{outD}(\omega)$ is the admittance looking into the T_{V2} drain terminal:

$$\begin{aligned} Y_{outD}(\omega) &= \frac{y_{ds2}(\omega)\left(Y_0(\omega) + Y_1(\omega) + j\omega C_{s2}\right)}{Y_{SC}(\omega)} + j\omega C_{d2} \\ &= G_{outD} + j\omega C_{outD} \end{aligned} \tag{11}$$

with $y_{ds2} = g_{ds2} + j\omega C_{ds2}$. From this, the corresponding output conductance G_{outD} and capacitance C_{outD} are

$$G_{outD}(\omega) \approx \frac{\left(G_0(\omega) + G_1\right)\left(G_0(\omega) + G_1 + G_2\right) g_{ds2}}{|Y_{SC}(\omega)|^2} \tag{12}$$

$$C_{outD}(\omega) \approx \frac{G_2 g_{ds2} C_{012}(\omega)}{|Y_{SC}(\omega)|^2} + \frac{G_{outD}}{g_{ds2}} C_{ds2} + C_{d2} \tag{13}$$

respectively, where $G_1 = g_{m1} + g_{ds1}$ and where the approximations are made by neglecting the second-order terms in the numerators. Although complicated, these expressions indicate how the output admittance varies with gain.

A first target is to keep $C_{outD}(\omega)$ invariant of gain tuning such that $Y_L(\omega)$ will always resonate with it, resulting in constant output matching under all the gain settings. The device capacitances remain relatively constant versus gain; however, G_1 reduces significantly as gain increases ($G_1 = 0$ at the highest gain mode where T_{V1} is OFF). When the gain is increased, the increase in G_2 needs to be large enough to balance the G_1 reduction such that $C_{outD}(\omega)$ can be kept consistent. This is achieved by biasing T_{V1} and T_{V2} near threshold at the low-gain mode and then biasing T_{V2} towards/in saturation region in high-gain mode. To realize this biasing scheme, the widths of T_{V1} and T_{V2} are designed to be large (double the width of T_{V0}). We note that with appropriate biasing, G_2 increases by 70% and as a result $C_{outDLow}(\omega) \approx C_{outDHigh}(\omega)$ is achieved around 20.2 GHz as shown in Fig. 4(a). This $C_{outD}(\omega)$ based T_{V2} bias-point G_m optimization also affects $\Delta\angle Y_{SC}(\omega)$ and $\Delta\angle\left(G_2 + j\omega C_{ds2}\right)$ from before. It reduces $\Delta G_{012}(\omega)$ and $|\Delta\tau_{SC}(\omega)|$ and increases $\Delta\tau_{G2}$.

We now have a condition where the output resonance is kept consistent across gain settings; however, there is still GDPV in the output admittance due to the variation in G_{outD}, as shown in Fig. 4(b). Our strategy is to use this GDPV in Y_{out} to cancel the GDPV from the current splitting.

In particular, the output admittance $Y_{out}(\omega)$ is modeled as a shunt RLC and calculated as:

$$\begin{aligned} Y_{out}(\omega) = &\underbrace{\left(G_L(\omega) + G_{outD}(\omega)\right)}_{G_{out}(\omega)} \\ &+ j\underbrace{\left(\omega\left(C_L + C_{outD}(\omega)\right) - \frac{1}{\omega L_L}\right)}_{B_{out}(\omega)}, \end{aligned} \tag{14}$$

where $G_L(\omega)$, C_L and L_L are the lumped-element model of the load conductance, capacitance and inductance. Accordingly, the phase variation of the output admittance

$\Delta\angle Y_{out}(\omega)$ is calculated using Q-factor differences as in (6), where at the resonance frequency ω_{out}, we have

$$Q_{out}(\omega_{out}) = \omega_{out}\frac{C_L + C_{outD}(\omega_{out})}{G_{out}(\omega_{out})} = \omega_{out}\frac{\tau_{out}(\omega_{out})}{2}, \tag{15}$$

where $\tau_{out}(\omega_{out})$ is the slope of the phase versus frequency. Assuming that $\tau_{out}(\omega_{out})$ is consistent around the resonance frequency such that the phase varies linearly with frequency and that the resonance frequencies are the same for both high and low gain settings because of the identical $C_{outD}(\omega)$, we approximate $\underset{\omega\to\omega_{out}}{\Delta\angle Z_{out}(\omega)}$ as:

$$\underset{\omega\to\omega_{out}}{\Delta\angle Z_{out}(\omega)} \approx *20c|\Delta\tau_{out}(\omega_{out})|(\omega - \omega_{out}), \tag{16}$$

which is negative below resonance and positive above.

D. JOINT ANALYSIS OF GDPV AND SIMULATION AND MEASUREMENT RESULTS FOR VGA

We now jointly consider the effects of the three phase variation factors analyzed in the above two subsections and minimize $\Delta\angle Z_{Eq}(\omega)$ at the desired frequency. From equations (7) and (9), we see that GDPV from the current steering function is positive; hence, we introduce a negative GDPV from the output admittance to optimize the overall performance. This is achieved by designing the output match to occur slightly higher than the desired operating frequency.

The relationship between the operating frequency ω_0 and the resonant frequency ω_{out} is determined by equalizing all GDPVs as follows:

$$\Delta\tau_{G2}\omega_0 + |\Delta\tau_{SC}(\omega_0)|\omega_0 \approx |\Delta\tau_{out}(\omega_0)|(\omega_{out} - \omega_0). \tag{17}$$

From this, we obtain the following relationship:

$$\omega_0 \approx \frac{\omega_{out}}{\left(\frac{\Delta\tau_{G2}+|\Delta\tau_{SC}(\omega_0)|}{|\Delta\tau_{out}(\omega_0)|} + 1\right)}. \tag{18}$$

As a result of this choice, the output impedance will be better matched at higher frequency, indicating a compromised output reflection coefficient at the target frequencies. It is also observed from (18) that larger $|\Delta\tau_{out}(\omega_0)|$ will make ω_{out} closer to ω_0, which is better for the output impedance matching; however, to keep the phase variations small within a certain bandwidth, $|\Delta\tau_{out}(\omega_0)|$ needs to be designed small as it indicates how fast the phase variation changes with frequency. Thus, a de-Qing of the output load is desirable as it mitigates Q_{outD} variations (studied in the last subsection), resulting in a slower change of phase variation, i.e. a smaller $|\Delta\tau_{out}(\omega_0)|$.

The VGA design shown in Fig. 2 was designed according to the methodology just described and implemented within the full 20 GHz RX element. The input matching of the VGA is implemented by the inter-stage fully differential transformer between the VIPS and the VGA and the three-dimension (3D) view of the layout is shown in Fig. 5. The

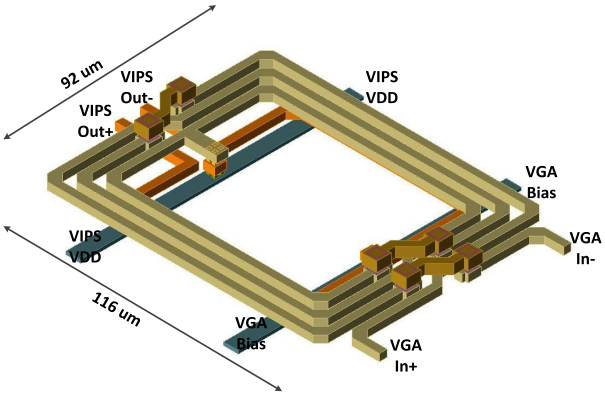

FIGURE 5. 3D view of the inter-stage transformer layout.

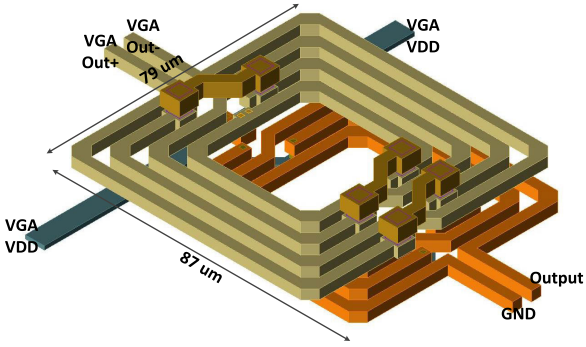

FIGURE 6. 3D view of the output balun layout.

TABLE 1. Key parameters used in the VGA modeling.

Gain	C_{012} (fF)	C_{ds2} (fF)	C_{d2} (fF)	G_0 (mS)	G_1 (mS)	G_2 (mS)	g_{ds2} (mS)
Low	272	40	48	16	55.9	55.9	7.9
High	259	50	48	16	0	94.5	14

output matching of the VGA is implemented by a balun and the 3D view of the layout is shown in Fig. 6. In both layouts, the primary and the secondary inductors are implemented by two vertically-adjacent metal layers (OA and OB) and the DC bias and supply are injected through the metal layer (UA) that is below these two signal layers. The final VGA model parameters are shown in Table 1 where also L_L, C_L, and G_L are 0.424 nH, 64 fF, and 4.6 mS, respectively.

The VGA was then simulated, fabricated, and measured and the results are compared to our analysis. First, the simulated, analytical and measured gain tuning *range* is shown in Fig. 7 showing near-perfect agreement and validating (3). An 8.8-9.7 dB gain tuning range is achieved. Second, the predicted and simulated VGA phase versus frequency are shown in Fig. 8, showing zero total GDPV at 20.2 GHz. Both the individual contributions and the joint effects of the three phase variation factors are included, comparing our analytical results to simulations and measurements (note that only the modeling result of T_{V2} phase variation is presented as it is difficult to simulate). We see that the phase variation of Z_{out} is negative at 20 GHz, selected to counteract the phase

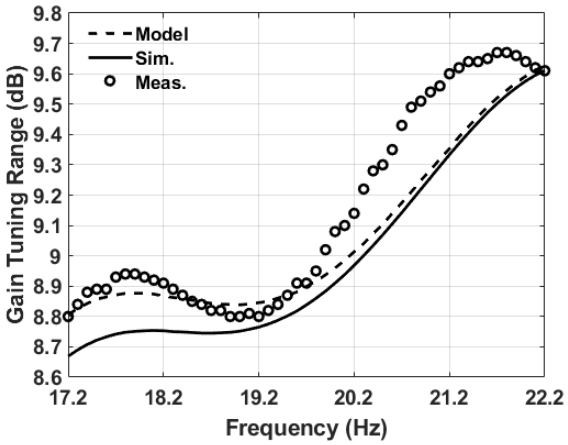

FIGURE 7. Modeled (from (3)), simulated, and measured gain tuning range.

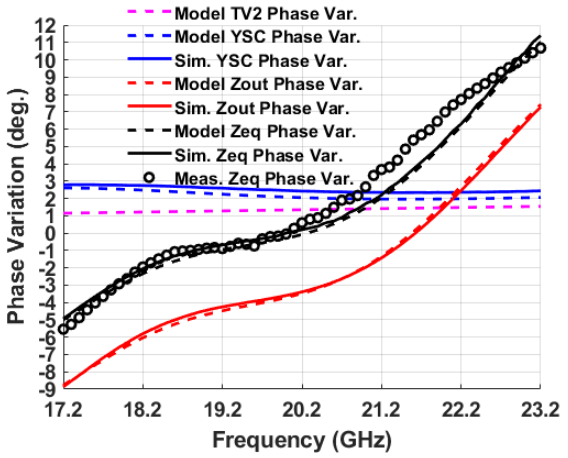

FIGURE 8. The individual contributions and the joint effects of the three phase variation factors, comparing predictions (the dashed pink curve is according to (7); the dashed blue curve is according to (9); the dashed red curve is according to (6) and (15); the dashed black curve is according to (4), (7), (9) and (15)), simulations, and measurements.

variation of the T_{V2} and $-Y_{SC}$ terms. Altogether GDPV of the VGA is represented by phase variation in Z_{Eq}, which crosses zero at 20.2 GHz. Once again, near-perfect agreement is seen between measurement, simulation and analytical results, validating our approach.

IV. VECTOR INTERPOLATOR ANALYSIS

In this section, we apply the same approach for minimizing GDPV to the VGAs used within the vector interpolator phase shifter (VIPS) and present a modified design technique.

A. VIPS MECHANISMS

The middle block within Fig. 2 shows the schematic of the fully-differential VIPS [20], [21]. The quadrature coupler splits the input signal into I and the Q signals that are then fed into baluns. Differential signals are amplified by two identical VGAs, where each VGA is used to tune the polarity and/or the amplitude of the corresponding I or Q vector. Differential control voltage $\Delta V_C = x$ controls the I-VGA and $\Delta V_C = y$ controls the Q-VGA. Finally, the two vectors are summed in current domain at the output to achieve interpolation.

In these two VGAs, the input transistor functions are similar to those of the standalone VGA studied in the previous section; however, unlike the previous VGA, the outputs of the VIPS VGAs are cross-connected and combined in the current domain to drive the load. We therefore analyze the shorted load circuit and the output impedance in a fully-differential manner, as shown in Fig. 9(a).

Following our prior method, the equivalent transimpedance of each VGA versus control voltage x is

$$Z_{Eq}(x) \approx \frac{\Delta G_{1-2}(x)}{Y_{SC}(x)} Z_{out}(x), \tag{19}$$

where $\Delta G_{1-2}(x) = G_2(x) - G_1(x)$ is the transconductance *difference* of the cascode transistor pair. This approximation is valid based on the fact that C_{ds} variation at different biasing currents is small, i.e. $C_{ds1}(x) \approx C_{ds2}(x) \approx C_{ds}$. Note that compared to the previous VGA, in the VIPS VGAs, the full cross-coupling of the current commutators means that the signal transfer is zero at $x = 0$. Further, $x > 0$ or $x < 0$ corresponds to the positive or negative polarity, with larger magnitude of x corresponding to higher gain.

The phase interpolation property of the VIPS is included by introducing a quadrature addition of the two Z_{Eq} terms, as follows:

$$Z_{IQ}(x,y) \approx \left(\frac{\Delta G_{1-2I}(x)}{Y_{SCI}(x)} + j \frac{\Delta G_{1-2Q}(y)}{Y_{SCQ}(y)} \right) Z_{out}(x,y) \tag{20}$$

B. GDPV ANALYSIS OF VIPS

We see from (20) that the calculation of $\Delta\angle Z_{IQ}(x,y)$ across all possible vector settings is complicated; thus, we analyze the response along the axis settings, i.e., when $x = 0$ or $y = 0$. This allows us to leverage the prior analysis completed for the VGA and also gives relevant GDPV for the VIPS.

Following this approach, we calculate the equivalent transimpedance along the I axis (when $y = 0$) as:

$$Z_{IQ}(x,0) \approx \frac{\frac{\Delta G_{1-2I}(x)}{Y_{SCI}(x)}}{\underbrace{Y_{outDI}(x) + Y_{outDQ}(0) + Y_L}_{Z_{out}{}^{-1}(x,0)}}, \tag{21}$$

from which we obtain

$$\Delta\angle Z_{IQ}(x,0) \approx -\Delta\angle Y_{SCI}(x) + \Delta\angle Z_{out}(x,0). \tag{22}$$

This indicates that the overall phase variation is introduced by the intermediate node impedance with load shorted and the output node impedance. The $-\Delta\angle Y_{SCI}(x)$ is calculated similarly as before as:

$$-\Delta\angle Y_{SC}(x) \approx \omega_c |\Delta\tau_{SC}(x)| > 0, \tag{23}$$

indicating a leading phase in positive lower gain settings.

As shown in Fig. 9(b), Y_{outDI} is a differential admittance. To calculate it, we first analyze the output admittance Y_{1-2} of

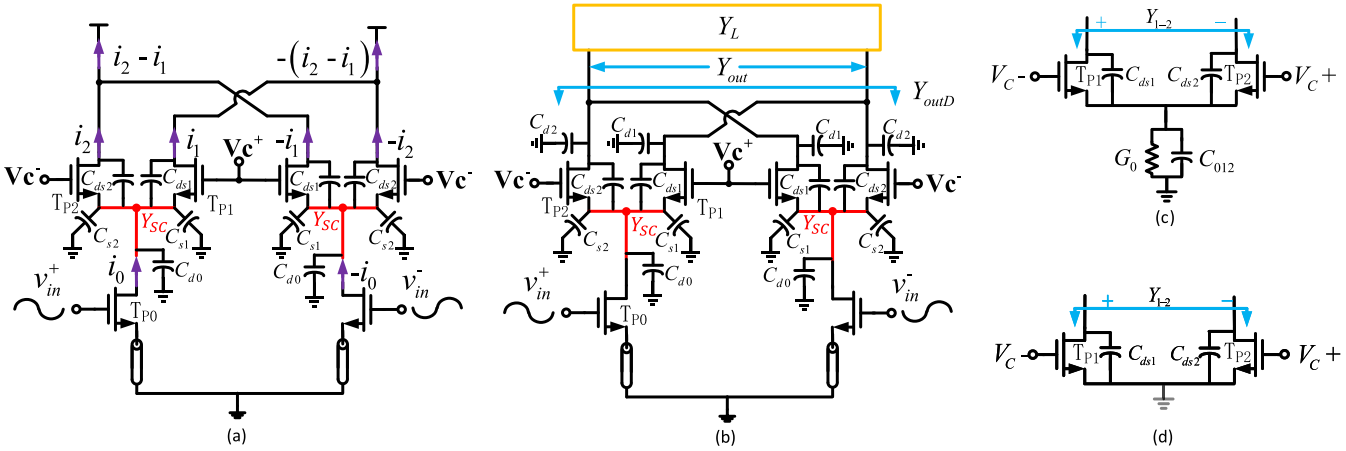

FIGURE 9. (a) Small signal current analysis of the VIPS VGA. (b) Admittance analysis of the VIPS VGA. (c) Differential output admittance of a cascode transistor pair with a tail admittance. (d) The intermediate node is ac shorted and any tail admittance is shielded when T_{P1} and T_{P2} are biased the same.

the circuitry shown in Fig. 9(c). Small-signal analysis shows

$$Y_{1-2} = \frac{\frac{y_{ds1}+y_{ds2}}{2} + (g_{m1}y_{ds2} + g_{m2}y_{ds1} + 2y_{ds1}y_{ds2}) / (G_0 + j\omega C_{012})}{2 + 2(g_{m1} + g_{m2} + y_{ds1} + y_{ds2}) / (G_0 + j\omega C_{012})}. \quad (24)$$

Then we obtain the output admittance of a single VGA as

$$Y_{outDI}(x) = 2\left(j\omega C_d + Y_{1-2}(x)\right), \quad (25)$$

where all y_{ds} and g_m become functions of x and where $C_d \approx C_{d1} \approx C_{d2}$. We now must analyze this for maximum and minimum control voltage settings.

The minimum I-vector magnitude is obtained for $x = 0$. Here, differential pair T_{P1} and T_{P2} are biased the same, and (24) can be simplified to $Y_{1-2} = \frac{y_{ds}}{2}$. This can be regarded as simply two transistors' output admittance in series, as shown in Fig. 9(d). In this condition, we obtain

$$Y_{outDI,min} = 2\left(j\omega C_d + y_{ds}(x = 0)\right). \quad (26)$$

For maximum gain setting, it is complicated to get symbolic expressions for $B_{outDI}(|x|)$ and $G_{outDI}(|x|)$ as we did for the VGA. Instead, we leverage approaches from the VGA methodology and develop a qualitative analysis to show that B_{outDI} and G_{outDI} change in opposite directions, resulting in larger Q variation. When $|x|$ increases, we obtain:

1. The differential output susceptance will increase, i.e. $B_{outDI}(|x_{Low}|) < B_{outDI}(|x_{High}|)$ and this is independent of frequency, because more C_{012} will be seen by and in series with C_{ds} to form the output susceptance (see Fig. 9(c)). As this susceptance increase is due to the tail capacitance, unlike the previous VGA, we are not able to achieve invariant output susceptance by optimizing G_m. For this reason and to avoid unnecessary parasitic capacitance, in this VIPS VGA design, we set the cascode transistors' dimensions the same as the G_m transistors' dimensions, which are small compared with the previous VGA's. Accordingly, the phase variation of the intermediate node impedance is expected to be large.

TABLE 2. Key parameters used in the VIPS VGA modeling.

Gain	C_{012} (fF)	C_{ds} (fF)	C_d (fF)	G_0 (mS)	g_{m1}, g_{m2} (mS)	g_{ds1}, g_{ds2} (mS)
0	213	27	24	16.5	40.3,40.3	6.4,6.4
Max	213	27	24	16.5	0.47,62.6	0.065,10.9

2. The differential output resistance will increase. Equivalently, we have $G_{outDI}(|x_{Low}|) > G_{outDI}(|x_{High}|)$. The reason is that more tail resistance will appear as $|x|$ increases, which increases the output resistance.

The above admittance analysis indicates $Q_{outDI}(|x|)$ increases with $|x|$. Similar as before, to reduce the phase variation introduced by $Q_{outDI}(|x|)$, the quality factor of the load impedance is designed to be low, leading to a low Q_{out} and a small ΔG_{out}. However, unlike the previous VGA where the output susceptance is invariant and the phase variation results from the conductance difference, in this VIPS VGA, the output susceptance difference $\Delta B_{out}(|x|)$ dominates the phase variation. Given that the relationship $B_{out}(|x_{Low}|) < B_{out}(|x_{High}|)$ always holds regardless of frequency, we find

$$\Delta\angle Z_{out}(x) = \omega_c |\Delta\tau_{out}(x)| > 0, \quad (27)$$

where ω_c is the center frequency. This indicates a phase variation from the output impedance that increases with gain. Unlike the previous VGA, this leading phase persists before and after the resonance; thus, according to (22), the phase variation of the output impedance enhances that of the intermediate node impedance rather than canceling. Despite this, steps can still be taken to minimize GDPV.

C. SIMULATION RESULTS OF VIPS

The VIPS shown in Fig. 2 is designed based on the above analysis and guidelines and its performances are shown as follows. Fig. 10(a) shows the *normalized* S_{21} polar plot (calculated phases are rotated to match s-parameter simulation). These results are generated by sweeping x and y

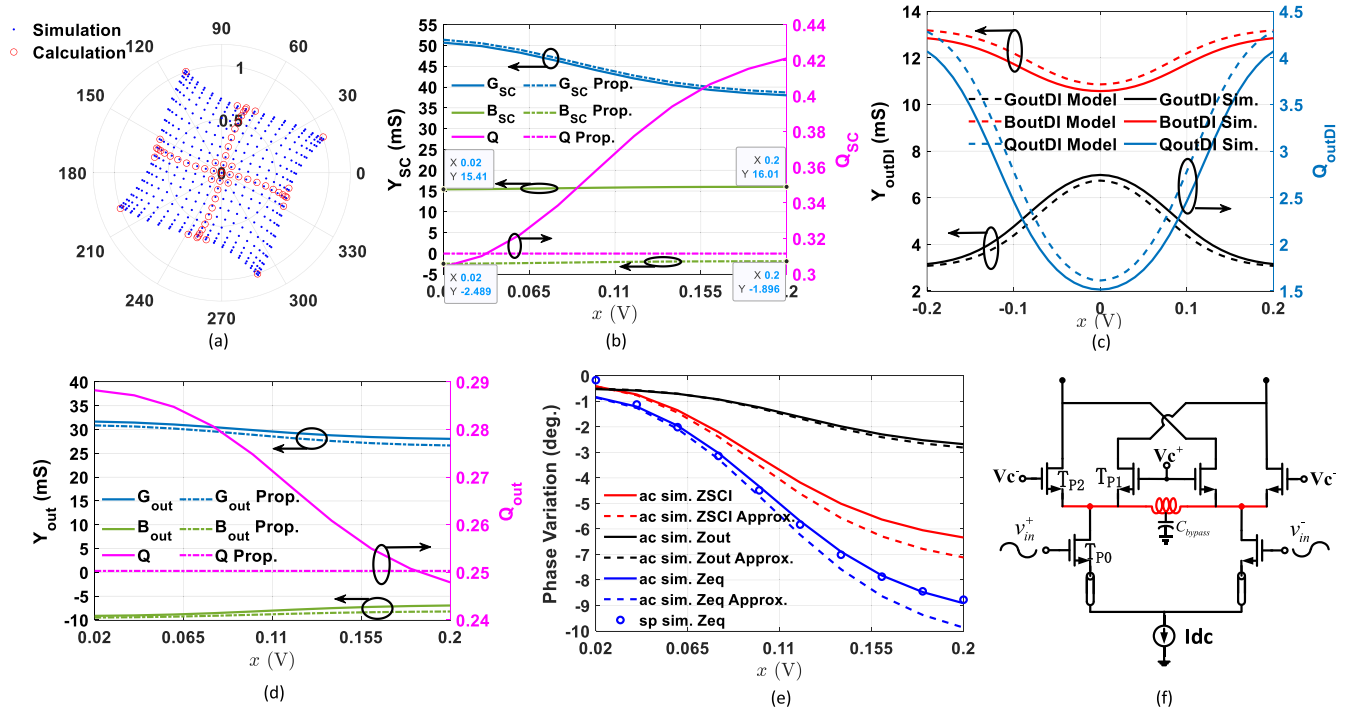

FIGURE 10. (a) Simulated and calculated normalized S_{21} polar plot vs. x and y; (b) analytical intermediate-node admittance Y_{SC} vs. x, for implemented and proposed designs; (c) simulated and analytical differential output drain admittance Y_{outDI} and Q factor vs. x; (d) simulated total VIPS output admittance and Q factor vs. x for $y = 0$ for implemented and proposed designs; and (e) the individual and total phase variations vs. x for $y = 0$ of the full VIPS (the approximations refer to (6)). (f) A proposed resonance technique to reduce GDPV in a VIPS, validated in simulation only.

where the equivalent transimpedance calculation is according to (20). All calculated values use parameters shown in Table 2 which are extracted from simulation at 20.2 GHz. Excellent agreement between theory and simulation is seen. From this plot, we see the axis variations in red, indicating GDPV.

Regarding individual components of GDPV, Figs. 10(b), (c), and (d) (solid curves) show the variations of G, B, and Q corresponding to Y_{SC}, Y_{outDI}, and Y_{out}, respectively, and then the overall phase variation in Fig. 10(e) (note that the dash-dotted curves in Figs. 10(b) and (d) refer to a proposed modification to the VIPS to be discussed in the Appendix). Fig. 10(b) shows the admittance and the quality factor of the intermediate node with output load shorted as x varies. G_{SC} reduces by 24% across gain-control range, whereas this value is only 13% in the previous VGA with G_m optimization. This results in a larger phase variation of 6° (see red curves in Fig. 10(e)) compared with 2.5° in the previous VGA. Fig. 10(c) shows the simulated and modeled Y_{outDI} (x) (according to (25)). The conductance variation is large; however, this large conductance variation is mitigated by the low-Q load admittance. This is shown in Fig. 10(d), where the solid blue curves show a smaller overall conductance variation. As a result, the phase variation of the output impedance is relatively small as the black curves shows in Fig. 10(e).

Altogether, the total phase variation of the VIPS is plotted as the blue curves show in Fig. 10(e). Simulations and analytical results match well, validating our theory. However, we do observe that the VIPS will exhibit higher GDPV compared to the VGA and this is largely a result of the large variation in Y_{SC}. To address this variation, a design modification is proposed, as shown in Fig. 10(f), where a shunt inductor is introduced to resonate the capacitance at the intermediate node. In so doing, phase variation in Y_{SC} and Y_{out} can largely be eliminated as shown with the dash-dotted line results in Figs. 10(b) and (d). Further analysis and discussion is found in the Appendix. This revised design was realized after measurements and is only validated in simulation.

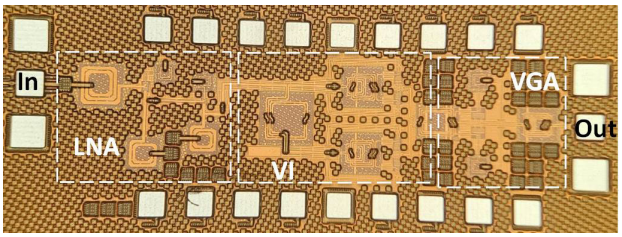

FIGURE 11. Die micrograph of the 20 GHz beamformer element.

V. BEAMFORMER MEASUREMENT RESULTS

A 20 GHz beamforming receiver element was designed according to the VGA and VIPS principles just described (without proposed Y_{SC} resonance). An element was realized in 45nm RFSOI technology from GlobalFoundries. A die micrograph of the chip is shown in Fig.11. The circuit occupies an area of 1.65×0.46 mm^2, excluding pads. In this prototype, on-chip digital-to-analog converters (DACs) are

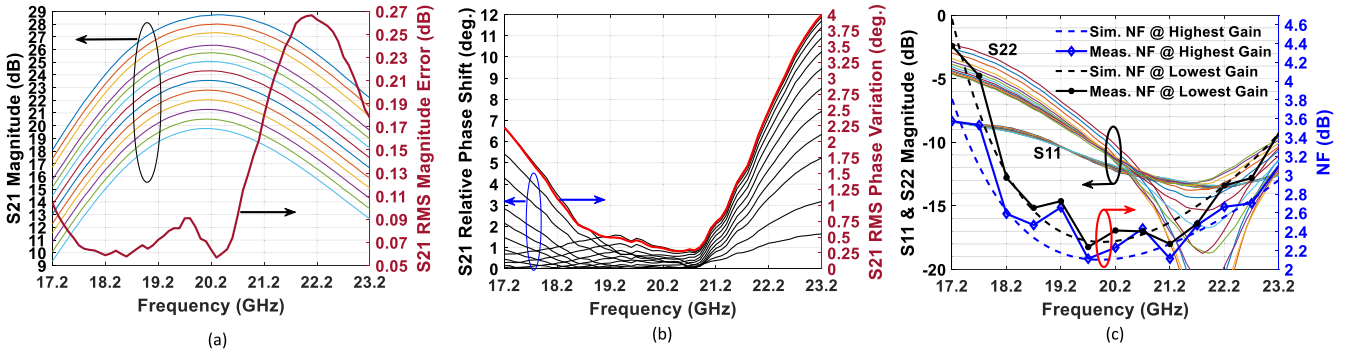

FIGURE 12. (a) Measured gain tuning of the RX beamformer channel. (b) Measured phase variation of the gain tuning. (c) S_{11}, S_{22} and NF with gain tuning.

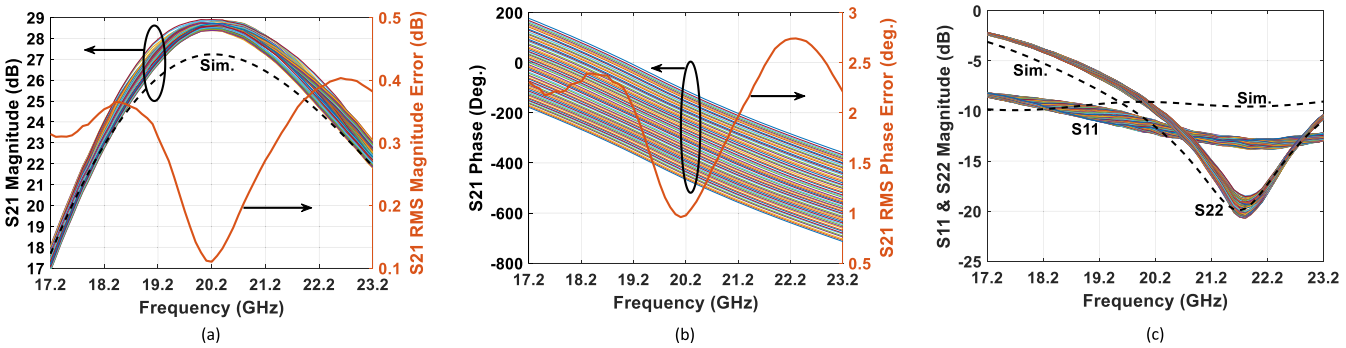

FIGURE 13. (a) S_{21} magnitude plot of the RX beamformer. (b) S_{21} phase plot of the RX beamformer. (c) S_{11} & S_{22} magnitude plot of the RX beamformer.

not included; thus, the VIPS and VGA are controlled by off-chip supplies operating as DACs.

The prototype was measured using wafer probing. In summary, the beamforming element achieves 29 dB maximum gain, 2.2 dB NF, and +2 dBm oP_{1dB}, while consuming 111 mW. The results agree closely with simulations. Additional measurements versus VGA and VIPS control settings follow.

In the gain tuning capability measurement, we sweep the VGA control voltage from 0 to 200 mV with a unit voltage step of 10 mV. We then select the voltage settings that provide a uniform gain step of 0.75 dB. Fig. 12(a) shows the measured gain performances. A 9 dB gain tuning range with $<$ 0.2 dB dB RMS gain error is achieved. The gain peak is 29 dB at 20.2 GHz. The GDPV is shown in Fig. 12(b). Minimum GDPV is seen directly at the desired frequency range, with less than 1° RMS phase variation across 18.3 to 21.4 GHz (15.6% fractional bandwidth). Note that this low GDPV is achieved by design and not through any additional calibration.The measured S_{11}, S_{22} and NF are shown in Fig. 12(c). As discussed earlier, the output impedance is better matched at a higher frequency, i.e., 21.8 GHz, to achieve the low intrinsic GDPV. Excellent agreement between measured and simulated NF are seen. The NF is 2.2 dB at the highest gain and 2.4 dB at the lowest gain, respectively. This suggests that individual per-element noise contributions agree with the simulations that show the LNA NF is 1.7 dB, VIPS NF is 12 dB, and VGA NF is 3.5 dB.

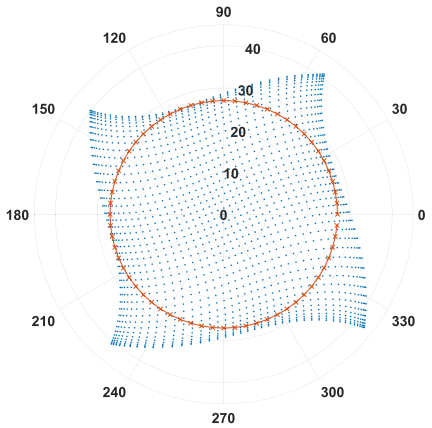

FIGURE 14. The measured S_{21} polar plot of the RX beamformer. The red circle with uniformly spaced 64 points indicates the targeted gain and the ideal phase settings used in the calibration.

In the phase shift measurement, we sweep the VIPS control voltage from -200 mV to 200 mV with a unit voltage step of 10 mV. The measured polar plot is shown in Fig. 14. The intrinsic GDPV is noticeable by observing the twisting of the constellation. The red circle with constant magnitude and uniformly spaced 64 points (i.e., 6 bits) represents the ideal response, based on which a look-up table is created to obtain the desired calibrated gain and phase. Figs. 13(a)-(c) show the measured gain response, phase response and input/output reflection coefficients at the highest gain state with the

TABLE 3. Comparison of RF/mmWave VGAs.

Reference	**This work**	TMTT'22 [22]	RFIC'18 [3]	ISSCC'17 [4]	MWCL'19 [7]	IMS'19 [8]
Principle for Invar. Phase	**G_m and load optimization**	Active cross-coupling neutralization	Parasitic cap. cancellation	Parasitic cap. management	RC compensation	Inductor compensation
Process	**45nm SOI**	65nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS	90nm CMOS
Gain Control Mechanism	**Analog**	Analog	Digital	Digital	Analog	Analog
Frequency (GHz)	**18.3-21.4**	24-28	34-36	26-36	30-34.5	26-30.5
Fractional BW	**15.6%**	15.4%	5.7%	32.3%	14.0%	15.9%
Δ Gain (dB)	**9**	6.2	7.8	8	10.6	9.8
Gain Resolution (dB)	**0.75**	0.2	0.5	1	NA	NA
RMS Gain Error (dB)	**< 0.2**	< 0.13	$< 0.13^*$	$< 0.3^*$	NA	NA
RMS Phase Var. (°)	**< 1 0.28@20.5GHz**	< 0.92 0.63@27.8GHz	< 1 0.7@35GHz*	$< 6^*$ 5@31GHz*	< 3 0.8@32GHz*	< 1.8 1@29GHz*
oP_{1dB} (dBm)	**2**	6.4	2.5	NA	-0.6	-4
Power Cons. (mW)	**27**	29	15.6	30.3	26.7	17.9

$*$ Estimated from figures.

TABLE 4. Comparison of RF/mmWave RX Beamformers.

Reference	**This work**	JSSC'22 [24]	JSSC'21 [25]	TMTT'21 [26]	JSSC'17 [27]	TCAS II'20 [28]	RFIC'16 [29]
Process	**45nm SOI**	65nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	130nm SiGe	45nm SOI
Frequency (GHz)	**18.7-22.1**	21.0-30.6	28	24-28	$26.8\text{-}28.6^{\&}$	22-27	23-29
3-dB Fractional BW	**15.9%**	37.2%	N/A	15.4%	6.5%	20.4%	23.1%
Peak Gain (dB)	**29**	14.2	18	23.2	$30^{\&}$	28.5	12.2
Δ Gain (dB)	**9**	31.5	8^*	24	8	6	6
Gain Resolution (dB)	**0.75**	0.5	0.5^*	0.75	NA	NA	0.4
RMS Gain Error (dB)	**< 0.26**	$< 0.22^{\#}$	NA	< 0.4	NA	NA	NA
Phase Var. of Gain Control(°)	**0.28-2 (RMS)**	$1.8\text{-}3.5^{\#}$ (RMS)	2.5^* (28GHz)	< 1.1 (RMS)	3	$7^{\&}$ (24GHz)	$2.8^{\&}$ (26GHz)
Phase Shifter Type	**VIPS**	VIPS	VIPS	VIPS	Tunable TL	VIPS	Switched LC
Phase Res.(°)	**5.625**	5.625	11.25	0.8	4.9	5.625	11.25
RMS Phase Error (°)	**< 2**	$< 1.8^{\#}$	$< 2^{\&}$ (26.5-29.5 GHz)	< 0.5	0.8	$< 5^{\&}$	< 4
Gain Var. of Phase Control (dB)	**< 0.3 (RMS)**	$0.4\text{-}0.5^{\#}$ (RMS)	< 0.4 (RMS)$^{\&}$ (26.5-29.5GHz)	< 0.3 (RMS)	< 1.4	< 3	0.4-0.7
NF (dB)	**2.2-2.4 (20.2GHz)**	$4.6^{\$}$ (26GHz)	$4.9^{\$}$ (28GHz)	$> 4.5^{\$}$	$6.0^{\$}$	3.3 (25GHz)	4-4.7
iP_{1dB} (dBm)	**> -26**	-23.7 to -22.2	-29	-16.1	-22.5	$-29^{\&}$	-8
Power Cons. (mW)	**111**	82	88	45	103	48	42

$*$Simulation. & Estimated from figures. $ With T/R switch. # 24-29.5 GHz

calibrated voltage settings. The RMS gain error is < 0.3 dB across the bandwidth and the minimum is 0.1 dB at 20.2 GHz. A 5.625° phase resolution is achieved. The RMS phase error is $< 2°$ across the bandwidth and the minimum is 1° at 20.2 GHz. The input reflection coefficients are < -10 dB across the band while the output impedances are matched at 21.8 GHz due to the VGA load design. The measured iP_{1dB} is > -26 dBm across all the phase settings at the highest gain.

Table 3 compares the beamformer's gain tuning performances with state-of-the-art VGAs. This element's VGA achieves the lowest RMS phase variation and comparable fractional bandwidth without requiring the additional circuitry to minimize the GDPV like the other references. Specifically, compared with [22], this work achieves similar RMS phase variation but lager gain tuning range. Compared with [3], this work achieves much wider fractional bandwidth in the same low RMS phase variation region. Table 4 summarizes the full beamformer channel's performances and compares them with those of prior art. This work achieves the lowest phase variation of gain control. The 2.2 dB NF of this work is low compared with those reported in literature yet is slightly higher than that of recent products (e.g., 2 dB from [23]).

VI. CONCLUSION

In this paper, phase and gain control dependencies of the classic current steering VGA and the classic cross-connected VGA-based VIPS have been analyzed in depth. For the former, a G_m and load optimization technique has been proposed such that the phase variations of different partial circuitries are well balanced and canceled at the desired frequencies. In this way, a very low overall GDPV is achieved without any additional compensation circuitry. This GDPV reduction technique has been experimentally validated in a 20 GHz receive beamformer design.

For the latter, as presented here and in the Appendix, a design technique and a circuit model are proposed to achieve ideal vector interpolation and they are validated through simulations. First, by adding an appropriate shunt inductor to the intermediate node, we are able to achieve invariant Q at both the intermediate node and the output node, thus, nearly eliminating GDPV. Then, we propose

a quasi-empirical model of the equivalent transimpedance, through which, I/Q crosstalk has been analyzed and guidelines are provided to reduce this nonideality.

The proposed design techniques and guidelines are effective to reduce the gain and phase dependencies in a beamformer, especially given that no additional compensation circuitry or extra calibrations are required. The presented beamformer achieves low phase variation during gain tuning, fine gain resolution and low gain error with excellent RF performance, which is well-suited for mm-wave applications.

APPENDIX

The realized VIPS exhibits both GDPV and I/Q crosstalk, as evidenced in the the measurement result in Fig. 14. GDPV is seen in the twisting of the axes whereas crosstalk is seen in the stretching of the diagonals. These errors commonly exists in typical active vector interpolators [11], [12], [13]. In this section, design modifications are proposed for the VIPS to largely eliminate these non-idealities. These new approaches were realized after the design and measurement of the 20 GHz beamformer; thus, all results are evaluated in simulation only. We will first propose a simple but effective resonant technique such that the GDPV in the VIPS can be further reduced. After this, I/Q crosstalk is analyzed and new design guidelines are provided to reduce this nonideality.

A. REDUCING GDPV IN VECTOR INTERPOLATOR

To reduce GDPV in the interpolator, the quality factors associated with both the intermediate node and the output admittance need to be invariant. We begin from the intermediate node, as it introduces a large portion of phase variation. Note that at this node, Q varies because $|G_{SC}|$ and $|B_{SC}|$ change in the opposite directions. To make $|B_{SC}|$ change inversely, an inductor can be added at the intermediate node to make B_{SC} slightly negative. As shown in Fig. 10(f), a design modification is proposed where a 438 pH differential inductor from the design kit is connected between the two differential intermediate nodes. The inductor center node is ac shorted to the ground through a 10 pF bypass capacitor. The inductance value is selected such that $\frac{|B_{SCLowest}|}{|B_{SCHighest}|} = \frac{|G_{SCLowest}|}{|G_{SCHighest}|}$, achieving an invariant Q. This is illustrated in Fig. 10(b), where the new Y_{SC} and Q_{SC} are shown as dash-dotted lines. From this, we see that Q_{SC} is reduced to a nearly constant value of 0.32. As another benefit, due to the susceptance reduction at the center node, the output susceptance becomes more inductive with high-gain settings. Thus, $|\Delta B_{out}(|x|)|$ becomes smaller, achieving an invariant Q at the output node as well (dash-dotted purple curve shown in Fig. 10(d)). For the same impedance matching network, this does shift the frequency where peak gain is achieved from 20.2 GHz to 19.8 GHz.

To evaluate the GDPV, S_{21} spoke plots are shown in Fig. 15(a) and (b) to compare the phase variation of the VIPS without/with the intermediate-node inductor. For both VIPS, we obtain the control voltage settings from the low gain calibrations and the calibrated results are shown by the inner circles. Then we scale the control voltages by 2X, 3X and 4X and obtain the other three circles from the inside to the outside. GDPV, shown as the phase deviations from the spokes with the scaled control voltages can be clearly observed from Fig. 15(a) for the classic VIPS. In the highest gain settings, GDPV is around 8° along the axes while it can reach up to 14° along the diagonals. In contrast, for the proposed VIPS, the phases stay on the spokes for all the scaled control voltages, indicating a very low GDPV ($< 0.5°$ along the axes and $< 2°$ along the diagonals). The normalized S_{21} polar plot is shown in Fig. 15(c). Compared with that of the classic VIPS shown in Fig. 10(a), the axis "twist" is nearly eliminated.

B. REDUCING IQ CROSSTALK IN VECTOR INTERPOLATOR

I/Q crosstalk refers to the dependency of the IVGA response on Q-vector setting and the QVGA response on I-vector setting. It is mathematically captured by $Z_{out}(x, y)$ in (20). We see that the output impedance is therefore a function of both I and Q VGA control voltages.

While we could continue to analyze this crosstalk using our existing equations, a quasi-empirical model can better help illustrate the behavior. Trigonometric functions are used to mimic the transconductance and admittance variations with the control voltage change because these variations all have peak and valley values and follow a sinusoidal trend. For this, we make the following observations and assumptions:

1. We leverage the results in the prior section where intermediate-node inductors are used to eliminate the GDPV in the individual VGAs of the interpolator. Further, we assume resonance at the output, which results in elimination of all susceptance terms in Z_{IQ}.

2. We note that as the control voltage changes, the tansconductance difference of the cascode transistor pair, i.e., $\Delta G_{1-2}(x)$ changes between 0 and $\pm G_{Max}$ and that it follows a sine function trend. We therefore model $\Delta G_{1-2I}(x) = G_{Max}\sin(x), -\pi/2 \le x \le \pi/2$ and $\Delta G_{1-2Q}(y) = G_{Max}\sin(y), -\pi/2 \le y \le \pi/2$ for I path and Q path, respectively, because they are tuned independently. Please note that these sine functions are capturing the transistor behavior as opposed to any sine/cosine weighting that may be deliberately introduced to the interpolation.

3. Similar to the above, G_{SC} and G_{outD} can be modeled with trigonometric functions to fit the variations shown in Figs. 10(b) and (c) according to cosine.

Putting all of this together and according to (20), the equivalent transimpedance of the VIPS can be modeled as:

$$Z_{IQ}(x, y) \approx \frac{G_{Max}}{\Delta G_{outD}} \frac{\frac{sin(x)}{\Delta G_{SC}\cos(x)+G_{SC\,\min}} + j\frac{sin(y)}{\Delta G_{SC}\cos(y)+G_{SC\,\min}}}{\sigma(x, y) + 2G_{outD\,\min}/\Delta G_{outD} + G_L/\Delta G_{outD}}, \tag{28}$$

where $\sigma(x, y) = \cos(x) + \cos(y)$ is defined as the *crosstalk* factor and it contributes to the crosstalk-induced gain variation. The S_{21} polar plot according to (28) is shown

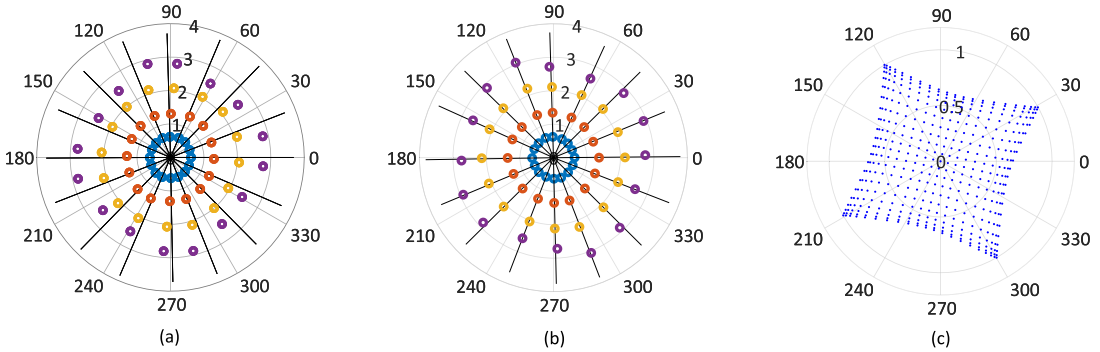

FIGURE 15. (a) Simulated S_{21} spoke plot of the classic VIPS. (b) Simulated S_{21} spoke plot of the VIPS with the proposed resonance technique. (c) Simulated normalized S_{21} polar plot of the VIPS across all settings with the proposed resonance technique. The axis twist is reduced.

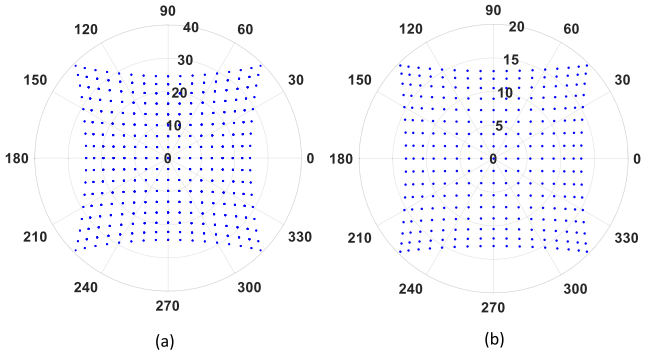

FIGURE 16. (a) The modeled equivalent transimpedances according to (28). (b) The modeled equivalent transimpedances according to (28) where we increase G_L such that $2G_{outD\,\min} + G_L$ is doubled.

in Fig. 16(a). This is plotted using the parameter values obtained from Fig. 10 and the following: $G_{Max} = 29.5$ mS, $\Delta G_{SC} = 12$ mS, $G_{SC\,\min} = 38$ mS, $\Delta G_{outD} = 3.6$ mS, and $2G_{outD\,\min} + G_L = 28$ mS.

To better understand and then reduce I/Q crosstalk, we perform the following analysis. We have $0 \le \sigma\,(x, y) \le 2$. On one extreme, $\sigma\,(x, y) = 0$ is achieved when $x = \pm\pi/2$ and $y = \pm\pi/2$. It maps to the four corner points at the very ends of the two diagonals on the polar plot, which means that $Z_{IQ}\,(x, y)$ achieves its largest value, corresponding to the highest VIPS gain. On the other extreme, $\sigma\,(x, y) = 2$ is achieved when $x = y = 0$. This maps to (0, 0) on the polar plot which has no gain, and its effect is inconsequential. Furthermore, if we look at the vector Q length along its axis, where vector I is 0 ($x = 0$), we have $\sigma\,(0, y) = 1 + \cos(y)$. For maximum Q vector, $y = \pi/2$ and $\sigma = 1$. As such, the Q-vector's length is shorter along its axis compared to the diagonal where $\sigma = 0$. This explains why the curves towards the center are compressed.

To reduce I/Q crosstalk, according to (28), the invariant part of output admittance, i.e., $2G_{outD\,\min}/\Delta G_{outD} + G_L/\Delta G_{outD}$ needs to be large enough such that $\sigma\,(x, y)$ variation is relatively small. For the second term, as G_L and ΔG_{outD} can be designed independently, it is evident that a low Q load admittance would benefit as it is also beneficial to reduce GDPV in the previous analysis. For the first term, we note that $G_{outD\,\min}$ is primarily set by the OFF-state transistor admittance. If we increase it, we will largely increase the ON-state transistor admittance as well, which will increase ΔG_{outD}. For this reason, we reduce ΔG_{outD}, which means a reduction of g_{ds} ($x = 0$), i.e., the peak value of G_{outD} as shown in Fig. 10(c). One effective method to achieve this while still keeping a consistent dc current is to reduce the cascode transistors' W/L and correspondingly increase the biasing voltage. In this way, $2G_{outD\,\min}/\Delta G_{outD} + G_L/\Delta G_{outD}$ will increase while the current division ratio (the numerator of (28)) will decrease due to a reduction of g_m. To conclude, we are able to reduce I/Q crosstalk by de-Qing the load impedance and/or decreasing the cascode transistors' intrinsic admittance. However, both results in a compromise of the gain. For example, we increase G_L such that $2G_{outD\,\min} + G_L$ is doubled and the resulting S_{21} polar plot is shown in Fig. 16(b). It is notable that I/Q crosstalk is effectively mitigated while the gain is reduced by half.

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