IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 28 March 2023, accepted 28 April 2023, date of publication 23 May 2023, date of current version 21 July 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3279088

RESEARCH ARTICLE

Characterizing Semiconductor Devices for All-Electric Aircraft

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This work was supported in part by Airbus UpNext.

ABSTRACT Cryogenic propulsion with hydrogen fuel cells replacing fossil fuels is a promising solution to cut carbon emissions in the aviation sector. Hydrogen will also be used for cooling the superconducting machines and power converter circuits. This article aims to test devices suitable for power electronic converters supplying a 1.6 MW superconducting machine. SiC MOSFET and Si IGBT modules with ratings of 1200 V and more than 450 A are selected to assess their performance at different temperatures. Four tests are conducted to determine: 1) the forward voltage drop, 2) the breakdown voltage, 3) the switching behavior, and 4) their operation with two modules in parallel. A bespoke current sensing rig has been developed that avoids the need to extend conductors outside the cryogenic zone in the switching losses measurement test. This configuration introduces minimal stray inductance into the circuit, which minimizes errors in the measurement. One of the aims of this article is to assess the suitability of different module technologies for SiC MOSFET and Si IGBTs in cryogenic applications. Six power modules (SiC MOSFETs and Si IGBTs) were evaluated at both room and cryogenic temperatures. Three of the modules employed conventional bond wire technology, while the other three utilized solid cover (SLC) technology that has no internal bond wires. It was found that the modules which employed SLC technology were the only ones able to survive the extreme temperatures. Following this, a comparison was made between the energy losses of the three SLC modules (two Si IGBTs and one SiC MOSFET) that were able to withstand low temperatures. The results indicated that the performance of the SiC MOSFET module worsens at cryogenic temperatures, whereas the performance of the Si IGBT modules improves with decreasing temperatures. Finally, an inverter simulation was conducted with each of the IGBT modules to estimate the efficiency.

INDEX TERMS Cryogenic, current measurement, double pulse test, IGBT, MOSFET.

I. INTRODUCTION

Hydrogen aircraft have been the focus of research to meet the targeted restrictions enforced by governments worldwide in terms of carbon and noise emissions produced by the aviation sector. Research is currently focused on electrifying aircraft and utilizing energy sources other than fossil fuels to power commercial flights [1], [2], [3], [4]. The architecture of a hydrogen-electric aircraft is presented in [4], where the copper conductors in machines and cables are expected to be replaced by their superconducting counterparts as superconductors are known to be lighter and have higher power density and thus are more practical to implement for hydrogen aircraft [2]. To maintain the optimum operating conditions for superconductors which require ambient temperatures of 77 K and lower, a cooling system needs to be in place and thus hydrogen can act as both a coolant and a fuel for the aircraft. Since a cryogenic cooling system is in place, it is better, from

The associate editor coordinating the review of this manuscript and approving it for publication was Marcelo Antonio Pavanello.

an engineering point of view (thermal and mechanical design) to have the power electronics located in the same temperature zone as the rest of the system, because this avoids the need for bulky and costly insulation arrangements between the machines and power electronic circuits [5]. Power electronic devices would operate at a slightly higher temperature than hydrogen but will still be within the cryogenic range, which usually refers to temperatures below 123 K [2]. Using power electronics at cryogenic temperature has its own benefits as the following aspects normally improve: 1) lower switching losses, 2) lower conduction losses, and 3) higher power density [1], [2]. The efficiency of a cryostat has been calculated to around 7 % at 77 K [6], [7], thus in the end it might be more costly to run the system at cryogenic temperature. However, as the cryogenic system is already in place, using power electronics at cryogenic temperature would reduce heat leakage and make the system more compact.

The most suitable devices to operate at lower temperatures, according to the literature, are Si MOSFETs and GaN HEMTs as their conduction losses decrease up to 90 % [1], [2]. However, Si MOSFETs and GaN HEMTs are only usable at relatively low voltage ratings and thus require a complicated multilevel configuration to reach the target ratings. Possible alternatives with higher voltage ratings are SiC MOSFETs and Si IGBTs, both of which can sustain higher voltages and have a larger current capacity. SiC MOSFETs can operate at a higher switching frequency than IGBTs at room temperature. However, SiC MOSFETs are known to have a higher on-resistance ($R_{DS(ON)}$) at cryogenic temperature [8], [9], [10], [11], which would increase their conduction losses [2]. To overcome the issue of higher $R_{DS(ON)}$ a cryogenically cooled three-level active neutral point clamped (ANPC) converter using SiC MOSFETs was implemented in [10], where the junction temperature was kept above 225 K to keep losses down and prevent damage to the device insulation. Conversely, IGBTs [11], [12] have shown a decrease in the forward voltage at cryogenic temperature.

Even though the literature has tested SiC MOSFETs and IGBTs at cryogenic temperature, data on module package performance at cryogenic temperature are sparse. Thus, the main purpose of this article is to characterize the performance of SiC MOSFETs and Si IGBTs with voltage ratings up to 450 V and current ratings up to 2000 A in module packages at temperatures between 77-300 K. The findings of this article are that some module package configurations tend to fail in cryogenic conditions, and thus give a recommendation for which devices are best suited. The devices that did not fail underwent four different tests; 1) forward voltage drop test, 2) breakdown voltage test, 3) paralleling, and 4) double pulse test (DPT).

This article investigates the DPT setup where the test was optimized to be implemented at cryogenic temperature with the use of cryogenic current transformers; this improves upon the conventional measurement technique used in the literature which requires extending long wire leads for testing at cryogenic temperature, which is known to introduce large leakage inductance and affect the measurements. The new setup has shown clearer measurement than the conventional technique used in the literature.

Thus, this article mainly covers two key issues: 1) testing devices in module packages and 2) designing and developing cryogenic current sensors. To determine the most suitable device, seven different semiconductor switches (SiC MOSFETs and Si IGBTs) were evaluated at both room and cryogenic temperatures. The conventional power modules were found to malfunction when exposed to low temperatures, while the SLC power modules performed consistently well. The performance of Si IGBTs with SLC technology improved at cryogenic temperatures as their energy losses decreased. Conversely, the performance of SiC MOSFETs worsened with decreasing temperatures as their on-resistance increased significantly and they could not be readily paralleled at cryogenic temperature, thus are not a suitable candidate for the required application. Finally, a simulation was built to estimate the system efficiency at room and cryogenic temperatures. The article introduces a simple custom-designed current sensor that incorporates a nano-crystalline core and provides accurate measurements at cryogenic temperatures.

The article is organized as follows: Section II discusses the background of using cryogenic power electronics for all-electric aircraft. Section III discusses the experimental setup for testing the semiconductor device characteristics. Section IV discusses the design and development of the cryogenic current sensor. Section V shows the experimental results. Section VI shows the calculation of the inverters' efficiency of using SiC MOSFET and Si IGBT at room and cryogenic temperatures. Finally, Sections VII and VIII present the discussion and conclusion.

II. BACKGROUND

The architecture of the hydrogen aircraft proposed in [4] where hydrogen is set to be used as both coolant and fuel for the aircraft as shown in Fig. 1. By locating the power electronics circuits in the cryogenic temperature zone, less mechanical and thermal isolation is required, easing the construction of the final implementation.

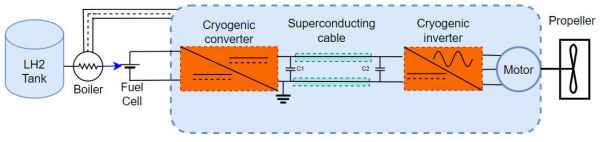


FIGURE 1. Architecture of the all-electric aircraft.

The requirements for the semiconductors set by the Airbus UpNext program are shown in Table 1. The operating voltage is shown in Table 1 which is set at 450 V. To ensure reliable operation a safety factor of 50 % should be added, meaning that the breakdown voltage should be not less than 675 V.

Also, as the blocking voltage of the semiconductor device decreases with temperature, devices with a rating of 1200 V are therefore most suitable for our selection. The device (or parallel devices) is expected to supply a current of 2000 A and to operate at a switching frequency of 3 kHz.

A market survey was made of the available devices that meet the specifications shown in Table 1. From [1] and [2], the Si MOSFET and the GaN HEMT exhibit the best performance at cryogenic temperature, as their $R_{DS(ON)}$ can decrease by 80 % for the Si MOSFET and 90 % for the GaN HEMT. However, the main objective of this article is to identify devices above 450 V and 2000 A suitable for operation at cryogenic temperatures. Currently, there are no commercial GaN HEMT or Si MOSFET modules that can meet the targets set by Airbus.

TABLE 1. Semiconductor rating requirements.

Parameter	Magnitude
Rated voltage (V)	450
Output current (A)	2000
Switching frequency (Hz)	3000

From the market survey, SiC MOSFETs and Si IGBTs are available in modules that can supply a higher current output than discrete devices. To fulfill the criterion of the current set in Table 1, Si IGBTs, and SiC MOSFETs will be tested in parallel. Table 2 shows the estimated behavior of the SiC MOSFETs and Si IGBTs at cryogenic temperature according to the literature. The main parameters used for comparison are; 1) $R_{DS(ON)}$ or forward voltage ($V_{Forward}$) which determines the conduction losses of the device, 2) breakdown voltage, which is affected by the change of temperature on the device ($V_{Breakdown}$), and 3) the switching losses (E_{SW}) at different temperatures. It can be observed that Si IGBTs have improved performance at cryogenic temperatures as the forward voltage decreases by 22 %. Even though the SiC MOSFET's conduction losses increase at cryogenic temperature, they are still acceptable. Moreover, SiC MOSFETs can be used with their junction temperature above 200 K, as in [10], to reduce their losses, and they are known for their ability to operate at a higher switching frequency than that of the IGBTs.

TABLE 2. Approximate performance trends of SiC MOSFET and IGBT as temperature decreases from room temperature to 77 K.

Device type	Parameter	Trend as the temperature is reduced to 77 K
SiC MOSFET [1], [2], [6]-[9]	$R_{DS(on)}$	+300%
	$V_{Breakdown}$	-20%
	T_{on}	Sparse data
Si IGBT [1], [2], [11]-[14]	$V_{forward}$	-22%
	$V_{Breakdown}$	-30%
	E_{SW}	-70%

Table 3 lists SiC MOSFETs and Si IGBTs that meet the specifications in Table 1. It is noted that the modules with IGBTs included silicon anti-parallel diodes. These devices were chosen so that their performance at cryogenic temperatures could be characterized and evaluated, and their applicability for future all-electric aircraft determined. Device 3 was tested to confirm that, even though some module packages break down at cryogenic temperatures, discrete devices can be used at those temperatures without necessarily suffering damage. The following section will discuss the experimental setup for testing the devices.

TABLE 3. Semiconductor ratings.

Device number	Device type	Package type	Module technology	Voltage rating (V)	Current rating (A)
Device 1	SiC MOSFET	Module	Conventional	1200	500
Device 2		Module	SLC	1200	495
Device 3	Si IGBT	Discrete	N/A	600	160
Device 4		Module	Conventional	650	130
Device 5		Module	Conventional	1200	900
Device 6		Module	SLC	1200	690
Device 7		Module	SLC	1200	800

III. CHARACTERIZATION OF SEMICONDUCTOR DEVICES AT CRYOGENIC TEMPERATURE

This section discusses the characteristic tests for the selected semiconductor devices at cryogenic temperatures. Four tests are conducted to study the performance of the devices: 1) forward voltage drop, 2) breakdown voltage, 3) double pulse test, and 4) static paralleling test.

A. FORWARD VOLTAGE TEST

Figure 2 depicts the configuration for this test, which uses a GSP10-1000DC dc power supply in the constant-current mode. To produce the needed current output, an NI LabVIEW 2018 SP1 system controls the power supply. The voltage across the device under test (DUT) is measured using a NI 9229 data acquisition card with a sampling frequency of 25 kHz. A PT100 platinum resistance temperature sensor is attached to the DUT to measure its temperature during the test.

The experiment begins with the DUT immersed in LN2 (liquid nitrogen), the power supply switched on to provide the required current, and the voltage across the device is measured. The DUT is then removed from the LN2 and placed in the ambient temperature, where its temperature increases passively. As the temperature of the device rises, the experiment is repeated to capture the device characteristics at different temperatures. During each experimental run, there is a negligible temperature rise on the device.

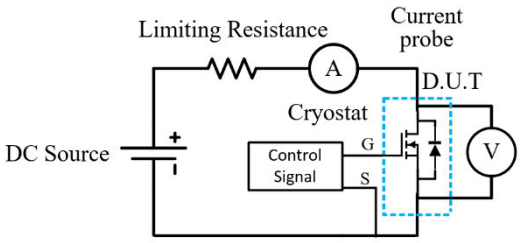


FIGURE 2. Forward voltage test circuit.

B. BREAKDOWN VOLTAGE TEST

The setup for the breakdown voltage test is shown in Fig. 3 and comprises a Glassman high voltage EJ (3kV – 200mA) power supply and a cDAQ 9185 data acquisition card with NI 9229 with a sampling frequency of 25 kHz. To monitor temperature, a PT100 sensor was attached to the device. The voltage on the power supply is set in accordance with the datasheets, and the avalanche breakdown voltage is calculated by measuring the current flowing through the device.

As with the forward voltage test, the DUT is immersed in LN2, and the power supply is turned on to apply the required voltage. The voltage across the DUT and the current passing through it are observed throughout the test. The DUT is then removed from LN2 and placed in the ambient, where its temperature increases passively. As the temperature of the DUT rises, the experiment is repeated to capture the characteristics of the device at different temperatures.

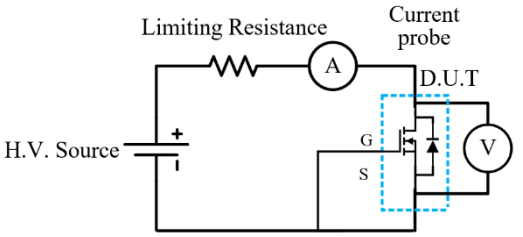


FIGURE 3. Breakdown voltage test circuit.

C. STATIC PARALLELING TEST

Figure 4 shows the static paralleling test where a Genesys GSP10-1000DC power supply was used to source the required current to the devices. A shunt resistor with a value of 100 $\mu\Omega$ was used to measure the current passing through devices. The voltage across the device is measured by an NI 9229 card with a sampling frequency of 25 kHz on a cDAQ 9185. This test is only conducted at room and cryogenic temperatures.

D. DOUBLE PULSE TEST

The setup for the double pulse test (DPT) is shown in Fig. 5, where a TDK Lambda GEN 600-5.5 power supply provides the input voltage. A Keysight MSO-X 2024A oscilloscope

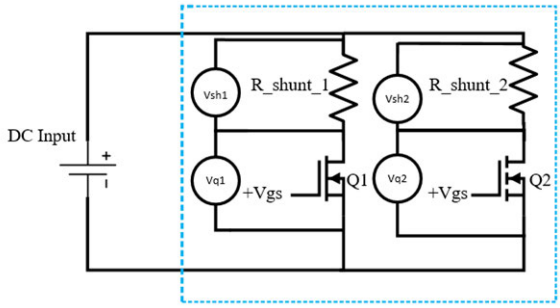


FIGURE 4. Static paralleling test circuit.

was used to capture the measurements and a PT100 sensor was attached to the device to monitor the temperature. The voltage is measured directly across the device but, for measuring the current, a specially developed cryogenic sensor was used. The double pulse test was only conducted at 77 K and 300 K. Like the static paralleling test, as there is a limited amount of data available, extrapolating data to lower temperatures would be inaccurate.

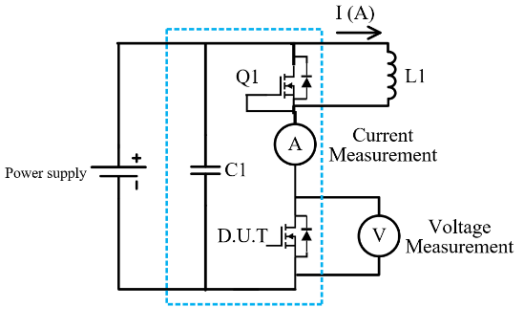


FIGURE 5. Double pulse test circuit.

Figure 6 shows idealized waveforms from the DPT, where the DUT is switched on at t_0 to charge the coil *L1* and switched off at t_1. The DUT has switched on again at t_2 and finally switched off at t_3.

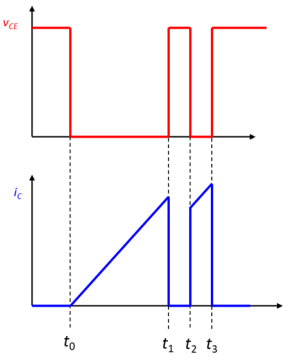


FIGURE 6. Voltage and current waveforms from the double pulse test circuit.

For the DPT, the testing voltage has been set at 450 V. The gate driver is shown in Fig. 7 where the DUT switching speed is adjusted by changing the gate resistance ($R_{g(\text{off})}$) which is chosen to be 68 Ω in this article.

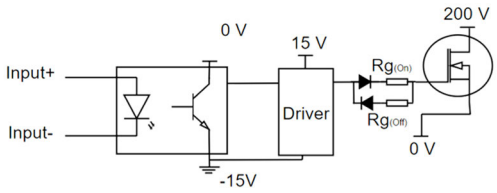


FIGURE 7. Gate driver used for double pulse test.

The higher gate resistance helps ensure that the device is switched off without oscillations. The gate resistance ($R_{g(\text{on})}$) is chosen to be 1.6 Ω. The gate driver resistors are the same for both the SiC MOSFET and the IGBT.

E. SUMMARY OF CHARACTERIZATION TESTS

The characterization tests are summarized in Table 4 for each test and the parameter extracted include on-resistance $R_{DS(ON)}$ for the SiC MOSFETs or the forward voltage $V_{Forward}$. The breakdown voltage is given at each temperature. The static paralleling test is used to measure the complexity of paralleling two devices at cryogenic temperatures, where $I_{Device1}$ and $I_{Device2}$ are measured to compare if they share the current equally. For the double pulse test, the voltage rise and fall times T_{rise} and T_{fall} are measured to give an indication of the device switching losses at lower temperatures.

TABLE 4. Parameters extracted from characterization tests.

Test	Purpose	Parameter extracted
Forward voltage	Conduction losses	$V_{Forward}$ or $R_{DS(on)}$
Breakdown voltage	Breakdown voltage	V_{Br}
Static paralleling	Complexity of paralleling	$I_{Device\ 1}$ and $I_{Device\ 2}$
Double pulse	Switching losses	T_{rise} and T_{fall}

IV. SELECTING A CURRENT SENSOR FOR DPT

Existing current probes are not designed to operate at cryogenic temperatures and will become damaged. Thus, most literature uses resistive shunts within the cryogenic zone [16] which does not provide Galvanic isolation, or extended conductors to carry the current under measurement to outside the cryogenic zone where it can be measured with a current probe [17]. As the lengths of these conductors increase, their parasitic inductances increase, which affects the measurement accuracy [18].

A Tektronix TCP303 current probe with a bandwidth of 15 MHz was used for initial tests at room temperature. However, using that probe presented some drawbacks:

- The bulk of the measuring head raises stray inductances in the loop required to accommodate it. This problem is exacerbated if currents in two parallel devices are to be measured.
- It cannot be used in cryogenic temperature zones as the packaging is not designed for those temperatures.
- Its capacity is limited to 150 A (RMS). The peak current is limited to 500 A, but this is still too low for the required testing program.
- There is a propagation delay (typically 53 ns) through the probe and amplifier system.

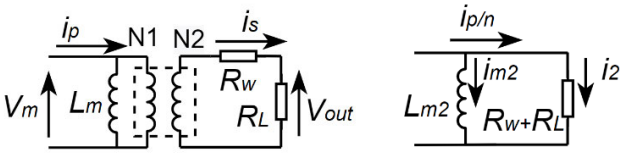
To address the issues, other current measurement techniques were considered [19] as summarized in Table 5. From that table, it was deduced that using a current transformer at cryogenic temperature is the most suitable solution.

TABLE 5. Comparison between current measurement devices.

Symbol	Shunt resistor	Rogowski coil	Current transformer
Advantages	-Inexpensive. -Simple.	-High bandwidth. -Open coil.	-Accurate -Low sensitivity to stray fields.
Disadvantages	-No inherent isolation. -Measure a small voltage	-Complicated compensation circuit (integrator).	-Requires desaturation circuit.

A simple CT equivalent circuit is shown in Fig. 8, where R_w is the secondary winding resistance. The CT must meet several requirements. The peak magnetizing current (I_{pk}) drawn must not be excessive as this fundamentally defines the accuracy. Secondly, the core material must not saturate. With respect to Fig. 6, the voltage-time product (vt) applied across the CT's secondary winding N_2 is given by

$$vt = \frac{I_{pk}(R_w + R_L)(t_1 - t_0)}{2N_2}. \tag{1}$$



(a) (b)

FIGURE 8. Equivalent circuit of the current transformer, a) parameters of the primary and the secondary of the current transformer, b) equivalent circuit with parameters referred to the secondary side.

The interval between t_0 and t_1 is taken as being much larger than the intervals between t_1 and t_2, and between t_2 and t_3. The peak magnetizing current $I_{mag_{2pk}}$) referred to the secondary side is given by dividing the vt product by the secondary-side inductance L_{m2}:

$$I_{mag2(pk)} = \frac{I_{pk}\,(R_w + R_L)\,(t_1 - t_0)}{2nL_{m2}}. \tag{2}$$

L_{m2} is given by:

$$L_{m2} = \frac{\mu_0 \mu_r A_e N_2^2}{l_e}. \tag{3}$$

where μ_r is the relative permeability of the core material, A_e is the effective area of the core, and l_e is the effective length of the core. The percentage error E is given by dividing $I_{mag_{2(pk)}}$ by the nominal secondary current at the end of a pulse:

$$E = \frac{I_{mag2(pk)}}{(I_p/n)} \times 100. \tag{4}$$

It is seen from (2) that to achieve low droop, a high L_{m2} and low R_w and R_L are needed. From Fig. 8 if R_L decreases, R_w becomes significant in defining the accuracy. Importantly here, R_w falls with temperature.

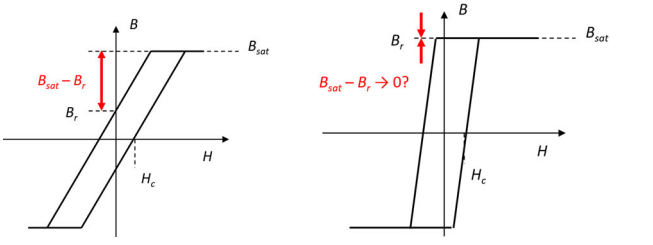
As mentioned, sufficient saturation flux density B_{sat} is needed to support the vt product. Faraday's Law gives

$$\Phi = \frac{\int v dt}{N}. \tag{5}$$

and from this, the flux swing B_{sw} is given by

$$B_{sw} = \frac{vt}{N_2 A_e}. \tag{6}$$

B_{sw} is, therefore, calculated to identify if it is lower than B_{sat}. However, with respect to Fig. 9, an important feature is that some core materials have a high remnant flux density B_r, and if this is not addressed then the available flux density swing is reduced from B_{sat} to $B_{sat} - B_r$. Figure 9 shows that B_r needs to be well below B_{sat} to avoid core saturation and measurement inaccuracies. However, very simple ancillary circuitry can be used to extend the available flux density swing.



(a) (b)

FIGURE 9. ***B-H*** **curves for magnetic cores; a)** B_{sat} **is much lower than** B_r**, b)** B_{sat} **is almost equal to** B_r**.**

To select cores that are suitable for cryogenic operation, the following must be considered;

- High permeability at the temperature of interest;
- Sufficient saturation flux density B_{sat};
- Low losses (heating is not problematic, but consequent current drawn by the resistive part of the magnetizing branch may affect accuracy).

Following an evaluation of the core materials' performance at cryogenic temperatures, it is seen that, compared to room temperature:

- Ferrite core permeability drops by 90% [20], [21].
- The permeabilities of nano-crystalline and amorphous materials only drop by 18% and 22% respectively [21].

Based on a market and literature review, two different amorphous and nano-crystalline cores were found suitable for cryogenic application. Table 6 shows a comparison of two candidate CT designs using these cores. The inaccuracies resulting from CTs assembled around both core types were calculated and presented in Table 6.

TABLE 6. Magnetic core specifications.

	Amorphous	Nano-crystalline
Manufacturer / Part number	Hitachi/ MP1903M4AS	Vacuumschmelze / T60006L2020W450
Material	Metglas	Vitroperm
B_{sat}	0.55 T	1.2 T
Dimensions	Inner diameter: 11.86 mm Outer diameter: 21.24 mm Outside height: 4.7 mm	Inner diameter: 10.20 mm Outer diameter: 22.60 mm Outside height: 10.2 mm
R_w and L_{m2} at 300 K	$R_{r/t}$=611 mΩ $L_{r/t}$=55.38 mH	$R_{r/t}$=1.284 Ω $L_{r/t}$=174 mH
R_w and L_{m2} at 77 K	$R_{c/t}$=105 mΩ $L_{c/t}$=41.18 mH	$R_{c/t}$=190 mΩ $L_{c/t}$=229 mH
Calculated inaccuracy	0.0146%	0.0066%
Desaturation	Requires compensation circuit for core resetting at 150 A	Requires compensation circuit for core resetting at 400 A

The developed CT ratio was 100:1 with 0.2-mm copper wire. For the Hitachi amorphous core, the magnetizing current was calculated using room temperature (RT) values, and with $I_{pk} = 600$ A, $R_L = 1\ \Omega$, and $t = t_1 - t_0 = 10\ \mu$s, then $I_{mag_{2(pk)}} = 873\ \mu$A. As the nominal secondary current is 6 A, then the inaccuracy of the core is 0.0146%. For the Vacuumschmelze nano-crystalline core the magnetizing current was calculated using RT values, and with $I_{pk} = 600$ A, $R_L = 1\ \Omega$, and $t = t_1 - t_0 = 10\ \mu$s, then $I_{mag2(pk)} = 393.1\ \mu$A. As the nominal secondary current is 6 A, then the inaccuracy of the core is 0.0066%. Table 6 shows that the amorphous core CT design saturates at a lower current than the nano-crystalline core CT design. Thus, based on higher saturation current and lower inaccuracy, the CT designed around the Vacuumschmelze nano-crystalline core was selected.

A. TESTING CURRENT SENSOR PERFORMANCE

The designed CT's performance was evaluated by comparing it with that of the Tektronix TCP303 current probe. Figure 10 presents the experimental results where the CT had a matching performance with that of the Tektronix probe in

terms of magnitude. Figure 10 demonstrates that the CT is slightly faster than the Tektronix probe in terms of the current measurement, thus higher accuracy can be obtained when calculating the energy dissipated during switching.

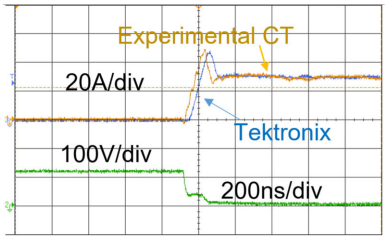


FIGURE 10. I_{drain} measurement captured by Tektronix probe (blue) and bespoke current sensor (yellow). V_{drain} is measured using differential probe (green).

B. DESATURATION CIRCUITS FOR CURRENT SENSOR

To increase the capacity of the CT and avoid core saturation, two simple circuit configurations are evaluated for desaturation, which is presented in Fig. 11. Figure 11 (a) shows the first current desaturation technique where a fast diode rectifier is used in the circuit [22], and the oscillatory action between the CT's magnetizing inductance and stray capacitance resets the core.

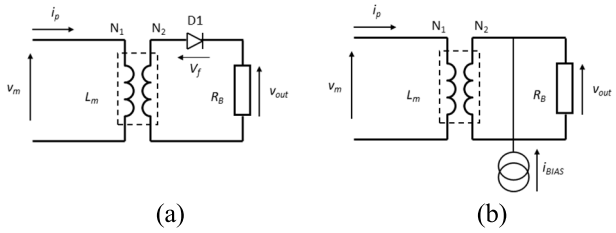


FIGURE 11. Different desaturation circuits, a) by using a diode on the secondary side of the transformer and b) by injecting a bias current into the secondary winding.

It was found that the circuit in Fig. 11 (a) saturates at 400 A. Figure 11 (b) shows the second current desaturation technique, which is established just by injecting a small bias current into the secondary winding of the CT. This increases the saturation point of the CT beyond 400 A of the circuit in Fig. 11 (a). Figure 12 shows the current sensor with the desaturation circuit in Fig. 11 (b) installed for the DPT circuit. Table 7 presents a comparison between the newly designed current sensor and the Tektronix TCP303 probe. The results demonstrate that the newly developed current sensor is an effective option compared to the Tektronix TCP303. It can operate in cryogenic temperatures, provides a lower propagation delay, and can measure primary current without saturation.

V. EXPERIMENTAL RESULTS

In this section, semiconductor devices are tested at cryogenic temperatures to estimate their performance. The section will first present the experimental results from the SiC MOSFET, and then the results for the different Si IGBT devices.

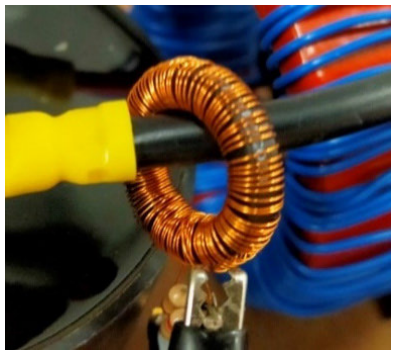


FIGURE 12. Current sensor for measuring DPT.

TABLE 7. Parameters extracted from characterization tests.

Parameter	Tektronix TCP303 current probe	Developed current sensor
Bandwidth (MHz)	15	200
Maximum current AC (A)	150	600
Operating temperature (K)	300	77-300

A. POWER MODULES USING SiC MOSFETs

1) DEVICE 1 (CONVENTIONAL MODULE)

The device was tested at room and cryogenic temperature, after which it was determined that this device is not appropriate for cryogenic applications as when it has undergone several thermal cycles cracking noises were heard from the device, and its gate current increased to 0.5 A. Mainly the increased gate current means that the device has experienced gate failure and thus is not suitable for use in cryogenic temperature applications.

2) DEVICE 2 (SLC MODULE)

Device 2 has been tested at different temperatures and did not suffer the same failure as Device 1. Figure 13 shows the forward voltage across the device at different temperatures. From Fig. 13 it is deduced that, with the decrease in temperature, the forward voltage increases leading to higher conduction losses (up to a 216 % increase). These results are consistent with the literature review in Section II.

Figure 14 shows the on-resistance of the SiC MOSFET at 200 A and for temperatures between 77 K and 300 K. From the figure, the on-resistance increases exponentially with the decrease of temperature causing higher conduction losses.

The negative temperature coefficient is shown in Fig. 14 at cryogenic temperature, making it more difficult to parallel. At $V_{gs} = 24$ V, the on-resistance increased by 100% more than its room temperature value. At $V_{gs} = 16$V, the on-resistance increased by 1000 %. Based on the experimental results, the SiC MOSFET is better to be used at temperatures above 200 K as in [10]. From that curve, the

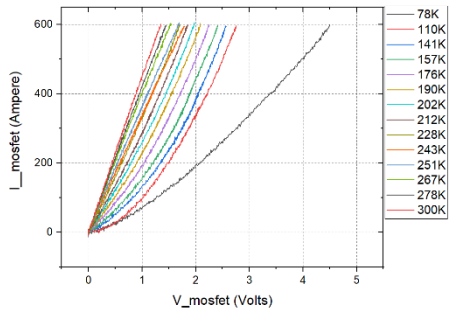


FIGURE 13. Forward voltage vs. temperature of Device 2.

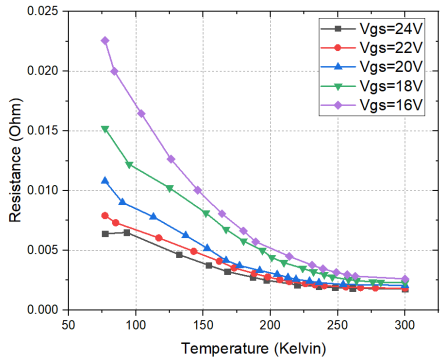


FIGURE 14. On-resistance vs. temperature of Device 2.

on-resistance decreased by 350 % at 77 K. Figure 15 shows the breakdown voltage of Device 2 at different temperatures. The breakdown voltage decreased with the decrease in temperature to be around 850 V at 77 K, which is consistent with the literature.

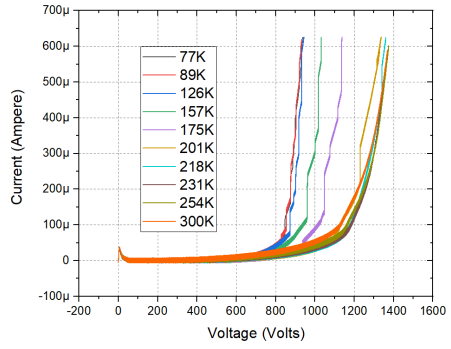


FIGURE 15. Breakdown voltage test vs. temperature of Device 2.

Figure 16 shows the breakdown voltage at different temperatures, where temperatures 20 K and 4 K are extrapolated using linear regression. As seen from the figure the breakdown voltage is decreased by 42 % at 77 K, which is consistent with the literature.

Figure 17 shows the paralleling test results for the SiC MOSFETs at different temperatures. The gate-source voltage is set to $V_{gs} = 22$ V and the junction temperature T_j at the beginning of the test is $T_j = 77$ K. Figure 17 (a) shows that

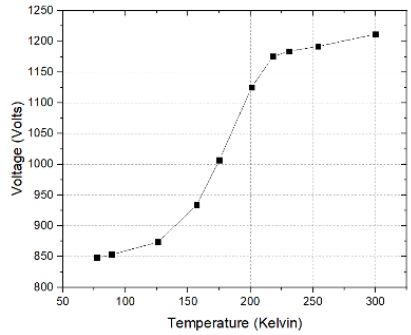


FIGURE 16. Breakdown voltage vs. temperature of Device 2.

MOSFET 1 is carrying 15 A more than MOSFET 2 at room temperature. Figure 17 (b) shows that this current gap gets bigger at cryogenic temperature with MOSFET 1 carrying approximately 55 A more than MOSFET 2. Based on this experiment, it can be concluded that SiC MOSFETs are not suitable for sharing at cryogenic temperature because of the resulting negative temperature coefficient.

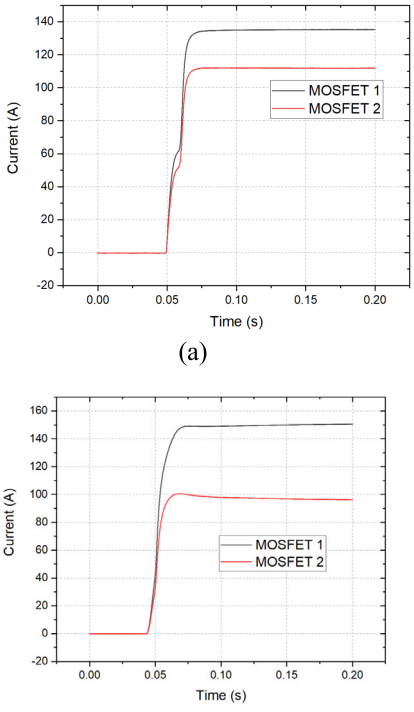


FIGURE 17. Paralleling test results of Device 2 at a) room temperature and b) cryogenic temperature.

Figure 18 shows the double pulse test at room and cryogenic temperatures.

From the experiment, it was found that the T_{rise} and T_{fall} have increased at cryogenic temperatures, and hence higher switching losses are expected when operating the device at

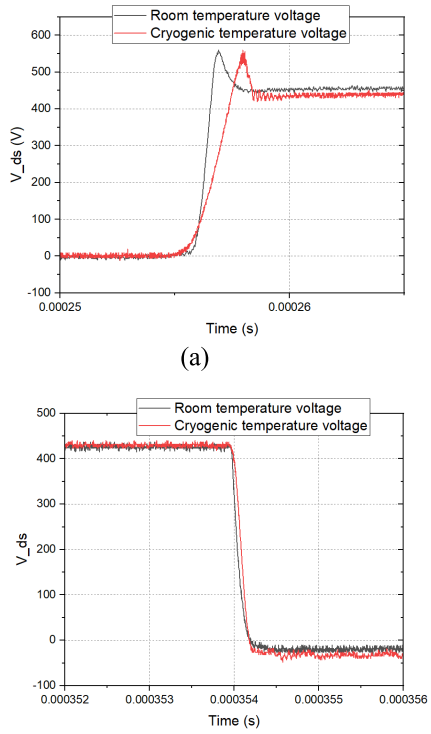


FIGURE 18. Double pulse test results of Device 2 at a) rising edge and b) falling edge.

cryogenic temperatures. The instantaneous switching losses were calculated and presented in Fig 19.

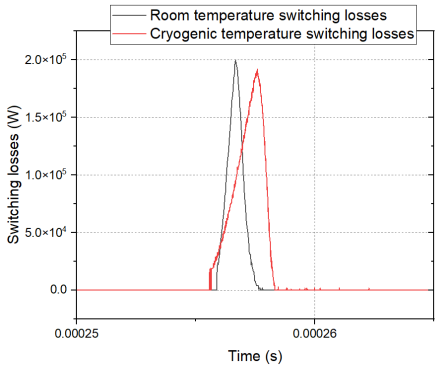


FIGURE 19. Instantaneous switching-on losses for Device 2.

Table 8 summarizes all the experimental results for Device 2. The $R_{DS(ON)}$ of the MOSFET has increased by 216 %, and the device's T_{rise} and T_{fall} times have shown to increase with the decrease in temperature by 178.3 % and 155 % respectively. The device's breakdown voltage decreases as well at cryogenic temperatures by 26 %, which must be considered in the inverter design consideration. Even though the device's performance worsens at cryogenic temperatures, SiC MOSFETs have lower conduction losses than IGBTs and thus remain a strong candidate for being used in semiconductor circuits at cryogenic temperatures. Overall, Device 2 should be considered a candidate for making semiconductor circuits at cryogenic temperatures.

TABLE 8. Device 2 performance at cryogenic temperature.

Symbol	Room temperature	Cryogenic temperature
R_{DS} ($m\Omega$)	2.1	6.64
% Change	+216%	
V_{BR} (V)	1250	915
% Change	-26.8%	
T_{rise} (ns)	575	1600
% Change	+178.3%	
T_{fall} (ns)	56	143
% Change	+155%	
Paralleling	Require complex circuitry to optimize current sharing	

B. POWER MODULES Si IGBT

1) DEVICE 3 (DISCRETE Si IGBT)

A discrete IGBT was tested at room and cryogenic temperatures to study the device's integrity at such extreme temperature conditions. The device underwent several cycles of cooling down to 77 K and then warming up to 300 K. It was found that it was able to run smoothly without suffering damage from the cycling. Figure 20 shows the forward voltage of the device at 300 K and 77 K.

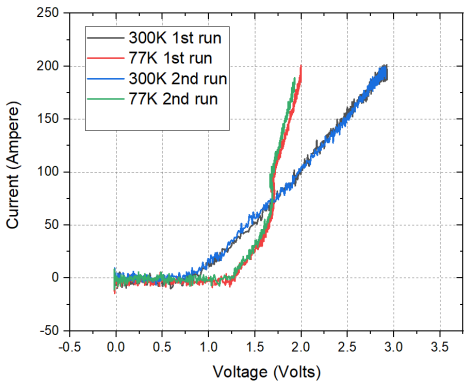


FIGURE 20. Forward voltage test of Device 3.

The breakdown voltage has been tested at cryogenic and room temperatures as shown in Fig. 21. From the figure the breakdown voltage of the device decreases with the decrease in temperature which is consistent with the literature review done earlier.

2) DEVICE 4 AND DEVICE 5 (CONVENTIONAL MODULES)

Devices 4 and 5 have suffered similar conditions as those of Device 1. The devices suffered from cracking sounds and their gate current increased indicating device degradation leading to gate failure and eventually total device

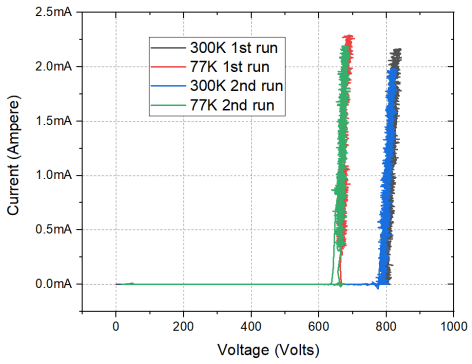


FIGURE 21. Breakdown voltage test of Device 3.

malfunction. Based on this experiment, it was concluded that these devices are not suitable for cryogenic applications.

3) DEVICE 6 (SLC MODULE)

This device was selected because it has different insulation in the packaging (epoxy resin) and a different architectural design than Device 4 and Device 5. After numerous thermal cycles from cryogenic to room temperature, the device performed flawlessly.

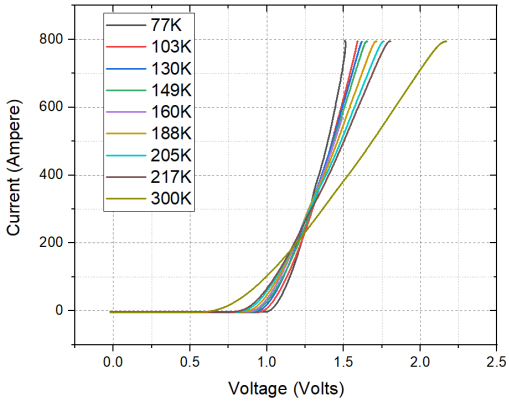
Figures 22 (a) and (b) show the forward voltage of the device at different temperatures. The decrease in the forward voltage with the temperature (and thus lower losses) is more apparent in Fig. 22 (b).

Figure 23 shows the breakdown voltage test where it can be seen that the breakdown voltage decreases with the decrease of the temperature. These results are consistent with the literature review discussed in the previous section.

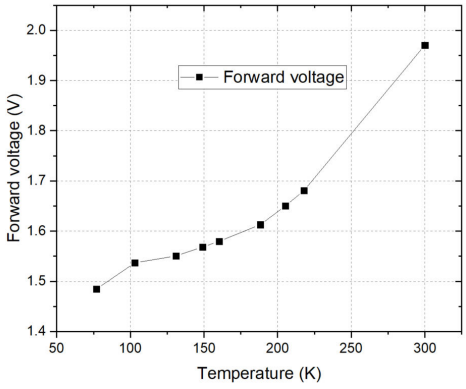
Figure 24 shows the results from the static paralleling test. Both devices were able to share the current of 500 A equally at cryogenic and room temperatures. Thus, this offers an advantage over the SiC MOSFET device tested previously.

Figure 25 shows the results from the double pulse test. The T_{rise} and T_{fall} have decreased at cryogenic temperature, thus lowering switching losses. Figure 26 the instantaneous switching losses are shown where the losses are almost the same at room and cryogenic temperatures.

Table 9 summarizes all the experimental results for Device 6. The conduction losses have decreased by 21 %. The switching T_{rise} and T_{fall} of the device tend to decrease with the decrease in temperature by 10 % and 36 %, respectively. The breakdown voltage of the device decreases as well at cryogenic temperatures by 22 %, which must be considered in the inverter design consideration. Overall, despite the decrease in breakdown voltage at cryogenic temperatures, Device 6 is a good candidate for semiconductor circuits at low temperatures. The device's improvements in conduction losses and switching speed can provide benefits for certain applications.



(a)



(b)

FIGURE 22. Forward voltage test of Device 6.

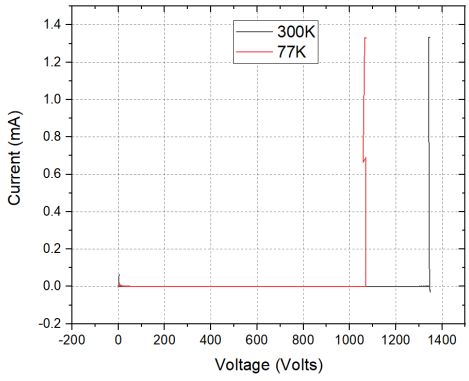
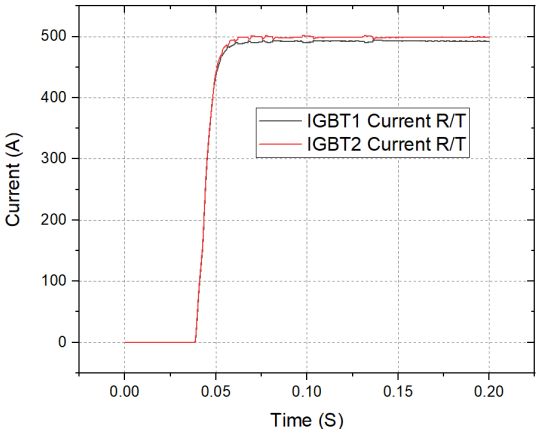


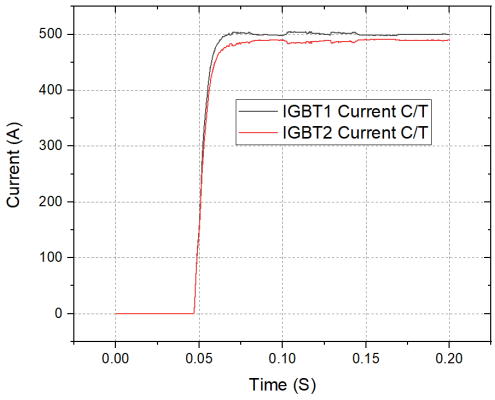
FIGURE 23. Breakdown voltage test at room and cryogenic temperature for Device 6.

4) DEVICE 7

This device has the same insulation as Device 6, where epoxy resin is used. The device also was solid cover technology like that of Device 6. The device operated smoothly after undergoing several thermal cycles from cryogenic to room temperature. Figures 27 (a) and (b) show the forward voltage of the device at different temperatures. The decrease in the



(a)

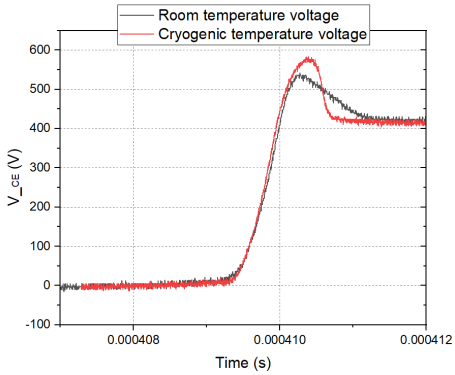


(b)

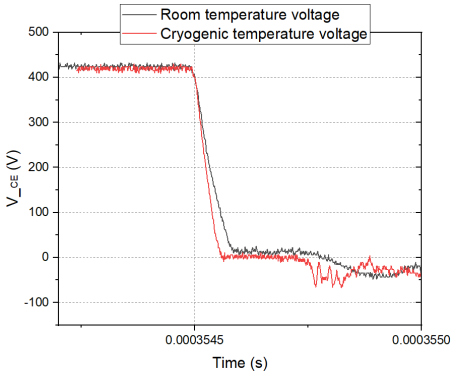
FIGURE 24. Paralleling test results of Device 6 at a) room temperature and b) cryogenic temperature.

TABLE 9. Device 6 performance at cryogenic temperature.

Symbol	Room temperature	Cryogenic temperature
$V_{Forward}$ (V)	1.83	1.445
% Change	-21%	
V_{BR} (V)	1338	1039
% Change	-22%	
T_{rise} *(ns)*	510	460
% Change	-10%	
T_{fall} *(ns)*	69	44
% Change	-36%	
Paralleling	Easy to parallel	



(a)



(b)

FIGURE 25. Double pulse test results of Device 2 at a) rising edge and b) falling edge.

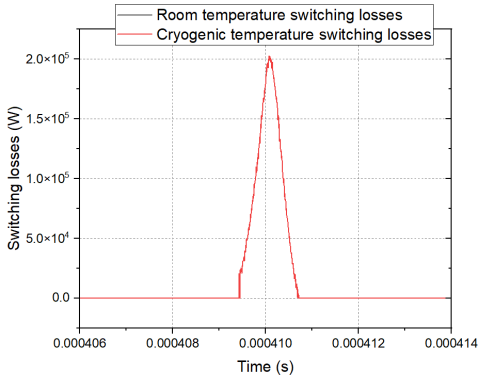


FIGURE 26. Instantaneous switching-on losses for Device 6.

forward voltage with the temperature (and thus lower losses) is more visible in Fig. 27 (b).

Figure 28 shows the results from the breakdown voltage test. As the temperature decreases, the device breakdown voltage decreased as well, similar to the device 6.

Figure 29 shows the results from the static paralleling test. Both devices were able to share the current of 500 A closely at cryogenic and room temperatures. These are very similar to those for Device 6.

Figure 30 shows the results from the double pulse test. T_{rise} and T_{fall} have decreased at cryogenic temperatures, thus lowering switching losses. Figure 31 shows the instantaneous switching losses at room and cryogenic temperatures.

Table 10 summarizes the experimental results for Device 7. It can be concluded from the table that the conduction losses decrease by 22 % with the decrease in temperature due to lower forward voltage at cryogenic temperature. Also, from

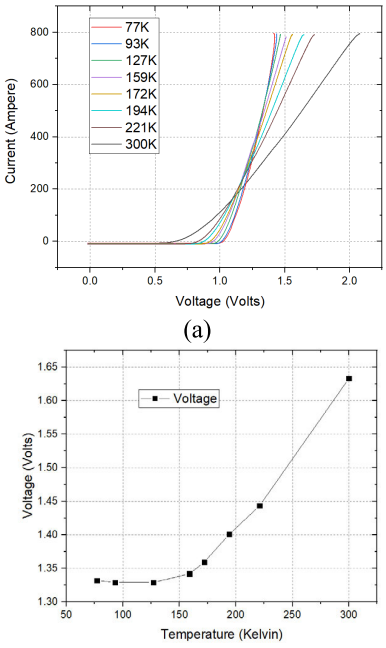


FIGURE 27. Forward voltage test of Device 7.

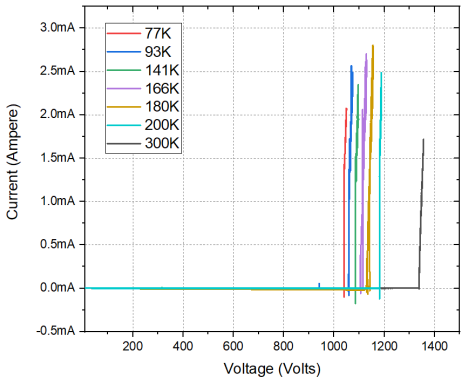


FIGURE 28. Breakdown voltage test at room and cryogenic temperature for Device 7.

TABLE 10. Device 7 performance at cryogenic temperature.

Parameter	Room temperature	Cryogenic temperature
$V_{Forward}$ (V)	1.76	1.37
% Change	-22%	
V_{BR} (V)	1338	1039
% Change	-22%	
T_{rise} (ns)	483	430
% Change	-10%	
T_{fall} (ns)	68	52
% Change	-23%	
Paralleling	Easy to parallel	

the table, the T_{rise} and T_{fall} times decrease by 10 % and 23 % respectively with the decrease in temperature.

Like Device 6, the breakdown voltage decreases with temperature, therefore when employing the device, a safety margin should be incorporated in the design consideration. Overall, Device 7 is a strong option for low-temperature semiconductor circuits.

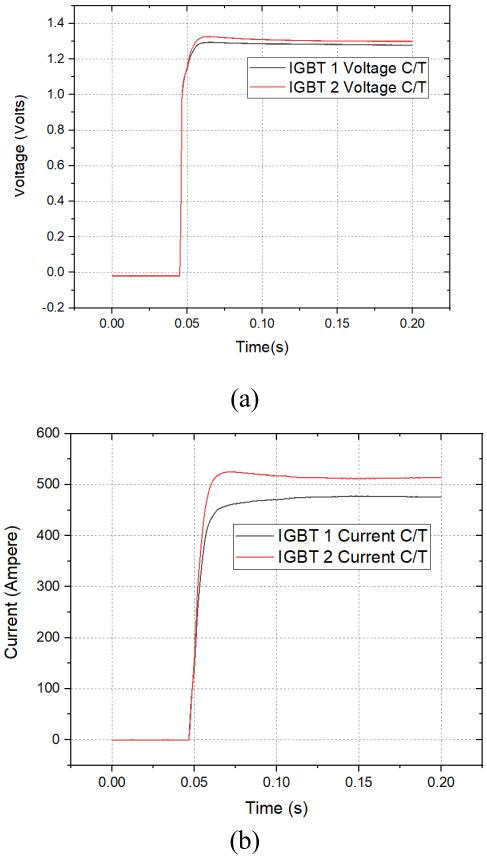


FIGURE 29. Paralleling test results of Device 7 at a) room temperature and b) cryogenic temperature.

5) SUMMARY

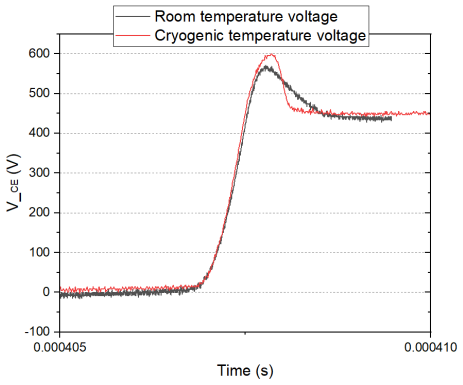
The performance of the three power modules is presented. Device 2 (SiC MOSFET) is not a suitable candidate for the inverter system as the paralleling test has shown the uneven distribution of current at cryogenic temperatures. Devices 6 and 7 have better paralleling at cryogenic temperatures and thus are more suitable candidates for semiconductor circuits at that temperature.

TABLE 11. Performance of inverters at different temperatures.

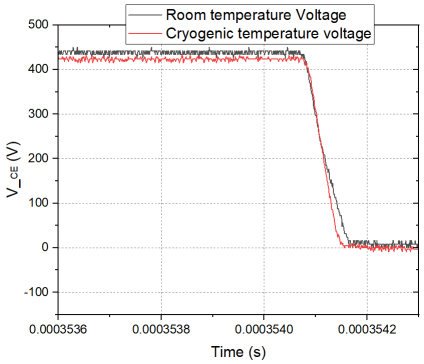
Device	Room Temperature	Cryogenic temperature	Change (W)
Device 6	96.84 %	97.06 %	-1999
Device 7	96.88 %	97.11 %	-2089

VI. CALCULATION OF SYSTEM PERFORMANCE AT ROOM AND CRYOGENIC TEMPERATURES

Based on the parameters listed in Table 1, a simulation was built on PLECs to estimate the system losses at room and



(a)



(b)

FIGURE 30. Double pulse test results of Device 7 at a) rising edge and b) falling edge.

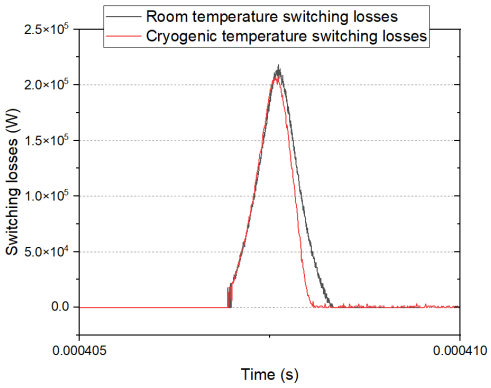


FIGURE 31. Instantaneous switching-on losses for Device 7.

cryogenic temperatures. Even though Device 2 did not fail at cryogenic temperature, it is not suitable for paralleling as presented in presented in the previous section. Thus, the simulation was run for the two IGBT devices (Device 6 and 7) as they were found to function well at cryogenic temperature. Table 11 shows the efficiency of Devices 6 and 7 at different temperatures. Inverter employing Devices 6 and 7 (Si IGBT) had improved efficiency with the decrease of temperature.

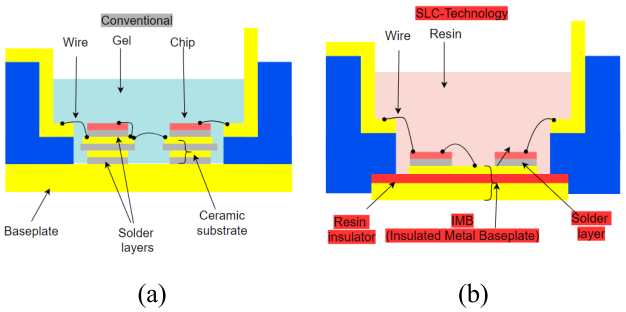


FIGURE 32. Comparison between conventional and solid cover (SLC) IGBT technology; a) conventional architecture and b) solid cover architecture. [23].

VII. DISCUSSION

Section V has presented the experimental results of different devices suitable for an all-electric aircraft. Six different power modules were tested at room and cryogenic temperature, three of which were able to survive the extreme cryogenic conditions.

The three devices that have failed when immersed in LN2 conventional modules (Devices 1, 4, and 5) suffered from gate failure and cracking noises were heard from the device. The structure of the conventional module is shown Fig. 32 (a), where several bond wires are used and are known to suffer from degradation of the solder layer under the substrate after undergoing heat cycling [23]. Conversely, devices with SLC technology (Devices 6, and 7) as illustrated in Fig. 32 (b) did not suffer from gate degradation or failure. They were able to operate satisfactorily under cryogenic conditions. The modules with SLC structure have outperformed the conventional mainly due to their enhanced heat cycle capabilities, which is achieved by combining a resin-insulated metal baseplate and direct potting resin.

The SLC has an insulated metal baseplate (IMB) which eliminates a solder layer under the insulator and hence reduces the strain of the solder layer under the chips [23].

The three devices that were able to survive the cryogenic temperature (Devices 2, 6, and 7) were tested at room and cryogenic temperatures to identify which is most suitable for the application in this article. Device 2 (SiC MOSFET) has shown that it requires complicated arrangements to work optimally in cryogenic temperature, mainly it requires a) operating the junction at temperatures above 200 K as in [10] to reduce the losses, and b) active current sharing as the device has negative thermal coefficient. Thus, they are less favorable to use than IGBTs. Conversely, Device 6 and Device 7 have shown that their conduction and switching losses decrease with the decrease of temperature. These devices have also shown easy paralleling at cryogenic temperatures. Thus, these devices are more promising to be used at such temperatures. The preliminary examination done in this article on different SLC technologies suggests that this particular package architecture and the IMB within it are the main reasons why these devices can withstand cryogenic conditions. Further study is necessary to elucidate the underlying causes.

VIII. CONCLUSION

In this article, different semiconductor devices were tested at cryogenic temperature to select the most suitable device for an all-electric aircraft. A bespoke cryogenic current sensor was built, which was able to decrease the noise in the DPT circuit and measure the current faster than commercial off-the-shelf current clamps. The experimental results indicated that IGBT Device 7 was the most suitable device for cryogenic aircraft applications. This device was found to be able to withstand harsh environmental conditions, had lower conduction losses than SiC MOSFET devices, and was easy to use in parallel configurations. These characteristics make IGBT Device 7 a good fit for use in cryogenic aircraft applications, which can lead to greater energy efficiency and reduced weight compared to traditional aircraft.

REFERENCES

[1] K. Rajashekara and B. Akin, "A review of cryogenic power electronics–status and applications," in *Proc. Int. Electr. Mach. Drives Conf.*, Chicago, IL, USA, May 2013, pp. 899–904.

[2] H. Gui, R. Chen, J. Niu, Z. Zhang, L. M. Tolbert, F. Wang, B. J. Blalock, D. Costinett, and B. B. Choi, "Review of power electronics components at cryogenic temperatures," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5144–5156, May 2020.

[3] S. Venuturumilli, F. Berg, M. Zhang, and W. Yuan, "Investigation of HTS cable impact on turbo-electric aircraft performance," *IET Electr. Syst. Transp.*, vol. 10, no. 1, pp. 62–67, Mar. 2020.

[4] J. K. Nøland, "Hydrogen electric airplanes: A disruptive technological path to clean up the aviation sector," *IEEE Electrific. Mag.*, vol. 9, no. 1, pp. 92–102, Mar. 2021.

[5] A. Elwakeel, Z. Feng, N. McNeill, M. Zhang, B. Williams, and W. Yuan, "Study of power devices for use in phase-leg at cryogenic temperature," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, pp. 1–5, Aug. 2021.

[6] H. Chen, P. M. Gammon, V. A. Shah, C. A. Fisher, C. Chan, S. Jahdi, D. P. Hamilton, M. R. Jennings, M. Myronov, D. R. Leadley, and P. A. Mawby, "Cryogenic characterization of commercial SiC power MOSFETs," *Mater. Sci. Forum*, vols. 821–823, pp. 777–780, Jun. 2015.

[7] T. Chailloux, C. Calvez, N. Thierry-Jebali, D. Planson, and D. Tournier, "SiC power devices operation from cryogenic to high temperature: Investigation of various 1.2 kV SiC power devices," *Mater. Sci. Forum*, vols. 778–780, pp. 1122–1125, Feb. 2014.

[8] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, "Cryogenic and high temperature performance of 4H-SiC power MOSFETs," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, USA, Mar. 2013, pp. 207–210.

[9] H. Gui, R. Ren, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Characterization of 1.2 kV SiC power MOSFETs at cryogenic temperatures," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 7010–7015.

[10] R. Chen, J. Niu, R. Ren, H. Gui, F. Wang, L. Tolbert, B. Choi, and G. Brown, "A cryogenically-cooled MW inverter for electric aircraft propulsion," in *Proc. AIAA/IEEE Electr. Aircr. Technol. Symp. (EATS)*, Aug. 2020, pp. 1–10.

[11] K. Tian, J. Qi, Z. Mao, S. Yang, W. Song, M. Yang, and A. Zhang, "Characterization of 1.2 kV 4H-SiC power MOSFETs and Si IGBTs at cryogenic and high temperatures," in *Proc. 14th China Int. Forum Solid State Lighting, Int. Forum Wide Bandgap Semiconductors China*, Nov. 2017, pp. 140–143.

[12] R. Singh and B. J. Baliga, "Cryogenic operation of asymmetric N-channel IGBTs," in *Proc. 4th Int. Symp. Power Semiconductor Devices*, 1995, pp. 561–566.

[13] A. J. Forsyth, S. Y. Yang, P. A. Mawby, and P. Igic, "Measurement and modelling of power electronic devices at cryogenic temperature," *IEE Proc.-Circuits Devices Syst.*, vol. 153, no. 5, pp. 407–415, Oct. 2005.

[14] Y. Wei, M. M. Hossain, and A. Mantooth, "Cryogenic static and dynamic characterizations of 650 V field stop trench Si IGBT," in *Proc. IEEE 22nd Workshop Control Modeling Power Electron. (COMPEL)*, Nov. 2021, pp. 1–6.

[15] Z. Zhang, H. Gui, R. Ren, F. Wang, L. M. Tolbert, D. J. Costinett, and B. J. Blalock, "Characterization of wide bandgap semiconductor devices for cryogenically-cooled power electronics in aircraft applications," in *Proc. AIAA/IEEE Electr. Aircr. Technol. Symp. (EATS)*, Jul. 2018, pp. 1–8.

[16] R. Ren, H. Gui, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, D. Costinett, B. J. Blalock, and B. B. Choi, "Characterization and failure analysis of 650-V enhancement-mode GaN HEMT for cryogenically cooled power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 66–76, Mar. 2020.

[17] H. Y. Gou, Y. Chen, M. G. Tang, R. B. Zhao, X. S. Tan, and L. Yang, "Dynamic-switching energy dissipation behaviors of cryogenic power MOSFET at 77 K," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 8, pp. 1–2, Nov. 2021.

[18] J. Schweickhardt, K. Hermanns, and R. M. Herdin. (May 2023). *Tips and Tricks on Double Pulse Testing*. [Online]. Available: http://www.rohde-schwarz.com

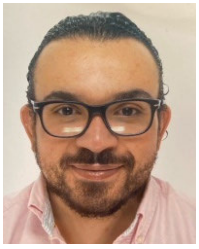
[19] S. Ziegler, R. C. Woodward, H. H.-C. Iu, and L. J. Borle, "Current sensing techniques: A review," *IEEE Sensors J.*, vol. 9, no. 4, pp. 354–376, Apr. 2009.

[20] E. C. Hannah, "Low temperature magnetic cores and a preamp for low impedance cryogenic sources," *Rev. Sci. Instrum.*, vol. 52, no. 7, pp. 1087–1091, Jul. 1981.

[21] S. Yin, M. Mehrabankhomartash, A. J. Cruz, L. Graber, M. Saeedifard, S. Evans, F. Kapaun, I. Revel, G. Steiner, L. Ybanez, and C. Park, "Characterization of inductor magnetic cores for cryogenic applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Vancouver, BC, Canada, Oct. 2021, pp. 5327–5333.

[22] N. Mcneill and N. K. Gupta, "Assessment of the error in the average current sensed by the unidirectional current pulse transformer," *IET Circuits, Devices Syst.*, vol. 2, no. 2, pp. 265–276, Apr. 2008.

[23] T. Radke, N. Lakshmanan, T. Takashi, and S. Asada, "Enhanced power density and expanded line-up of the 7th gen industrial IGBT modules utilizing the improved thermal conductivity of the highly reliable SLC-technology," *Bodo's Power Syst.*, vol. 10, pp. 16–22, Jun. 2016.



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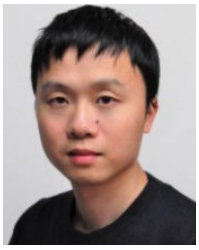

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